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the small systems journal

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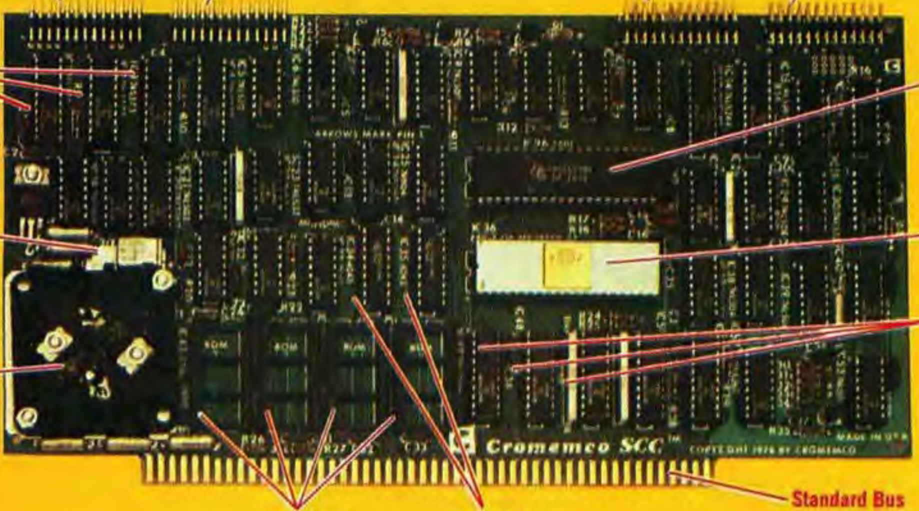

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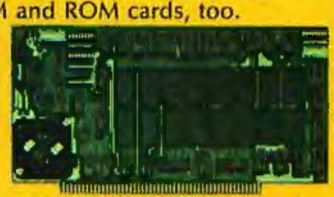
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In The Queue

BYTE September 1979
Volume 4, Number 9

Foreground


page 6


page 10

Background


page 34

Nucleus

Cover Art: **Fantasy on Homebrewing** *by Robert Tinney.*

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In This BYTE

About the Cover
On this issue's cover, Robert Tinney has created a "fantasy on homebrewing." In the middle of a sylvan glade, we see the form of a computer being sculpted by some homebrewer. A couple of humanoid forest denizens look on with wonder, perhaps hoping to get a glimpse of our homebrewer on his return to the workplace.

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Editorial

The Rationale of Yet Another Homebrew System

by Carl Helmers

In this issue of BYTE, we are placing a special emphasis on the homebrewing of computers: the craft of assembling the hardware and software of a system from standard components in nonstandard ways. This month's editorial provides a continuation of notes begun in July on the design and assembly of my new homebrew 6809 system. In this editorial, we complete the final details of the physical layout and power supplies of the system, as well as the overall design of the system. We shall also begin a discussion of the actual processor card. Future installments in this series on homebrew, general purpose, computer hardware will record details of the system beyond this article's goal of defining a backplane bus structure.

As noted earlier ("Editorial," June 1979 BYTE, page 6), the intent of this exercise is to develop a specialized controller node for a loosely coupled system of processors involved with musical applications. The multiple processors initially contemplated were a Pascal-oriented, large personal computer and an ALF products model AD-8 music synthesizer with its 6502 used for housekeeping. In addition to this coordinating task, the 6809 would provide a central point for the connection of keyboards, displays and other hardware required by musical applications.

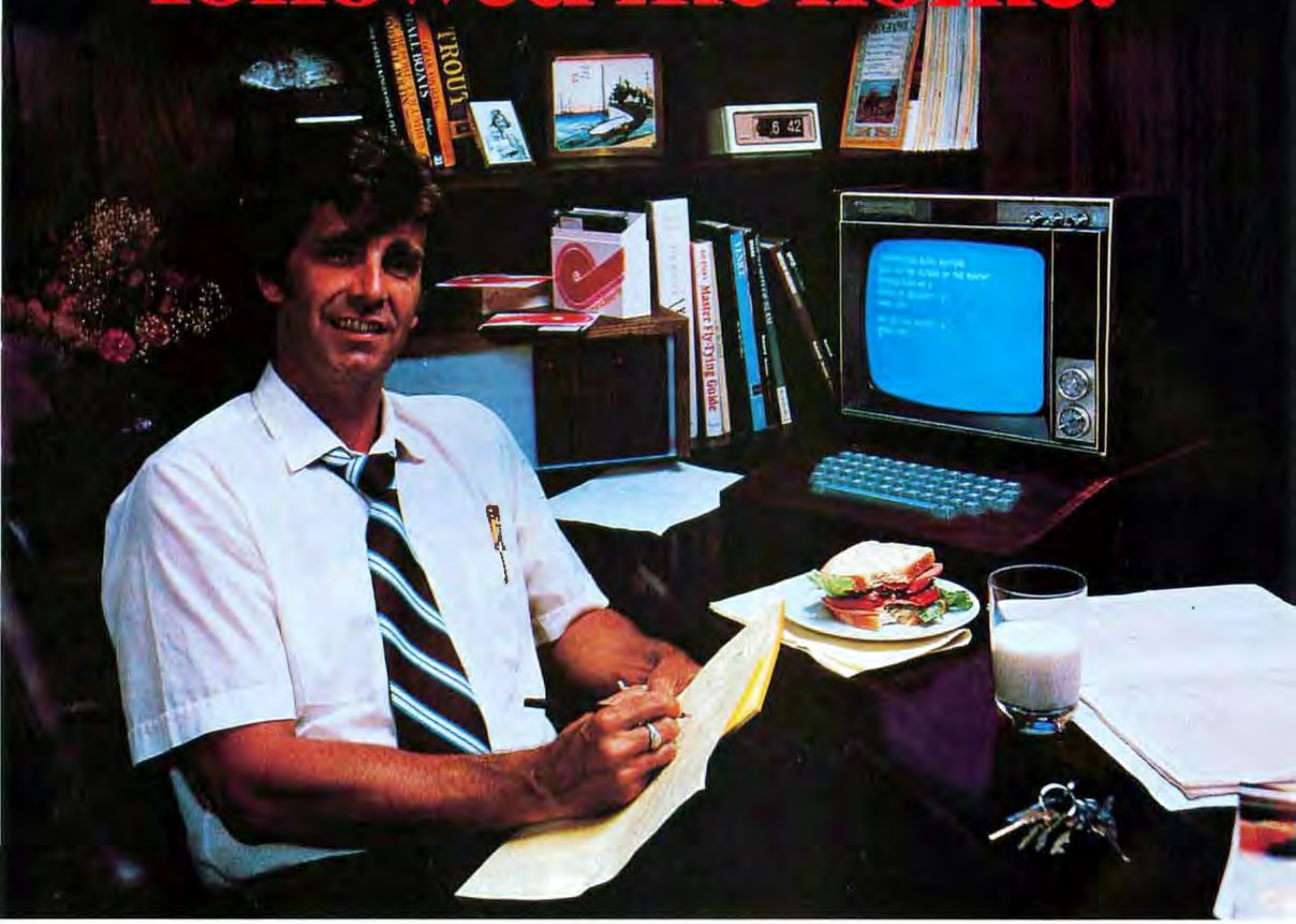
But ideas change and evolve. Since the 1st installments were written, plans have become slightly more grandiose with my recent acquisition of a New England Digital "Synclavier" music synthesizer and its associated Able/60 minicomputer. Located in Norwich VT, New England Digital is a combined spin-off of the music and electrical engineering departments of Dartmouth College across the Connecticut river in NH. The computer for the music synthesizer employs the XPL language as its high-level user interaction. The New England Digital version of XPL is augmented by a floating-point data type. With the exception of an adaptation of UCSD Pascal, which is expected to be available soon, all systems software is written in XPL, including what is described as a 3-pass optimizing XPL compiler.

[XPL is the language described in the book *A Compiler Generator*, by McKeeman, Wortman, et al, published circa 1968. The commonly used microcomputer language PL/M, 1st designed and implemented by Gary Kildall, is very similar to XPL in syntax and semantics. XPL is a simple subset of PL/I, with data types restricted to character and integer forms.]

At this point, I now have a need for multiple processor communications beyond the level of 1 large machine (a Western Digital P-engine) driving a smart peripheral through a serial communications link. The smart peripheral will still handle specialized details like the parallel interface to the older synthesizer and the eventual interface to an electronically controlled player piano.

See photo notes on pages 8 and 9, text continued on page 202

"My Shugart followed me home."



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Hardware Basis...

These photographs depict some further details of the physical hardware of the new homebrew 6809 computer system. As noted earlier, Vector Electronic Co components were used for the assembly of a backplane. Photographs 1 through 5 show various aspects of the new design's packaging.

(1)

Photo 1: The new computer system's final physical mounting basis is a mahogony box with guide blocks for the backplane assembly. Power supplies are located underneath the box. Power for the computer and accessories will be controlled by the standard, household wall switch mounted on the side of the box. Power connections to the backplane power buses will pass through a hole underneath the backplane in this photo. The hole provides an exit path for the flow of hot air from the power supplies.

Individual boards of the system plug into the backplane from the top as shown here. The backplane assembly slides into the grooves of the 2 guide blocks. These blocks are bolted to the top of the box using 1/4-20 machine-screws and threaded inserts. The grooves for the backplane board were cut 1/16th of an inch wide with a router and edge guide. The woodshop tools required to fabricate this case included a table saw, electric hand drill, drill press, router, belt sander, sabre saw, and the usual collection of hand tools.

(2)

Photo 2: The power supply modules are attached to 2 wooden brackets which are screwed into the main box by means of 1/4-20 machine-screw threaded inserts. The power supply modules are mounted on the brackets using #8-32 threaded inserts. Ordinary brass finish door stops serve as legs to keep the assembly off the table top, thus allowing natural convection to cool the power supply modules.

No attempt is made to calculate heating factors. The inverted cup shape of the box seems like an excellent trap for heat, however, the large hole beneath the backplane assembly at the top of the box provides a relatively low-impedance outlet for the heated air from below. If the temperatures observed under load are excessive, then a fix will be necessary. In a commercial or industrial engineering situation where production of a product is contemplated, this "patch up after problems" strategy is not the recommended practice due to the possibilities of costly errors, but for one of a kind products in a noncommercial and highly experimental context, it is certainly acceptable and can economize on time.

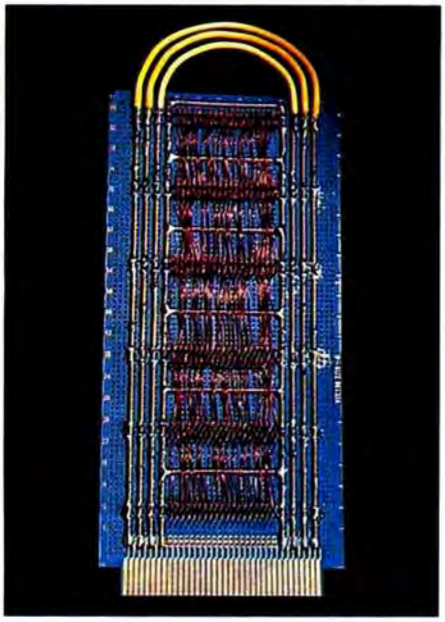
(3a)

Photo 3: (a) Brass machine-screw inserts to provide metal to wood fastening in the

(3b)

(5a)

(4)



(5b)

assembly of the computer housing. These particular parts were purchased from the Brookstone Co Peterborough NH.

(b) When inserting the machine-screw fasteners into hardwood, better results were obtained when the hole drilled in the wood was 1/64th of an inch larger than the recommended size in the instructions. A short section of the machine-screw to be used, together with a hex nut, provide a tool for driving the insert as shown in this picture. When using the #8-32 inserts in hardwood, a slightly larger hole than suggested in the instructions is a necessity. Unless the extra clearance is given, the torque on the #8-32 bolt used in driving the insert will cause the insert to twist apart after 1 or 2 uses.

Photo 4: The backplane is the first and the most tiresome wiring involved with assembly of a small computer. Its definition is provided by the simple instructions:

FOR each free socket, pin BY NUMBER
OF each socket,
CONNECT that pin to the same pin
of the next socket in the backplane!

The backplane assembly was described in the notes of the July 1979 BYTE, page 194. This photo shows the finished backplane after all wiring and installation of bypass capacitors has been completed.

Photo 5: The wiring of the backplane, as well as the rest of this computer, was done with the Vector Electronic Co's "slit-N-wrap" technique. An electric eraser was used to motorize the connections, with an adapter custom-made on a small lathe. It is recommended that motorized wiring be employed with the "slit-N-wrap" technique. In previous experimental electronics built with this technique, reliability problems were encountered with manual termination of the wires to wire-wrap socket posts. Motorized wrapping with this tool provides a uniform and higher force for stripping the insulation off the wire.

At (a) is the adapter: a hollow tube made from 2 junk box spacers, a #10-32 bolt with a hole drilled through it, a brass union between the 2 spacers, and a large brass adapter to which a #10-32 nut is soldered. (This latter kludge is what happens when one makes an adapter on a Sunday afternoon and a #10-32 tap is not available!) At (b) the completed adapter is mounted in the Bruning Electric Eraser in a typical use situation.

Ciarcia's Circuit Cellar

Joystick Interfaces

Steve Ciarcia
POB 582
Glastonbury CT 06033

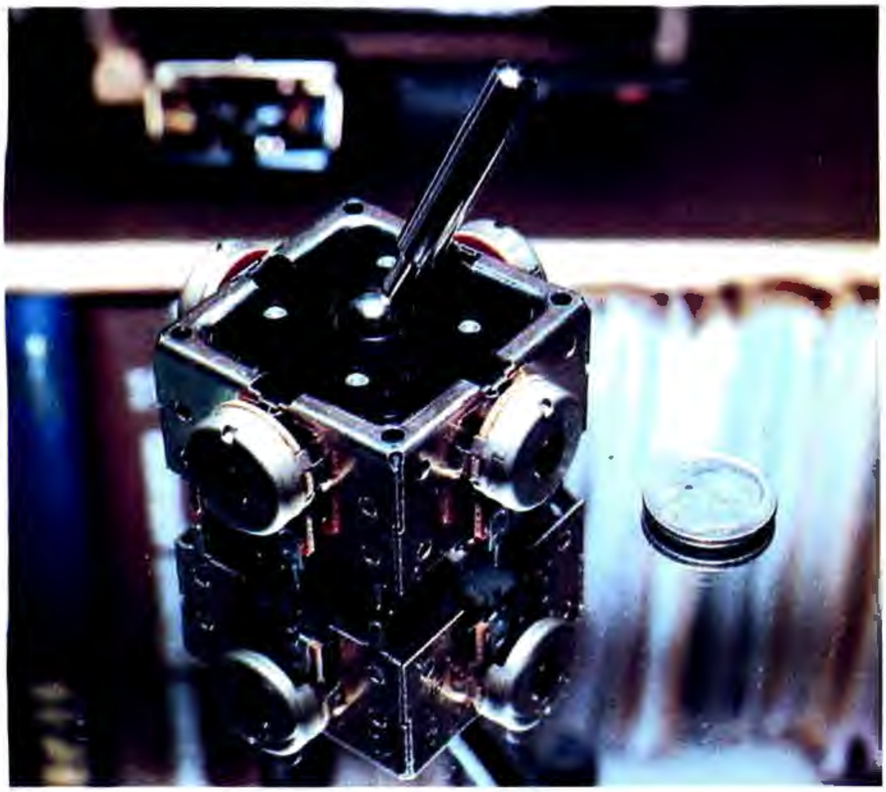


Photo 1: *A typical joystick with 4 potentiometers.*

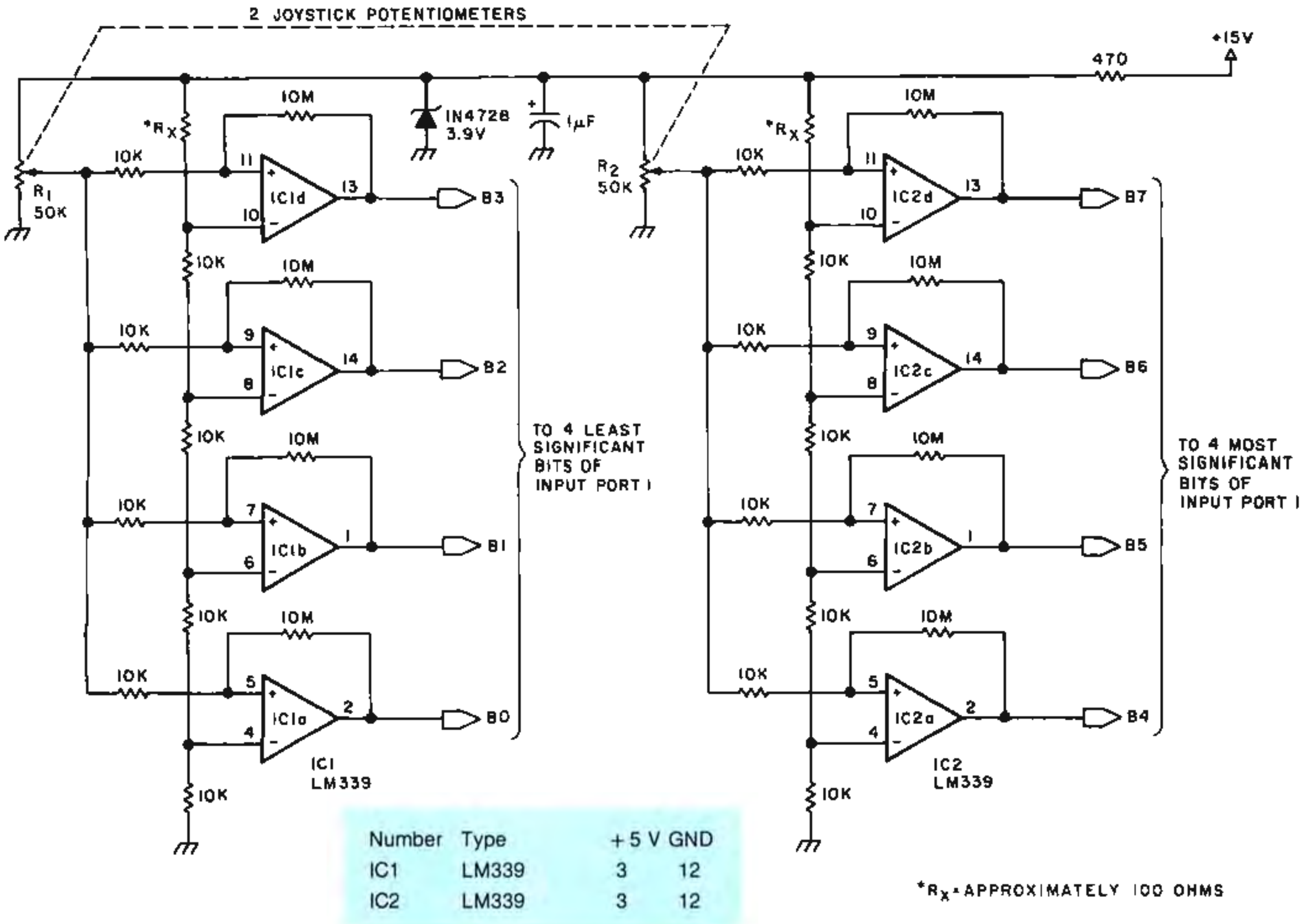
Photo 2: Note how moving the stick moves the gimbal arrangement, which in turn changes the settings of the potentiometers.

The thought that often comes to mind when the word joystick is mentioned to a computer enthusiast is of a spacewar-type game. A photon torpedo is fired from an opponent's starship, and the thruster joystick is deftly moved to reposition the craft out of its path. All of this occurs without having to take your eyes off the screen. Eye/hand coordination is almost "instinctive." With a glance to the upper right of the video screen, the joystick is tilted to the upper-right corner of its 360° range. This moves the spacecraft toward that coordinate. Reverse thrust is accomplished by moving the joystick in the opposite direction, as though you are pulling back on the throttle of a real craft. Such is the general experience with joysticks. However, the potential use of these devices greatly exceeds that of game playing.

A joystick, for those people who are unfamiliar with one, is shown in photo 1. It is an electromechanical device with resistance outputs proportional to the X,Y displacement of a central ball and lever. Photo 2 illustrates the mechanical connections to the potentiometers.

When the stick is positioned in the center of its axes, the X and Y potentiometers show resistances in the center of their ranges. When the stick is tilted to the upper right, both potentiometers are at their full-resistance limit, while the opposite (lowest resistance) is true when in the lower-left position. The outputs of the 2 potentiometers accurately track, as if on an X,Y coordinate axis, the position of the joystick. It should be noted that while it takes only 2 potentiometers to define 2-dimensional travel, most joysticks are manufactured with 4 potentiometers. This is a remnant of the days when joysticks were connected directly to the 4 deflection-plates of a cathode ray tube (video screen).

It is one thing to *consider* interfacing a joystick to a computer, and quite another to *do* it. A joystick is a mechanical X,Y positioning device. Even with proportional output resistances, an input interface must be designed to convert position from an analog to a digital representation which can be used by the computer. A further consideration is the resolution, or percent, of full-scale travel per bit sensitivity. Is the application so gross that center and full-scale are the only points of interest, as in a



Number	Type	+5 V	GND
IC1	LM339	3	12
IC2	LM339	3	12

Figure 1: Low-resolution static interface. This interface is for 1 2-potentiometer joystick. For 4-potentiometer joysticks, build a second circuit like this one, and interface it to another input port. Note that if the comparator does not trigger at full-scale setting, a small resistor may have to be added at Rx (marked with asterisk).

game control, or is the application one which requires fine control, such as a cursor-positioning device in a high-resolution graphics system?

All joystick interfaces are not created equal. There is a trade-off between hardware and software. The lower the resolution, the fewer the parts. The higher the resolution, the greater the electrical complexity or the software interaction with the interface. It is also important to recognize that computer systems which operate *only* in a high-level language like BASIC cannot use an interface design that requires an assembly language subroutine as an integral component. In such instances only a static interface can be used.

Included in this presentation are 4 interface designs which should cover most requirements, as well as demonstrate the considerable differences between them. The 4 types are:

- low-resolution static
- high-resolution fully static hardware
- software-driven pulse-width modulated
- high-resolution analog-to-digital

Low-Resolution Static Interface

First of all, *static* simply means that the interface hardware determines the potentiometer position value and presents it in constant, parallel digital form to the computer. When the interface is attached to any parallel input port, this joystick value can be read with a single INPUT command in BASIC. As far as the computer is concerned, the value is fully static, and the computer reads whatever data is there when the INPUT is executed. The interface hardware has the responsibility of asynchronously updating the digital value as the stick is moved.

Often the joystick is simply used to indicate relative direction and magnitude. In a wheelchair, for instance, full linear control of speed and direction would require rather expensive drive electronics. Most chairs use simple relay contacts and provide 2 or 3 selectable speeds. A joystick control built for this application would not have to have a resolution of 8 bits, but could, in fact, suffice with 2. Figure 1 shows a low-resolution static output joystick interface suitable for use in this application.

Each potentiometer is connected as a voltage divider between a reference voltage source of 3.9 V and ground. The voltage output of each potentiometer is, in turn, fed to a 2-bit, parallel analog-to-digital converter. This type of converter uses 4 comparators set for 25%, 50%, 75%, and 100% of full scale. If a voltage, when applied, is less than 0.975 V, all comparator outputs will be at 0 V. At 1.0 V, corresponding to the joystick being moved 25% of full scale, the least significant bit (LSB) of the converter will be a logic 1, while the other bits are low. Similarly, at full input all

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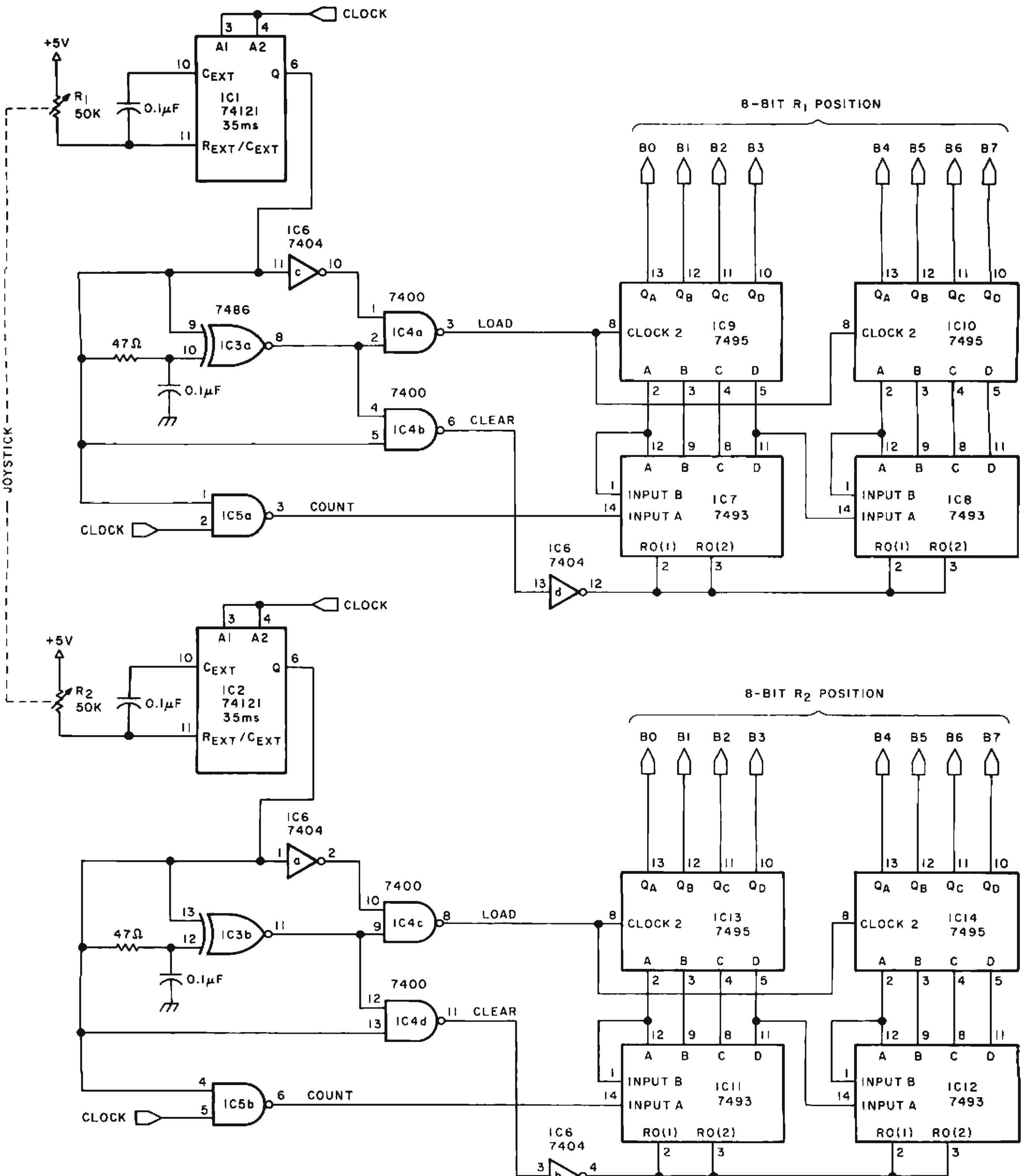
comparators will be triggered, and bits 0 thru 3 will be logical 1s.

Additional encoding logic can be added to produce a true 2-bit representation from the 4 comparators, but it is just as easy for a computer to interpret it directly. With a 4-bit connection as shown, used in a BASIC program, 25% of full scale would be 1 decimal, 50% of full scale would be 3 decimal, 75% of full scale would be 7 decimal, and full scale would be 15 decimal. It should be easy to trigger any action by a coincidence with these values. The real significance of this method is that the potentiometer position is presented statically to the computer and requires no other interaction. This makes it ideal for direct use with BASIC.



High-Resolution Static Interface

It is quite possible that 2 bits of resolution is not enough for your application, but direct compatibility with a slow, high-level language is still a requirement. Expanding the parallel comparator method will work in theory, but you must realize that a 4-bit analog-to-digital converter uses 15 comparators, and an 8-bit, parallel analog-to-digital converter needs 255 comparators! So much for that method.

Realizing that the output of the joystick is a variable resistance, we can use this to advantage. This resistance can set the *time constant* of a function which has a pulse width proportional to joystick position. Figure 2 illustrates an interface design which uses this technique.

The 2 joystick potentiometers R1 and R2 control the pulse width of a one-shot (monostable multivibrator). The one-shot has a pulse width of 35 ms when the potentiometer is at 50 k ohm full scale and something less than 100 μs at 0% of full scale. A 7.5 kHz clock signal asynchronously triggers the one-shots. When the one-shot fires, its duration is proportional to the joystick position and will vary from approximately 0 to 35 ms. Using midscale pulse width of 17 ms as an example, the circuit timing is as in figure 3.

On the leading edge of the one-shot signal, a *clear* pulse is generated through an edge detector configured 7486 device. The clear pulse resets the 2 7493s which form an 8-bit counter. Once cleared, the counters start counting clock pulses for the duration of the one-shot's period. On its trailing edge, a *load* pulse is generated which loads this 8-bit count into an 8-bit storage register. The computer is connected to read this 8-bit value through a parallel input port. Successive clearing and counting operations update the register every 35 ms or so (worst case). The clock rate is 7.5 kHz which has a period of 133 μs. If the one-sho. has a pulse width of 17 ms, then 127 clock pulses would be gated to the counter. Of a total possible 255 counts, 127 would represent 50% of full scale.

Software-Driven Interfaces

So far I have discussed only static interfaces. If the computer used with the joystick has sufficient speed and excess computing time available, then it is reasonable to use the computer to directly determine the one-shot period.

Figure 4 shows a circuit which directly connects to the computer bus and demonstrates this technique. The circuit as shown is wired for I/O (input/output) port decimal 255 or hexadecimal FF. The 4 joystick potentiometers are used as the timing resistors on 4 NE555-type one-shots. When an OUT 0, FF is executed in assembly language, it triggers all 4 one-shots. To keep track of the pulse widths, a 74125 3-state driver gates the one-shot outputs onto the data bus during an IN FF instruction. By looping through this program a number of times and keeping track of the logic levels of the 4 one-shots, the computer can accurately determine joystick position in terms of loop counts of instruction times. Listing 1 is a program which does this for 1 potentiometer.

High-Resolution Analog-to-Digital

While all methods are in *some* way analog-to-digital converters, *the* last

Number	Type	+5 V	GND
IC1	74121	14	7
IC2	74121	14	7
IC3	7486	14	7
IC4	7400	14	7
IC5	7400	14	7
IC6	7404	14	7
IC7	7493	5	10
IC8	7493	5	10
IC9	7495	14	7
IC10	7495	14	7
IC11	7493	5	10
IC12	7493	5	10
IC13	7495	14	7
IC14	7495	14	7
IC15	NE555	8	1

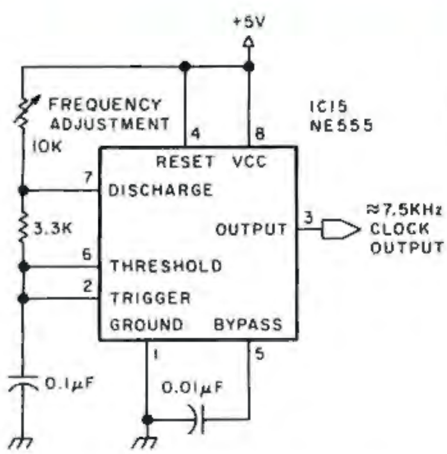


Figure 2: High-resolution, static interface. Each potentiometer in the joystick controls the pulse width of a one-shot. The pulse width can vary from 35 ms at full-scale to 100 μs at 0. If a joystick with 4 potentiometers is used, a duplicate circuit may be constructed for the 3rd and 4th potentiometers.

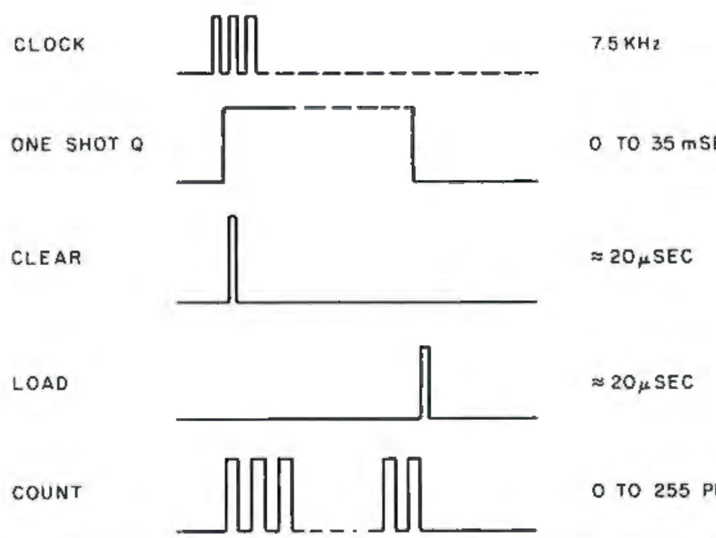


Figure 3: Timing diagram for interface of figure 2. The driving clock signal is 7.5 kHz. The one-shot can be triggered for periods of 0 to 35 ms, depending upon the position of the joystick. When a reading is to be taken, the counters are cleared. Counts are made until the one-shot signal drops, and then a load signal is sent to the interface. At this point the counter is read to determine the position of the joystick.

```
        MVI    B      clear B
        OUT    FF,0   trigger one-shots
AGAIN   INR    B      increment B register
        IN     FF     read potentiometers
        ANA    01     isolate bit 0
        JNZ    AGAIN  continue as long as one-shot is high
        HLT           value is in B register
```

Listing 1: A typical assembly language program for using the joystick interface of figure 4. After the one-shots are triggered, the program loops and checks the status of bit 0. When this bit is set, the conversion value is in register B. This program assumes that there is only 1 value being checked, and it is being input through bit 0.

method is in fact an 8-bit absolute-analog-to-digital converter, typical of the type used in computerized measurement applications. IC1 is an 8-bit digital-to-analog converter that produces an output voltage proportional to a digital input applied to pins 5 thru 12. For a complete explanation of this device, I refer you to a previous " Ciarcia's Circuit Cellar" article, "Control the World" (September 1977 BYTE, page 30). This article also outlines calibration and test procedures.

Number	Type	+5 V	GND
IC1	NE556	14	7
IC2	NE556	14	7
IC3	7430	14	7
IC4	7400	14	7
IC5	74125	14	7

The 3 basic sections are a computer-controlled voltage source (ICs 1 and 2), an analog-input multiplexer (IC3) which selects an individual joystick potentiometer by a 2-bit address code, and a comparator (IC4) which compares these voltages. In operation, the digital-to-analog converter is first set to 0 V out (hexadecimal 00 digital input to it) and 1 potentiometer is selected through the multiplexer. If V0 from the digital-to-analog converter is less than V_{in} from the potentiometer, the output will be logic 0. Next, the digital-to-analog converter input setting is incremented, and the comparator output is checked again.

Eventually an input count will be reached which will exceed V_{in}. The comparator output will then be a logic 1. The digital-to-analog converter input count is now the value of the voltage V_{in}. The worst case requires 256 iterations using this

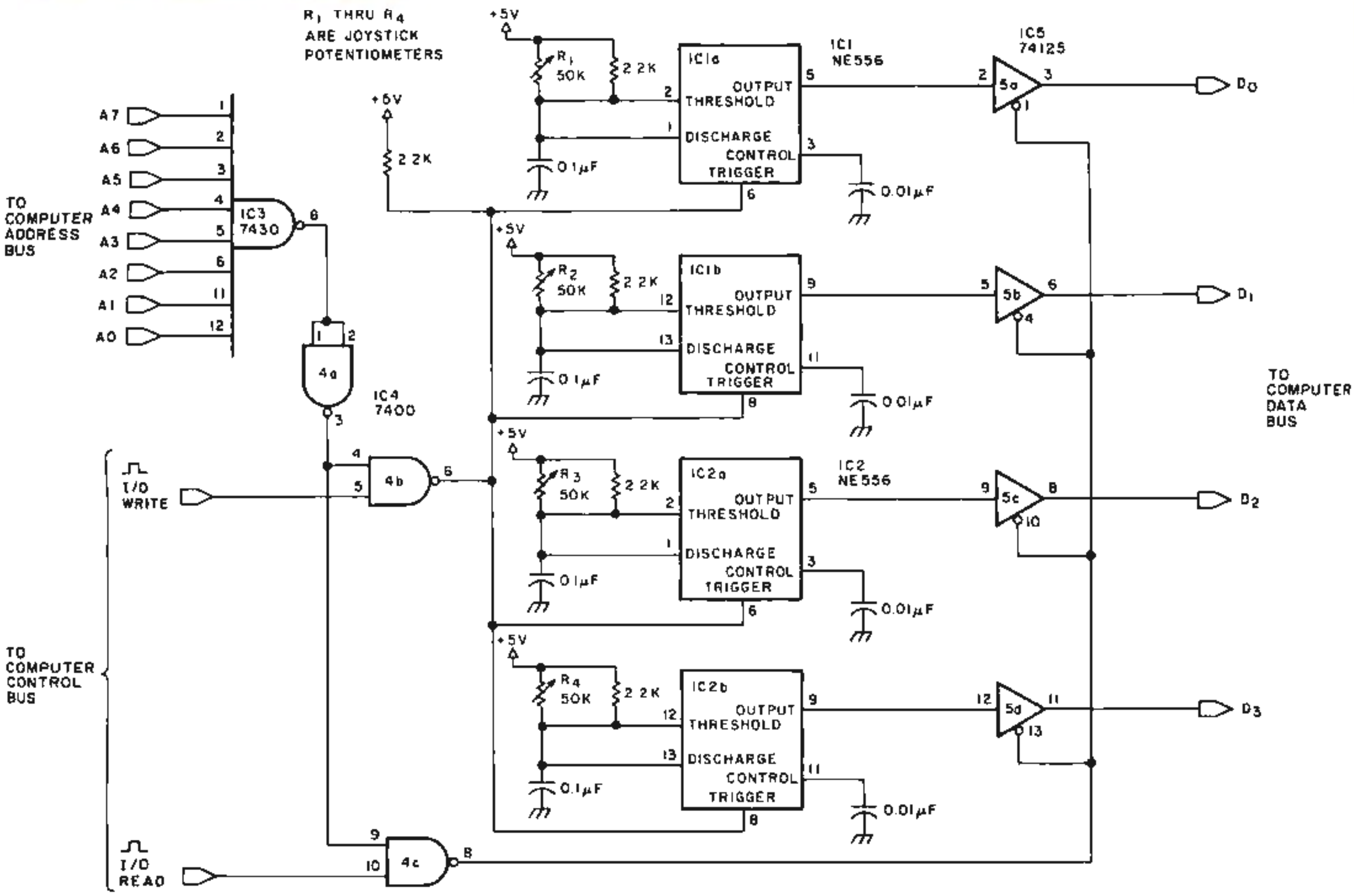


Figure 4: Software-driven interface. If the computer can directly read the input from the joystick interface, the hardware required can be greatly simplified. When hexadecimal FF is output to port 0, all 4 one-shots are triggered. The pulse width is then determined by a program running through a short loop looking at the logic levels of the 4 one-shots. Listing 1 shows a typical program for this application.

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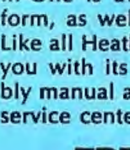

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Number	Type	+5 V	GND	+15 V	+15 V
IC1	MC1408-L8	13	2	3	
IC2	LM301A			4	7
IC3	CD4051		4		8
IC4	LM301A			4	7

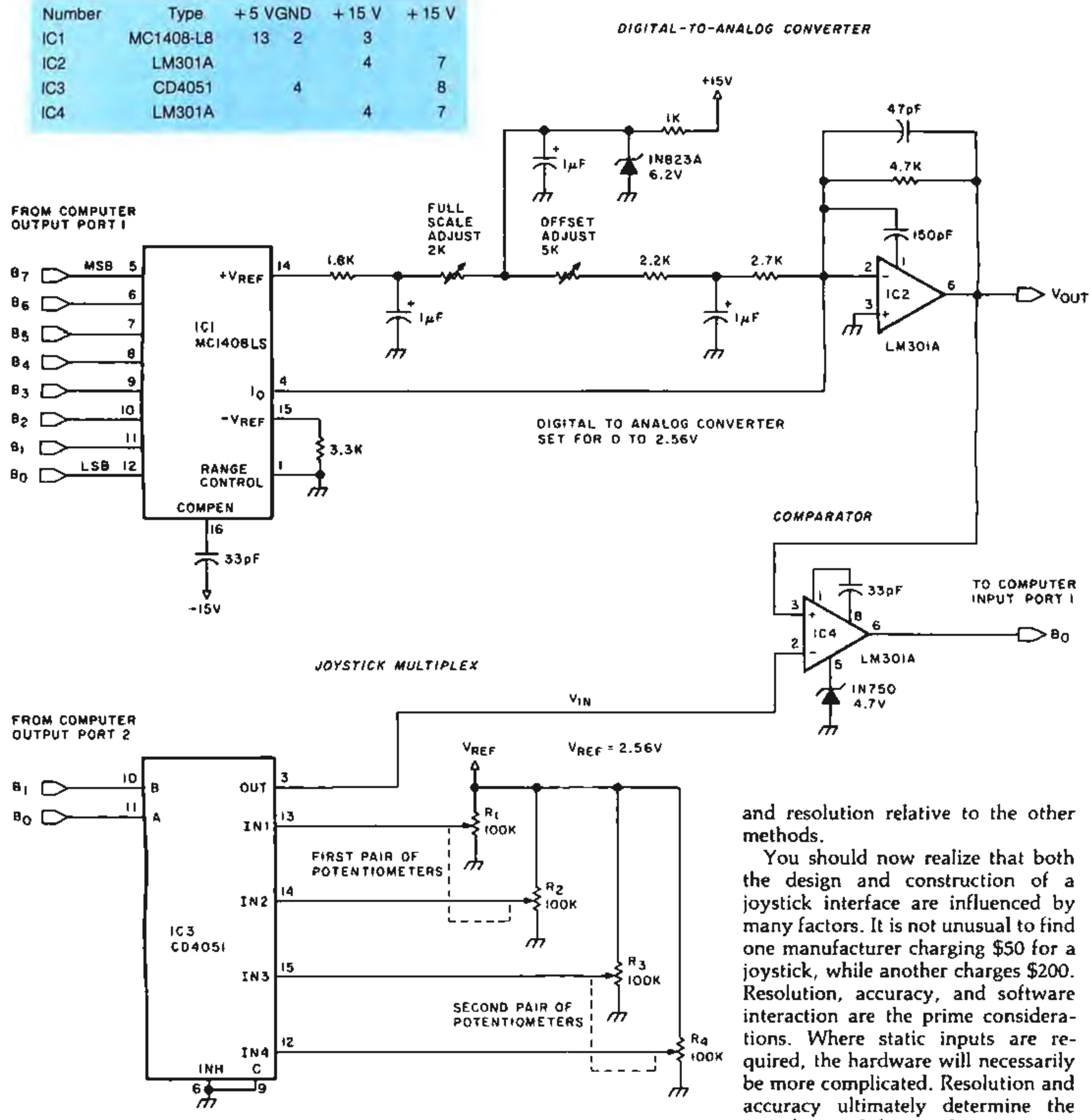

Figure 5: High-resolution analog-to-digital conversion. This hardware-oriented device multiplexes 4 voltage inputs (from the joystick potentiometers) and has the capability of handling 4 more voltages.

method. A better technique is successive approximation where the computer progresses through a binary search to "zero in" on the final value. A full explanation of successive approximation is delineated in my article entitled "Talk to Me: Add a Voice to Your Computer for $35" (June 1978 BYTE, page 142).

With the digital-to-analog converter set for a full-scale value of 2.56 V, each count is equivalent to 10 mV. Only 4 channels of the CD4051 are used for the joysticks, leaving another 4 channels as auxiliary inputs from external sources. Thus it is possible for this interface to serve a dual role because of its high accuracy and resolution relative to the other methods.

You should now realize that both the design and construction of a joystick interface are influenced by many factors. It is not unusual to find one manufacturer charging $50 for a joystick, while another charges $200. Resolution, accuracy, and software interaction are the prime considerations. Where static inputs are required, the hardware will necessarily be more complicated. Resolution and accuracy ultimately determine the complexity of the interface.

For simple spacewar-type games, the circuit of figure 1 should suffice. For more demanding applications such as cursor control in a high-resolution graphics system, figure 5 may be the optimum choice. Be careful when buying joystick interfaces. Make sure that they mate with your program requirements and your system's abilities.

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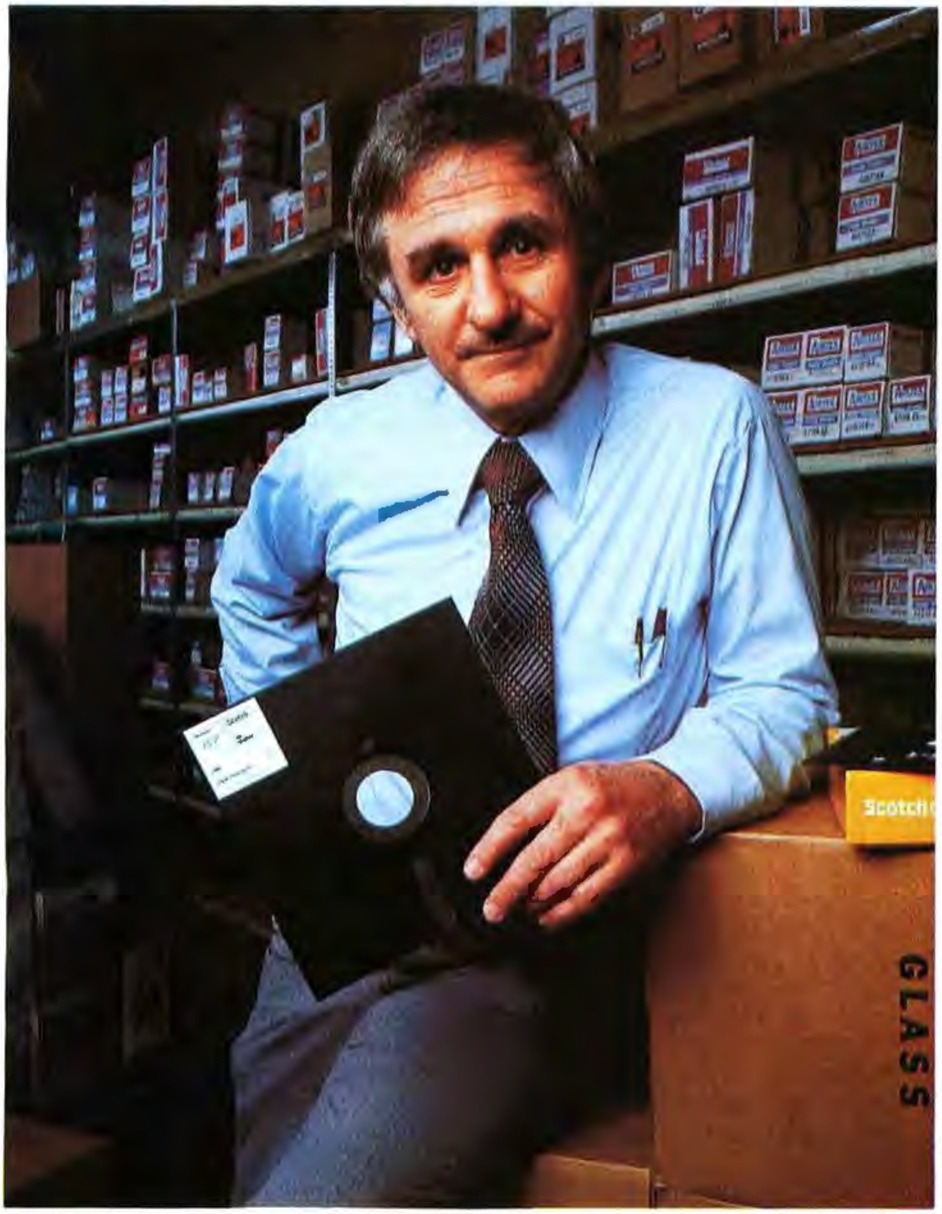

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Introduction to Multiprogramming

Mark Dahmke
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Multiprogramming has usually been considered out of reach of the average personal computer experimenter using a small or medium scale computer. Actually, anyone with a processor above the level of an 8008 can operate a multiprogram or multiuser system. The original purpose of multiprogramming was to allow more than 1 user to take advantage of a computer simultaneously. This increased the productivity of the machine by allowing programs to run while other programs were awaiting user input, access to a disk, etc.

This may seem to conflict with the advantages inherent in microprocessor based systems (single user systems and low cost). However, there are many instances where the ability to run more than 1 program at a time may be advantageous. Note that the statement "more than 1 program may run at a time" does not mean simultaneous execution. That is the definition of multiprocessing (more than 1 processor on the bus), not multiprogramming.

To describe multiprogramming more effectively, I shall refer to a more well-known function in computers: real-time interrupts. Suppose we are using a microcomputer to manage the environment in a small office building. Normally we want to continually poll (scan) the sensors that are distributed throughout the building and adjust heating, cooling and lights on the basis of temperature and time of day. Let us say that during normal operation, someone in the building wants to change the temperature of an office.

One way to do this is to have a video terminal and keyboard attached to the system that generates an interrupt when a keyboard request is made. Upon receiving the interrupt, the computer saves the status of the current program and enters or transfers control to the keyboard read routine. As soon as the user has made the desired change, the system loads the old status information and returns to the original program. This same interrupt technique could be used to design a time shared system that would allow several terminals to be hooked up to a processor. Each terminal would generate an interrupt, and whichever program was active would be put in a wait state. This arrangement only works well for a few terminals, though. You can imagine what would happen if everyone happened to press a key at the same time.

Figure 1 shows timing comparisons of several modes of operation already discussed. In figure 1a 2 independent processors are shown, each doing something different and neither interfering with the other. This is known as multiprocessing. The processors may or may not be sharing I/O(input/output) terminals or memory.

In figure 1b 2 processors are shown in a *master-slave* arrangement. Perhaps the slave processor performs floating point arithmetic or some complex I/O function. The master processor can give the slave processor commands via an interrupt and continue other processing until the slave informs it that it has finished the desired operation.

Figure 1c shows a single processor with an interrupt being applied. The processor temporarily gives control to the routine specified by the interrupt hardware and begins executing it. When complete, it returns control to the main program. Figure 1d shows the multiterminal timeshare system. Usually the interrupt hardware contains provisions for daisy chaining or prioritizing the interrupts as they come in. Thus, if terminal 6 applies an interrupt and the processor is busy with terminal 7, terminal 6 is not allowed to interrupt the processor until terminal 7 is finished.

Using multiprogramming is like using real-time interrupts. A multiprogrammed system uses interrupts, but in a more efficient way. Imagine a simple 2 program situation. Suppose program A is running and no other

About the Author

Mark Dahmke is currently employed by the University of Nebraska Computer Network as a programmer/analyst in the Academic Computing Services section. He is also a senior computer science major. At home, Mark owns an 8080 based system with 32 K bytes of memory and dual iCOM floppy disk drives. His work involves graphics, electronics, writing, systems programming and speech synthesis.

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COMPUTER SYSTEMS 2338A WALSH AVENUE • SANTA CLARA • CA 95050 • (408) 244-5766 programs have been started. Then a user initiates (loads) another program called B. How will program B gain control of the system so that it might start to execute?

The process of passing control from one program to the next is usually handled by an operating system module referred to as an *interrupt call* routine. Normally, to save the programmer the trouble of making sure that this routine gets called at regular intervals, the routine is usually imbedded in many of the I/O driver routines or other standard utility subroutines on a system. Note that this technique will in no way upset any of the flags or registers of the routine it is called from.

This interrupt call program will:

1. Determine if any other programs are waiting to execute.
2. If so, save all registers and flags on the stack and save the address of the current program's stack pointer in a special table in memory.
3. Load the new program's stack pointer from the table, pop all registers and flags off the stack.
4. Return to the new program.

Loading the new stack pointer raises some interesting questions. If program B has not yet begun, how could its registers have been pushed onto its stack? Figure 2 shows the stacks of both programs as they would be at each step in the previously described interrupt call routine. Part of the job of the routine that initialized program B is to set up a dummy stack and stack pointer such that the program counter address on the top of the stack contains the entry point of program B. Thus, when the interrupt call routine reaches step 4, it will execute a return instruction, then pop the entry point address off the stack and begin executing program B. When the interrupt routine is called again, it will see that program A is waiting and will save all of program B's registers and flags, swap stack pointers and return to program A at the point where it was first interrupted.

All this activity will take place every time the interrupt routine is called, but if one of the programs gets caught in an infinite loop, the interrupt call routine may not get called. The simplest way to avoid this kind of problem is to add some hardware to provide external timed interrupts. As shown in figure 3, the interrupt timer is set to provide an interrupt every 10 ms. A reset line is provided

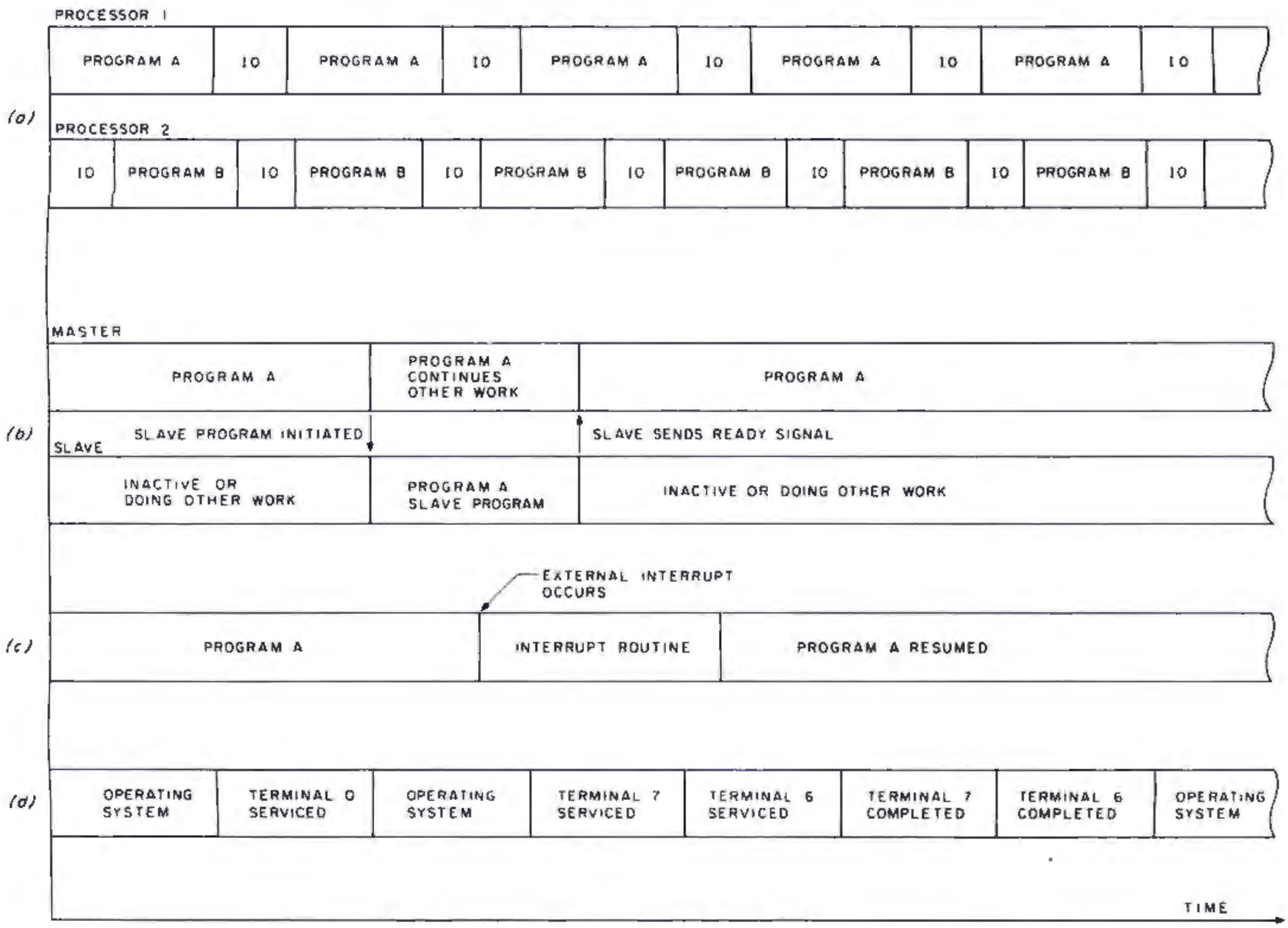


Figure 1: Timing diagrams for 4 different system organizations. Figure 1a is a multiprocessing example using 2 independent processors. Figure 1b is a multiprocessing example using 2 processors connected in a master-slave configuration. Figure 1c is a single processor with 1 level of interrupt. Figure 1d is a single processor with 8 levels of interrupts. Each of the 8 levels is activated by 1 of 8 terminals.

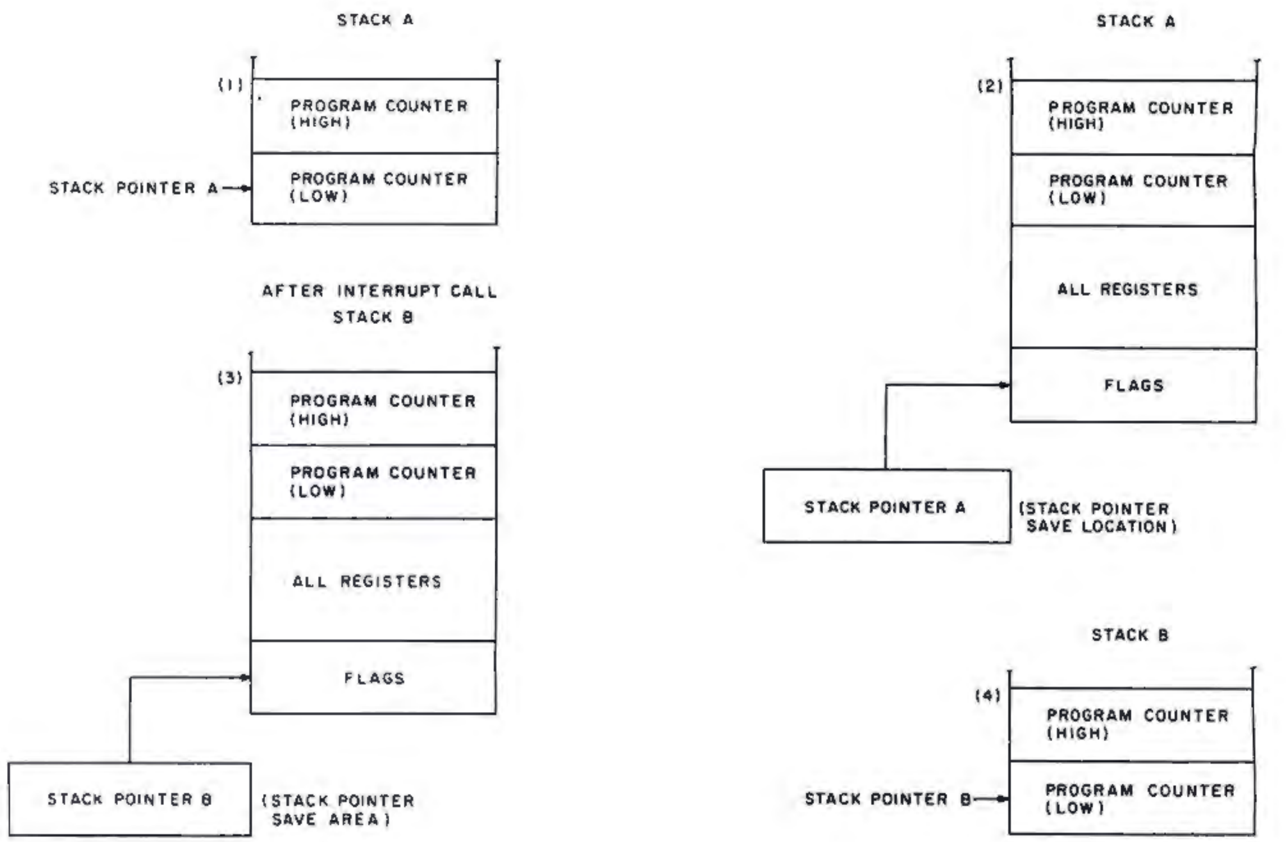


Figure 2: Arrangement of all stacks and stack pointers at each interval of an interrupt call routine.

in the event that the interrupt routine is manually called (through the software method). The timer may be reset to give the program its full 10 ms. A disable line is provided to allow the user to turn off the timer for special applications (software timing) in which the processor must not be interrupted.

Figure 4 shows our previous example of figure 1, but with the extra hardware generated interrupts added. In figure 4a some software interrupts are mixed in with the hardware interrupts. The timer is reset after each call to the interrupt routine. Figure 4b is the same except that the timer is not reset after each call.

A Complete System

There are limitless ways to go about developing a computer system that will be easy to use. A look at the current market shows this to be true, perhaps even to a greater extent on the small systems level. I will not attempt to describe all possible variations available on a multiprogramming system, but I will try to give as generalized a view as possible.

First, we must consider what is necessary to make a useful system. The following are essential:

1. Some form of operating system that allows simplified user com-

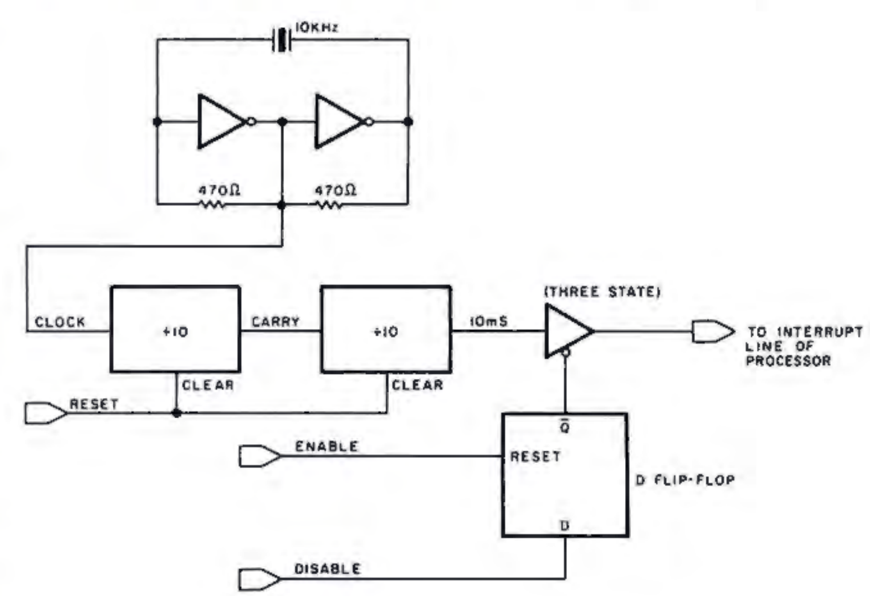


Figure 3: Simple hardware interrupt timer set for 10 ms intervals.

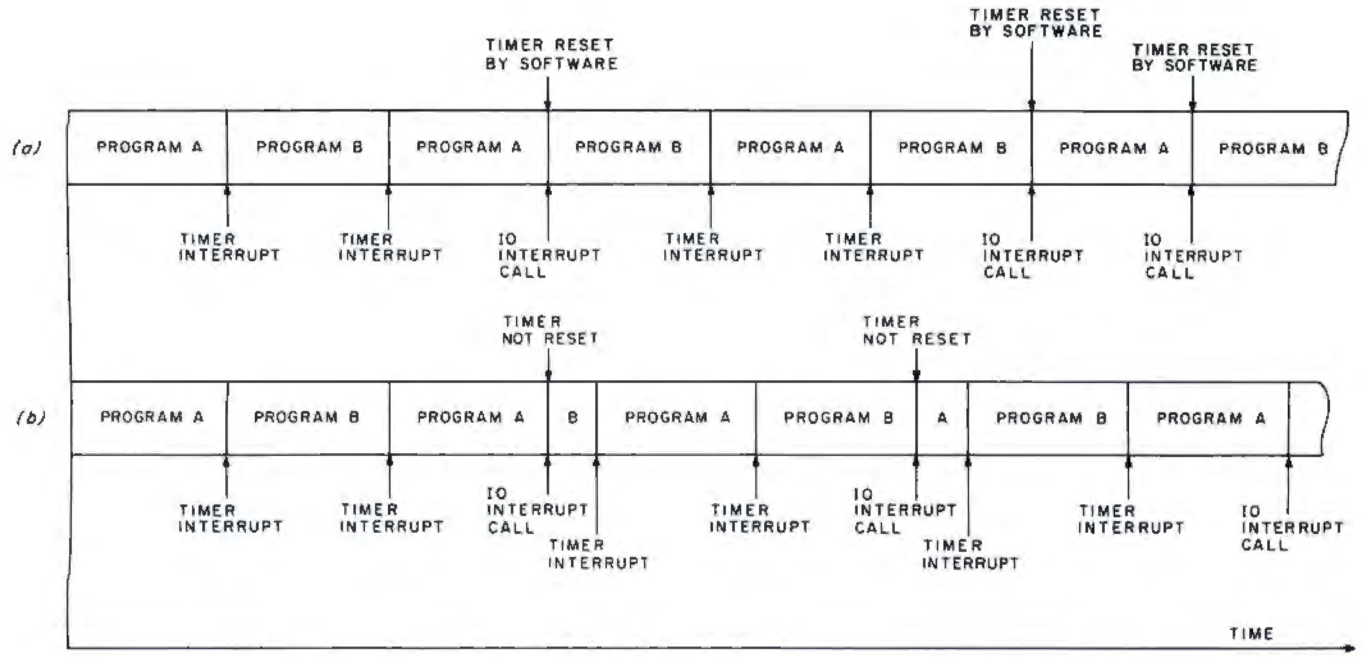


Figure 4: Interrupt timing example of figure 1 reviewed with the addition of a hardware timer. The timer may be used in 2 ways: The example in figure 4a resets the timer on each interrupt call. This allows each program to receive its full 10 ms time slot. The example in figure 4b does not reset the timer. Therefore, a hardware interrupt occurs every 10 ms.

munications (ie: BASIC, DOS, CPM).

2. Convenient mass storage I/O (cassette or disk).
3. Sufficient memory to handle all programs.

Another consideration might be the internal architecture of the processor, but that is another level of problem.

Figure 5 shows the memory layout of a typical multiprogramming system. To maintain a simple system, I have combined the operating system with the timesharing routines that support all terminals (video displays, keyboards and teletypewriters). This means that each time the operating system gains control (through an interrupt call or timer interrupt), it will complete its own activity and then transfer control to the timesharing program for the remainder of the time slot. If the operating system is given highest priority, the response times of the terminals should not suffer. The operation of the timeshare program can be treated as a multiprogram system in miniature, where each terminal is given a time slot, or it may be designed to simply scan the terminals, choosing a new terminal each time it is given control.

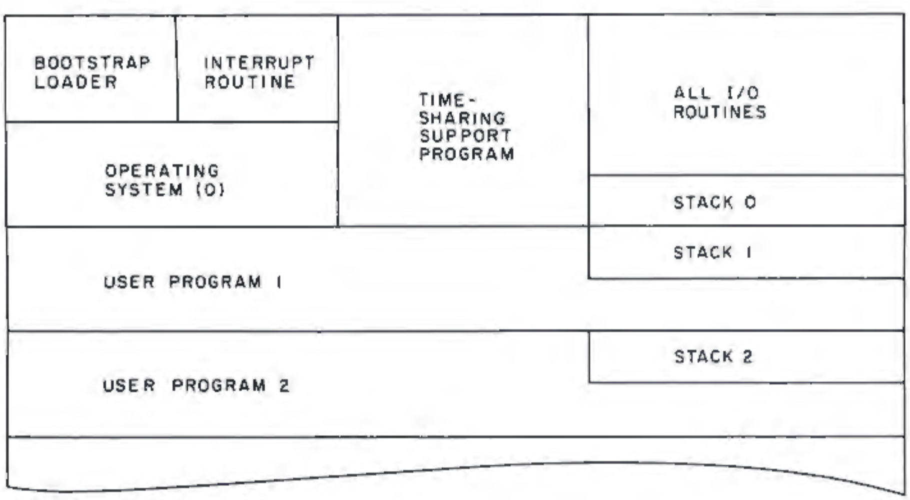
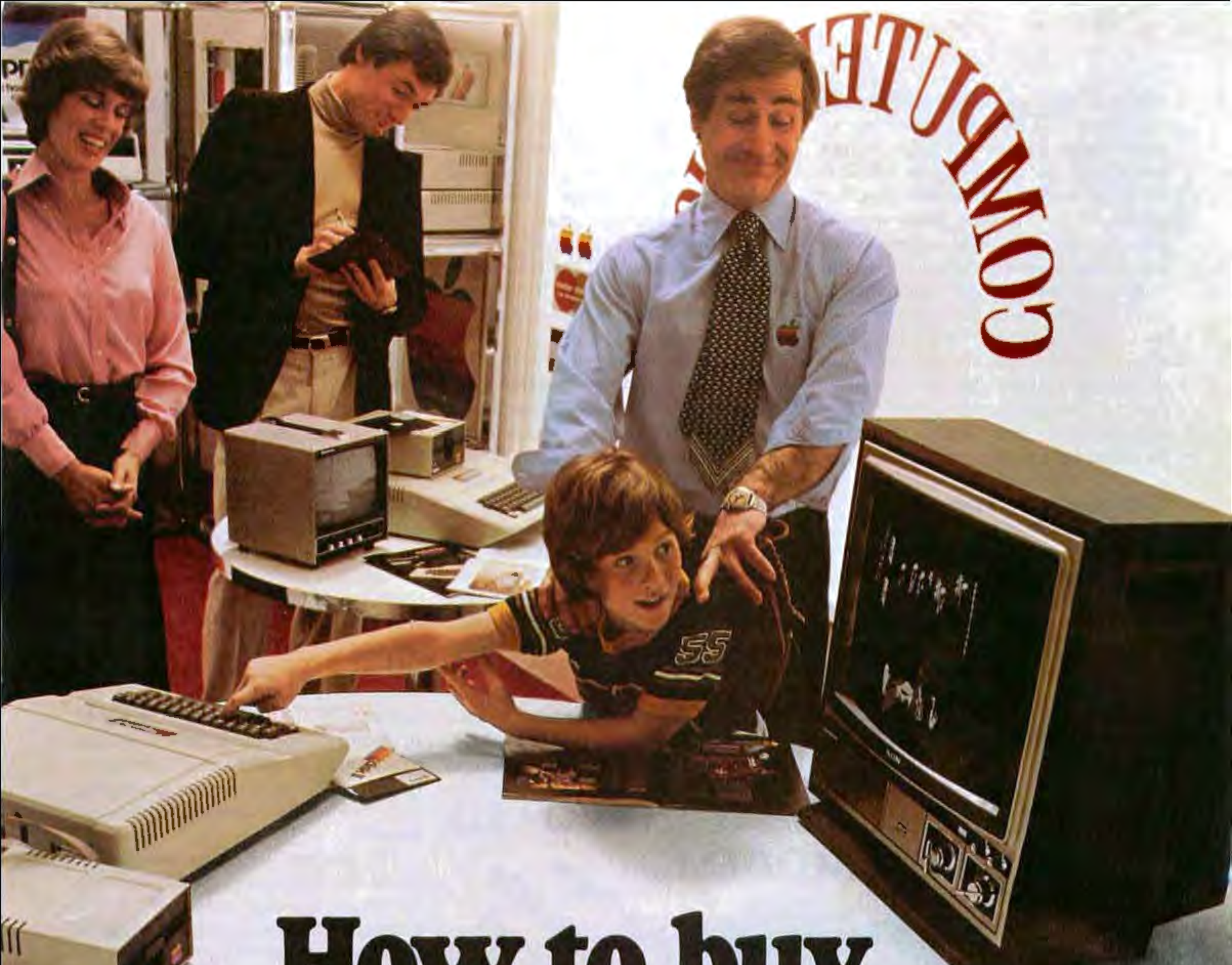


Figure 5: System geography of a typical multiprogramming system with space for the operating system and 2 other programs.

Controlling I/O

Many programmers have discovered the convenience of vectoring all I/O through 1 subroutine; this simplifies programming greatly and makes system changes much easier. Typically, 1 subroutine will accept an operand (if necessary) and an operator function code passed from the main program and will decide which I/O function to perform. In my hypothetical computer, this approach will be used. Note that in some large computer systems, the I/O driver programs can only be accessed by executing a special kind of interrupt call that informs the operating system that the user's program desires to perform some kind of input or output operation. The operating system then takes charge, performs the I/O for the program in question, and returns pointers telling where the input data was stored in memory or that the requested output function has been completed.

This type of I/O handling is necessary because the I/O controllers are extremely complex and are capable of performing an entire I/O operation



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without processor intervention. In fact, it would be very inefficient to make the processor of a large system perform these menial tasks when it could be working on more important programs. In microcomputer systems we are not normally concerned with the optimization of I/O functions and it does not really hurt performance to have the processor perform most of the I/O. Consequently, the I/O driver routines in the system I am describing will not be considered as part of the operating system. They are just utility subroutines that may be called by the user's program.

Defining the Necessary Tables

With only 2 programs very few, if any tables are needed to tell the interrupt routine which program was active at the instant the system was interrupted and which program is next in line. But imagine a system capable of supporting 10 or more programs: some form of priority scheduling will be needed, as well as a table to hold all of the stack pointers of the inactive programs.

To handle the list of programs (herein referred to as tasks), we must define a *task control table* that keeps track of a number of pointers and descriptors. First, each entry will begin with the task number that uniquely defines each task. Next, we will include the priority of the task on an arbitrary scale of 0 to 10. It will then get the processor before a task of lower priority (10 is highest). If 2 tasks have the same priority, the first one in line in the task control table will get control. The task control table must also keep track of the last value of the stack of each task and whether or not the task may be interrupted (in the case of critical timing loops).

Another important status byte that must be kept is the *current activity indicator*. This byte contains the task number of the currently active task. Now let us assume that we have 3 different tasks running and all have been initialized (stored in the task control table). The first task has a task number of 0 and a priority of 10. Generally the operating system is given the task number 0 designation. Since the operating system and timeshare program (user terminals) are considered one big program in this example, task 0 is also the designation of the timeshare system. Task 1 is a program that one of the users submitted (initiated) from a terminal; it has a priority of 10. Task 2 was also loaded and initiated by a user through the timeshare terminals, and it has a priority of 10.

Imagine that the timeshare program calls the I/O driver program to write a character out to a terminal. Since there could be many terminals connected to the system, how does the program know which one to write to? It would be very inefficient to have different routines for each device, but the only way that a program could tell the I/O driver which specific display to write to is for the calling program to know the physical address of that terminal. Passing the actual address of the device ruins the neatness of the I/O routine, though. It is more convenient to specify the function to be performed (1 = write to video display; 2 = read keyboard; 3 = write to cassette; 4 = read cassette).

The solution is to have another entry in the task control table called a *communications control block* pointer that points to the location of the communications control block for the particular task. Since each task is given its own block, the user may define his or her own functions and addresses. Thus each program may have its own video display, keyboard, cassette interface and disk. The communications control block contains a list of function numbers, the address of the I/O port or memory mapped port, and the address of the I/O subroutine that will perform the operation. Figure 6 shows the arrangement of all tables.

Starting and Stopping

To initialize a new task, the user adds entries to the appropriate tables through a console command and causes a dummy stack and stack pointer to be created. To stop a task, the last thing done in the task is to call a subroutine that would remove its task control table entry. This is equivalent to a CALL EXIT in FORTRAN found on many larger systems.

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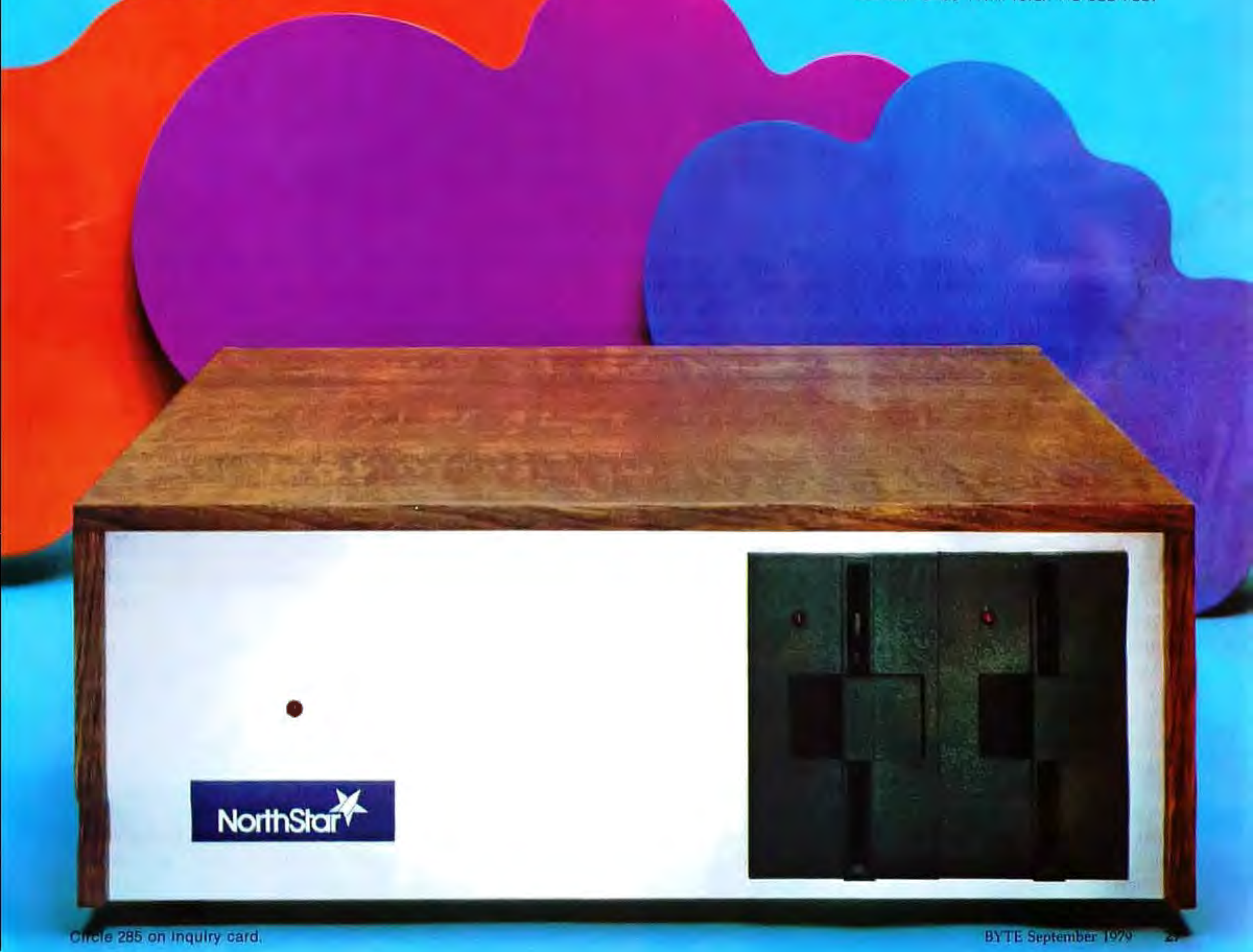


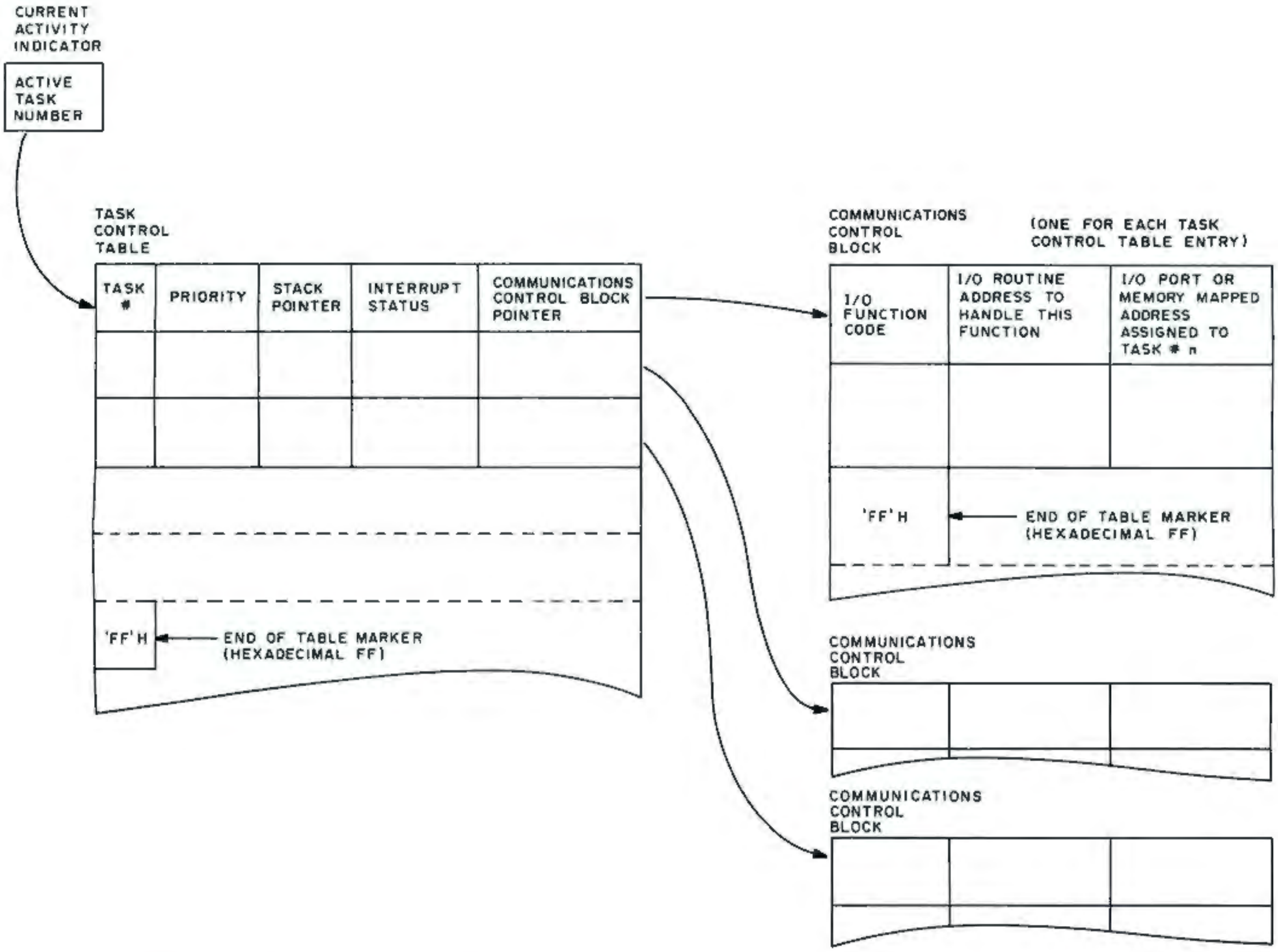


Figure 6: Control table organization. The current activity indicator contains the task number of the active task. The task control table contains the task number, task priority, last value of stack pointer, interrupt status flag (1 for yes, 0 for no interrupts), and the pointer to the task's communications control block. The communications control block contains the I/O (input/output) function code, address of I/O driver routine associated with the function code, and the I/O port or memory mapped address assigned to the task for the particular function. One entry is provided for each function code used in the task. The owner of the task may add entries to the communications control block for specialized I/O driver requirements.

Example

The easiest way to show how all tables and pointers affect each other and the system is to observe them during a short period of machine activity. As we begin, task 0 (the operating system and timeshare routines) has control, and a timer interrupt is occurring. There are 2 other tasks in memory: task 1 has priority 5 and task 2 has priority 4.

First, as the interrupt routine is entered it saves all registers and flags of task 0 on stack 0 and saves the task 0 stack pointer in the task 0 task control table entry (see figure 7). Next, it scans the task control table for the task of next highest priority, moves the new task number (task 1) to the current activity indicator, moves the task 1 stack pointer from the task control table to the processor's stack pointer, pops all of task 1's registers and flags off of stack 1, and executes a return, which has the effect of popping the program counter and jumping to that address.

Task 1, while executing, encounters a call to the I/O driver routine with a request for a keyboard input (see figure 8). When the I/O driver routine is entered, it scans the task control table to find the communication control block pointer entry for task 1 (the routine determines which task called it by looking at the current activity indicator), then scans the communication control block for the function number entry corresponding to the one passed by the main program. Even though the computer may have 5 or more keyboards attached to it, the port address found in the communication control block gives it the address of the keyboard assigned to task 1.

Since the keyboard read routine is a common one, the address referred to in the communication control block points to a subroutine located within the operating system area. Note that if the user had need for some special I/O subroutine, he could locate it in his own memory area and put the address in his communication control block as another function code.

Returning to the example, the keyboard read subroutine is called from the I/O driver, reads the keyboard port assigned to task 1, and returns to the I/O driver with the ASCII code. The I/O driver returns to the main program with the ASCII code in a register or memory location. In figure 9 the next timer interrupt has occurred, so control returns to the interrupt handler routine. Again, the interrupt routine saves all registers and flags of task 1 on stack 1, looks at the current activity indicator to see which program was last active, saves the stack pointer in the task 1 task control table entry, scans the task control table for the next highest priority task, and finds that task 2 should get control. The stack pointer for task 2 is loaded from the task control table, all registers and flags are popped off of stack 2 and again a return is executed that causes task 2 to take control.

In the next step (shown in figure 10), task 2 has encountered the equivalent of a CALL EXIT or STOP command and has finished processing. This CALL EXIT calls a terminator routine which again finds out who called it (via the current activity indicator) and simply eradicates the task control table entry for that task. To keep things neat, all succeeding table entries are moved up 1 notch. Then, control is returned to the interrupt handler, which will find the next task in line. In this case, since no other tasks of lower priority are waiting, control is returned to the highest priority task 0.

Error Handling

On a single program system, error handling is something that the user can watch for manually. When several programs are running, the system must have routines to handle errors rapidly so that other programs will not be slowed down or destroyed. There are many common errors that are relatively easy to deal with. Executing an invalid op code or forgetting to put in the 2nd or 3rd byte of a multibyte op code can be handled through a simple system restart (through the interrupt handler routine) without losing continuity. But what about a program loop that accidentally destroys part or all of another user's program? On an IBM 360, all memory blocks assigned to a task are given a unique 4-bit protect key (which is the same as the task number) that is stored in external hardware.

One approach might involve having 2 external 16-bit registers that could be loaded by the interrupt routine with the high and low memory addresses of the active task. Then, every time the address bus has a valid address on it, it is tested against these registers. However, special precautions would have to be taken in those cases in which a utility in low memory (I/O driver routine etc) is called, or when memory mapped I/O ports outside these address limits are used.

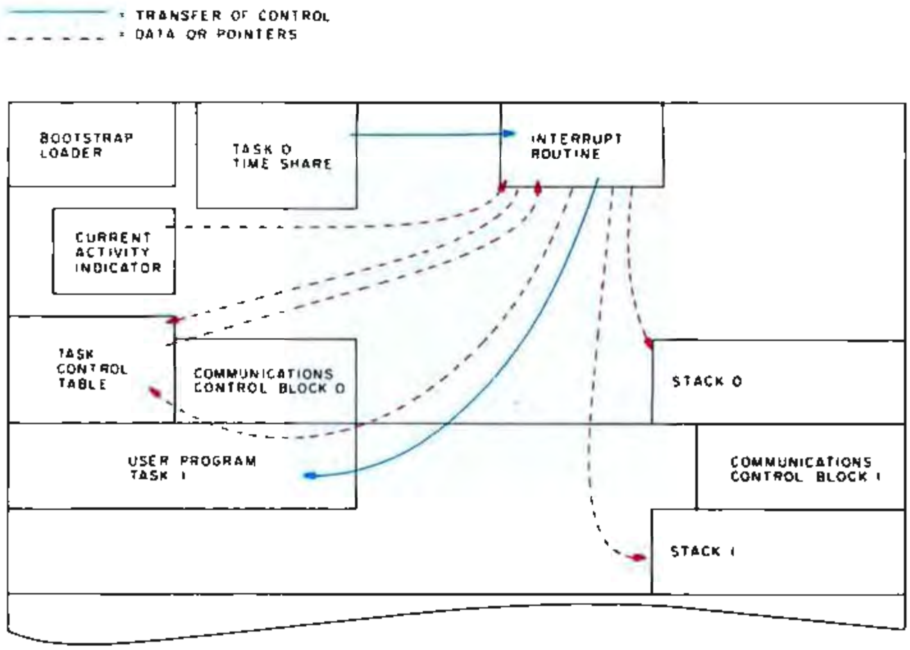


Figure 7: Task 0 has control of the processor and has just been interrupted. The interrupt routine looks at all pointers, saves the status, and then transfers control to task 1.

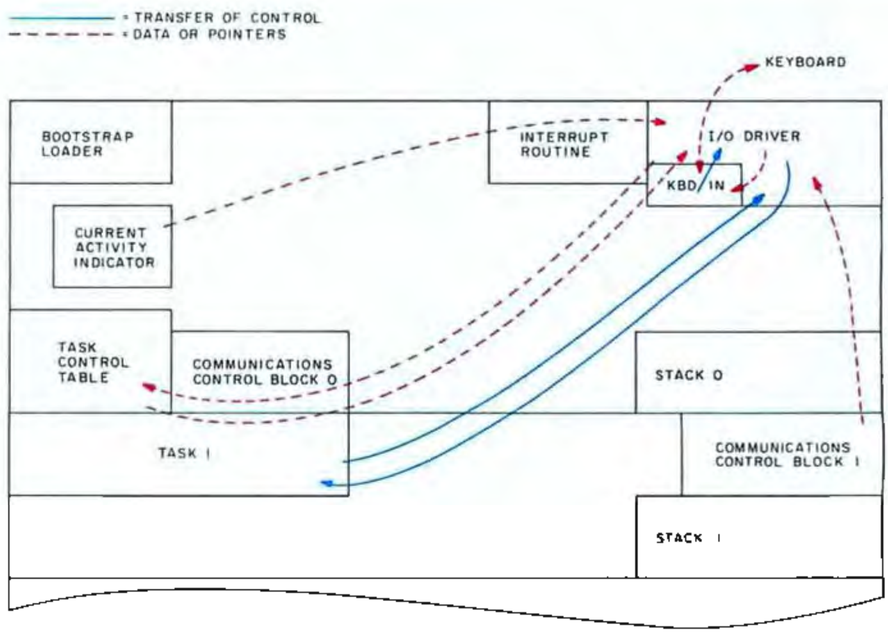


Figure 8: Task 1 has requested keyboard input from its assigned keyboard. When the input is completed, the I/O (input/output) driver returns control to task 1.

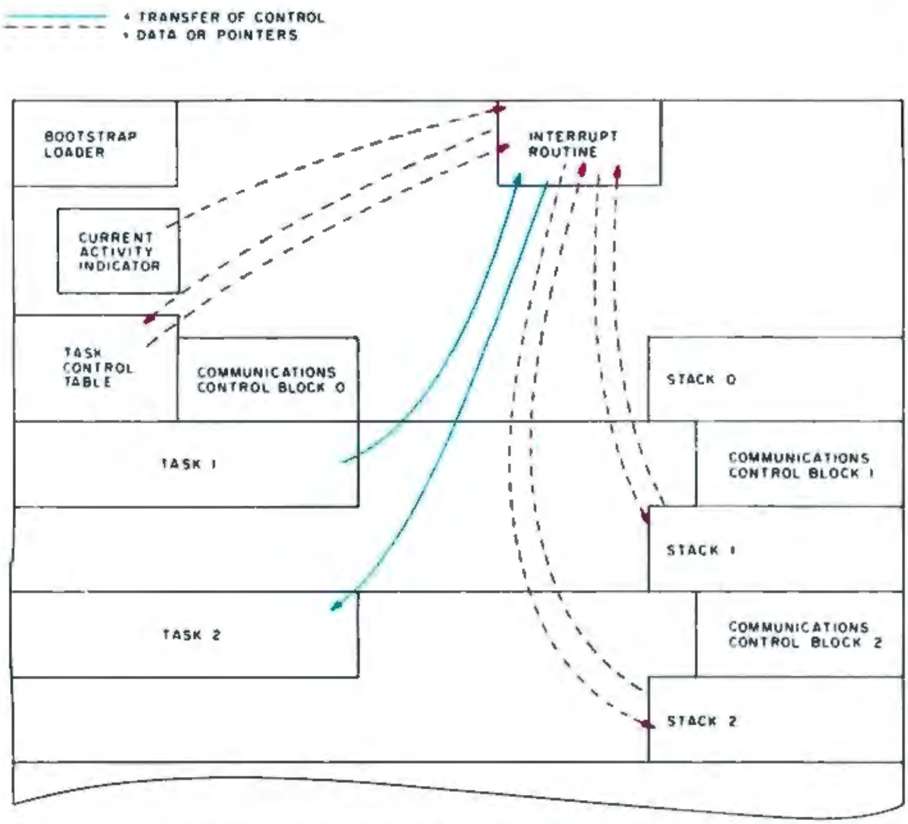
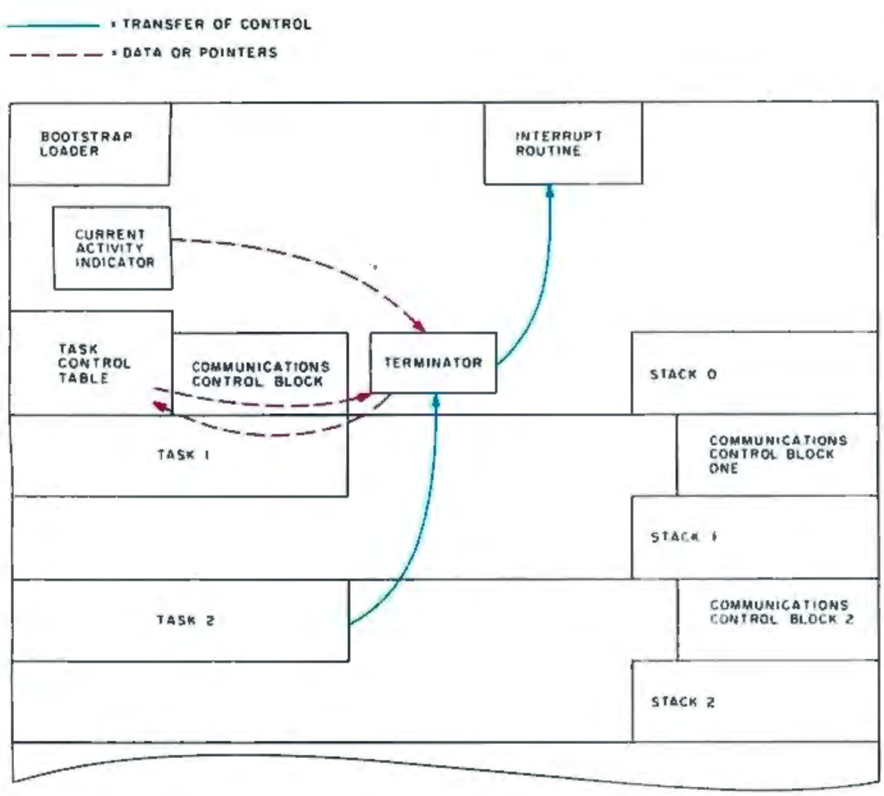


Figure 9: Task 1 has been interrupted and turns control over to the interrupt routine. Control is then passed to task 2.



Resolving Allocation Conflicts

Allocating I/O devices has been a problem since the early days of computers. Devices like tape drives and card readers (sequential devices) are nonshareable: only 1 program may use them at a time. However, disk drives are considered shareable, since the head may be positioned at random to gather data. The simplest method that can be applied to the system described in this article would be to have the initiator program check all communication control blocks to make sure that certain devices are not assigned more than once.

I/O Software Considerations

As mentioned earlier, I/O techniques in use on small systems leave all control up to the processor. If special timing is needed or if strobes or ready flags have to be checked, software is used instead of extra hardware, as in the case of larger systems. This in itself is good from the standpoint of economy, but requires that special care be taken when writing the driver and controller software.

For example, suppose a cassette read routine uses a universal asynchronous receiver transmitter (UART) implemented in software as an algorithm instead of hardware. In a nonmultitasking system, the program may simply loop and time down between bits, but in a multitask system the timer interrupt would surely halt the activity and execute other programs. It may be well over 30 ms before it can return to the cassette read routine. It is easy to see what can happen to critical timing loops on a system that uses any kind of interrupts.

The solution? If you must do the critical timing in software, it is necessary to turn off the interrupt timer while in the critical loop and reactivate it when in noncritical parts of the routine. If external hardware is used, and internal timing is reduced

Figure 10. Task 2 has completed its execution and encounters a CALL EXIT. Control is given to the terminator routine which performs some cleanup operations and removes the task 2 entry from the task control table, effectively destroying the task. Control is then given to the interrupt routine which again scans the task control table to find the next task awaiting execution.

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to noncritical loops, the intervention of the multitask interrupt timer will not normally affect the system. If the interrupt timer causes an interrupt just before a byte is received by the UART but returns in time for the next byte to be received, the easiest way to assure that the cassette read routine does not drop a byte is to set the timing of the interrupt oscillator to at least twice as fast as the transmission rate of the UART. This greatly reduces chances of losing a byte.

An alternate approach is to have even more hardware that forces the interrupt timer to timeout and return control to the program awaiting the *data transfer* operation when the incoming data is present. A third way involves the use of direct memory access (DMA) capability, in which the external controller reads the UART and deposits the data directly into memory. With this approach, the calling program need only initialize the external registers and go into a wait state until the transfer is complete, allowing the rest of the tasks to execute normally. This last approach is used on many large systems and constitutes what is called a *channel*.

Managing the System

As you can see, many levels of activity are required to control a multiprogramming system properly. It is also apparent that some minimal hardware is required to prevent one user from obtaining exclusive control of the processor or writing over someone else's program or data. The use of control tables and a standard interrupt routine are also important as a way of letting the interrupt routines and I/O drivers know which task had control of the processor last.

If the user plans to run BASIC software or some other kind of language interpreter, the safety features discussed earlier may be implemented as part of the interpreter. To run a lower-level operating system that allows the user to generate assembler level code will generally require the hardware described in this article, thus safeguarding the system and its users from accidental loss of programs or data. In general, the use of timed interrupts allows for a fairly even distribution of processor activity, and depending on the cycle time of the host system, between 4 and 12 tasks may be handled without too noticeable a delay in response time. ■

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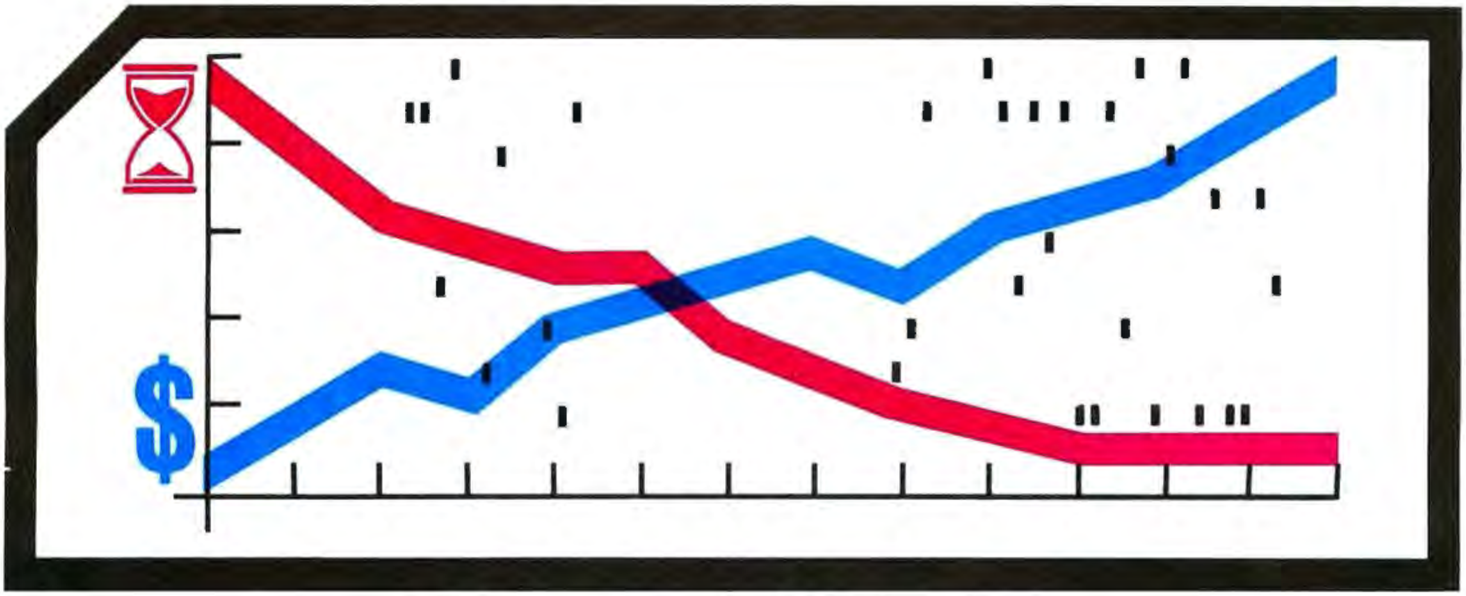

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Interface a Chessboard to Your KIM-1

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Chess is a fascinating game. Computer chess is especially fascinating because the complex analysis which determines each move is performed by a machine instead of a human. Computer chess offers an excellent way to demonstrate the power and versatility of personal computers.

Most computer chess systems are unable to "see" a chessboard. A human playing against a computer will usually set up a chessboard beside the computer, and the moves will be communicated to and from the machine through the use of a keyboard and a display in some type of abstract notation.

Keyboard entry of moves is undesirable. It is inconvenient, error prone, and inelegant. The abstract notation promotes errors and makes play difficult for people who do not know the notation system. Furthermore, errors may not be detected until many intervening moves have occurred.

An ideal chess-playing system would contain a digital television camera to observe the board and a mechanical arm to move the pieces. *[A mechanical arm designed for exactly this application was described in the article "A Hobbyist Robot Arm," by Keith Baxter and Timothy Daly in the February 1979 BYTE, page 84...***RSS***]* A less costly alternative is to construct a chessboard which can electronically communicate with the computer. The computer may then "look" at the board position through its I/O(input/output) ports. A means of indicating the computer's moves on the chessboard itself may also be provided.

In the system that I have constructed, the user makes his move on the electronic chessboard, instead of typing each move on a keyboard. The computer's moves are displayed on the chessboard through the use of discrete light emitting diodes (LEDs), arranged in an X,Y coordinate system. The LEDs show the user exactly which chessman the computer wants to move, and to which square. In addition to being aesthetically pleasing, this system makes it impossible to enter your move in-

Photo 1: Two pawns, a White Knight, and a loose rivet are shown on top of the electronic chessboard. One row of 8 light emitting diodes (LEDs) is placed along the left side of the board, and another row is placed along the bottom of the board as seen by the human player. Two LEDs are lit to indicate a single square, using an X,Y axis system. A single large hole is drilled in the center of each square to accept entrance of the rivet which is glued to the bottom of each chessman. The rivet completes an electrical circuit between 2 pieces of wire that run from smaller holes through the large central hole. This switching arrangement allows the computer to detect the presence or absence of a piece at each square of the board. In this prototype, an additional set of 3 wires is seen in each square; these wires remain from an earlier, unsuccessful switching attempt.

About the Author

Jeff Teeters is an undergraduate student at the University of Wisconsin at River Falls where he majors in mathematics.

correctly, and easy to interpret the computer's move. The board is continuously scanned so that even if the user moves the computer's piece incorrectly, the mistake is detected immediately. A speaker is connected to the computer to let unwary users know (by a buzz) when they misinterpret a computer move. This speaker also emits a brief sound when the chess program has decided on a move and when it has been recorded into the computer's internal board representation.

This project is designed for specific use with Peter Jenning's Microchess, running on a KIM-1 with about 0.5 K bytes of extra memory. Implementation on other 6502 based computer systems should be relatively easy since only a few minor software modifications would be needed. The required hardware consists of a chess set, a package of cheap switching diodes, 2 integrated circuits, 16 discrete LEDs and 32 copper rivets.

The chessboard should have a thin, nonconductive surface that is easy to drill holes through. This surface must be supported by side panels so there is a hollow space of about 2 cm under the board for wiring. I used a cheap plywood chess set that is designed to fold into a storage box for the chessmen. The copper rivets should be small in diameter, about 12 mm long, and have a flat top. The ones that I used were size 9 rivets manufactured by the Tower Corporation of Madison IN.

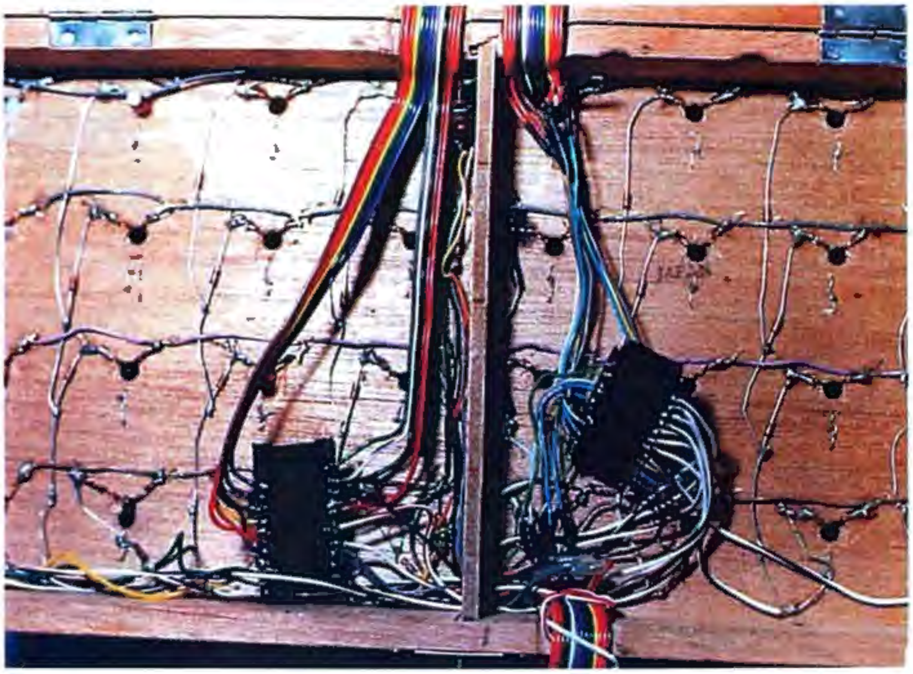

Photo 2: The bottom of the chessboard. The switching diodes and connecting wires are soldered directly to the wire contacts in the central holes. The 2 integrated circuits are type SN74154 decoder/demultiplexers. Note the tips of rivets protruding through some of the holes.

System Concepts

KIM-1 Microchess uses an internal board-status table to keep track of the whereabouts of the chessmen. This table contains 32 square numbers which indicate the position of the 32 pieces. It is important to realize that Microchess generates moves solely on the basis of what is in that table, and not how it was placed there. My plan of attack was simple. I had only to wire a chessboard to the computer and write an interface program that would translate moves on the chessboard into changes in the table. Since this program will be needed only when moves are physically being made, it can be called from Microchess and used in place of the Microchess keyboard I/O (input/output) routines. After the user has finished moving, control can be transferred back to Microchess to compute the machine's next move.

The Microchess to chessboard interface program is logically straightforward. If no move is being made, the table should be an accurate representation of the board. A move is detected when the table does not correctly represent the current board position. If an empty square appears on the board where the table indicates that a chessman resides, then the user has just picked up that man. If the table shows an unoccupied square which the board indicates is occupied, a chessman has just been set down in that square. A move is constituted by the user picking up a man and setting it down in some other location. A capture is completed by picking up 2 men and setting 1 down in the space formerly occupied by the other. Because the Microchess table is updated each time a simple move or capture is made, the table always gives an accurate representation of the current board position.

Photo 3: The complete chessplaying system. The completed electronic chessboard stands in the foreground. The chessboard and the sound-effect speaker are connected to the KIM-1 computer residing in the suitcase in the background.

Hardware Details

Note that the chessboard interface program can keep track of the moves that are made simply by knowing if individual squares are occupied by a piece or are empty. The circuit which provides this information to the computer is illustrated in figure 1. For purposes of square identification, the chessboard is conceptually cut in half. The 2 pieces are placed logically end to end, forming an arrangement

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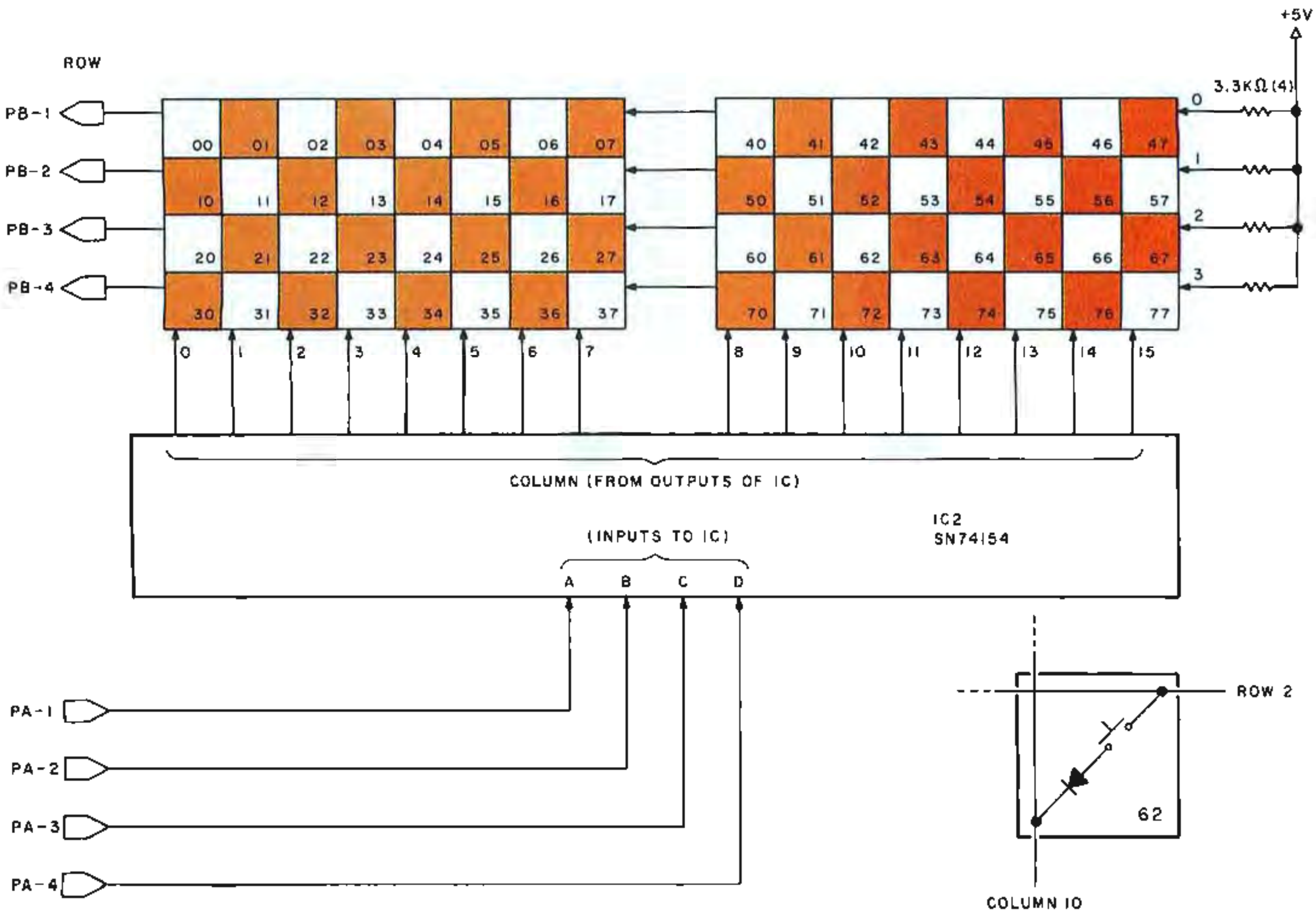

Figure 1: Circuit which determines whether or not a given square is occupied. The chessboard is conceptually cut in half. It is placed so that the squares form a 4 by 16 matrix. For each square, a diode and a switch are wired in series between the appropriate row and column lines. A closed switch indicates an occupied square; an open switch indicates an empty square.

of 4 rows and 16 columns. A diode matrix allows the hardware to identify the individual squares.

The integrated circuit in figure 1 is a type SN74154 4 to 16 line decoder/demultiplexer. The 4 input lines to the device are connected to the KIM-1 I/O port A. Each of the 16 output lines is linked to a column in the matrix. This portion of the circuit allows the KIM-1 to select 4 squares out of the total of 64. The 4 rows of the matrix are connected to the I/O port B. Row and column addressing allows scanning of a single square. Each square of the chessboard has a switch. A closed switch indicates that the square has a piece on it; an open switch shows that the square is empty.

To determine whether or not a piece is on a particular square, the interface program first selects the column by sending the correct binary code to the 4 input lines on the SN74154. This brings 1 of the 16 output lines low, while the diodes keep the rest high. If the switch is closed (ie: a piece is on the square), then the corresponding row-line will be pulled low and the matching port-B data register bit will be a 0. Thus, by selecting the column through port A and testing the row bits in port B, it is possible to determine the status of every square on the board.

Switch Experimentation

Now for the hard part: what can be used as a switch? The actual mechanical operation remains the only unresolved detail. All that is needed is some means of closing the switch whenever a piece is set down, and opening it when one is picked up. There are several ways to accomplish this—some of which are better than others.

In my first attempt I put aluminum foil on the bottom of the pieces and used simple wire contacts on top of the board. I punched 6 holes into each square using a large needle to form the corners of 2 concentric, equilateral triangles. Three strands of wire were looped through the holes forming 3 symmetric contacts (see figure 2a). The third contact was used only to balance the pieces.

The concept is simple. The piece is set on top of the wire contacts and the aluminum foil makes the necessary connection. Unfortunately it didn't work. The contacts were not sufficiently stable, and the slightest vibration rocked the pieces, leading the program to believe that the user was trying to move 5 or 10 pieces at once.

That problem might have been solved by mounting magnets on the pieces and using a chessboard with a nonconductive magnetic surface.

a

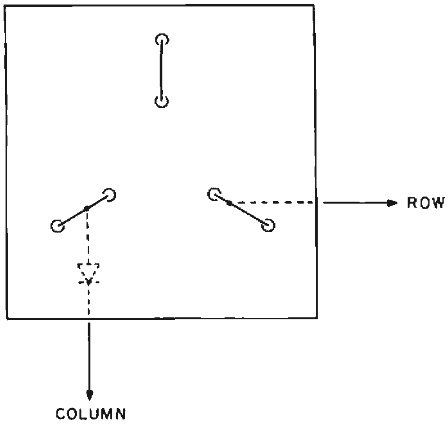

Figure 2a: The first attempt to form a switch for the squares. Three symmetric contacts on top of each square were made by looping bare wire through holes in the board. Two of the contacts were wired to the row and column lines on the back side of the board. (The third wire was simply to balance the piece upright.) The pieces had aluminum foil glued to their bottoms. When such a chessman was set down on the contacts, electrical continuity was achieved. Unfortunately, vibration caused intermittent contact and confused the computer.

b

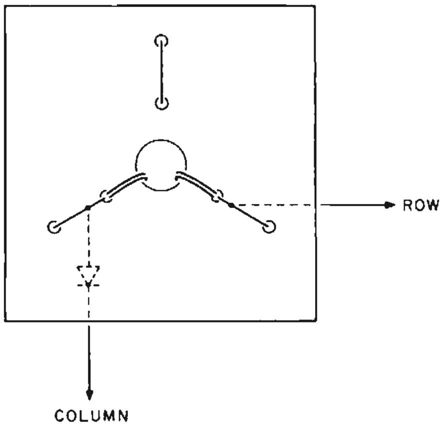

Figure 2b: The second attempt to form a square switch. This attempt was successful. Copper rivets were glued to the bottom of the chessmen. A large hole was drilled in the center of each square to receive the rivet. Two wires were looped through the large central hole from 2 smaller holes (left over from the first switch attempt). The rivet closes the electrical circuit.

c

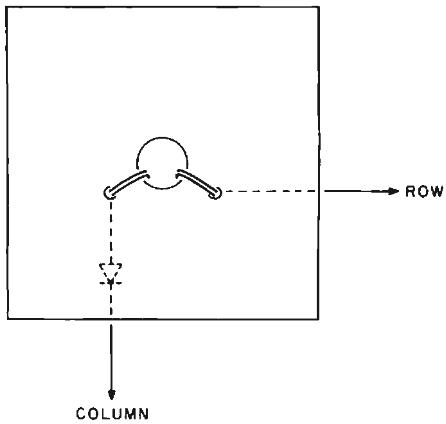

Figure 2c: Illustration of the appearance of a square which uses rivet switches, and which previously did not have other methods installed in it. The reader may do it correctly the first time.

Another possibility would be to eliminate wire contacts entirely and use reed switches or some type of photocell. Unfortunately, one such device must be mounted under each square, necessitating a total of 64 devices. Although they would have undoubtedly worked, 64 photocells or reed switches would have cost more than I was willing to spend on the project.

Switch Success

I eventually figured out a contact method that was both cheap and reliable. I drilled a small hole in the center of each square, just large enough to slide in a copper rivet. Two strands of bare copper wire from 2 of the inner contact holes used in my first attempt were looped *through* the larger central hole forming 2 contacts inside of the hole (see figure 2b). The felt on the bottom of the pieces was peeled off and the tapered copper rivets were glued onto the metal weight underneath the felt with an instant bonding adhesive.

I have found that these contacts work quite well. The tapered copper rivets slide easily in and out of the hole, while slight pressure from the sides of the hole forces the rivet to make good contact with the copper wire. The pieces remain intact and the electrical contacts remain solid, even when the chessboard is held upside down and shaken gently. Of course when you wire your chessboard, you should leave out the 3 symmetric wires that I tried on my first version. Only the 2 strands which were looped through the rivet hole need to be installed (see figure 2c).

Hardware for Computer Output

The LEDs are wired according to figure 3. The integrated circuit is another 4 to 16 line decoder whose 4 inputs are connected to the I/O ports. Note that decoder outputs 0 thru 7 are connected sequentially to the rank— indicating (Y axis) LEDs with the 0-bit output being connected to the uppermost LED. Likewise, the file—indicating (X axis) LEDs are connected left to right with outputs 8 thru 15. The chip-enable line is connected to I/O port pin PB0 so that the LEDs can be turned off while Microchess is computing a move.

Mounting of the LEDs on the sides of the chessboard is relatively straightforward. I used a large needle to punch the holes for the leads prior to insertion. Glue can be used to hold them in place. Be sure to orient the chessboard so that a white square is in the lower right-hand corner of the side facing the human player. This means that the 2 rows of LEDs installed on the left side and bottom of the board will meet at a corner containing a black square.

The speaker is connected to output port pin PA0 in the manner described in the *KIM-1 User's Manual* on page 57. See figure 4 for an illustration of the I/O port connections.

Software

The necessary modifications to Microchess are shown in listing 1. The Microchess to chessboard interface program with source and object listing is given in listing 2. Although I used a nonstandard meta-assembler, most of the mnemonics are similar to, if not the same as, the MOS Technology standard mnemonics. The listings are fairly well documented.

There are, however, some general concepts that may be difficult to deduce from the listings. The workhorse of the chessboard interface program is subroutine GET-MOVE. GET-MOVE calls the KIM monitor routine GETKEY before doing anything else, in order to see if the user has pressed the **DA** key (which is used when setting up a new position) or the **PC** key (which clears

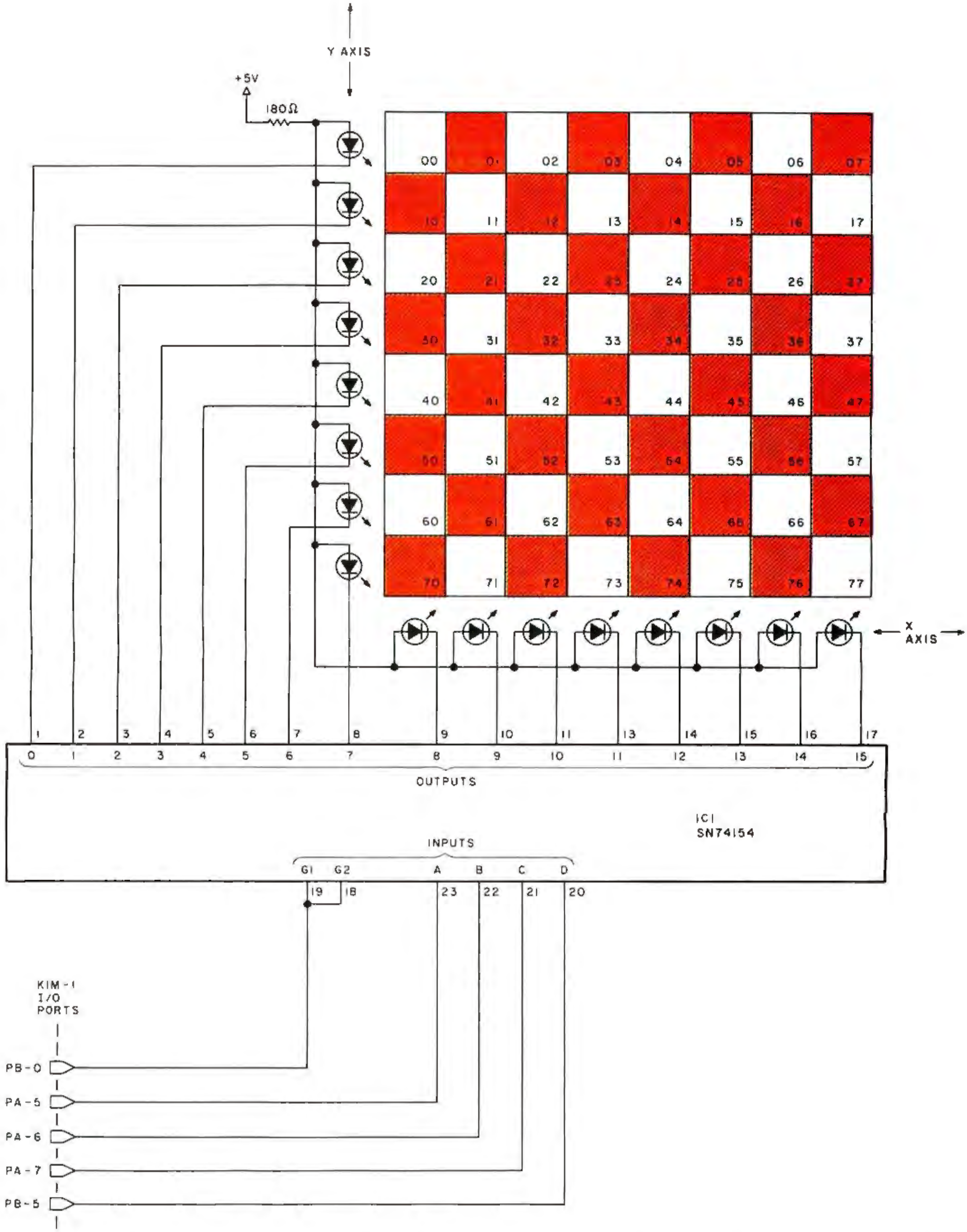

Figure 3: Circuit for lighting the light emitting diodes (LEDs) that indicate the computer's move. The computer moves as follows. The program lights the X and Y axis LEDs which together indicate the single square on which the piece to be moved resides. The person picks up the indicated piece. After the user picks up the piece, different LEDs light up that point to the square to which the piece is to be moved. The person then places the chessman as indicated. A mistake causes the computer to emit a characteristic sound. The chip-enable line of IC1 is connected to I/O (input/output) port pin PB 0 so that the LEDs may be turned off while the chess program is computing its next move.

the board for a new game). If neither the DA nor PC key is depressed, GET-MOVE scans the chessboard, square by square, searching for pieces that were recently picked up or set down. This is done by comparing the

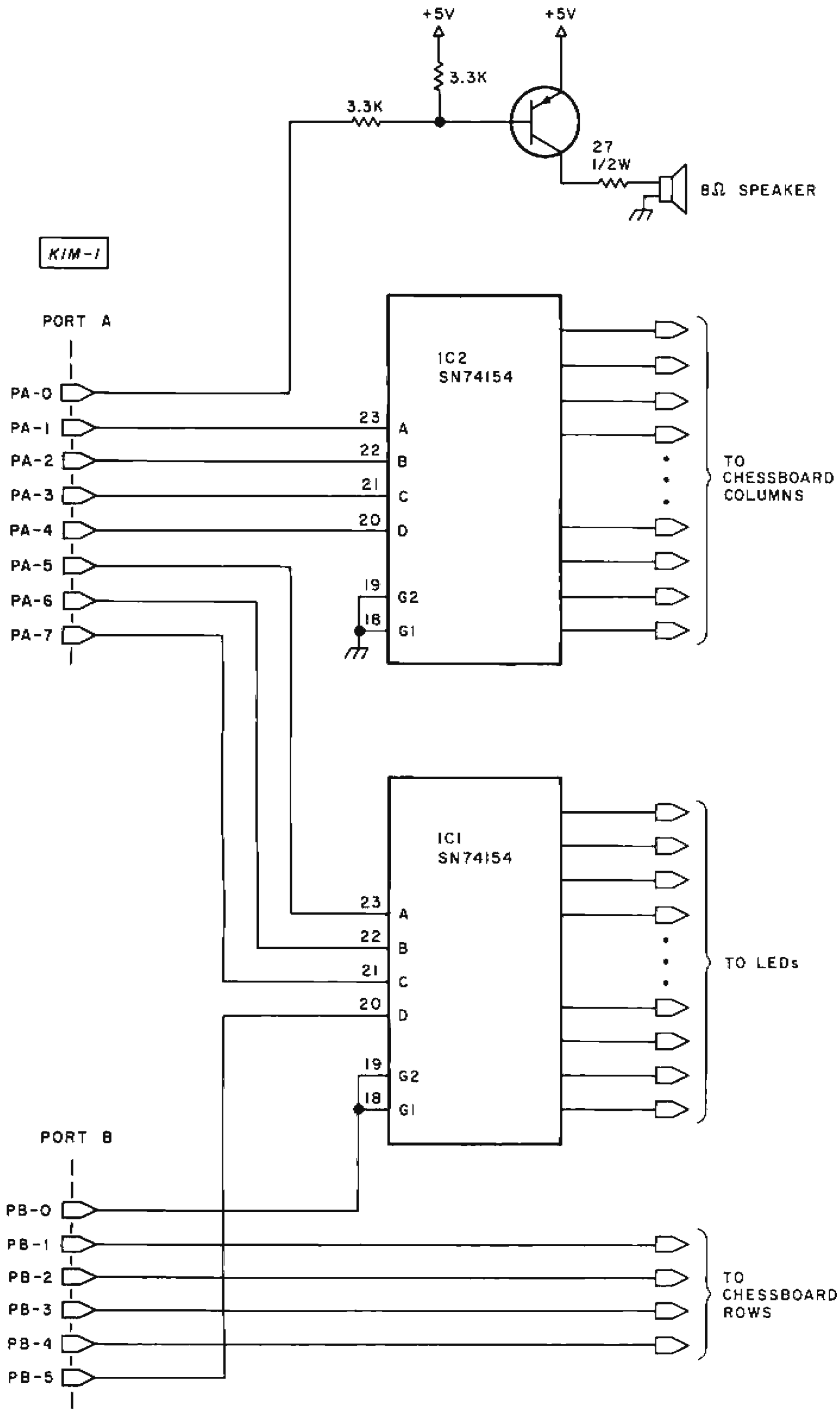

Figure 4: Schematic diagram of chessboard input connections for the KIM-1. If the speaker is built into the chessboard, a 16 conductor cable is required to connect the board to the KIM-1 application connector. Thirteen conductors control the chessboard and light emitting diodes; 3 are needed for speaker, ground, and +5 V supply. The cable should be of sufficient length that the chessboard may be set in a convenient position for game playing.

Microchess board-status table to the current board position, as previously described. There is one important exception. When the user picks up a piece to make a move, SHOULDBEUP-FLAG is made nonzero, and the square where the piece used to be is stored in hexadecimal addresses FA and F9. A nonzero SHOULDBEUP-FLAG tells subroutine GET-MOVE that the 2 squares in FA and F9 should not be occupied, even if they are shown in the table. This is done to prevent GET-MOVE from continuously reporting that the same piece was picked up.

Upon exit from the subroutine, the result of the search is stored in the accumulator and in location UP-CLEAR-DOWN. A +1 is returned if a piece has been picked up, a 0 if there is no change, and a −1 if a piece was set down. If a piece *was* picked up or set down, then CHANGING-SQUARE will contain the number of the square where the pickup or set-down occurred. Likewise, if a piece was picked up, then CHANGING-PIECE will contain the hexadecimal designation of that piece as outlined on page 3 of the Microchess player's manual.

While GET-MOVE is scanning the chessboard, it also lights up the X and Y axis LEDs that point to the square in LIGHT-SQUARE. If SPEAKER-FLAG is nonzero, the speaker is rapidly toggled to produce a hum.

Subroutine CLEAR-STACK resets the Microchess and the machine stack pointers back to their initial values. The subroutine is called from various parts of the interface program to prevent the stacks from overflowing into Microchess code.

After Microchess has computed each move, control is transferred to the start of the interface program at hexadecimal address 2000. The user must physically move the pieces for the computer. The piece designation and the from and to squares of the calculated move are stored in the KIM display at hexadecimal addresses FB, FA, and F9 respectively. Because of the no-operation instructions inserted at address 03E1, the move has not been recorded in the board-status table. Addresses 2000 through 2040 of listing 2 contain code

Text continued on page 46

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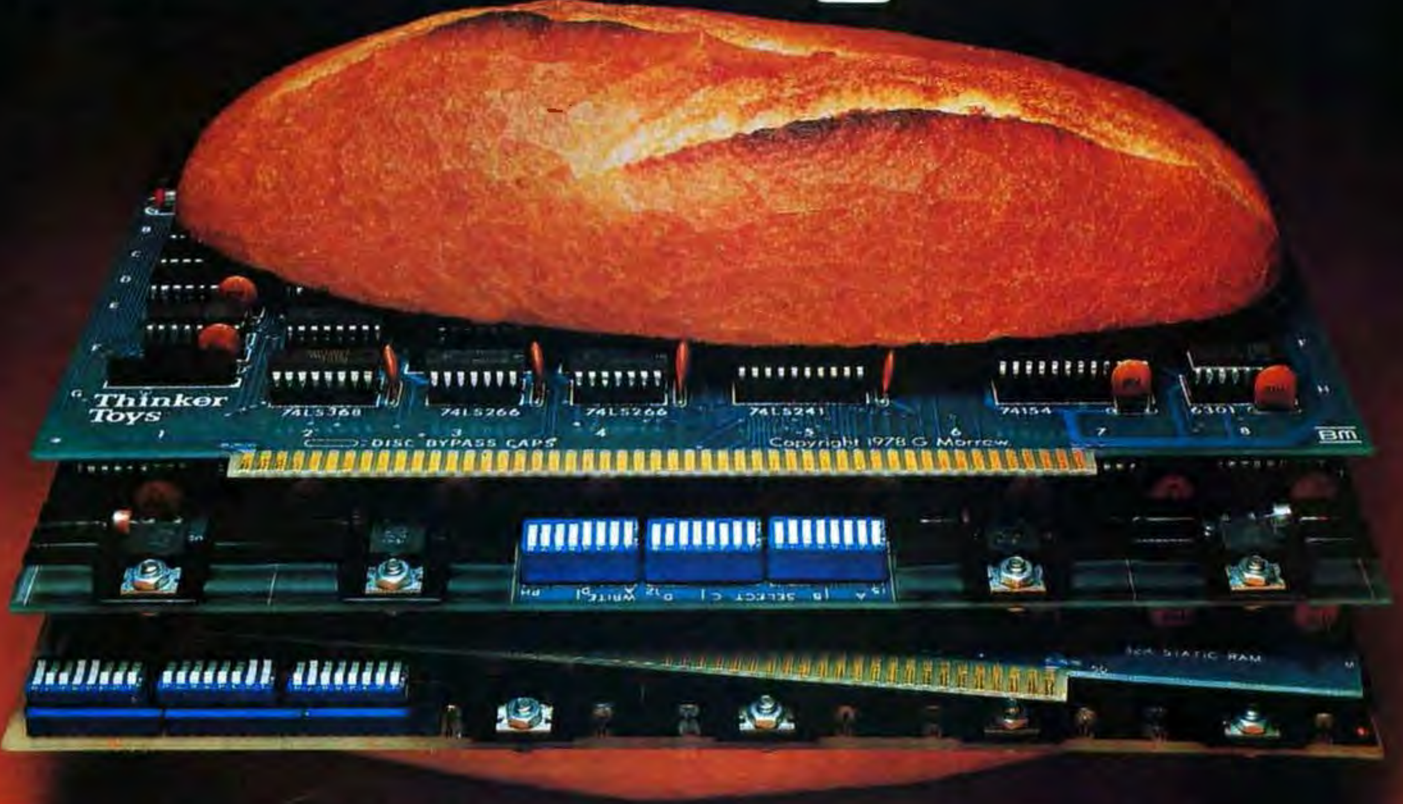

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Listing 1: Modifications which were made to Peter Jennings' KIM-1 Microchess program to allow for the use of the electronic chessboard. Change the specified locations in memory with the KIM monitor.

Address (Hexadecimal)	New Code (Hexadecimal)			Comments
0008	A9	FF		Set up Port A-DDR
000A	8D	01	17	
000D	A9	21		Set up Port B-DDR
000F	8D	03	17	
0012	4C	00	20	Jump to interface program
0033	00			Toggle, must be −1 or zero
003F	60			Return from CLDSP
00B7	02	04		MASK-TABLE (used
00B9	08	10		to read row)
01AC	60			Return from DISP
03A7	B1			Use. SQUARE for flag
03E1	EA	EA	EA	Don't record move
03E9	20	39	00	Show all FFs
03EC	4C	00	00	(Concede defeat)

Listing 2: The Microchess to chessboard interface routine, a sort of chessboard device handler program. This listing is the output of an assembly with both source and hexadecimal object code shown. It is written in a nonstandard assembly language of the author's own design, although most of the mnemonics are similar to the MOS Technology standard mnemonics.

```
0000            !SET BIGC;ORG 2000;
2000            !  COMMENT  *** KIM-1 MICROCHESS TO CHESSBOARD INTERFACE ***
2000            !                   PROGRAM.  WRITTEN BY JEFF TEETERS. 9/8/78
2000            !;
2000            !DEFINE  .BOARD=50,                 % ADDRESS OF PIECE TABLE
2000            !        .BD-1=4F,                  % .BOARD LESS ONE
2000            !        .BK=60,                    % ADDRESS OF USERS PIECES
2000            !        .SP2=B2,                   % MICROCHESS STACK POINTER
2000            !        .SQUARE=B1,                % TO SQUARE USED BY MOVE
2000            !        CHANGING-SQUARE=27,        % RETURNED BY GET-MOVE
2000            !        CHANGING-PIECE=28,         % PIECE PICKED UP AT CH-SQR
2000            !        CLDSP=3900,                % CLEAR DISPLAY
2000            !        CLEAR-BOARD=1800,          % SET UP NEW GAME
2000            !        COUNT-FLAG=29,             % SET WHEN COUNTING DOWN
2000            !        DISP=9D01,                 % DISPLAY PIECE NAME IN FB
2000            !        FLASH-DISPLAY=1F1F,        % KIM MONITOR ROUTINE
2000            !        FROM-SQUARE=2A,            % USED WHEN UNMOVING CAPTURE
2000            !        GETKEY=6A1F,               % KIM MONITOR ROUTINE
2000            !        GO=A203,                   % ADDRESS OF CHESS PROGRAM
2000            !        LIGHT-SQUARE=2B,           % SQUARE LIGHTED BY LEDS
2000            !        MASK-TABLE=B7,             % USED TO READ ROW
2000            !        MOVE=4B03,                 % ROUTINE TO UPDATE .BOARD
2000            !        PORT-LIGHT=2C,             % USED TO BUILD IO PORT
2000            !        PORT-SQUARE=2D,            %   "              "
2000            !        PORT-A=0017,               % KIM-1 I/O PORT
2000            !        PORT-B=0217,               %  "          "
2000            !        RANDOMN=0417,              % KIM-1 INTERVAL TIMER
2000            !        REVERSE=B202,              % ROUTINE TO EXCHANGE SIDES
2000            !        SPEAKER-FLAG=2E,           % =1,GET-MOVE GENERATES TONE
2000            !        SHOULDBEUP-FLAG=2F,        % =1,SQUARES IN FA & F9 UP
2000            !        SWITCH-FLAG=30,            % SET IN EXCHANGE
2000            !        TCHANGING-PIECE=31,        % TEMPORARY CHANGING PIECE
2000            !        TCHANGING-SQUARE=32,       % TEMPORARY CHANGING-SQUARE
2000            !        TEMP=F3,                   % TEMPORARY STORAGE LOCATION
2000            !        TOGGLE=33,                 % ALTERNATLEY LIGHTS FA &  F9
2000            !        TUP-CLEAR-DOWN=34,         % TEMPORARY UP-CLEAR-DOWN
2000            !        UMOVE=3103,                % ROUTINE TO UNMAKE MOVE
2000            !        UP-CLEAR-DOWN=35,          % STATUS OF CHANGING-SQUARE
2000            !        "+"=12,                    % RETURN VALUE OF PLUS KEY
2000            !;
2000            !        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2000            !        %%%%%%%%%%    USER MOVE COMPUTER PIECE    %%%%%%%%%%
2000            !        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2000            !          %*********      PICK THE PIECE UP     *********%
2000  A9 00     !               LDA# 00                   %RESET FLAG
2002  85 2F     !               STA  SHOULDBEUP-FLAG
2004  A5 FA     !               LDA  FA                   %LIGHT "FROM SQUARE"
2006  85 2B     !               STA  LIGHT-SQUARE
2008  E6 2E     !PICK-IT-UP:    INC  SPEAKER-FLAG         %SOUND OFF
200A            !               LOOP
```

```
200A  20 6B 21  !                 JSR  GET-MOVE         %WAIT FOR PLAYER TO
200D  F0        !                 BEQ                   %%PICKUP PIECE.
200E  FB        !               ENDLOOP
200F  30 F7     !               BMI  PICK-IT UP         %ERROR, PIECE SET DOWN
2011  A5 27     !               LDA  CHANGING-SQUARE    %IS PIECE PICKED UP
2013  C5 FA     !               CMP  FA                 %%CORRECT ONE?
2015  D0 F1     !               BNE  PICK-IT UP
2017  A6 FB     !               LDX  FB                 %YES, SET TABLE ENTRY
2019  A9 CC     !               LDA# CC                 %%TO "CC"
201B  95 50     !               STAX .BOARD
201D            !          %*********     SET THE PIECE DOWN      *********%
201D  A5 F9     !               LDA  F9                 %LIGHT TO SQUARE
201F  85 2B     !               STA  LIGHT-SQUARE
2021  E6 2E     !SET-IT-DOWN:   INC  SPEAKER-FLAG       %MAKE NOISE
2023            !               LOOP
2023  20 6B 21  !                 JSR  GET-MOVE         %WAIT FOR CHANGES
2026  F0        !                 BEQ
2027  FB        !               ENDLOOP
2028  A5 F9     !               LDA  F9                 %IS USER MOVEING
202A  C5 27     !               CMP  CHANGING-SQUARE    %%CORRECT PIECE?
202C  D0 F3     !               BNE  SET-IT-DOWN
202E  A5 35     !               LDA  UP-CLEAR-DOWN      %YES
2030  10 08     !               IF NEGATIVE THEN
2032  A6 FB     !                 LDX  FB               %UPDATE TABLE.(PIECE
2034  A5 27     !                 LDA  CHANGING-SQUARE  %%SET DOWN, MOVE HAS
2036  95 50     !                 STAX .BOARD           %%BEEN COMPLETED.)
2038  10        !                 BPL
2039  08        !               ELSE
203A  A6 28     !                 LDX  CHANGING-PIECE   %CAPTURED PIECE HAS
203C  A9 CC     !                 LDA# CC               %%BEEN PICKED UP...
203E  95 50     !                 STAX .BOARD           %%UPDATE TABLE AND
2040  30 DF     !                 BMI  SET-IT-DOWN      %%WAIT FOR SET DOWN.
2042            !               ENDELSE
2042            !     %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2042            !     %%%%%%%%%%%     USER MOVE USER'S PIECE      %%%%%%%%%%
2042            !     %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2042  E6 2E     !               INC  SPEAKER-FLAG       %MAKE NOISE
2044  A9 00     !WAIT-FOR-MOVE: LDA# 00                 %CLEAR UP FLAG
2046  85 2F     !               STA  SHOULDBEUP-FLAG
2048  85 29     !SET-COUNT:     STA  COUNT-FLAG         %SET COUNT FLAG
204A  20 39 00  !SET-DISPLAY:   JSR  CLDSP              %CLEAR DISPLAY
204D  20 6B 21  !GET-MOVE1:     JSR  GET-MOVE
2050  D0 41     !               IF ZERO THEN
2052            !        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2052            !        %%%%%%%%      NO CHANGE IN BOARD      %%%%%%%%
2052            !        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2052            !             %*********  CHECK FOR "GO" KEY  *********%
2052  20 6A 1F  !                 JSR  GETKEY
2055  C9 13     !                 CMP# 13               %13=VALUE OF "GO" KEY
2057  F0 17     !                 BEQ  GO-COUNTDOWN
2059            !             %*********  CHECK FOR "E" KEY   *********%
2059  C9 0E     !                 CMP# 0E
205B  D0 16     !                 IF ZERO THEN          %USER WANTS TO
205D            !                   LOOP                %%SWITCH SIDES
205D  20 6A 1F  !                     JSR GETKEY
2060  C9 0E     !                     CMP# 0E           %DEBOUNCE KEYBOARD
2062  F0        !                     BEQ
2063  F9        !                   ENDLOOP
2064  A5 30     !                   LDA  SWITCH-FLAG    %TOGGLE FLAG
2066  49 FF     !                   EOR# FF
2068  85 30     !                   STA  SWITCH-FLAG
206A  20 B2 02  !SWITCH-SIDES:      JSR  REVERSE        %PERFORM EXCHANGE
206D  20 5D 21  !                   JSR  CLEAR-STACK
2070  4C 4C 21  !GO-COUNTDOWN:      JMP  START-COUNTING
2073            !                 ENDIF
2073            !             %******** "GO" OR "E" NOT FOUND ********%
2073  A5 29     !                 LDA  COUNT-FLAG       %COUNTING DOWN?
2075  F0 12     !                 IF NOTZERO THEN
2077  C6 FB     !                   DEC  FB             %YES.
2079  A5 FB     !                   LDA  FB
207B  D0 06     !                   IF ZERO THEN
207D  20 5D 21  !                     JSR CLEAR-STACK %PLAY CHESS
2080  4C A2 03  !                     JMP GO
2083            !                   ENDIF
2083  A9 0F     !                   LDA# 0F             %STILL COUNTING DOWN,
2085  65 2B     !                   ADC  LIGHT-SQUARE   %%LIGHT NEXT SQUARE.
2087  D0        !                   BNE
2088  03        !                 ELSE
```

Listing 2 continued on page 46

Listing 2 continued from page 45:

```
2089   AD 04 17  !            LDA@ RANDOM#        %WAITING FOR MOVE...
208C             !         ENDELSE                %%LIGHT RANDOM SQUARE
208C   85 2B     !         STA  LIGHT-SQUARE
208E   A5 FB     !         LDA  FB
2090   4C 4A 20  !         JMP  SET-DISPLAY
2093             !      ENDIF
2093   10 49     !      IF NEGATIVE THEN
2095             !   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2095             !   %%%%%%%%      NEW PIECE SET DOWN     %%%%%%%%
2095             !   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2095             !     %********* TAKING BACK CAPTURE? *********%
2095   A5 B2     !         LDA  .SP2
2097   C9 C8     !         CMP# C8                %UNDOING PREVIOUS
2099   F0 0C     !         IF NOTZERO THEN        %%  CAPTURE?
209B   A5 2A     !            LDA  FROM-SQUARE
209D   C5 27     !            CMP  CHANGING-SQUARE
209F   D0 06     !            IF ZERO THEN
20A1   20 31 03  !               JSR  UMOVE     %     YES.
20A4   4C 44 20  !               JMP  WAIT-FOR-MOVE
20A7             !            ENDIF
20A7             !         ENDIF
20A7             !     %*********USER ADDING NEW PIECE**********%
20A7   20 6A 1F  !         JSR  GETKEY            %WAIT FOR KEY ENTRY
20AA   C9 15     !         CMP# 15                %%OF HEX NAME OR "+"
20AC   F0 1C     !         IF NOTZERO THEN
20AE   C9 12     !            CMP# "+"
20B0   D0 0C     !            IF ZERO THEN
20B2   A5 FA     !               LDA  FA        %FOUND "+", ENTER NEW
20B4   10 97     !               BPL  GET-MOVE1 %%PIECE INTO TABLE IF
20B6   A6 FB     !               LDX  FB        %%NOT IN ALREADY
20B8   A5 27     !               LDA  CHANGING-SQUARE
20BA   95 50     !               STAX .BOARD
20BC   10 B6     !               BPL  WAIT-FOR-MOVE
20BE             !            ENDIF
20BE   85 F3     !            STA  TEMP           %FOUND HEX DIGIT
20C0   A5 FB     !            LDA  FB             %%"OR" IT INTO
20C2   0A 0A     !            ASL  ASL            %%PIECE NAME.
20C4   0A 0A     !            ASL  ASL
20C6   05 F3     !            ORA  TEMP
20C8   85 FB     !            STA  FB
20CA             !         ENDIF
20CA   A5 27     !         LDA  CHANGING-SQUARE  %BUILD DISPLAY
20CC   85 2B     !         STA  LIGHT-SQUARE
20CE   85 F9     !         STA  F9                %%%F9=SQUARE ON BOARD
20D0   A5 FB     !         LDA  FB                %PUT PIECE NAME IN
20D2   29 1F     !         AND# 1F                %%RANGE
20D4   85 FB     !         STA  FB                %%%FB=PIECE NAME
20D6   AA        !         TAX
20D7   B5 50     !         LDAX .BOARD
20D9   85 FA     !         STA  FA                %%%FA=TABLE ENTRY
20DB   4C 4D 20  !         JMP  GET-MOVE1
20DE             !      ENDIF
20DE             !   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
20DE             !   %%%%%%%%      PIECE PICKED UP       %%%%%%%%
20DE             !   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
20DE             !     %**********  USER PLAY WHITE?  **********%
20DE   A5 B1     !      LDA  .SQUARE              %SEE IF USER MAKING
20E0   C9 CC     !      CMP# CC                   %%THE FIRST MOVE.
20E2   D0 05     !      IF ZERO THEN
20E4   E6 B1     !         INC  .SQUARE           %YES, CHANGE .SQUARE
20E6   4C 6A 20  !         JMP  SWITCH-SIDES      %%AND EXCHANGE
20E9             !      ENDIF
20E9             !     %**********   WAIT FOR CHANGE   **********%
20E9   20 5D 21  !      JSR  CLEAR-STACK          %CLEAR POSSIBLE JUNK
20EC   A5 27     !      LDA  CHANGING-SQUARE
20EE   85 FA     !      STA  FA                   %DISPLAY SQUARE NUM
20F0   85 F9     !      STA  F9
20F2   85 2B     !      STA  LIGHT-SQUARE
20F4   20 9D 01  !      JSR  DISP                 %DISPLAY PIECE NAME
20F7   A9 01     !      LDA# 01
20F9   85 2F     !      STA  SHOULDBEUP-FLAG      %SET FLAG
20FB             !      LOOP
20FB   20 6B 21  !         JSR  GET-MOVE          %AWAIT MOVE2
20FE   F0        !         BEQ
20FF   FB        !      ENDLOOP
2100             !     %********** PIECE SET BACK DOWN **********%
2100   10 11     !      IF NEGATIVE THEN
```

Listing 2 continued on page 48

Text continued from page 42:

to light the correct LEDs and modify the board-status table as the user completes the computer's move. The speaker sounds briefly after each correct step is completed. If a wrong piece is moved or a piece is set down on a wrong square, the speaker will hum continuously to signal an error.

The logic for interpreting the user's move starts at location 2042. If COUNT-FLAG is 0, the user has not yet moved. Subroutine GET-MOVE is repeatedly called from location 204D in anticipation of the user's move.

If the accumulator is 0 upon return from GET-MOVE, then the board position remains unchanged and the user has not made a move. GETKEY is called to see if the user has depressed either the GO or E key. If the E key is depressed, the Microchess routine REVERSE is called to swap the user and computer entries of the board-status table. After the exchange is completed or if the GO key is depressed, a branch is made to START-COUNTING at hexadecimal address 214C.

Three provisions are made for a delayed return back to Microchess. COUNT-FLAG is made nonzero, a countdown is initiated by setting the display to 0F, and control is then transferred back to address 204D where GET-MOVE is repeatedly called as before.

After each return from GET-MOVE the display is decremented by 1 until it equals 0. This provides an approximate 10 second delay during which the user can make a new move or retract an old one. At the end of the countdown, a branch is made to the Microchess routine GO which calculates the computer's next move.

If the GET-MOVE call at 204D returns a negative value then the user has set down a *new* piece, and control is transferred to address 2095. In an ordinary game of chess, putting a new piece on the board would be considered cheating. I have allowed it here to prevent 2 possible problems.

The first problem is caused by indecisive players who change their minds while in the middle of a move. Suppose such a player picks up 2 chessmen, as if to capture, and then decides to set both down again. When the first man is set down the program will think that the user has completed a capture, modify the board-status

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Listing 2 continued from page 46

```
2102   A5 27      !                  LDA  CHANGING-SQUARE  %FROM SQUARE =
2104   C5 FA      !                  CMP  FA               %%TO SQUARE?
2106   D0 03      !                  IF ZERO THEN
2108   4C 44 20   !                     JMP  WAIT-FOR-MOVE %YES, NO MOVE MADE.
210B              !                  ENDIF
210B   85 B1      !                  STA  .SQUARE          %NO,
210D   20 4B 03   !                  JSR  MOVE             %%RECORD MOVE,
2110   4C 4C 21   !                  JMP  START-COUNTING   %%AND COUNT DOWN.
2113              !               ENDIF
2113              !            %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2113              !            %%%%%%%%     2'ND PIECE PICKED UP    %%%%%%%%
2113              !            %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2113              !              %*********   WAIT FOR SET DOWN  *********%
2113   A5 27      !               LDA  CHANGING-SQUARE
2115   85 F9      !               STA  F9                  %F9=TO SQUARE
2117   85 B1      !               STA  .SQUARE
2119              !2-UP:          LOOP
2119   A5 33      !                  LDA  TOGGLE           %FLASH LIGHTS FOR TO
211B   10 06      !                  IF NEGATIVE THEN      %%AND FROM SQUARES.
211D   A5 FA      !                     LDA  FA
211F   E6 33      !                     INC  TOGGLE
2121   F0         !                     BEQ
2122   04         !                  ELSE
2123   A5 F9      !                     LDA  F9
2125   C6 33      !                     DEC  TOGGLE
2127              !                  ENDELSE
2127   85 2B      !                  STA  LIGHT-SQUARE
2129   20 6B 21   !                  JSR  GET-MOVE         %WAIT FOR SET DOWN
212C   F0         !                  BEQ
212D   EB         !               ENDLOOP
212E   10 29      !               IF NEGATIVE THEN
2130              !              %*********    PIECE SET DOWN    *********%
2130   A5 27      !                  LDA  CHANGING-SQUARE
2132   C5 F9      !                  CMP  F9               %C-S = TO SQUARE?
2134   F0 0C      !                  IF NOTZERO THEN       %%NOPE,
2136   C5 FA      !                     CMP  FA            %= FROM SQUARE?
2138   D0 1F      !                     BNE  ERROR-3       %%NOPE, ERROR
213A   A6 F9      !                     LDX  F9
213C   85 F9      !                     STA  F9            %TO & FROM SQUARES
213E   85 B1      !                     STA  .SQUARE       %REVERSED, SWITCH BACK
2140   86 FA      !                     STX  FA
2142              !                  ENDIF
2142   A5 FA      !                  LDA  FA               %SAVE FROM SQUARE FOR
2144   85 2A      !                  STA  FROM SQUARE      %%USE IF UNDOING MOVE
2146   20 9D 01   !                  JSR  DISP             %SET .PIECE
2149   20 4B 03   !                  JSR  MOVE             %RECORD MOVE
214C              !              %********* INITIALIZE COUNT DOWN ********%
214C   A9 00      !START-COUNTING:   LDA# 00               %CLEAR FLAG
214E   85 2F      !                  STA  SHOULDBEUP-FLAG
2150   85 2B      !                  STA  LIGHT-SQUARE
2152   A9 0F      !                  LDA# OF               %LOAD DELAY
2154   E6 2E      !                  INC  SPEAKER-FLAG     %SOUND OFF
2156   4C 4B 20   !                  JMP  SET-COUNT
2159              !               ENDIF
2159   E6 2E      !ERROR-3:       INC  SPEAKER-FLAG        %SOME TYPE OF ERROR,
215B   D0 BC      !               BNE  2-UP                %%WAIT UNTIL CORRECTED
215D              !
215D              !
215D              !
215D              !SUBROUTINE  CLEAR-STACK:            %RESETS BOTH STACK MARKERS
215D   68 A8 68   !               PLA  TAY  PLA            %STORE RETURN ADDRESS
2160   A2 FF 9A   !               LDX# FF   TXS            %RESET MACHINE STACK
2163   A2 C8      !               LDX# C8                  %RESET CHESS STACK
2165   86 B2      !               STX  .SP2
2167   48 98 48   !               PHA  TYA  PHA            %SET UP RETURN
216A   60         !               RTS
216B              !
216B              !
216B              !
216B              !SUBROUTINE  GET-MOVE:             %SCANS CHESSBOARD
216B              !       %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
216B              !       %%%%%%%%%%%    CHECK FOR "DA" OR "PC"    %%%%%%%%%%
216B              !       %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
216B   20 6A 1F   !               JSR  GETKEY
216E   C9 11      !               CMP# 11                  %11="DA" KEY
2170   D0 0B      !               IF ZERO THEN
2172   A2 1F      !                  LDX# 1F               %FOUND "DELETE ALL"
```

Listing 2 continued on page 50

table accordingly, and proceed to countdown. During the countdown the second man would pop in and there would be no way to know what it was.

In order to prevent this, each capturing move is saved in the Microchess stack. When a new piece is set down, the stack pointer is checked to see if the previous move was a capture. If it was, and if the location of the new piece corresponds to the square where the capturing piece used to be, then the Microchess routine UMOVE is called to restore the board-status table.

The second problem arises when the user wants to add new pieces to the current board, or set up an entirely new board position. Previously the only way to add new pieces was to stop the chess program and enter the square numbers manually into the board-status table using the KIM-1 monitor. This method is both inconvenient and error prone. The control logic for the "new improved" method occupies hexadecimal addresses 20A7 through 20DE.

After setting the new pieces down, the user simply types the piece name (its numeric designation) into the hexadecimal keyboard. The designation is displayed in FB, the current board-status table entry in FA, and the square where the new piece was set down is stored in F9. If the current table entry is "CC" (indicating that the piece is not currently on the board), the user may enter the piece into the table by pressing the + key.

Interpreting the User's Move

If the original call to GET-MOVE at hexadecimal address 204D returns a positive value, it means that the user has picked up a piece, and control will transfer to address 20DE. If .SQUARE contains "CC", the Microchess board-status table has just been initialized, and the user is making the first move of a new game. The board-status table has been initialized assuming that the user would play Black. A branch may be made to address 206A where the user and computer table entries are exchanged.

After checking to see whether or not the user is playing White, GET-MOVE is again called at hexadecimal address 20FB. If the piece is set down at a new square, the move has been completed and a countdown is started. If, after picking up a piece a

Listing 2 continued from page 48:

```
2174   A9 CC     !                    LDA# CC
2176             !                    LOOP
2176   95 50     !                       STAX .BOARD        %FILL PIECE TABLE
2178   CA        !                       DEX                %%WITH "CC"
2179   10        !                       BPL
217A   FB        !                    ENDLOOP
217B   30 1F     !                    BMI  JMP-TO-MAIN
217D             !                 ENDIF
217D   C9 14     !                 CMP#  14                 %14="PC" KEY
217F   D0 21     !                 IF ZERO THEN             %%(PLEASE CLEAR)
2181   20 18 00  !                    JSR  CLEAR-BOARD      %SET UP NEW GAME
2184   85 B1     !                    STA  .SQUARE          %FLAG .SQUARE WITH CC
2186   A9 00     !                    LDA# 00               %CLEAR FLAGS
2188   85 2F     !                    STA  SHOULDBEUP-FLAG
218A   85 30     !                    STA  SWITCH-FLAG
218C             !                    LOOP                  %WAIT FOR CLEAR BOARD
218C   A5 27     !                       LDA  CHANGING-SQUARE
218E   85 F9     !                       STA  F9            %DISPLAY BAD SQUARE
2190   85 FA     !                       STA  FA
2192   85 2B     !                       STA  LIGHT-SQUARE
2194   20 9D 01  !                       JSR  DISP          %DISPLAY PIECE NAME
2197   20 A2 21  !                       JSR  START-SCAN
219A   D0        !                       BNE
219B   F0        !                    ENDLOOP
219C   20 5D 21  !JMP-TO-MAIN:        JSR  CLEAR-STACK      %RESET STACK
219F   4C 44 20  !                    JMP  WAIT-FOR-MOVE
21A2             !                 ENDIF
21A2             !          %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21A2             !          %%%%%%%%%%%  START SCANNING CHESSBOARD    %%%%%%%%%%
21A2             !          %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21A2             !                 %*********  SET UP PORT-LIGHT  *********%
21A2   A5 30     !START-SCAN:      LDA  SWITCH-FLAG         %SIDES EXCHANGED?
21A4   F0 07     !                 IF NOTZERO THEN
21A6   A5 2B     !                    LDA  LIGHT-SQUARE     %YES,
21A8   49 77     !                    EOR# 77               %%PL=77-"LIGHT-SQUARE"
21AA   4C        !                    JMP
21AB      AF 21  !                 ELSE                     %NO,
21AD   A5 2B     !                    LDA  LIGHT-SQUARE     %%PL="LIGHT-SQUARE"
21AF             !                 ENDELSE
21AF   85 2C     !                 STA  PORT-LIGHT
21B1             !                 %********INITIALIZE U-C-D & TC-S********%
21B1   A9 00     !                 LDA#  00
21B3   85 35     !                 STA  UP-CLEAR-DOWN
21B5             !                 LOOP
21B5   85 32     !                    STA  TCHANGING-SQUARE
21B7             !                 %*********DO MISCELLANEOUS I/O**********%
21B7   20 1F 1F  !                    JSR  FLASH-DISPLAY    %FLASH DISPLAY
21BA   A5 2E     !                    LDA  SPEAKER-FLAG
21BC   F0 03     !                    IF NOTZERO THEN
21BE   EE 00 17  !                       INC@ PORT-A        %TOGGLE SPEAKER
21C1             !                    ENDIF
21C1             !              %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21C1             !              %%%%%%%% IF SHOULDBEUP-FLAG NOT SET  %%%%%%%%
21C1             !              %%%%%%%% SEE IF SQUARE IN PIECE TABLE%%%%%%%%%
21C1             !              %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21C1   A9 00     !                    LDA# 00               %ASSUME SQUARE OK
21C3   85 34     !                    STA  TUP-CLEAR-DOWN
21C5   A5 2F     !                    LDA  SHOULDBEUP-FLAG  %IN MIDDLE OF MOVE?
21C7   F0 0A     !                    IF NOTZERO THEN
21C9   A5 32     !                      LDA TCHANGING-SQUARE%YES, IS SQUARE IN
21CB   C5 FA     !                       CMP  FA            %%DISPLAY? IF SO
21CD   F0 15     !                       BEQ  NOT-IN-TABLE  %%PRETEND THAT ITS
21CF   C5 F9     !                       CMP  F9            %%NOT IN PIECE TABLE.
21D1   F0 11     !                       BEQ  NOT-IN-TABLE
21D3             !                    ENDIF
21D3             !              %**********SEARCH PIECE TABLE***********%
21D3   A2 1F     !                    LDX# 1F
21D5             !                    LOOP
21D5   B5 50     !                       LDAX .BOARD
21D7   C5 32     !                       CMP TCHANGING-SQUARE
21D9   D0 06     !                       IF ZERO THEN
21DB   86 31     !                          STX  TCHANGING-PIECE
21DD   E6 34     !                          INC TUP-CLEAR-DOWN  %FOUND SQUARE
21DF   D0 05     !                          BNE  BUILD-PORTS
21E1             !                       ENDIF
21E1   CA        !                       DEX
21E2   10        !                       BPL
```

Listing 2 continued on page 52

player decides to set it down on the same square, the move is ignored.

If the GET-MOVE call at location 20FB reports that a second piece has been picked up, a capture is in progress and control branches to location 2113. FROM-SQUARE is defined as the square from which the first chessman is picked up. Similarly, TO-SQUARE is associated with the chessman that is picked up second. GET-MOVE is again called at hexadecimal address 2129.

If a piece is set down on either the TO or FROM squares then the program assumes that a capture has been made. The Microchess routine MOVE is called to modify the board-status table, and a countdown is initiated.

If a piece is set down on a square other than the FROM or TO square, or if a third piece is picked up, a branch will be made to hexadecimal address 2159, and the speaker will hum to indicate an error.

Using the System

Playing the chessboard-interfaced version of Microchess is easy. Moves are made by physically picking up the pieces and setting them down on a new square, as in a normal game of chess with a human opponent. The only difference is that the opponent (the KIM-1) is unable to pick up a chessman, so you have to move the pieces to the location indicated by the LEDs.

The KIM display will be all 0s and the LEDs will blink from square to square in a semirandom fashion when it is your turn to move. After you move, the KIM display will count-down from 0F, and the Y axis LEDs will blink sequentially from the top to the bottom of the board. During this countdown you have the option to change your move. When the display reaches 0, the machine will begin computing a response, and no moves can be made until it is your turn again.

Operating the System

The interfaced version of Microchess is started at address 0000, just as the unmodified Microchess. The speaker will probably hum. To start a new game, press the PC key. The speaker's sound will cease. Choose the White or Black pieces, and set up the board with your choice

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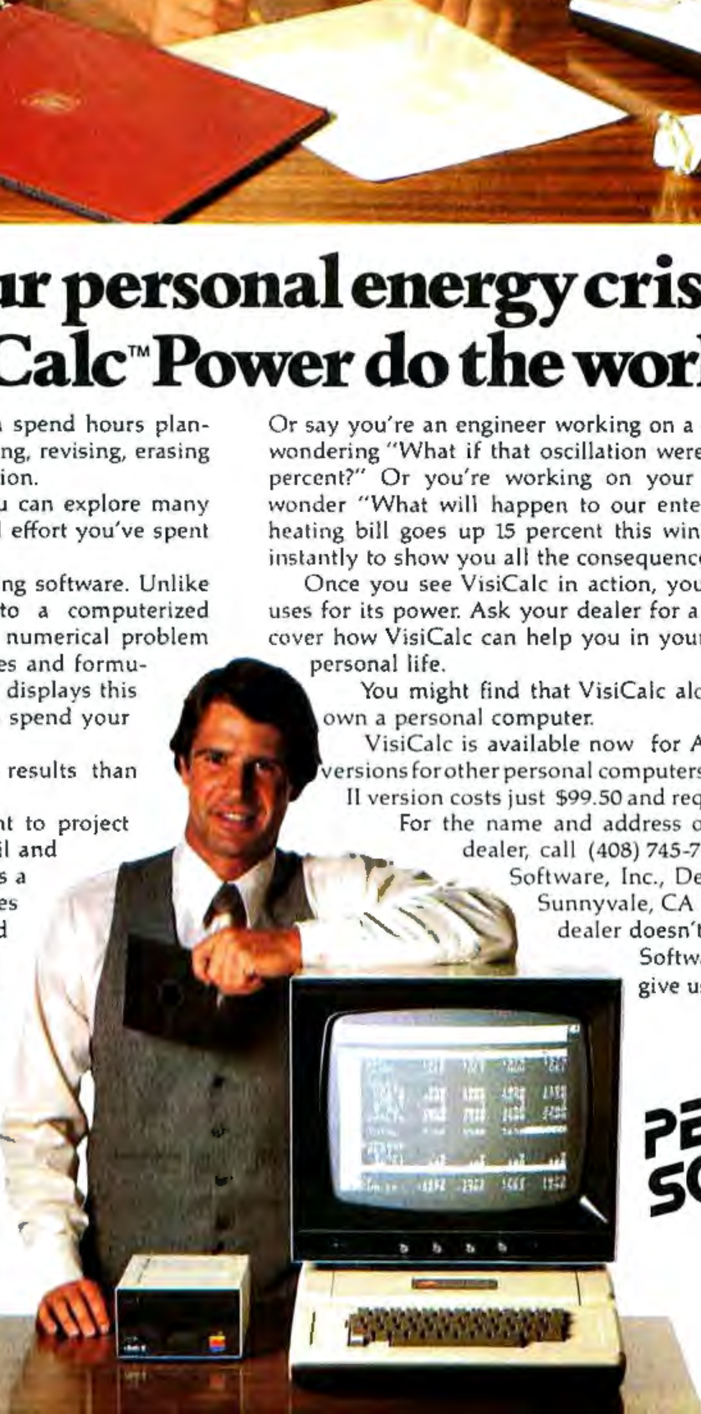

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Circle 301 on inquiry card.

Listing 2 continued from page 50.

```
21E3   F1        !                  ENDLOOP
21E4   C6 34     !NOT-IN-TABLE:     DEC  TOP-CLEAR-DOWN  %SQUARE NOT IN .BOARD
21E6             !            %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21E6             !            %%%%%%%%%%       BUILD I/O PORTS      %%%%%%%%%
21E6             !            %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
21E6             !             %**********SET UP PORT-SQUARE***********%
21E6   A5 30     !BUILD-PORTS:      LDA  SWITCH-FLAG     %SIDES EXCHANGED?
21E8   F0 07     !                  IF NOTZERO THEN
21EA   A5 32     !                     LDA  TCHANGING-SQUARE  %YES, SET PS TO
21EC   49 77     !                     EOR# 77                %%77-"TCH-SQUARE"
21EE   4C        !                     JMP
21EF      F3 21  !                  ELSE                      %NO,
21F1   A5 32     !                     LDA  TCHANGING-SQUARE  %%PS="TCH-SQUARE"
21F3             !                  ENDELSE
21F3   85 2D     !                  STA  PORT-SQUARE
21F5             !             %****************PORT-A*****************%
21F5   A5 2C     !                  LDA  PORT-LIGHT
21F7   30 04     !                  IF POSITIVE THEN
21F9   0A 0A     !                      ASL  ASL        %NEGATIVE=X AXIS,
21FB   0A 0A     !                      ASL  ASL        %POSITIVE=Y AXIS.
21FD             !                  ENDIF
21FD   29 70     !                  AND# 70
21FF   EE 02 17  !                  INC@ PORT-B         %DISABLE LEDS
2202   0A        !                  ASL                 %DON I TOGGLE SPEAKER
2203   85 F3     !                  STA  TEMP
2205   A9 01     !                  LDA# 01
2207   2D 00 17  !                  AND@ PORT-A
220A   05 F3     !                  ORA  TEMP
220C   8D 00 17  !                  STA@ PORT-A         %STORE ALL BUT COLUMN
220F   A5 2D     !                  LDA  PORT-SQUARE
2211   29 40     !                  AND# 40
2213   4A 4A 4A  !                  LSR  LSR  LSR
2216   05 2D     !                  ORA  PORT-SQUARE
2218   29 0F     !                  AND# 0F
221A   0A        !                  ASL
221B   0D 00 17  !                  ORA@ PORT-A
```

Listing 2 continued on page 54

of color placed closest to the bottom X axis LEDs. After the chessmen are in place, the display will show all 0s. If you are playing White, make your opening move. If the computer is playing White, press the GO key.

To set up the pieces in a new configuration, or to continue a game that was halted earlier, set the chessboard up with the chessman in their desired position. Start the chess program as described above, but instead of pressing the PC key, press the DA key. Type in the name of each piece using the hexadecimal keyboard as you would when adding a new piece. Start the play by either making a move or by pressing the GO key.

To add a new piece to the board, set the piece on the desired square. The KIM-1 display will show 3 bytes of information. The first byte will be a random piece designation (as described on page 3 of the Microchess player's manual). The second byte is the square that the piece is on, according to the Microchess board-status table. If the piece has been captured, "CC" will be displayed. The third byte is the number of the square

Listing 2 continued from page 52:

```
221E   8D 00 17   !                    STA@ PORT-A          %OR IN COLUMN
2221              !                %****************PORT-B****************%
2221   A5 2C      !                    LDA  PORT-LIGHT
2223   18         !                    CLC
2224   69 80      !                    ADC# 80              %TOGGLE PL FLAG BIT
2226   85 2C      !                    STA  PORT-LIGHT
2228   29 80      !                    AND# 80
222A   4A 4A      !                    LSR  LSR             %SET X OR Y AXIS AND
222C   8D 02 17   !                    STA@ PORT-B          %%ENABLE LEDS
222F              !              %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
222F              !              %%%%%%%  DID STATUS OF SQUARE CHANGE? %%%%%%%
222F              !              %%%%%%%    IF SO RECORD THE CHANGE    %%%%%%%
222F              !              %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
222F              !                %***************READ ROW****************%
222F   A5 2D      !                    LDA  PORT-SQUARE
2231   29 30      !                    AND# 30
2233   4A 4A      !                    LSR  LSR
2235   4A 4A      !                    LSR  LSR
2237   AA         !                    TAX
2238   B5 B7      !                    LDAX MASK-TABLE
223A   2D 02 17   !                    AND@ PORT-B
223D              !                %***********CHECK FOR CHANGES***********%
223D   D0 06      !                    IF ZERO THEN
223F   A5 34      !                       LDA  TUP-CLEAR-DOWN  %SQUARE OCCUPIED...
2241   10 10      !                       BPL  NEXT-SQUARE     %AND IN TABLE.
2243   30         !                       BMI
2244   04         !                    ELSE
2245   A5 34      !                       LDA  TUP-CLEAR-DOWN  %SQUARE EMPTY...
2247   30 0A      !                       BMI  NEXT-SQUARE     %%AND NOT IN TABLE
2249              !                    ENDELSE
2249              !                %*******FOUND A CHANGE, RECORD IT*******%
2249   85 35      !                    STA  UP-CLEAR-DOWN
224B   A5 32      !                    LDA  TCHANGING-SQUARE
224D   85 27      !                    STA  CHANGING-SQUARE
224F   A5 31      !                    LDA  TCHANGING-PIECE
2251   85 28      !                    STA  CHANGING-PIECE
2253              !           %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2253              !           %%%%%%%CHECK NEXT SQUARE OR RETURN IF ALL DONE%%%%%%
2253              !           %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
2253   E6 32      !NEXT-SQUARE:        INC  TCHANGING-SQUARE   %ADD ONE TO
2255   A9 08      !                    LDA# 08                 %%TCHANGING-SQUARE
2257   25 32      !                    AND  TCHANGING-SQUARE
2259   0A         !                    ASL
225A   18         !                    CLC
225B   65 32      !                    ADC  TCHANGING-SQUARE %ADD "CARRY"
225D   29 77      !                    AND# 77              %MASK OUT GARBAGE

225F   85 32      !                    STA  TCHANGING-SQUARE
2261   F0 03      !                    BEQ  RETURN
2263   4C         !                    JMP                  %%%GO CHECK NEXT SQUARE
2264      B5 21   !                 ENDLOOP
2266   A9 00      !RETURN:          LDA# 00
2268   85 2E      !                 STA  SPEAKER-FLAG
226A   EE 02 17   !                 INC@ PORT-B
226D   A5 35      !                 LDA  UP-CLEAR-DOWN
226F   60         !                 RTS
2270              !
END OF ASSEMBLY
```

upon which the new piece was set down. Modify the first byte by typing in the correct name of the new piece. If the piece has been previously captured, it may be added to the piece table by typing the + key.

To change sides (Black to White, or vice versa), type the **E** key. A countdown will be initiated. Do not change sides before the opening move of the game; the King, Queen, and other pieces could become incorrectly reversed.

Conclusion

Although it may require a lot of solder, building the hardware is neither hard nor exacting work. As with most projects, if it doesn't work the first time the problem can usually be traced to an incorrect program, faulty wiring, or bad integrated circuits. In this particular project, the program is already written, the wiring is easy to check, and there are only 2 integrated circuits.

The electronic chessboard can, of course, be used for activities other than chess. Almost any game that is played with an X,Y type grid can be played by the computer, among these: checkers, tic-tac-toe, and nim.

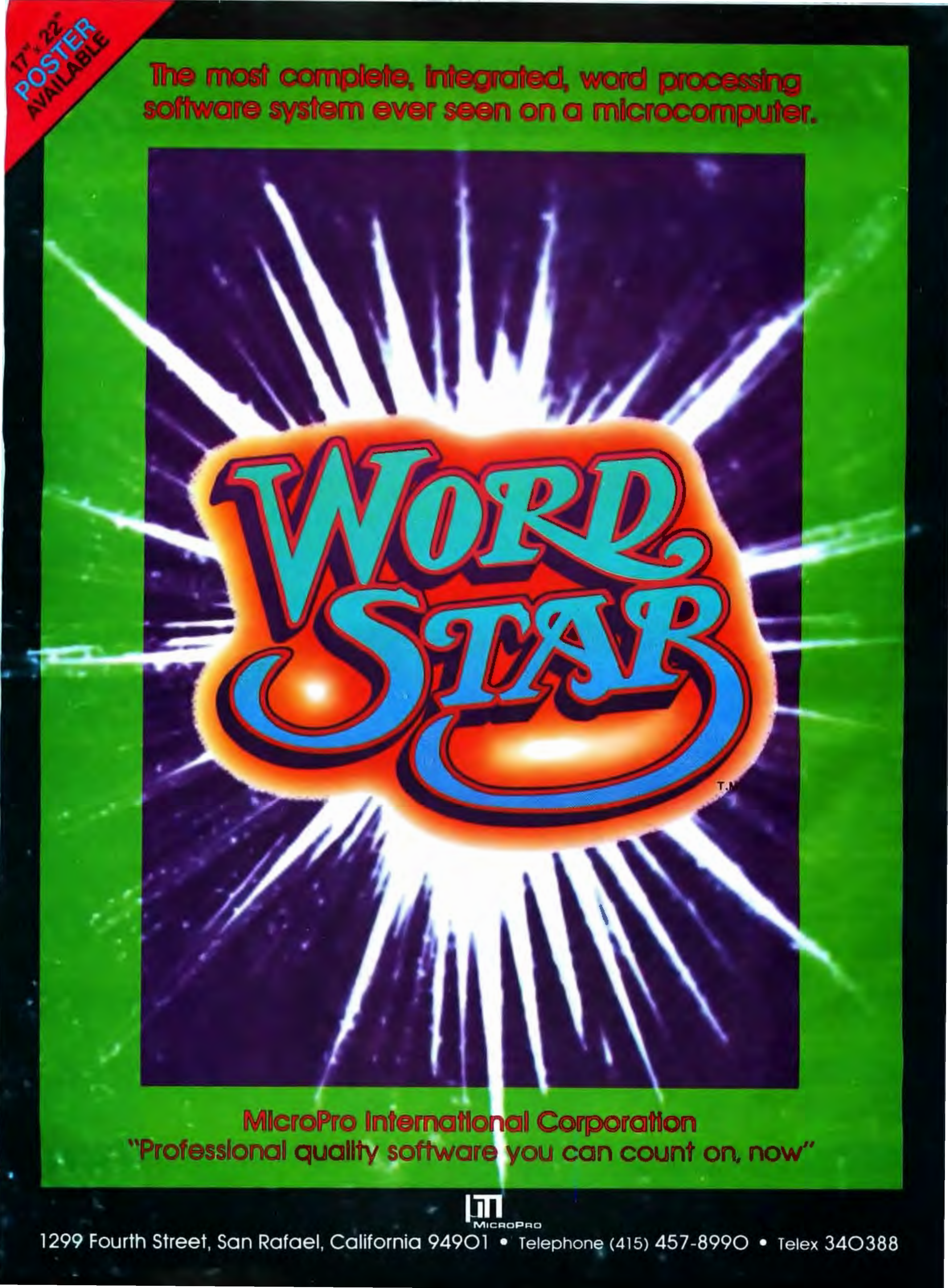
I have found that the chessboard interface makes playing chess with the KIM-1 much more enjoyable. Even if you lose the chess game, the method of playing is sure to be impressive. ■

Editor's Note

The program described in this article was designed to be "foolproof" for the beginning chess player. The countdown period for changing a move will greatly ease the frustration often experienced by players of computer games, the sinking feeling of "Oh no, I didn't mean that, and there's no way to take back the move!" More programmers should pay such attention to the user interface of their systems.

More experienced chess players generally abide by the following rule: a piece once touched by the player must *be moved, and an opponent's piece once touched* must *be captured. Such users would probably wish to delete the countdown period to speed the progress of the game.*

*An electronic chessboard operating in a similar fashion appeared in the article "Chess 4.7 versus David Levy" by J R Douglas (December 1978 BYTE, page 84). That board, constructed by Dr David Cahlander of Control Data Corp, uses 1 light emitting diode (LED) in each square of the chessboard to indicate the computer's move, and uses magnetic switches placed under the squares which are activated by the metal weights in the pieces. Controlled by a 6800 microprocessor, Cahlander's board transmits and receives moves to and from a remote computer on which the Chess 4.7 program runs...***RSS**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A Similarity Comparator for Strings

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Dept of Chemistry
University of Maryland
College Park MD 20742

The trouble with computers is that they have no common sense. If a computer is directed to search a file looking for a particular string of characters, a simple typographical error will cause the computer to report that no match has been found; even though there was something very close in the file. The statement "If A$=B$ THEN. . . " is taken literally by the computer; even the slightest difference is not tolerated.

Wouldn't it be better if a computer, finding no exact match, would report the *best* match, or the 5 best matches listed in order of closeness of match? To do this, a routine is needed that returns a quantitative estimate of the similarity between 2 strings. That is what the routine illustrated here does; it computes a similarity index on a scale of 0 thru 100 percent.

Listing 1 gives a BASIC string comparator program. The heart of the program is in lines 100 thru 290; lines 10 thru 90 are there only to allow the routine to be demonstrated with 2 manually input strings. The fundamental idea is simple: each character in one string is compared to each character in the other string. This is done so that *groups* of characters that match are weighted more heavily than the same number of matches of individual characters. This allows, for example, "POOL" and "POOR" to be rated more nearly equal than "POOL" and "POLO", even though the latter 2 strings have more characters in common.

```
10  LET T=0
20  LET P=3
30  PRINT "FIRST WORD" ;
40  INPUT A$
50  LET A=LEN (A$)
60  PRINT "SECOND WORD" ;
70  INPUT B$
75  IF A$=B$ THEN PRINT "EXACT MATCH"
80  LET B=LEN (B$)
90  IF A>B  THEN LET B=A
100 FOR M=1 TO B
110 LET C=0
120 FOR I=1 TO M
130 LET K$=MID$ (A$, B-M+I,1)
140 LET L$=MID$ (B$,I,1)
150 IF K$=L$ THEN LET C=C+1
160 NEXT I
170 LET C=C↑P
180 LET T=T+C
190 NEXT M
200 FOR M=B+1 TO 2*B-1
210 LET C=0
220 FOR I=1 TO 2*B-M
230 LET K$=MID$ (A$,I,1)
240 LET L$=MID$ (B$,M-B+I,1)
250 IF K$=L$ THEN LET C=C+1
260 NEXT I
270 LET C=C↑P
280 LET T=T+C
290 NEXT M
300 LET S=100*T/B↑P
310 PRINT S;"%"
320 LET T=0
330 GOTO 70
340 END
```

Listing 1: Listing of the similarity comparator program in Ohio Scientific Instruments 8 K BASIC (a Microsoft interpreter). The up arrow indicates exponentiation.

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The weighting of groups of characters is controlled by the variable P defined in line 20. If P is set to a value of 1, there is no special weighting of groups; only the total number of characters in common between the 2 strings is counted. If P is set greater than 1, groups are weighted more heavily, proportional to the value of P. If P is too large, however, all but the very closest matches result in low similarity index. A value of P=3 is a good compromise.

Line 300 scales the index to within a range of approximately 0 thru 100 percent. Two strings with no common characters give 0 percent similarity, while 2 identical strings give 100 percent similarity. Sometimes 2 nonidentical, but very similar, strings with many repeated letters (eg: "AAAAA" versus "AAA") will give 100 percent or greater than 100 percent similarity. This is seldom a problem with practical strings.

Strings of any type can be compared: names, addresses, numerals, or even strings containing spaces and punctuation. Long strings take a long time to compare, up to several seconds. An assembly language version should run much faster, if speed is important in your application.

The routine in listing 1 is written in Ohio Scientific Instruments 8 K BASIC, Version 1, and was run on a Challenger II system. The syntax of the string functions, particularly MID$, may be different in other BASICs. However, it should be compatible with most of the other BASIC interpreters which were developed by Microsoft. The program also runs without modification on an 8 K PET. ■

```
Sample Run                          Comments

RUN
FIRST WORD? POOL
SECOND WORD? POOL
EXACT MATCH
 103.1%                             >100% because of double letter
? POOR                              3 letter pattern "POO" matches.
 45.3%
? COOL                              Still a 3 letter pattern.
 45.3%
? POO                               Same match, because nonmatching
 45.3%                              characters do not count.
? POLO
 28.1%                              Two 2 letter matches, "PO" and
? LOOP                              "OL", do not count as much
 18.7%                              as one 3 letter match.
? PAIL
 12.5%                              Only 2 isolated letters.
? POOL ROOM
 10.4%
? MAIL ROOM
 1.5%
? PO/OL                             Presence of extra random
 14.4%                              character reduces match.
? OOOO                              Repeated letters result
 40.6%                              in unexpectedly high match.
?
OK
RUN
FIRST WORD? T.C. O'HAVER 710 HILLSBORO DR. SILVER SPRING MD.
SECOND WORD? TOM O'HAVER 710 HILLSBORO DR. SILVER SPRING MD.
 82.9%
? R.D. O'HAVER 710 HILLSBOROUGH RD. SILVER SPRINGS FL.
 10.3%
?
OK
```

Listing 2: A sample run of the program, with comments explaining the value of similarity assigned.

Note: *We entered this program into an Apple II computer using the Applesoft floating point BASIC. It ran without modification. The exact values of similarity computed did sometimes differ from those given in the sample run, but only in the fourth significant digit and beyond . . .*
RSS

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FOR SALE: Cromemco 16 K programmable memory 4 MHz, bank select. $400 or best offer. Will Ackel, 4860 Rolando Ct #22, San Diego CA 92115, (714) 287-6823.

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FOR SALE: SOL-20 computer by Processor Technology with 32 K, video display, cassette mass storage, Extended BASIC, IBM Selectric typewriter/printer, text editing and other software, complete documentation and manuals. Ideal for small business software development, 1.5 years old. $2500. Middleton Associates, 980 Yonge St Ste 404, Toronto Ontario, CANADA M4W 2J9, (416) 961-5136.

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Some Musings on Hardware Design

Clayton Ellis
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The purpose of this article is to acquaint the reader with some of the more interesting types of transistor-transistor logic (TTL) integrated circuits, the ease with which logic design can be accomplished, and to offer a few design considerations and trouble-shooting hints to stimulate the homebrew use of digital logic.

Taking the topics in the above order, we start with a look at some of the more complex types of TTL chips in the "74xx" series. (We will ignore simple gates for the most part.) An example is the 7442. This integrated circuit is a binary coded decimal (sometimes called BCD) to decimal decoder. What this means is that the circuit will decode 1 line out of 10 based on a 4 bit binary code. Figure 1 shows the pin connections. Regardless of what it is called, it works like this: pins 12 thru 15 are a 4 bit binary input, pin 15 being the 1's bit (bit 0), 14 the 2's bit (bit 1), 13 the 4's bit (bit 2), and 12 the 8's bit (bit 3). Pins 1 thru 7 and 9 thru 11 comprise the output pins, each pin staying high (logic 1 or a higher level voltage of about 3 to 5 V) unless the corresponding binary code is applied to the input. For example, let's say that pins 12 thru 15 are 0101. In other words, 12 is at a logical low (about 0 V); 13 is at a logical high level (above about 3 V, less than 5 V), etc. In this case, pin 6 (indicating a decimal 5) would be at a logical low level (about 0 V). All other pins relating to decimal output numbers would be at a logical high level. Note that only one output pin will be low at any given time, corresponding to the binary value of the input lines. "Ahh," you might ask, "what if the input pins are at some binary value other than 0 thru 9?" The answer is easy; this constitutes an invalid input, and all output pins will stay high. Only valid decimal values will select an output pin.

Now let's move on to a module similar to the 7442, the 74154. Referring to figure 2, the first apparent difference is the larger number of pins on the 74154. This integrated circuit is a 4 line to 16 line decoder. Its operation is the same as the 7442, with but two exceptions: there are now 16 valid output lines, and provision is made to allow

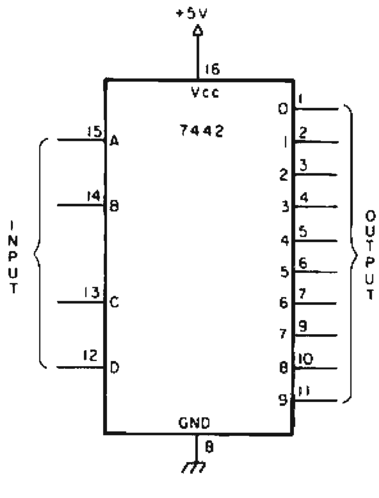

Figure 1: Pin connections for a 7442 TTL binary coded decimal to decimal converter.

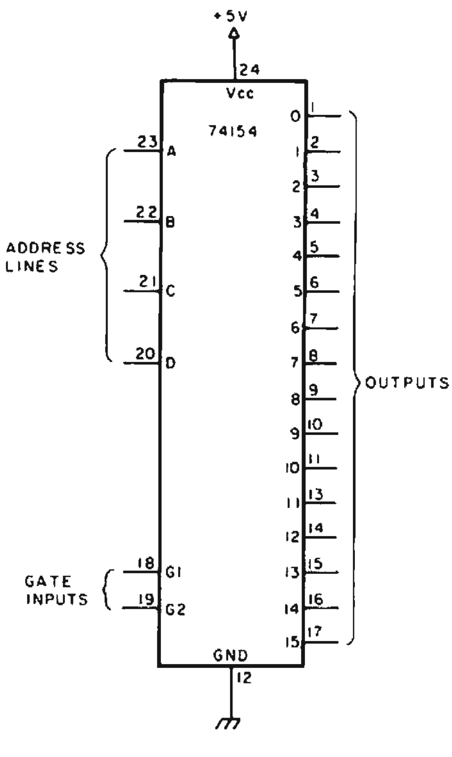

Figure 2: Pin connections for a 74154 TTL 4 line to 16 line decoder.

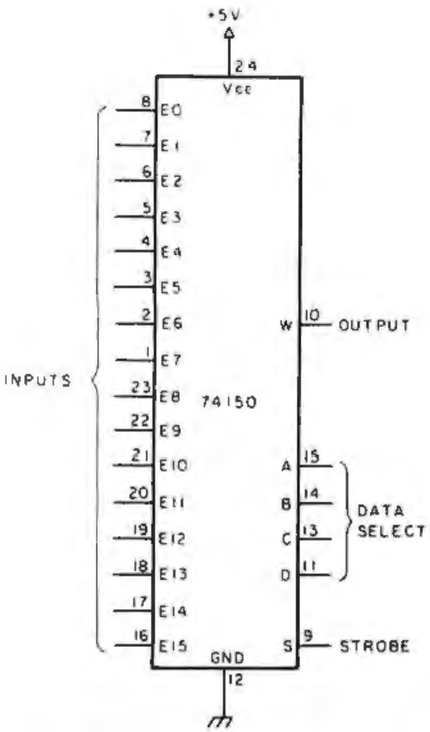

Figure 3: Pin connections for a 74150 TTL 1 of 16 line data selector.

two extra inputs to gate the individual line selected. Pins 18 and 19 perform this gating function. An example of use of this extra gating feature might look like this: pins 20 thru 23 might contain the binary equivalent of a decimal 14, pin 19 being low and pin 18 alternating from high to low (a periodic clock pulse.) The end result is that pin 16 (corresponding to line 14) will also periodically alternate high and low in following the signal on pin 18. The data at pin 18 is transferred to pin 14. If the binary code on pins 20 thru 23 were now changed to a decimal 7, then line 7 (pin 8) would follow the data on pin 18. We select one of 16 outputs for a signal applied to the gates. Now, if we could just have a binary controlled switch to select 1 of 16 inputs. Let's look at the 74150. Figure 3 shows the pinout of this one. This time there are 21 input pins and only 1 output pin.

Let's see how this one works. Binary input is on the 4 lines of pins 11 and 13 thru 15. Let's say a binary value of 12 is present. This selects the number 12 input line (pin 19) and transfers the level of this line, be it steady, high, low or some alternating clock signal, to pin 10, the output line. Notice, though, that in order for the data to be transferred, pin 9 (the strobe input) also must be low. A high level on the strobe input prevents any data transfer from any input. This feature is used to allow data transfer only at selected intervals, such as

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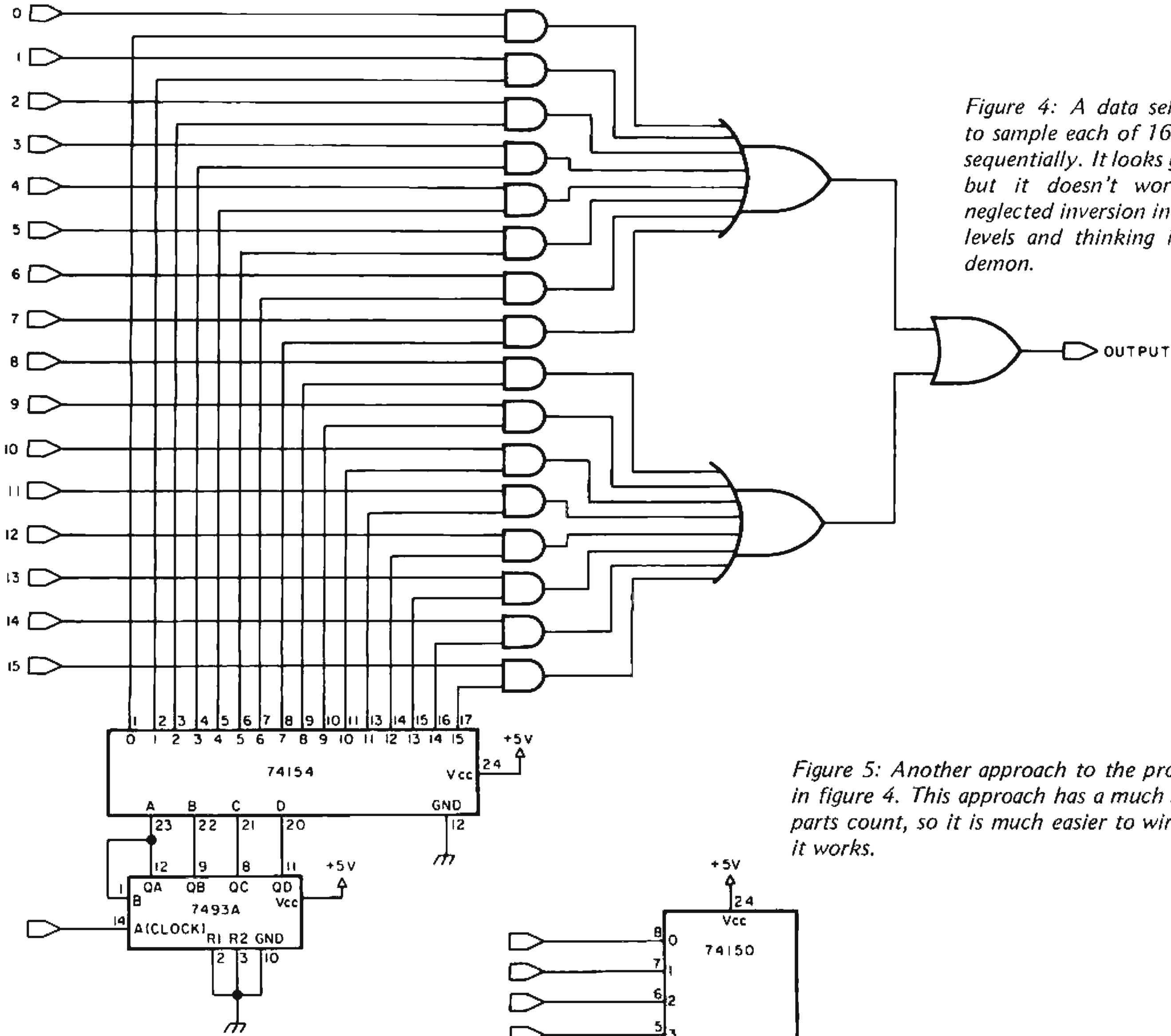
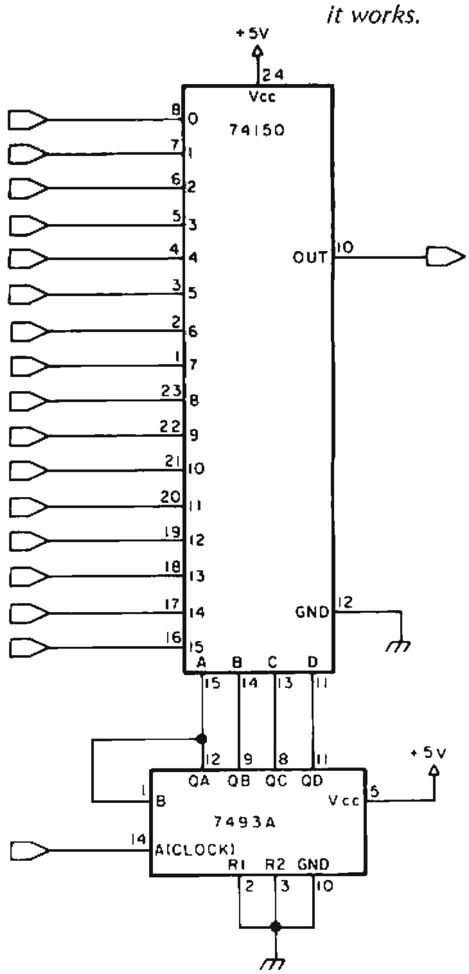


Figure 4: A data selector to sample each of 16 lines sequentially. It looks good, but it doesn't work. A neglected inversion in logic levels and thinking is the demon.

Figure 5: Another approach to the problem in figure 4. This approach has a much lower parts count, so it is much easier to wire and it works.



when the input would contain valid data, or when the output is useful only at specific intervals.

Now that we have taken a look at a few of the more involved logic blocks, let's look at how easy it is to design the somewhat more complicated circuits using the simple TTL blocks in conjunction with one or more of the above type of logic blocks.

If we want to build a sequencing device to look at a number of incoming lines, and if we are to use a given clock signal to coordinate all this, we can use the logic circuit in figure 4. A very simple and straightforward circuit, right? Not quite. Let's take a second look. All the inputs but the one selected by the 74154 are going to be enabled at one time. The selected pin goes low, remember? By this time, if not before, you probably recalled the look we just took at the 74150 and are wondering why we did not use it. Figure 5 shows the circuit using the 74150. The foregoing just illustrates a good point (and one to keep in mind whenever you undertake any logic design). There

- Get circuit requirements down on paper in block form.
- Break each block down into required logic.
- Use the most integrated block available for each function as in the example of figure 5 unless the cost of such a module is much higher than two or possibly three less intricate ones.
- Don't go overboard with smaller blocks. This increases the density and complexity of interconnection, greatly increases the chances of errors and reduces system reliability.
- Cross-check all designs, as you may have redundantly developed the same signal line. Sometimes most of one segment of a circuit can be eliminated with an inverter or small amount of additional gating.
- If possible, have a friend familiar with digital logic go over the layout. Your friend can sometimes suggest circuit reductions that you missed simply because you were thinking one way while your friend used a different approach. The same review may even spot an error in the logic. With all those inversions, gating, etc, it is easy to do. Spotting an error at this stage can save hours at the breadboard stage.

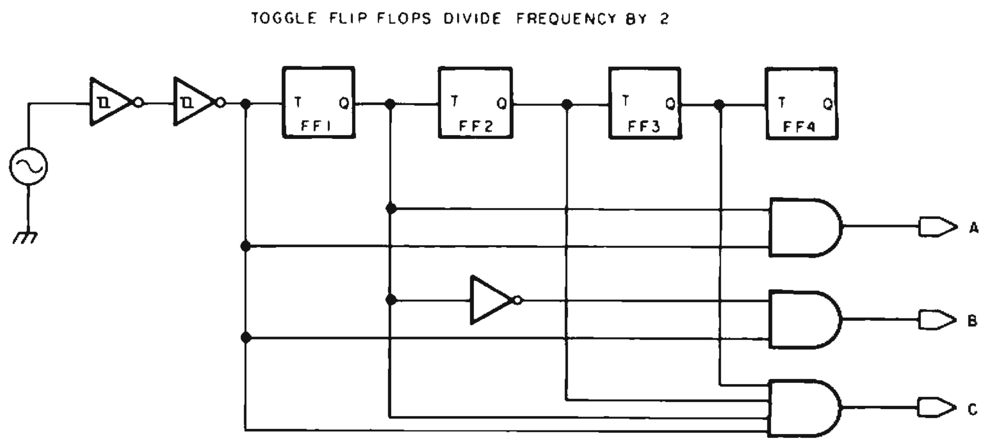
Table 1: Approach to finding the simplest logic circuit for a given function.

are many ways to accomplish a specific function. So many, in fact, that large companies who do digital logic design in large quantities invariably use some form of computer aided logic design. The homebrew enthusiast obviously can't go that far, but the approach summarized in table 1 usually works fairly well.

Timing

Another good point to keep in mind is to think time (not in terms of how long it takes to design a circuit, or build it, but time relationships in the circuitry itself). This brings us back to a term, clock, that we have been using freely up to now. We all know that a clock is merely a line, usually derived from a square wave oscillator, right? This line is then used to coordinate all necessary gating, shifting, setting and resetting, etc, that goes on within the circuitry itself, right? Well, that is part of it, but who said it had to be a single line? Some computers use a number of clock lines, perhaps as many as 8 or 10. The only thing these multiple clock lines have in common is that they are usually all derived from the same oscillator and may be individually gated on or off, counted, decoded or subjected to any other valid logic manipulation.

Figure 6 shows a typical clock circuit detailing some of these practices. As you can readily see, almost any combination of clock times can be selected, and the flip flops can be extended as far as needed to select a single clock pulse or a repetitive series of clock pulses. The point to remember is that all pulses are derived from the same clock and each pulse on any line will be of the same duration as any other clock pulse. The single clock pulse shown on line C of the timing chart in figure 6 will start at the same time as the fourth clock



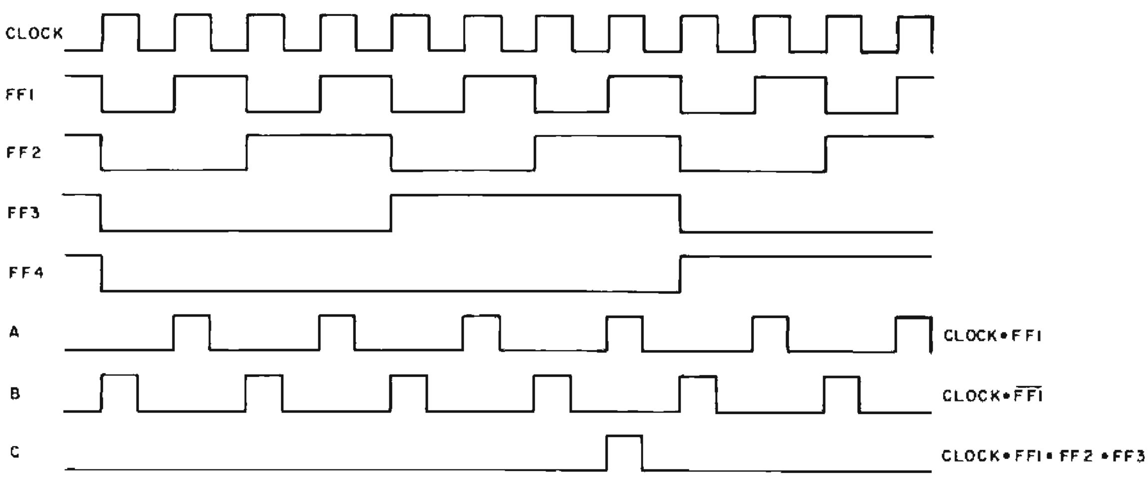


Figure 6: A hypothetical clock circuit to give two different phases (lines A and B) at two different repetition rates. Lines A and B are at 1/2 the clock rate. Line C is at 1/8 the clock rate with the same pulse duration.

pulse on line A, and the duration will be identical.

There is one fly in the ointment at this point. I just noted that the two clock pulses would start at the exact same time. That is not quite true, however, and depending on how fast the clock is running, and exactly what is being gated, this may or may not be a problem.

In an actual circuit, the clock pulse on line A would go positive slightly ahead of the pulse on line C. This is due to the delay (called propagation delay) across each flip flop encountered by the leading edge of the pulse. This delay is on the order of nanoseconds for each gate encountered. Let us assume an arbitrary 5 ns delay for each gate. Then the delay from the input of FF1 to the output of the AND gate driving line A would be 10 ns. This is 5 ns for FF1 and 5 ns for the AND gate. The delay from the input to FF1 to the output of the AND gate driving line C would be not 10 ns, but 20 ns: 5 ns for each of the three flip flops and 5 ns for the AND gate. The pulse on line C would actually start 10 ns after the one of line A. This will also make a difference in the duration of the pulse on each line; as the plus level arriving later than the clock pulse at the input to the AND gate determines when the output of the AND gate goes positive. However, the trailing edge of the clock pulse input determines when the AND gate output goes negative.

This, in effect, shortens the duration of the pulse on the output line by a time (in nanoseconds) determined by the various propagation delays. If the clock frequency of the circuit is on the order of tens or hundreds of kilohertz, then a delay of tens of nanoseconds would be of little consequence; but if the clock frequency of the circuit is something like 20 or 25 MHz, the delay can become a thorn in the side of the designer. This holds true for all data and control lines we well as clock lines.

This propagation delay can be used to an advantage too. Figure 7 illustrates using this delay to generate a narrow pulse. Here the positive going (leading) edge of the input is applied to an AND gate, but the negative going (trailing) edge of the inverted version applied to the other leg of the AND gate is delayed by the total of the propagation delay across the three inverter blocks. The resultant output is a narrow pulse equal in duration to the delay across the inverters. This method of generating a pulse is only useful in cases where we don't care *exactly* how long the pulse lasts since gates and inverters are subject to manufacturing variations.

To satisfy the rather picky individual or very high speed circuit, I have to say also that the output pulse is not only derived from the inverter delay, but is delayed from the leading edge of the original pulse by the amount of the delay across the AND gate itself. Figure 8 illustrates this. The short delays shown on waveform C are due to the AND gate propagation delay. For most situations, this is carrying propagation delay accounting to extremes, but in certain high speed circuits each delay may have to be accounted for. If 20 or 30 gates are involved, the cumulative effects add up rather fast.

Also to be considered is the capacitive effect of the interconnection lines: the distributed and stray capacitance which are in parallel with the output of each gate add slightly to delay times. It takes a finite amount of time to charge this capacitance at

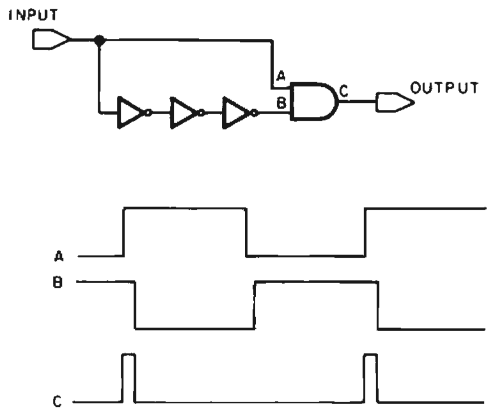


Figure 7: A pulse generator for nanosecond range pulses. Pulse length is determined by the propagation time through the gates between the input and point B. More sophisticated methods are required if an accurate pulse length is required.

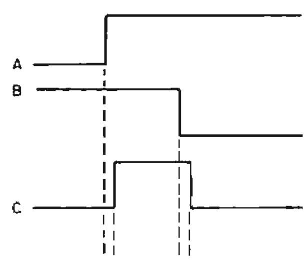


Figure 8: A magnified view of the pulse shown in figure 7. The output pulse is delayed by the propagation time of the AND gate. This time varies but is typically about 10 ns for normal transistor-transistor logic, less for the high speed and Schottky version and more for the low power integrated circuits.

each gate turn on, and the gate will not switch until a certain voltage input level is reached. All of which leads right into the last subject I'd like to touch on. How do you see all this in an actual circuit? Believe me when I say that it takes a good oscilloscope. To have a good display in the tens of nanoseconds range, it takes an oscilloscope with a bandwidth of at least 60 to 100 MHz.

Does this mean that anyone without such an oscilloscope can't do much with higher speed TTL? Not necessarily. Remember we said that propagation delay only becomes a problem at high speeds and multiple gate delays. There are a number of ways around this. One is to keep clock frequencies and data changes as slow as possible. Don't use a fast clock or data encoding just for the sake of speed, run it as fast as necessary and no faster. If you can tolerate a slow clock speed, use it. Another method is to try and bring each data line that is to be gated with another line through the same number of gates as the line it is to be gated with. In other words, if one line originates at about the same source as another that it is to be gated with, but passes through 9 levels of gating, and the other line passes through 3, the delays at high speeds can be a problem. This could be compensated for by changing the way the lines are gated to bring the delays in each line closer to the same length. Another help in extreme cases is to run the line with the lesser number of gates through several pairs of inverters. This introduces a delay to compensate for the delay in the other line. In other words, make the faster line wait for the slower one. An even better solution is to design your circuits "synchronously" so that only one clock source ever changes the *state* of a flip flop or memory cell.

As to seeing these problems on the slower oscilloscopes, there are several hints that will help. Very little serious work with timing relationships can be undertaken without a dual trace capability (although a good deal can be done otherwise with TTL with just a single trace scope). Even with a dual trace oscilloscope, the fastest sweep speed may not reveal a lot of timing detail if not set up correctly and the alternate sweeps may not be time correlated without a common synchronization signal. A number of tests can be made with a single trace oscilloscope if it has provisions for external synchronization.

In general, synchronize the oscilloscope sweep as far ahead in time as is realistic for the signals in question, in order to allow time for the sweep to start before the pulse actually arrives. It goes without saying that the synchronization signal must be common to all signals being examined.

If you still can't see any difference, try estimating the approximate delay for each line from source to common logic block. Most logic handbooks list typical delays for integrated circuits. If the problem is in a counter circuit of some type which counts "up," the count for a given sequence will usually be too high in value if delay problems are the cause. Rarely will the count of an "up" counter be too low, as the usual situation is advancing the counter by an extra pulse generated by mismatched delays, especially if a lot of exclusive ORing is being done. The situation where early turn off or disabling of the counter causes a missed count is quite unlikely, mainly because the delay is of a much shorter duration than the pulses being counted.

These problems are all good to be aware of, but don't let them deter you from starting that project you were thinking about. You may go a long time before you see one of the problems described. Don't let the lack of a superb oscilloscope deter you either. A lot of very intricate and fast digital circuitry is being built every day with nothing more than a single trace 1 MHz AC coupled oscilloscope. With a little experience, you can tell a great deal about a given TTL circuit with one of these inexpensive oscilloscopes.■

A Low-Speed Analog-to-Digital Converter for the Apple II

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The development of microprocessor-based computer systems has progressed to the point where it is now practical to utilize these systems in a scientific or laboratory application. To be useful in a scientific application the computer must have the capability of converting analog signals to digital signals. Very few home computers have this capability. Certainly it is a straightforward task to design an analog-to-digital converter (ADC), but the real problem lies in connecting the converter to the computer.

The Apple II computer, with 8 peripheral-board connectors on the mother board, makes the job of designing and implementing special interfaces (such as the ADC) relatively easy. The peripheral-board connectors give the hardware designer access to all address, data, and control lines. In addition all control, address, and data lines have been buffered, and certain address bits have been decoded to give a device select ($\overline{DS}$) signal. What this means is that when a specific range of address locations is accessed, the $\overline{DS}$ line will give a low output signal. Since the peripheral-board connectors are on the main computer board, the finished interface board will be inside the computer and will be able to use the computer's power supply. Because of these characteristics, turning the Apple II into a real-time data analyzer becomes a matter of designing an analog-to-digital converter circuit, and control logic to meet the need of the application.

Number	Type	+5 V	GND	−5 V
IC1	MC14028	16	8	—
IC2	MC14049	1	8	—
IC3	SN7427	14	7	—
IC4	MC14013	14	7	—
IC5	MC14433	24	13	12
IC6	AD580	—	—	—
IC7	MC14503	16	8	—
IC8	MC14503	16	8	—
IC9	DM7432	14	7	—

Table 1: Voltages which must be supplied to integrated circuits in figure 1 for operating power.

Many of the applications that I had in mind were to be of a low-speed nature (eg: monitoring the temperature of experimental animals in medical physiology laboratories, analyzing the results of electrophoretic analysis). Therefore, a low-speed analog-to-digital converter built around the Motorola MC14433 integrated circuit seemed to be a cost effective approach. I was inspired by Steve Ciarcia's article, "On a Test Equipment Diet? Try an 8 Channel DVM Cocktail!" (December 1977 BYTE, page 76).

The left section of figure 1 shows the analog-to-digital converter circuitry. All data and status lines to the computer are isolated through the MC14503 3-state buffers (IC7 and IC8). The MC14433 (IC5) is allowed to convert continuously at a rate of approximately 15 conversions per second. This means that if the data transfer to memory starts immediately after the conversion ends, the Apple II can easily decode and store the data from one conversion before another conversion occurs. IC4, configured as an RS flip-flop that is initially reset by the computer, is set by the MC14433 after an analog-to-digital conversion has been completed. When the computer senses this change in status, it starts the decoding and data transfer process. IC6 is an AD 580 used to provide a stable reference voltage to the MC14433.

The right section of figure 1 shows the control logic that is necessary to coordinate the transfer of data to the computer, and control signals from the computer. The circuit is designed so that the peripheral card resides in I/O (input/output) slot 7 on the Apple II mother board. The device select signal will go low whenever hexadecimal memory locations C0F0 thru C0FF are addressed. The least

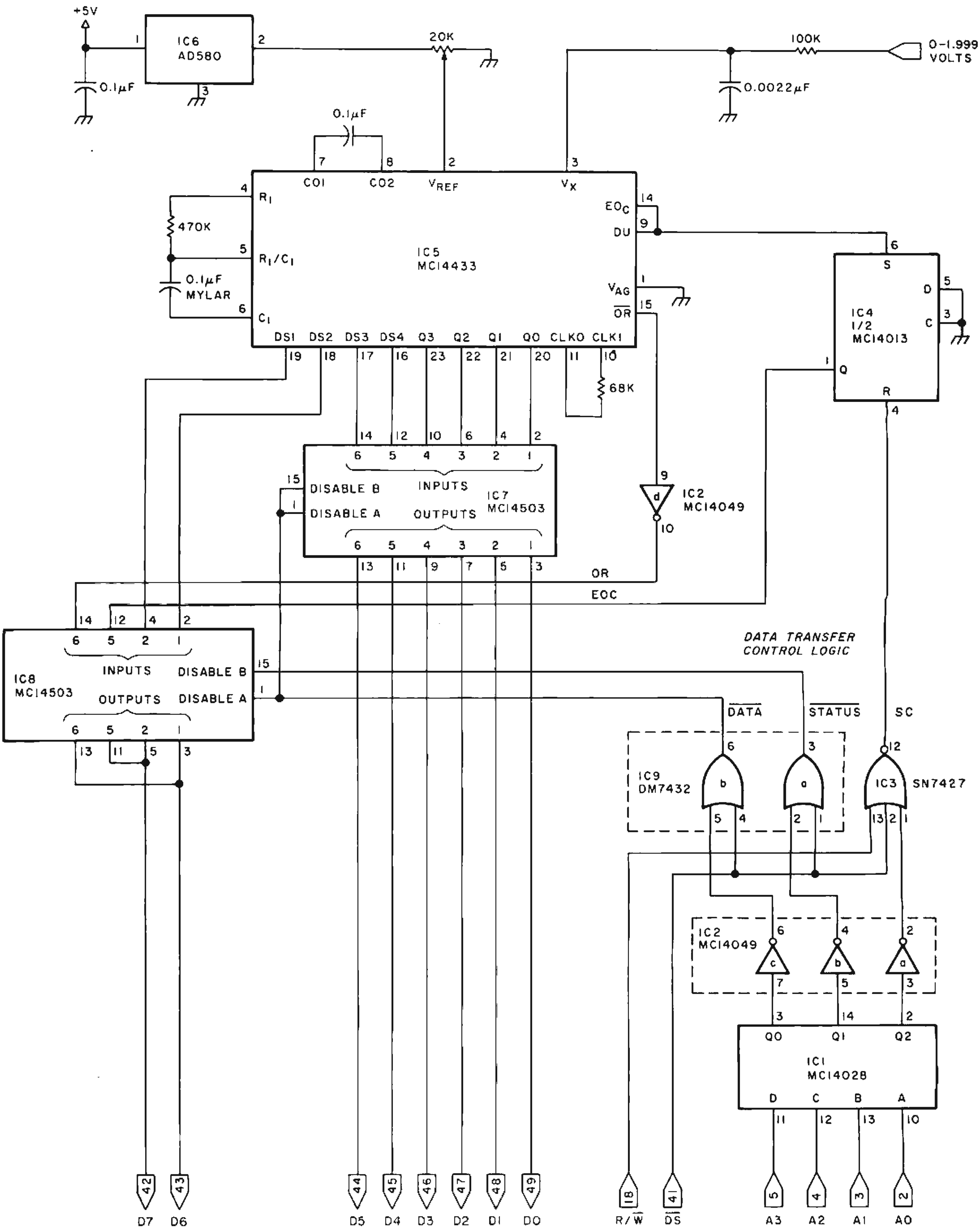
Text continued on page 74

Figure 1: Schematic diagram of analog-to-digital-conversion circuit and associated control-logic circuitry. The analog-to-digital (A/D) convertor is shown on the left side, the control logic on the right side. →

About the Author

Richard Hallgren is an Assistant Professor in the Dept of Biomechanics at Michigan State University. He is working on the application of microprocessor-based systems in scientific research.

ANALOG-TO-DIGITAL CONVERSION CIRCUIT



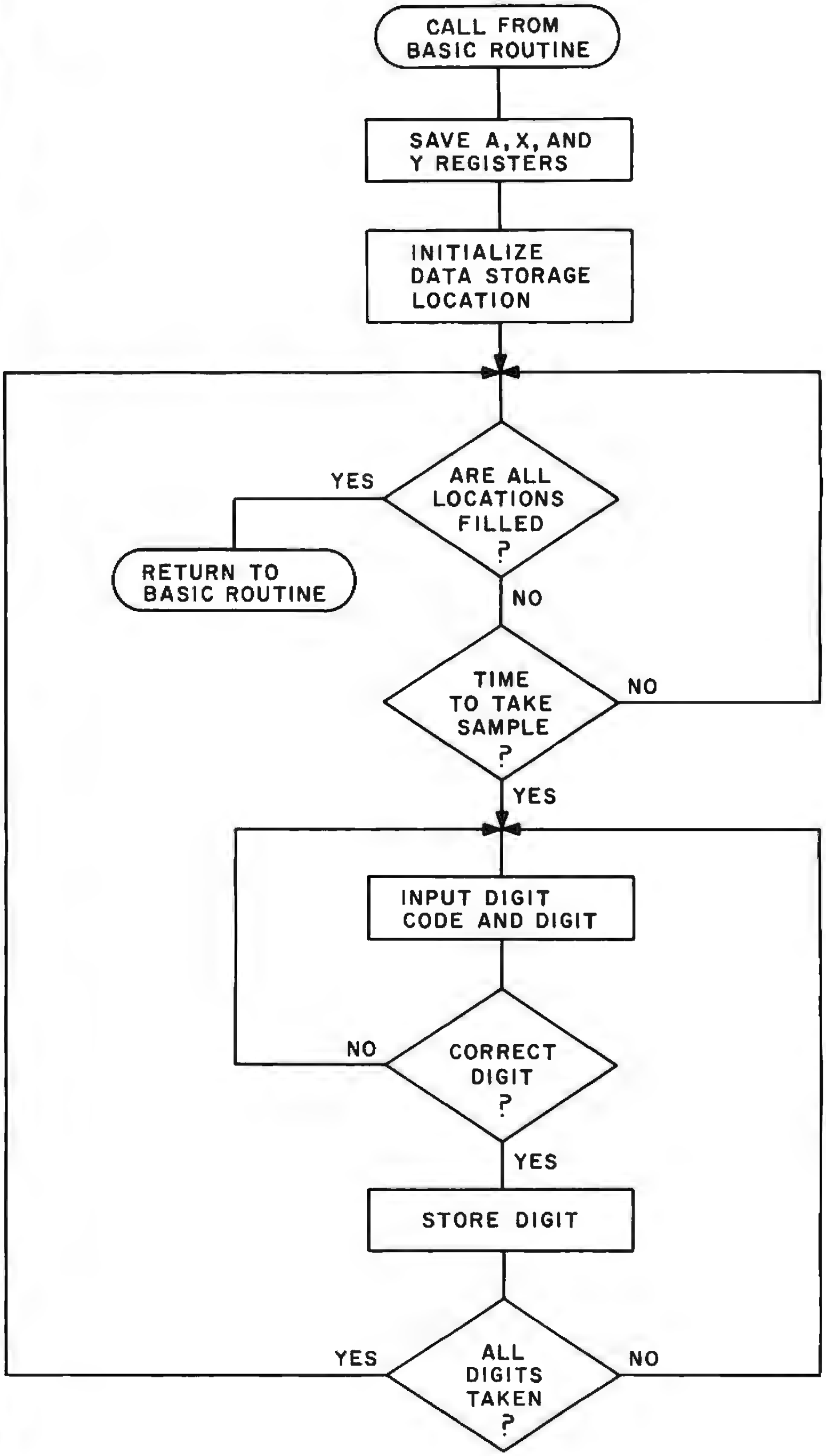


Figure 2: Flowchart of the machine language subroutine which takes samples from the analog-to-digital converter. This code is written for the 6502 processor used in the Apple II.

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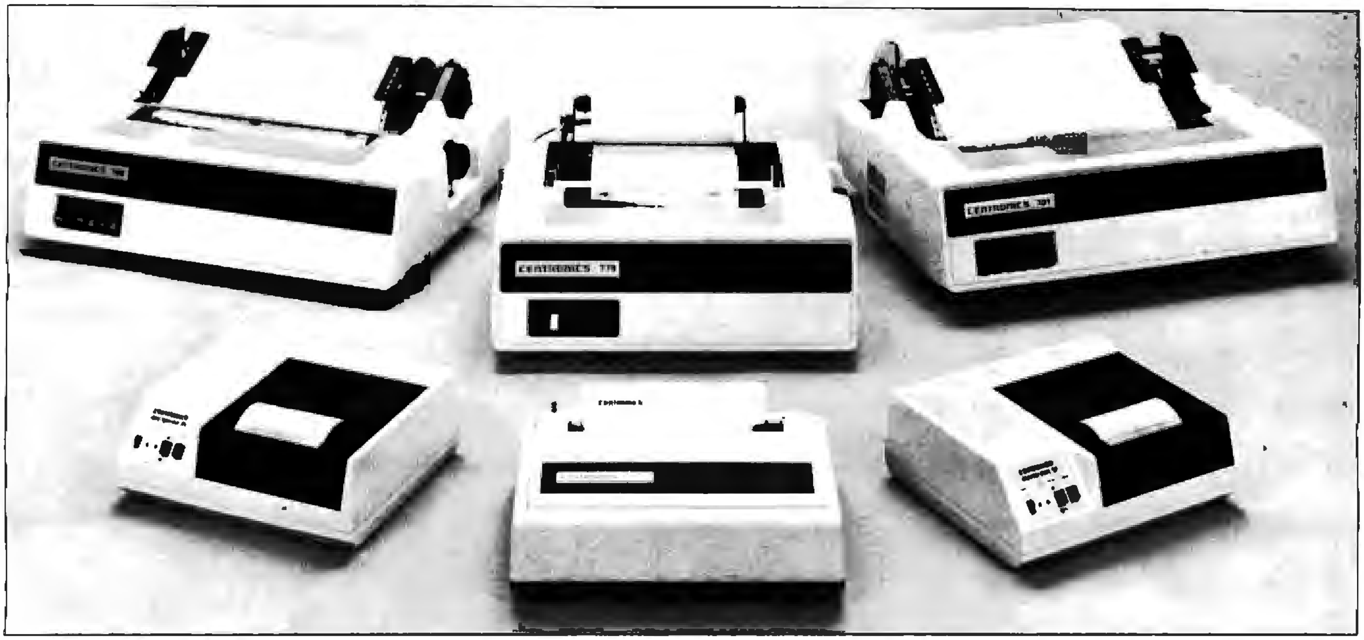

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Listing 1: The machine language subroutine for collecting data from the analog-to-digital converter, here shown in assembly language format. Memory locations 03FE and 03FF contain the hexadecimal interrupt jump vector 4040, which is the entry point of this routine.

Address	Instruction	Op Code	Operand	Comments
4000	AD B0 49	LDA	$49B0	
4003	8E B1 49	STX	$49B1	Save registers
4006	8C B2 49	STY	$49B2	
4009	08	PHP		
400A	A2 00	LDX	#$00	
400C	A9 00	LDA	#$00	
400E	85 0A	STA	$0A	Starting location of data storage
4010	A9 4A	LDA	#$4A	
4012	85 0B	STA	$0B	
4014	A9 00	LDA	#$00	
4016	8D A0 49	STA	$49A0	Final location of data storage
4019	A9 4E	LDA	#$4E	
401B	8D A1 49	STA	$49A1	
401E	78	SEI		Disable interrupt
401F	AD A1 49	LDA	$49A1	
4022	C5 0B	CMP	$0B	
4024	D0 0B	BNE	$4031	Have all data locations been filled?
4026	AD B0 49	LDA	$49B0	
4029	AE B1 49	LDX	$49B1	
402C	AC B2 49	LDY	$49B2	
402F	28	PLP		
4030	60	RTS		
4031	58	CLI		Enable Interrupt
4032	EA	NOP		
4033	4C 1E 40	JMP	$401E	
4036	EA	NOP		
4037	EA	NOP		
4038	EA	NOP		
4039	EA	NOP		
403A	EA	NOP		
403B	EA	NOP		
403C	EA	NOP		
403D	EA	NOP		
403E	EA	NOP		
403F	EA	NOP		
4040	8D F2 C0	STA	$C0F2	Start A/D conversion
4043	AD F1 C0	LDA	$C0F1	
4046	29 80	AND	#$80	
4048	C9 80	CMP	#$80	
404A	D0 F7	BNE	$4043	A/D conversion finished?
404C	AD F0 C0	LDA	$C0F0	Input data
404F	8D A2 49	STA	$49A2	Temporary data storage
4052	29 80	AND	#$80	
4054	C9 80	CMP	#$80	Check for first digit (MSD)
4056	D0 F4	BNE	$404C	
4058	AD A2 49	LDA	$49A2	
405B	29 0F	AND	#$0F	Peel off digit code leaving data
405D	81 0A	STA	($0A,X)	Store data
405F	A4 0A	LDY	$0A	
4061	C8	INY		Increment lower 8 bits of data storage
4062	84 0A	STY	$0A	
4064	D0 05	BNE	$406B	Carry out to upper 8 bits?
4066	A4 0B	LDY	$0B	
4068	C8	INY		Increment upper 8 bits of data storage
4069	84 0B	STY	$0B	
406B	AD F0 C0	LDA	$C0F0	Input data
406E	8D A2 49	STA	$49A2	
4071	29 40	AND	#$40	
4073	C9 40	CMP	#$40	Check for second digit
4075	D0 F4	BNE	$406B	
4077	AD A2 49	LDA	$49A2	
407A	29 0F	AND	#$0F	Peel off digit code leaving data
407C	81 0A	STA	($0A,X)	Store data
407E	A4 0A	LDY	$0A	
4080	C8	INY		Increment lower 8 bits of data storage
4081	84 0A	STY	$0A	
4083	D0 05	BNE	$408A	Carry out to upper 8 bits?
4085	A4 0B	LDY	$0B	
4087	C8	INY		Increment upper 8 bits of data storage
4088	84 0B	STY	$0B	
408A	AD F0 C0	LDA	$C0F0	Input data
408D	8D A2 49	STA	$49A2	
4090	29 20	AND	#$20	
4092	C9 20	CMP	#$20	Check for third digit
4094	D0 F4	BNE	$408A	
4096	AD A2 49	LDA	$49A2	
4099	29 0F	AND	#$0F	Peel off digit code leaving data
409B	81 0A	STA	($0A,X)	Store data
409D	A4 0A	LDY	$0A	
409F	C8	INY		Increment lower 8 bits of data storage
40A0	84 0A	STY	$0A	

Text continued from page 70:

significant 4 bits of the address are decoded by IC1 and are used for on board addressing. Performing a store accumulator (STA) operation to location C0F2 causes the SC (start conversion) line to go high and resets the flip-flop IC4. Performing a LDA (load accumulator) from hexadecimal location C0F1 transfers the end of conversion (EOC) and overrange (OR) status data into the computer. Performing a LDA from location C0F0 transfers the digit-select code and the binary coded decimal (BCD) value of the particular digit selected into the computer.

The software portion of the analog-to-digital converter project is divided into 2 parts:

- A machine language routine to provide high-speed transfer of data from the MC14433 to the computer memory.
- A BASIC routine written in Applesoft floating-point BASIC to take the data in memory and format it into a voltage that can be displayed as a function of time with the high-resolution graphics routine.

Since the Apple II does not have an internal real-time clock, I decided to use the interrupt request line (IRQ) as an input for an external clock. The advantage to this is that a calibrated pulse generator can be used to determine the sampling rate. If desired, the computer can perform other tasks between samples. Knowing when each sample was taken makes it possible to display the data as a function of time with the high-resolution graphics routine. Since the Apple II high-resolution graphics allows the display of 256 points I decided to store 256 points in memory before displaying the data, but there is no reason why the data could not be displayed as it is taken. Figure 2 shows the flowchart of the machine language program, and listing 1

```
40A2   D0 05      BNE   $40A9     Carry out to upper 8 bits?
40A4   A4 0B      LDY   $0B
40A6   C8         INY             Increment upper 8 bits of data storage
40A7   84 0B      STY   $0B
40A9   AD F0 C0   LDA   $C0F0     Input data
40AC   8D A2 49   STA   $49A2
40AF   29 10      AND   #$10
40B1   C9 10      CMP   #$10      Check for LSD (least significant digit)
40B3   D0 F4      BNE   $40A9
40B5   AD A2 49   LDA   $49A2
40B8   29 0F      AND   #$0F      Peel off digit code leaving data
40BA   81 0A      STA   ($0A,X)   Store data
40BC   A4 0A      LDY   $0A
40BE   C8         INY             Increment lower 8 bits of data storage
40BF   84 0A      STY   $0A
40C1   D0 05      BNE   $40C8     Carry out to upper 8 bits?
40C3   A4 0B      LDY   $0B
40C5   C8         INY             Increment upper 8 bits of data storage
40C6   84 0B      STY   $0B
40C8   A5 45      LDA   $45
40CA   40         RTI             Return from interrupt
```

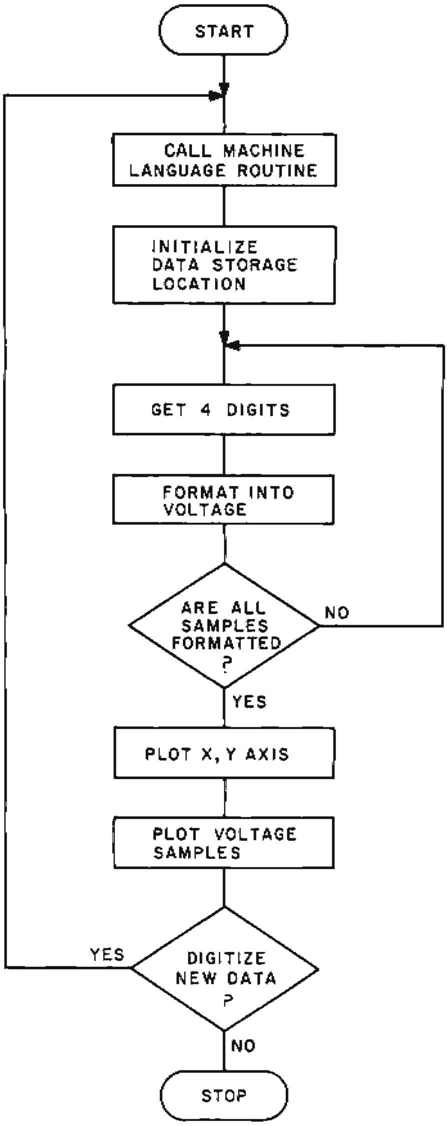
Listing 2: Program in Applesoft floating point BASIC which calls the machine language routine of listing 1 and then formats and displays the data received, using the high-resolution graphics capability of the Apple II.

```
       Program                                Comments

100    DIM Z (300)
101    HOME
102    GOTO 1000
110    CALL  16384                            Machine language routine
111    HOME : VTAB 24
112    PRINT "THE DIGITIZED DATA IS
        BEING FORMATTED  FOR PLOT
       ING"
113    X = 18944                              Starting address of data
115    FOR J = 0 TO 255
120    V1 = PEEK (X)                          Get first digit (MSD)
122    V2 = PEEK (X + 1)                      Get second digit
124    V3 = PEEK (X + 2)                      Get third digit
126    V4 = PEEK (X + 3)                      Get fourth digit (LSD)
128    X = X + 4
130      IF V1 > 7 THEN V1 = 0
132      IF V1 = 0 THEN GOTO 140              Decode MSD
134    V1 = 1
140    V$ = STR$ (V1) + STR$ (V2) +
         STR$ (V3) + STR$ (V4)                Convert digits into voltage XXX.X
150    Z(J) = VAL (V$)/1000
160      NEXT J
200      HGR: HCOLOR = 3                      High-resolution graphics
202      HPLOT 20,0 TO 20,150
204      HPLOT TO 279,150
208      HPLOT 18,0 TO 22,0
210      HPLOT 18,10 TO 22,10
212      HPLOT 18,20 TO 22,20
214      HPLOT 18,30 TO 22,30
216      HPLOT 18,40 TO 22,40
218      HPLOT 18,50 TO 22,50
220      HPLOT 18,60 TO 22,60
222      HPLOT 18,70 TO 22,70
224      HPLOT 18,80 TO 22,80
226      HPLOT 18,90 TO 22,90
228      HPLOT 18,100 TO 22,100
230      HPLOT 18,110 TO 22,110
232      HPLOT 18,120 TO 22,120
234      HPLOT 18,130 TO 22,130
236      HPLOT 18,140 TO 22,140
238      HPLOT 18,150 TO 22,150               Plot X-Y axis
240      HPLOT 4,47 TO 4,53
242      HPLOT 7,53
246      HPLOT 10,47 TO 10,53
248      HPLOT TO 14,53
250      HPLOT TO 14,47
252      HPLOT TO 10,47
260      HPLOT 7,103
262      HPLOT 14,97 TO 10,97
```

Listing 2 continued on page 78

Figure 3: Flowchart of the BASIC program which calls the machine language subroutine, formats the data obtained from the analog-to-digital converter, and displays it using high-resolution graphics.



shows the coded program with comments.

Upon entering the subroutine, all of the necessary registers are saved to enable a successful return from subroutine. The first thing that happens is that the *end of conversion* flip-flop is reset and the program loops until the MC14433 completes the next conversion and sets the flip-flop. The program then samples the data lines and decides whether or not the data represents the most significant piece of data. If it does not, the program continues to sample the data lines until the most significant piece of data has been obtained. This datum is then stored in memory, the memory storage locations are in-

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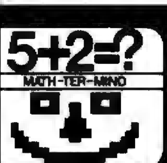

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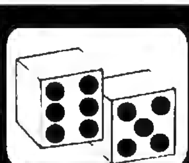
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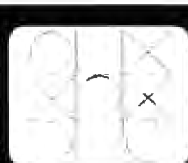
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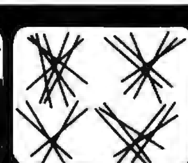
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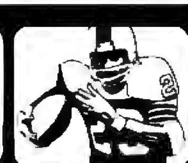
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Listing 2 continued:

```
264      HPLOT  TO 10,100
266      HPLOT  TO 14,100
268      HPLOT  TO 14,103
270      HPLOT  TO 10,103
272      HPLOT 14,147 TO 10,147
274      HPLOT  TO 10,153
276      HPLOT  TO 14,153
278      HPLOT  TO 14,147
280      HPLOT 30,148 TO 30,152
281      HPLOT 40,148 TO 40,152: HPLOT
         50,148 TO 50,152
282      HPLOT 60,148 TO 60,152: HPLOT
         70,148 TO 70,152
283      HPLOT 80,148 TO 80,152: HPLOT
         90,148 TO 90,152
284      HPLOT 100,148 TO 100,152: HPLOT
         110,148 TO 110,152
285      HPLOT 120,148 TO 120,152: HPLOT
         130,148 TO 130,152
286      HPLOT 140,148 TO 140,152: HPLOT
         150,148 TO 150,152
287      HPLOT 160,148 TO 160,152: HPLOT
         170,148 TO 170,152
288      HPLOT 180,148 TO 180,152: HPLOT
         190,148 TO 190,152
289      HPLOT 200,148 TO 200,152: HPLOT
         210,148 TO 210,152
290      HPLOT 220,148 TO 220,152: HPLOT
         230,148 TO 230,152
291      HPLOT 240,148 TO 240,152: HPLOT
         250,148 TO 250,152
292      HPLOT 260,148 TO 260,152: HPLOT
         270,148 TO 270,152
300      FOR J = 0 TO 255
310      HPLOT J + 20,150 - (Z(J) * 100)        Plot voltage
320      NEXT J
1000      PRINT "PRESS RETURN TO START A/D"
1010     K = PEEK ( - 16384)
1012      POKE - 16368,0
1014      IF K > 127 THEN GOTO 1020
1016      GOTO 1010
1020      TEXT
1022      HOME
1024      VTAB 24
1026   PRINT "256 DATA POINTS ARE
         BEING DIGITIZED"
1028      GOTO 110
1099      END
```

cremented, and the program begins to look for the 2nd piece of data. After the 4 digits representing the digitized voltage have been stored, the program checks to see if 256 samples have been stored. If they have not, control returns to the beginning of the subroutine. When all 256 samples have been stored, the program returns to the BASIC routine which called it.

The BASIC routine has the task of assembling the 4 digits from each conversion into a single number which is equal to the measured voltage. A flowchart is shown in figure 3. The machine language assembly routine has previously taken each of the 4 digits from a single conversion and has stored them in individual memory locations. The BASIC routine uses the string manipulation capabilities of Applesoft BASIC to fetch each digit from its memory location and to assemble all 4 digits into a single 4-digit voltage. After all 256 conversions have been changed into voltages and stored in a matrix array, the high-resolution graphics routine is called and the voltages are plotted as a function of time. It is convenient to have the voltages stored in a matrix array so that if further analysis of the data is required it can be easily retrieved. Listing 2 shows the coded BASIC program with comments.

To demonstrate the ability of a system to digitize and display low-frequency signals, a waveform generator was connected to the analog-to-digital converter. Photo 1 shows a 0.05 Hz sine wave which was digitized at 10 samples per second. Photo 2 shows a 0.05 Hz triangular wave which was digitized at 10 samples per second. Photo 3 shows a 0.001 Hz sine wave which was digitized at 1 sample per minute. The results are even more impressive when you consider that this is a data-acquisition system costing less than $2,000.

Photo 1: High-resolution display of a 0.05 Hz sine wave signal which has been digitized at 10 samples per second.

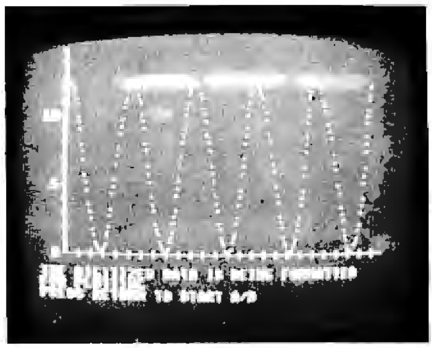
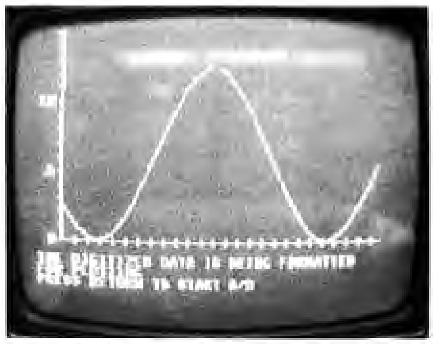


Photo 2: Display of a 0.05 Hz triangular wave digitized at 10 samples per second.

Photo 3: Display of a 0.001 Hz sine wave digitized at 1 sample per minute.



At present, a high-speed analog-to-digital converter is being constructed to digitize and analyze the electromyographic voltages which come from muscles. This will allow an investigator to gather data for further analysis of the complex neural-impulse waveform resulting from stretching a muscle. I anticipate that once researchers become aware of the data acquisition, data analysis, and system control that are possible with these low-cost systems, there will be a drastic increase in their use. ■

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NOTES ON BULLETIN BOARD

The Computerized Bulletin Board System (CBBS) in the Atlanta GA area is no longer being operated by DC Hayes Associates Inc. The Atlanta system is now being operated by the Atlanta Computer Society. The telephone number has been changed to (404) 394-4220. A description of a CBBS appeared in the article entitled "Hobbyist Computerized Bulletin Board" by Ward Christensen and Randy Suess, (November 1978 BYTE, page 150).

CITRUS COLLEGE OFFERS PERSONAL COMPUTING COURSES

Citrus College in Azusa CA is offering 2 personal computing courses to commence September 1979. Each class is 18 weeks long. The classes are:

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For further information, contact Ed Keith, Citrus College, 18824 E Foothill Blvd, Azusa CA 91702. ■

Operating Systems

Let's Have Some UNIX-Inspired Software

Jim Howell, 5472 Playa Del Rey, San Jose CA 95123

I would like to add to the comments made by James Jones ("Languages Forum," April 1979 BYTE, page 245) about operating systems.

First, I wholeheartedly agree with his letter. A job control language like OS/370 (or most other large systems, for that matter) would be terrible for personal computer use. Aside from the pile of job control required to do anything, there are other problems with OS-like systems. The numerous file formats and "access methods" make it difficult for programs to work together. Specifying files for the compiler or assembler to use as work files is a nuisance. A file specification (DD statement) also requires giving values for several parameters about which the user usually doesn't care or shouldn't have to specify. Some of these problems are helped by using procedures (sets of job control that the computer vendor or local systems programmer has stored on disk for general use), but these may not be what you need, and they also take up disk space. The space is not significant if your disks store 100 megabytes, but it could be significant for floppy disk users.

I would like to strengthen Mr Jones' suggestions that UNIX be used as a model for a microprocessor operating system. (UNIX is a trademark of Bell Labs.) I have used a UNIX system at work for about a year and it is a very pleasant system to work with. All files on UNIX are a series of bytes: no structure within files are imposed by the system. In particular, there is no concept of a "logical record" in UNIX. A "logical record" is the (usually) fixed size chunk in which files are read or written on big systems; often 80 bytes (for card or card-image files), or 120 or 132 bytes (for line printers). On UNIX, the end of a line in a text file is indicated by the use of a new-line character. This new-line character (line feed on UNIX) replaces the trailing blanks which are stored on systems that use logical records. The new-line character is read or written just like any other character. The size of a file is determined by how many bytes are written to it; predetermination of the file size (by guessing?) is not necessary, or even possible.

Job control language on UNIX is practically nonexistent. A command to run a program (such as a compiler or a user program) consists of the name of the program to be executed followed by any parameters that the program needs, separated by blanks. (Parameters are often file names and processing options.) The command processor, which runs as a user program, reads the command line, divides it into "words," and calls the system to execute the desired program. This system call also passes the parameters to the executed program. There is no need to describe files in the command since programs need only the name of a file in order to access it. Block sizes and such things are not required, even for new files, since there is only one format for files.

The following is a summary of the major system calls of UNIX that deal with file or an I/O (input/output) device. A file name in the open and create calls can also be a device name (such as the name for a terminal or printer).

Open	(name, mode) opens an existing file (or device) for further operations. "Name" is a pointer to a character string which is the name of the file (or device) and "mode" indicates reading, writing, or both.
Create	(name, prot) creates a new file, deleting any old file whose name is "name." This new file is opened for writing. (I would like to see a "mode" argument for this call, in addition to the two specified. This "mode" would mean the same as it does for "open.")
Read	(fildes, buffer, length) reads up to "length" bytes from the file whose descriptor is "fildes" into the "buffer". The file descriptor is a small, nonnegative integer which was returned by open or create. The number of bytes actually read is returned to the caller. A return of 0 means end of file.
Write	(fildes, buffer, length) writes "length bytes to the file "fildes" from the "buffer."
Seek	(fildes, offset, base) moves the read/write pointer of the file "fildes" to a new position within the file. "Offset" is how far to move the pointer, and "base" indicates from the start of the file, from the current position, or from the end of the file.
Close	(fildes) closes a file.

Each open file has a read/write pointer associated with it. Each read or write call starts reading or writing at the current pointer and advances the pointer by the number of bytes read or written. By moving the read/write pointer with the "seek" call, random access files (or even indexed-sequential or other access methods) can be implemented if required. Note that "read" and "write" are the lowest levels of I/O calls to the system, and that they apply to all devices. All device-dependent processing is inside of the operating system. The only thing that a user program needs to know about a file after it is opened or created is the returned number (file descriptor). There are no "control blocks" or other system-imposed structures in user programs. (System calls are available in UNIX to determine the type of device that is associated with an open file for the few programs that need this information.)

Most current microprocessor operating systems use a special character, such as control-z, to mark the end of text files. These systems take the view that "binary" files (files where all 256 possible bytes are valid) are only for executable programs, and in this case reading a few extra bytes from the last sector of the file will not cause any problems. Such a scheme prevents the use of binary files for other purposes where the exact end of the file must be known. Possible uses include a work file written by a compiler or assembler and libraries of subroutines in object format for linking with other programs. (For example you wouldn't want a 20 byte absolute value function to add 128 bytes to your program, simply because the end of a sector is the best you can do at locating the end of the function!) The end of a file should, as in UNIX, be indicated by a count of the number of bytes in the file, and the end of file when reading should be determined by comparing the read/write pointer of the file to the end-of-file byte count. (Writing past the end of a file causes the end of file pointer to move to the new read/write pointer position.)

The above is a description of some aspects of UNIX, and is also intended to be used as guidelines in writing any new operating systems for microprocessors (or even big systems). One other thing that might be considered by an operating system writer is the use of a high-level language for most of the operating system and for the programs that implement supplied commands. This would allow the operating system to be moved to another microprocessor without having to completely rewrite it.

I am about halfway through designing an operating system along the lines of the above suggestions. (I started before Mr Jones' letter appeared in BYTE.) Eventually I expect to implement it.

Let me conclude by listing three references which are recommended to those who are implementing a usable microprocessor operating system. The first two were also mentioned by Mr Jones. ■

REFERENCES

1. *Communications of the ACM*, July 1974. A revised version of the UNIX article appears in reference 3 below.
2. *Software Tools* by Kernighan and Plauger.
3. *The Bell System Technical Journal*, July thru August 1978, part 2. This issue contains about fifteen papers on UNIX. Read especially the first 3 or 4 papers, as well as the one called "UNIX on a Microprocessor" (single-user version on an LIS-11).

Soldering Techniques

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Anyone who can get 3 objects into the same vicinity can solder. Doing a professional job, however, requires some care and practice. This article draws on my experience in teaching electronics and a fine pamphlet prepared by NASA entitled "Soldering Electrical Connections, A Handbook" (United States Printing Office, NASA SP-5002). Good soldering techniques can save time, components and frustration.

Photo 1: After cleaning the tip of the soldering iron with a wet sponge, prepare it by adding a dab of solder.

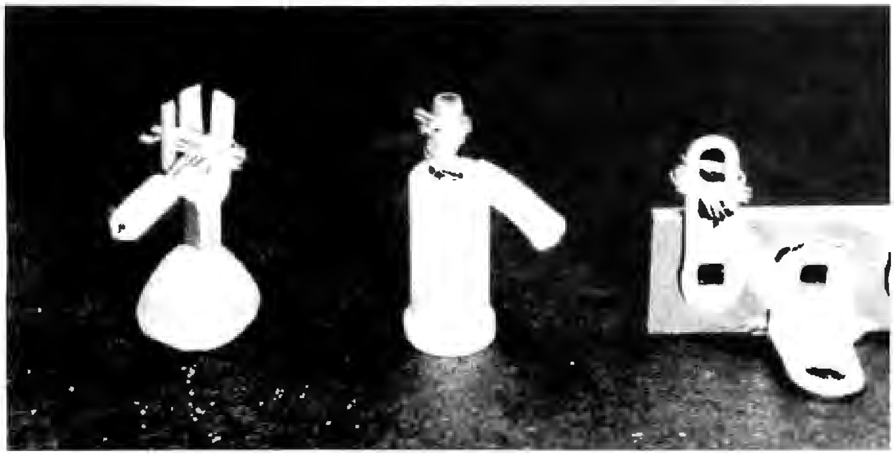

Photo 2: Before soldering, the joints should be mechanically fastened.

Good Soldering Techniques

Good soldering starts with a clean soldering iron tip and well-tinned parts. Just prior to use, the hot soldering iron should be cleaned by wiping it across a wet sponge. The thermal shock and wiping action will clean the tip and remove the excess solder. Then touch a bit of solder to the tip (photo 1). The iron is now ready for use. The parts to be soldered are ready when the solder flows quickly and evenly over their heated surfaces. If this does not happen, clean the parts by brushing, filing, or rubbing with a pencil eraser. Next flow a thin layer of solder over the clean surface. The parts are now tinned and ready to be soldered.

The prepared parts should be mechanically fastened together before making the soldering joint (photo 2). The solder should not be expected to supply mechanical strength. Clean the soldering iron tip, and add a dab of solder to the tip. Touch the soldering iron to the heavier of the parts to be joined, and begin wiping the solder on the junction between the two parts (photo 3).

Do not feed the solder into the soldering iron tip. When the components are hot enough, the solder will begin to melt into the joint. The solder should skate over the surfaces like butter on a hot pan. Now you must move quickly. Rapidly wipe the entire length of the connection with the solder, being careful not to apply too much. The solder should flow smoothly over the parts. If braided wire is used, the strands should still be visible (photo 4). Doing this well takes a lot of practice. Now remove

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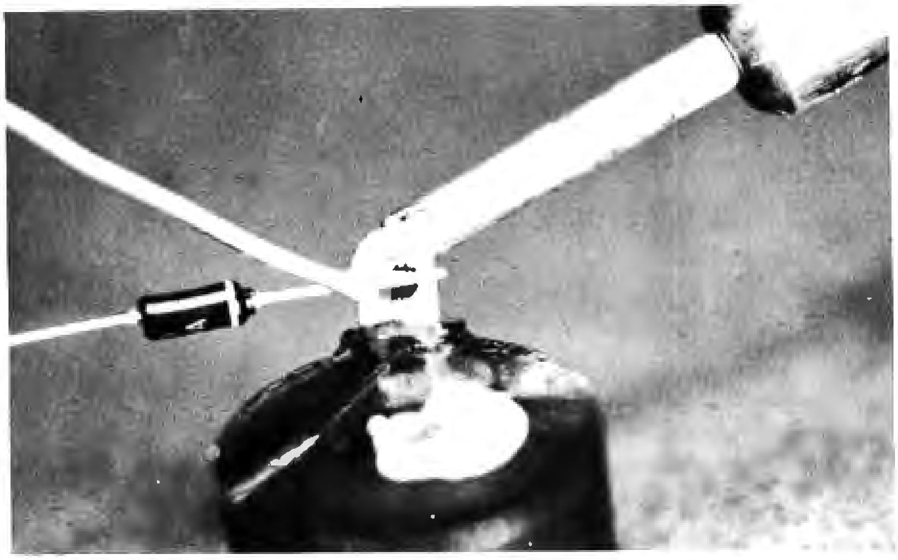

Photo 3: When soldering, touch the iron to the heaviest part. When the joint is hot enough, the solder will melt on the side opposite the iron.

Photo 4: In a well-soldered braided wire, the strands should still be visible.

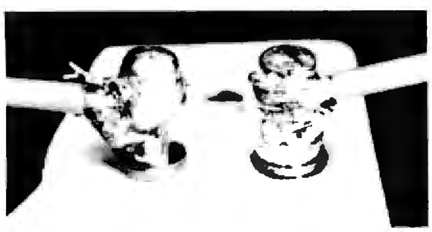

Photo 5: Excess solder, poor wetting of the wire, frosted surfaces, and blobs of solder represent poorly soldered joints.

the iron and hold everything perfectly still. Any motion while the solder is going from the liquid to the solid state will cause a cold joint. After the joint is cooled, the surface of the solder should look like a mirror. A good solder joint is an accomplishment.

A good way to begin might be to deliberately make some bad soldering joints. First, shake the two wires while the solder is cooling. Notice the undesirable frosted look. Now try leaving the iron on the joint for more than several seconds, and you will notice that a scum forms. Try putting too much solder on the joint. Often when this blob cools, the frosted surface will appear (photo 5). Try to find the two oldest wires you can. Twist them together and solder them. If they are covered with an oxide layer, the solder will not transfer from the soldering iron tip to the wires. Repeated heatings will probably cause the solder to melt around the joint. Notice how the solder does not flow onto the wires, but sticks to itself. The joint is now probably hot enough to burn the flux.

Inevitably, one has to unsolder some beautifully soldered joints. If the joint is that of a straight wire through a hole, a pull will often accomplish the task. (Be careful of the flying molten solder.) Often, one must remove the solder and then unwrap the wire. The best method uses a fine mesh of properly fluxed copper wire. (An example of this would be Solder-Wick, made by Solder Removal Co, 1077 E Edna Place, Covina CA 91724. Their 40-4-5 is a medium size, 40-6-2½ is for large joints, and 40-2-5 is for very small joints.) Push the mesh against the joint with the soldering iron. The solder will be wicked from the joint into the mesh. Solder suckers are also a popular way to remove solder. The tool is cocked, placed on a heated joint, and released. A plunger pulling air through the nozzle of the sucker gets most of the solder. This last suggestion is the least expensive way. Hold the circuit board and heat the joint. Rap the edge of the board smartly on the work bench. Solder flies in every direction, but the joint is clean.

Good soldering takes patience and practice. Fortunately, if properly done, the soldering joints are almost never the culprits when a circuit does not work. The following are some suggestions that will make soldering easier.

Tools

The soldering iron should be well tinned (covered with solder), and should quickly raise the joint to the working temperature. I prefer a 30 or 40 W element for a pencil soldering iron. Cleaning the tip with a wet sponge before soldering will bring the tip down to the correct temperature range (about 700°F). This slightly greater wattage will allow larger pieces to be soldered. Better yet are the temperature controlled pencil soldering irons. Soldering guns are too large and hot for all but the most massive soldering joints. If you buy a new soldering iron, wrap the tip with solder before turning it on. This will coat the tip with solder before it gets hot enough to oxidize. Place the iron in a protective cage towards the back of your work bench so that it can not burn anything. If the iron is not going to be used for a while, unplug it.

It is very tempting to buy less expensive solder. Don't do it. Solder costs very little compared to other components. The best solder is Eutectic, which is 63% tin and 37% lead. This mixture passes directly from a liquid to a solid stage without going through a plastic region. As a result, good soldering joints are easier to make. Solder composition is generally given by two numbers, such as 40-60. The first number is the amount of tin, the second is the amount of lead. The above solder is less expensive to make than Eutectic solder because tin is the expensive element. However, this solder has a plastic region of about 180°F. The joint must be held completely motionless while the solder is cooling through this plastic stage. Always use a rosin flux when soldering. Never let your iron touch acid flux. An 18 or 20 gauge solder with a rosin core works nicely.

There are a number of other useful tools. These include long nose pliers, diagonal cutting pliers, wire strippers, a slotted screwdriver, a dental pick, and plastic electrical tape.

Assembly Before Soldering

A convenient substrate upon which to build electronics is predrilled epoxy board. The holes should be on 0.1 inch centers in a square grid for digital work. Typical hole sizes are 0.042 or 0.062 inches. Vector-type terminals (Vector Electronic Co Inc, 12460 Gladstone Ave, Sylmar CA 91342) can be pushed into the holes and the discrete components soldered to the terminals. The majority of digital electronics come in the dual-in-line packages. A convenient way to mount dual-in-line packages is with circuit-stick-type subelements (Circuit-Stik Inc, 24015 Gardnier St, POB 3396, Torrance CA 90510). These are very thin sheets of glass epoxy with preetched copper lands on one side and glue on the other. The holes on the subelements are aligned with the holes on the predrilled circuit board, and carefully pressed together. The dual-in-line packages and components can then be pushed through from the other side of the board, and soldered to the preetched copper lands. One can then wire the correct lands together. Because the spacing between the pins of the dual-in-line packages is only 0.1 inches, hand soldering requires care. When working with dual-in-line packages, I prefer to solder sockets onto the board, and plug the dual-in-line packages into the sockets. This method makes troubleshooting easier.

It is important to be neat when soldering. Try to lay the board out logically. Do not crowd the components together. If it is your own design, you will probably want to add something after the board is made. Place all of the resistors the same way so that their color codes

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AWG	Diameter (mm)	Ohms per 1000m	Current Capacity (Amperes)
10	2.6	3.3	26
12	2.0	5.2	16
14	1.6	8.3	10
16	1.3	13	6
18	1.0	21	4
20	0.81	33	2.5
22	0.64	53	1.6
24	0.51	84	1.0
26	0.40	135	0.6
28	0.32	214	0.4
30	0.25	341	0.2

Table 1: Approximate values for various American Wire Gauge (AWG) sizes of copper wire.

can be read from the same side of the board. Run the wires in an orderly manner. I prefer to mount components like resistors, transistors, etc, slightly off the board. This improves the heat transfer, and makes it easier to slip in a probe for testing. Components that weigh 0.5 ounces or more should be mechanically mounted to the board. A little epoxy or silicon rubber works wonders for mounting these components.

Properly stripping wire is a dichotomy. First, the insulation should be cut and removed. Second, the wire should not be cut. (If stranded wire is used, a nick will cause only a few strands to break.) With practice, you can strip the insulation without cutting the wire. Try cutting slowly through a wire. Notice the difference in the feel between the insulation and wire. Now cut off the wire and start again with a clean end. Cut down until the wire is felt, then relax the stripper slightly. Now rotate the wire 45° and again squeeze a bit. This will cut the insulation all the way around, not just where the stripper teeth cut the deepest. Be sure to open the stripper slightly and pull the insulation off the wire. With practice, you can learn not to nick the wire. The secret is to stop cutting just before the cutter reaches the wire. A firm pull will usually break off the remaining insulation. If you still nick the wire, take heart, you have much company.

Table 1 gives the American Wire Gauge (AWG) size, the approximate diameter, ohms per 1000 meters, and current carrying capability of copper wire. Try to use a number of wires of different colors and gauges. This not only matches the current capability with the load, but also makes it easier to trace wires.

Finally, some words on safety: be sure that you have a stand for your iron; always wear shoes and safety glasses; and try not to flick solder on anything important. When cutting wires, hold the cutter so that the pieces fly away from you. To avoid potentially lethal shocks, it is best to have a rubber mat beneath your feet and stool.

By following these rules and techniques, almost anyone can learn to solder well. ■

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Clubs and Newsletters

Washington DC Computer Club

The Washington Amateur Computer Society (WACS) is an organization dedicated to personal computing. They are organized to provide a forum for the computer hobbyist and student of computing science. The Society meets on the last Friday of each month in the 1st floor lecture hall in Keane Hall on the campus of the Catholic University of America. The meetings start at 7:30 PM

JWAC, the club's newsletter, is published for Society members and exchange with other hobby organizations. The newsletter is primarily an electronics journal. Annual dues have been set at $3.50 per year to cover the cost of 1st class postage for the journal and to defray the expenses of exchanging correspondence with other personal computing organizations. Nonmembers may subscribe to the journal at the rate of $5 per year. WACS is interested in exchanging newsletters with other organizations to further the interchange of hobbyist information. Contact Washington Amateur Computer Society, c/o 4201 Massachusetts Ave, #168, Washington DC 20016.

Cromemco User Systems and Software Pool

Cromemco User, Systems and Software Pool is an independent group for users of Cromemco computers. Board owners are also welcome. The purpose of CUssP is the exchange among users of Cromemco hardware and software of operating notes, bugs and their fixes, evaluation of hardware and software, user written software, and other announcements relating to Cromemco and associated products.

The 1st volume of 3 newsletters included articles on changes in 16 K byte BASIC, CDOS I/O (input/-output) drivers, disk sectors and clusters, hardware modifications, etc. This volume is available for $10 in the US, Canada, and Mexico; and $12 in US funds for airmail delivery outside these regions. Membership with the 2nd volume is the same price as the 1st. There is also a special rate of 3 volumes (9 issues) for $25 in the US, Canada, and Mexico and $30 elsewhere.

Contact Cromemco User, Systems and Software Pool, POB 784, Palo Alto CA 94302.

Computer Graphics Letter Published by Harvard

Readers of the new *Harvard Newsletter on Computer Graphics* will be able to keep abreast of computer graphics in all its myriad ramifications. The newsletter monitors important commercial, technological, and product developments, as well as market, application, and learning opportunities. Among the regular departments are News and Trends, Products, Markets, Applications, R and D, Conferences and Seminars, Companies, Business and Financial, and State-of-the-Art Technology. The newsletter will be published twice a month.

The content will encompass management and statistical graphics, computer graphic-aided design, engineering and manufacturing, image processing, and automated cartography, plus other related areas. Trends in these areas, whether applied to big or small computers, standalone terminals, timesharing networks, users, vendors, will be followed. Readers will also learn where to obtain further information on the material covered.

The subscription fee for 1 year is $125; a 9-issue trial subscription is available for $45. Airmail outside of North America is $19.50 for 1 year or $9.75 for the trial. Contact William Nisen, Harvard University, Laboratory for Computer Graphics, 520 Gund Hall, Cambridge MA 02138.

Akron Ohio Digital Group

The Akron Digital Group meets on the 4th Wednesday of each month at 7 PM at the Kenmore Public Library, 2200 14th St SW, Akron OH. The club programs are aimed toward the small systems hobbyist with tips on programming and hardware application. Microprocessor classes are planned for the fall. Contact Lou Laurich, Akron Digital Group, 107 7th St NW, Barberton OH 44203.

TRS-80 Publication

Insiders: The TRS-80 Hardware Journal with Machine Software is a publication for any TRS-80 owner or user interested in more than BASIC. Both beginners and experts will find articles on machine language programming, hardware modifications, and other computer languages. Published since June of 1978, articles have described the differences in Level II read-only memories, how to get sound effects and music without a hardware modification, new languages for the TRS-80, and many other subjects. Regular features include a column which reviews various printers, the Disc File which covers the latest in DOS and compatible drives, a Dear Aunt TRiSh question and answer column, and learning machine language with Level II.

A new section of the journal will cover several of the new languages for the TRS-80. Future issues will include regular features on FORTRAN, FORTH, and other languages. Also, there will be regular articles on CP/M, reviews of various commercially available programs, and more on both Level II and DOS.

Subscriptions are available for 6 issues through Computer Cablevision, 2617 42nd St NW, Suite 2N, Washington DC 20007.

New PET Users Group Forming in Washington and Oregon

Individuals interested in forming a PET Users Group in the Oregon and Washington area should contact NW PET Users Group, c/o John F Jones, 2134 NE 45th Ave, Portland OR 97213.

COSMAC Users Group Active Again

After several unavoidable delays, the COSMAC Users Group is back in full operation and *The 1802 Peripheral* newsletter is being published on a monthly basis. Information about the group may be obtained by writing to Patrick Kelly, Director, COSMAC Users Group, POB 7162, Los Angeles CA 90022. Please include a stamp with your inquiry.

New Speechlab Users Group Formed

Heuristics Inc, manufacturer of Speechlab (a speech recognition unit for the Apple and all S-100 bus computers), has announced the formation of a users group. The users group requests that all interested Speechlab users send their unique uses of the hardware or software to Tom Larson, Director of Sales, Heuristics Inc, 900 N San Antonio Rd, Los Altos CA 94022. A directory of users and applications will be published at a later date.

Aim-65 Newsletter

The Target is a bimonthly newsletter for owners or prospective owners of Aim 65 systems. The subscription rate is $5 for 1 year. Contact Custom-Tronics, POB 4310, Flint MI 48504.

Solano TRS-80 Users Club

The Solano TRS-80 Users Club is an informal group that gets together to discuss mutual problems and experiences. Their meetings are held every 3rd Thursday starting July 5th at Owens-Illinois, 2500 Huntington Dr, Fairfield CA. Contact Dave or Steve Irwin, 550 Marigold Dr, Fairfield CA 94533, or call (707) 422-3347.

The Tulsa Computer Society

The Tulsa Computer Society meets the last Tuesday of every month at 7:30 PM. The meeting place is the Tulsa Vocational-Technical School seminar room at 3420 South Memorial Dr (behind Edison's Department Store). Membership in TCS is $6 annually and includes a 1 year subscription to the club's newsletter, *The I/O Port*. Contact The Tulsa Computer Society, POB 1133, Tulsa OK 74101.

Wichita Valley TRS-80 Users Group Sustains Computer Loss in Recent Tornado

In the recent tornado which wreaked unholy havoc on our city, many of us in the Wichita Valley TRS-80 Users Group lost our computers, our tape and disk library of software, and our library of computer books and periodicals. Even our club's library of software and publications was destroyed.

We all have plans to replace our personal computers and software, but at this time I am particularly interested in trying to help our club replace its loss.

Any club, publisher, software producer, or individual who wishes to do so, may contribute noncash items, such as software, back issues of computer publications, and books on computers.

Our address is the Wichita Valley TRS-80 Users Group, POB 4391, Wichita Falls TX 76308.

Thank-you, our club will be grateful.

J Wesley B Taylor
Club Secretary

Although this letter certainly speaks for itself, it is our sincere hope that you or your group will seriously consider contributing noncash computer related items to this needy organization.■

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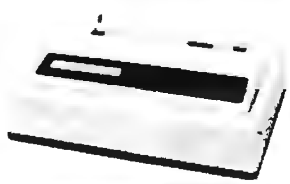

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The Nature of Robots

Part 4: Looking for Controlled Variables

William T Powers
1138 Whitfield Rd
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In this last part of my series of articles, a simple experiment with a human subject will be attempted; an experiment that can be expanded almost indefinitely. All of the principles from the previous parts will be used. Before the experiment starts, note the following main points that have been established:

- The behavior of an organism is not its output, but some consequence of its motor outputs acting together with unpredictable forces or other disturbances.
- For a more or less remote consequence of motor outputs to be repeatable in a disturbance-prone world, the behaving system must sense the consequence, and act to keep it matching some static or dynamic reference condition. By definition, that makes the organism a control system.
- Organisms acting as control systems control what they sense, not what they do.
- What is controlled is what is sensed, even when the sensing involves one or more stages of real-time computations based on primitive sensory signals.
- In a multiple-level control system, the higher levels act by varying the reference signals for lower-level systems. They control perceptions computed from many lower-level perceptions, some or all of which are controlled by the same lower-level systems.
- If there are *n* degrees of freedom at one level of control, in principle *n* higher-level systems could act independently and simultaneously by sharing the use of the lower-level systems. Any higher-level system acts by sending amplified copies of its error signal to many lower-level systems, each with the proper sign to achieve a negative feedback effect. Any lower-level system receives a reference signal that is the net effect of superimposed higher-level output signals. This worked for a 2-level system with 3 control systems at each level; there is no limit, in principle, to the number of levels or the number of systems at each level. In practice, there is reason to anticipate finding hundreds of systems at a given level, but no more than 10 or 12 distinct levels in a human being. This will be commented on later.

Abstract models and simulations are fine for conveying general ideas. However, if one does nothing but make models and simulations, it is easy to get involved in the math and engineering, and forget the real thing is there to be seen. Items described in the first 3 articles in this series represent something *real*. Real organisms work much the same way control systems work. They do not work in any of the other ways that have been proposed over the centuries (as far as their behavior is concerned). I am not talking metaphorically. There are excellent reasons to think that when the properties of organisms begin to be investigated in terms of control theory, hard data about the way we are organized will start to accumulate (up to a point, anyway).

The experiment to be described in this article is so simple that it may look elementary. Nevertheless, it is the starting point for a new approach to exploring the organization of human beings. Most new ideas start by looking like old ones, but with a twist that leads in unexpected directions. If you are familiar with tracking experiments, do not be too quick to decide what this is all about.

Equipment Required

The basic equipment needed to do this experiment is:

- *A joystick* with 1 degree of freedom (ie: a potentiometer with a stick on the shaft will suffice).
- *A reasonably fast analog-to-digital (A/D) converter* with 7-bit or more accuracy. My system uses the Cromemco D+7A, which has 7 analog channels in and 7 out, as well as 1 input and 1 output 8-bit port.
- *A memory-mapped display,* in which points are plotted on a video screen by depositing appropriate codes in a reserved segment of memory. This, or something equivalent, is essential for creating the moving objects that are involved in the experiment. I use the Polymorphics VTI with the display area in the 1 K bytes of memory starting at hexadecimal location D000. Out of deference to systems that do not have the VTI's graphics capability (however crude), I have used 64 horizontal elements in the alphabetic mode. Higher resolution would be much more desirable, but this much is enough to show the principles well.

If no memory-mapped display is available, but 2 digital-to-analog (D/A) outputs and a triggered oscilloscope are, the display that is needed can be created. Use 1 D/A

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converter to deflect the trace in the Y direction, and the other (or 1 bit of a digital port) to trigger the sweep. By starting the sweep and then outputting the 3 cursor values in sequence, a 3-segment trace can be created, with the motion of the cursors being up-and-down instead of side-to-side, as in the following program. Lay the oscilloscope on its side if that deviation bothers you.

Systems with built-in graphics under BASIC control, such as Apple, PET, or TRS-80, will probably allow the experiment to be done more simply than how I did it in listing 5. The basic requirement is to be able to read a number from a stored table, add the handle position to it, erase the old cursor, and use the sum to position the new cursor, doing this for 3 cursors at least 4 times per second - the faster the better. (An example of the simulation on the Apple II is shown in listing 6.)

Experimental Design

Imagine a display with 3 cursors on it, one above the other. Each cursor can move left and right. The subject looks at this display while holding a control handle. The instructions for the first experiment are very simple: the subject is asked to select *1* of the cursors, and hold it still, somewhere near the center of the screen as accurately as possible for the duration of the run. Engineering psychologists call this "compensatory tracking." They use it to investigate the limits of speed and accuracy of control in the presence of rapid disturbances of various kinds.

If the handle is held centered, each cursor will be seen to wander back and forth in a pattern that is independent of the other 2 cursors. In this experiment, the disturbances causing this wandering are made very slow and smooth. With even a slight amount of practice, every subject will be able to maintain essentially perfect control. Transfer functions will *not* be measured, nor will the limits of control be tested in the manner traditional in engineering psychology. A subject acting well within the range of normal operations under conditions where the phenomena of control can be clearly seen is desired. The subject selects a visual variable (position of 1 of the cursors), selects a reference level for that variable (a particular position), and maintains the perceived position at the reference position, while disturbances act that tend to move the cursor away from the reference position.

Figure 17 shows the setup in schematic form. The 3 disturbances are labeled D1, D2, and D3. The 3 cursor positions are labeled C1, C2, and C3. The position of the control handle is H. The position of each cursor is determined by the sum of H and one of the Ds. For cursor 2 the effect of the handle is reversed, so the 3 relationships are:

$$C1 = D1 + H$$
$$C2 = D2 - H$$
$$C3 = D3 + H$$

If the subject controls C3 in relation to a reference position of 0 (ie: midscreen), and does so perfectly, then $0 = D3+H$, or $H=-D3$. The handle position should be an accurate mirror image of the magnitude of the disturbance D3 at every moment, and the cursor C3 does not move at all. You will find that all subjects, after a little practice, will closely approximate these predictions.

This may seem elementary, obvious, boring and hardly worth the labor of getting the experiment up and running. Do not be deceived; this experiment appears to be simple because it is fundamental. It is fundamental because it can *prove* that all of the life sciences have been using the wrong model. There are also several extensions of the experiment that will show how to get started mapping the whole hierarchy of human control systems. There is no theory and no simulation that carries the impact of *seeing* how a real living control system works; especially when you can understand every detail of what is happening, either as subject or observer. The 3 previous articles in this series have been designed to give the ability to grasp what is happening here. This experiment is designed to give the gut feeling of *knowing*.

Program Structure

The program in listing 5 is written in North Star BASIC, Version 6, Release 3. It contains a machine-language subroutine for an 8080/Z80

Text continued on page 102

Figure, table, and listing numbering continued from part 3.

North Star Strings

The North Star BASIC string expression B$(I,J) corresponds to MID$ (B$,I,J) in other versions of BASIC. B$(I) corresponds to RIGHT$(B$,I), and B$(1,I) corresponds to LEFT$(B$,1,I).

Listing 5: North Star BASIC control-variable simulation. The necessary assembly language routines needed for execution are also given.

```
10 DIM H$(16),D1$(250),D2$(250),D3$(250),H1$(250),B$(82),S$(82)
20 DIM A$(2)
30 H$="0123456789ABCDEF"
40 INPUT "SEED FOR RANDOM GENERATOR (1 - 100) ",A\ Z=RND(A/100)
50 REM   ********************************
60 REM   CONVERT 2 HEX DIGITS TO DECIMAL
70 REM   ********************************
80 DEF FNB(A$)
90 U=ASC(A$(1,1))\IF U<58 THEN U=U-48 ELSE U=U-55
100 V=ASC(A$(2,2))\IF V<58 THEN V=V-48 ELSE V=V-55
110 RETURN 16*U+V
120 FNEND
```

```
130 REM   ************************************
140 REM   SET MACHINE-LANGUAGE PROGRAM ORIGIN
150 REM   ************************************
160 INPUT "MOST SIG. BYTE, SUBROUTINE LOCATION: ",S$
170 GOSUB 1130
180 !"6 SEC TO LOAD SUBROUTINE"
190 M1=256*A0\ M2=M1+9
200 DATA "02000000000000000004BDB19071F1F473A0800FE00C21C00782F"
210 DATA "3C477881E63F4F2A00003A08003C3CFE06DA2F00AF"
220 DATA "320800856F5E23563EA0127BE6C0B15F3EAA12722B73DB19EE80"
230 DATA "6F2600C9"
240 M=M1
250 READ B$\FOR J=1 TO LEN(B$)-1 STEP 2\ A=FNB(B$(J,J+1))
260 FILL M,A\ M=M+1\NEXT J\ IF A<>201 THEN 250
270 REM   ***********************
280 REM   INSERT RELOCATION BYTES
290 REM   ***********************
300 FILL M1+1,A0\ FILL M1+FNB("12"),A0
310 FILL M1+FNB("17"),A0\ FILL M1+FNB("23"),A0
320 FILL M1+FNB("2D"),A0
330 FILL M1+FNB("26"),A0\ FILL M1+FNB("31"),A0
340 REM   *************************
350 REM   SET LOCATIONS FOR DISPLAY
360 REM   *************************
370 INPUT "MOST SIG. BYTE,  DISPLAY   LOCATION: ",S$
380 GOSUB 1130
390 FILL M1+2,FNB("C0")\ FILL M1+3,A0\ FILL M1+5,A0+2
400 FILL M1+6,FNB("40")\ FILL M1+7,A0+3
410 REM   ***********************
420 REM   LOAD DISTURBANCE TABLES
430 REM   ***********************
440 W=3*3.1415927/250\R0=RND(0)\R1=32*R2=R1
450 !\!\!A!\!\        [ONE MINUTE TO LOAD DISTURBANCE TABLES]"
460 !\!"THE SCREEN WILL CLEAR AND THREE SCALES WILL APPEAR."
470 !\!"THEN THREE CURSORS WILL APPEAR, ONE FOR EACH SCALE."
480 !\!\PICK ONE CURSOR AND TRY TO HOLD IT IN ONE POSITION"
490 !\!"FOR THE DURATION OF THE RUN, AS EXACTLY AS YOU CAN."
500 !\!"                [STAND BY FOR PROMPT]"
510 N1=32\ N2=31\ N3=25\ N4=64\ N5=10
520 FOR J=1 TO 250
530 D1$(J,J)=CHR$(N1+N2*SIN(W*J))
540 D3$(J,J)=CHR$(64-ABS(J-125)/2)
550 NEXT J
560 !"     [LOADING RANDOM DISTURBANCE: STAND BY]"
570 N3=25\FOR J=1 TO 250
580 IF J-N3*INT(J/N3)=0 THEN R0=N4*RND(0)
590 R1=R1+(R0-R1)/N5\ R2=R2+(R1-R2)/N5\ D2$(J,J)=CHR$(R2)
600 NEXT J
610 INPUT"READY TO GO: HIT RETURN TO PROCEED. ",A$
620 FOR J=1 TO 16\!\NEXT
630 REM   ****************
640 REM   EXPERIMENTAL RUN
650 REM   ****************
660 !\!\!\GOSUB 680\!\!\!\!AGOSUB 680\!\!\!\!\GOSUB 680\!\!
670 GOTO 690
680 FOR I=1 TO 8\!"TTTTTTT+",\NEXT I\ RETURN
690 FILL M1+8,4\ REM            SYNCH CURSOR COUNTER
```

Listing 5 continued on next page

```
 700 N1=8\N2=127\N3=128\ FOR J=1 TO 250
 710 FOR L=1 TO 4
 720 OUT 25,N2\ OUT 26,N3
 730 H=CALL(M2,ASC(D1$(J,J)))
 740 H=CALL(M2,ASC(D2$(J,J)))
 750 H=CALL(M2,ASC(D3$(J,J)))
 760 NEXT L
 770 H1$(J,J)=CHR$(H)
 780 NEXT J
 790 REM   *********************
 800 REM   DATA PLOTTING PROGRAM
 810 REM   *********************
 820 GOSUB 1050\ IF YO<1 THEN 560
 830 !"AFTER PLOT, HIT RETURN TO CONTINUE"
 840 INPUT"WHICH CURSOR (1,2,3)? ",I
 850 IF I=0 THEN 560
 860 FOR W=1 TO 250 STEP INT(250/(YO+1))
 870 H=(ASC(H1$(W,W))-128)*XO/128
 880 ON I GOTO 890,900,910
 890 V=ASC(D1$(W,W))-32\ GOTO 920
 900 V=ASC(D2$(W,W))-32\ H=-H\ GOTO 920
 910 V=ASC(D3$(W,W))-32
 920 V=V*XO/64+1
 930 C=V+H+ZO\ IF C<1 THEN C=1\ IF C>XO THEN C=XO
 940 V=V+ZO\IF V<1 THEN V=1\ IF V>XO THEN V=XO
 950 H=H+ZO\ IF H<1 THEN H=1\ IF H>XO THEN H=XO
 960 B$=S$\B$(ZO,ZO)="."
 970 !#TO,\B$(V,V)="D"\ B$(H,H)="H"\ B$(C,C)="C"
 980 U=0\ IF V>U THEN U=V\IF H>U THEN U=H\IF C>U THEN U=C
 990 IF ZO>U THEN U=ZO\B$=B$(1,U)\ !#TO,B$,
1000 NEXT W
1010 INPUT1"",A$\ GOTO 820
1020 REM   *********************************
1030 REM   SET UP FOR PLOTTING (SUBROUTINE)
1040 REM   *********************************
1050 !\INPUT "Y-DIMENSION OF PLOT (0 = NEW RUN): ",YO\ YO=YO-2
1060 IF YO<1 THEN RETURN
1070 INPUT "X-DIMENSION OF PLOT (1-72): ",XO
1080 IF XO>72 THEN 1070\ IF XO<1 THEN 1070\XO=XO-2
1090 INPUT "OUTPUT DEVICE (T OR S)",A$
1100 IF A$="T" THEN TO=2 ELSE TO=0
1110 S$=""\FOR I=1 TO XO\S$=S$+" "\ NEXT I
1120 ZO=INT(XO/2)\ RETURN
1130 REM   ***********************************
1140 REM   CONVERT HEX IN S$ TO DECIMAL IN AO
1150 REM   ***********************************
1160 AO=0\K=1\FOR J=1 TO LEN(S$)-1\K=K*16\NEXT J\K=INT(K+.01)
1170 FOR I = 1 TO LEN(S$)
1180 FOR J=1 TO 16
1190 IF S$(I,I)=H$(J,J) THEN EXIT 1220
1200 NEXT J
1210 !"NOT HEX NUMBER"\ EXIT 160
1220 AO = AO + K*(J-1)\ K=K/16
1230 NEXT I
1240 RETURN
1250 REM   ********************************
1260 REM   UTILITY, CONVERT HEX TO DECIMAL
1270 REM    UP TO TEN HEXADECIMAL DIGITS
1280 REM          DO "RUN 1300"
```

```
1290 REM   ******************************
1300 DIM H$(16)\H$="0123456789ABCDEF"\!
1310 INPUT1"HEX= ",S$\GOSUB 1160\!"    DECIMAL= ",A0\GOTO 1310
```

```
                    *        MACHINE LANGUAGE SUPPORT ROUTINES
                    *
                             ORG    0
                    *
0000 0200           ADR0     DBL    ADR1
0002 0000           ADR1     DBL    0
0004 0000           ADR2     DBL    0
0006 0000           ADR3     DBL    0
0008 00             COUNT    DATA   0
0009 4B             START    MOV    C,E
000A DB19                    IN     25          GET HANDLE
000C 071F1F                  ARS                DIVIDE BY TWO
000F 47                      MOV    B,A         SAVE IN B
0010 3A0800                  LDA    COUNT       CHECK FOR MIDDLE ONE
0013 FE02                    CPI    2
0015 C21C00                  JNE    S1
0018 78                      MOV    A,B         IF MIDDLE ONE NEXT,
0019 2F                      CMA                MAKE HANDLE NEG.
001A 3C                      INR    A           (TWO'S COMPL.)
001B 47                      MOV    B,A
001C 78             S1       MOV    A,B
001D 81                      ADD    C           X=X+HANDLE
001E E63F                    ANI    :3F         LIMIT TO 63
0020 4F                      MOV    C,A         SAVE X IN C
0021 2A0000                  LHLD   ADR0        GET BASE ADDRESS
0024 3A0800                  LDA    COUNT       GET DISPLACEMENT
0027 3C                      INR    A
0028 3C                      INR    A           BUMP TWICE
0029 FE06                    CPI    6
002B DA2F00                  JLS    S2          CHECK MODULO 6
002E AF                      ZAR
002F 320800         S2       STA    COUNT
0032 85                      ADD    L           MAKE ADDRESS FOR
0033 6F                      MOV    L,A         CURRENT CURSOR.
0034 5E                      MOV    E,M
0035 23                      INX    H
0036 56                      MOV    D,M         DE=OLD SCREEN ADR.
0037 3EA0                    MVI    A,:A0       LOAD A SPACE
0039 12                      STAX   D           ERASE OLD CURSOR
003A 7B                      MOV    A,E
003B E6C0                    ANI    :C0         ZERO DISPLACEMENT
003D B1                      ORA    C           NEW DISPLACEMENT
003E 5F                      MOV    E,A         POINTER FIXED
003F 3EAA                    MVI    A,:AA       LOAD ASTERISK CURSOR
0041 12                      STAX   D           PUT IT ON SCREEN
0042 72                      MOV    M,D         SAVE CURSOR
0043 2B                      DCX    H           ADDRESS
0044 73                      MOV    M,E
0045 DB19                    IN     25          GET HANDLE AGAIN
0047 EE80                    XRI    :80         RANGE 0-255
0049 6F                      MOV    L,A
004A 2600                    MVI    H,0
004C C9                      RET
```

```
5     HIMEM: 8192
10    DIM D1%(250),D2%(250),D3%(250),H1%(250)
20    INPUT "SEED (0-100): ";A
30    Z = RND (A / 100)
40    REM  LOAD DISTURBANCE TABLES
50    W = 3 * 3.141592654 / 250
60    R0 = RND (0):R1 = R2 = 140
65    PRINT : PRINT : PRINT : PRINT : PRINT : PRINT : PRINT : PRINT
70    PRINT : PRINT : PRINT "LOADING DISTURBANCE TABLES"
75    PRINT
80    PRINT "WHEN SCREEN CLEARS, BACKROUND WILL"
85    PRINT
90    PRINT "APPEAR — THEN THREE CURSORS."
95    PRINT
100   PRINT "PICK ONE CURSOR AND HOLD IT IN"
105   PRINT
110   PRINT "ONE POSITION FOR THE DURATION OF"
115   PRINT
120   PRINT "RUN, AS ACCURATELY AS YOU CAN"
125   PRINT
130   PRINT "STAND BY FOR PROMPT MESSAGE"
140   FOR J = 1 TO 250
150   D1%(J) = 140 + 130 * SIN (W * J)
160   D3%(J) = (125 - ABS (J - 125)) * 270 / 125
170   NEXT J
175   PRINT
180   PRINT "RANDOM DISTURBANCE LOADING: STAND BYE."
185   N3 = 25:R1 = 140:R2 = 140
190   FOR J = 1 TO 250
200   N3 = N3 - 1: IF N3 > 0 THEN 210
205   N3 = 25:R0 = 280 * RND (5)
210   R1 = R1 + (R0 - R1) / 05:R2 = R2 + (R1 - R2) / 5
220   D2%(J) = R2
230   NEXT J
240   PRINT : INPUT "HIT RETURN FOR RUN";A$
250   HGR
255   HCOLOR= 3
260   POKE 49234, 0
261   FOR X = 1 TO 280 STEP 10
262   FOR Y = 43 to 143 STEP 50
263   HPLOT X,Y: HPLOT X,Y + 14
264   NEXT Y: NEXT X
270   FOR J = 1 TO 250
280   FOR K = 1 TO 4
290   H = PDL (0) - 128
299   HCOLOR= 0: HPLOT C1%, 45 TO C1%,55: HCOLOR= 3
300   C1% = D1%(J) + H
305   IF C1% < 0 THEN C1% = 0
306   IF C1% > 279 THEN C1% = 279
307   HPLOT C1%,45 TO C1%,55
309   HCOLOR= 0: HPLOT C2%,95 TO C2%,105: HCOLOR= 3
310   C2% = D2%(J) - H
315   IF C2% < 0 THEN C2% = 0
316   IF C2% > 279 THEN C2% = 279
317   HPLOT C2%,95 TO C2%,105
319   HCOLOR= 0: HPLOT C3%,145 TO C33%,155: HCOLOR= 3
320   C3% = D3%(J) + H
325   IF C3% < 0 THEN C% = 0
326   IF C3% > 279 THEN C3% = 279
327   HPLOT C3%,145 TO C3%,155
370   NEXT K
380   H1%(J) = H
390   NEXT J
400   HGR
405   POKE 49234, 0
410   FOR J = 1 TO 250
420   Y = 191 - J * 191 / 250
430   U = 88 / 280
435   H = INT (H1%(J) * U)
440   D1 = INT ((D1%(J) - 140) * U + 45)
450   D2 = INT ((D2%(J) - 140) * U + 135)
460   D3 = INT ((D3%(J) - 140) * U + 225)
461   C1 = D1 + H:C2 = D2 - H:C3 = D3 + H
462   IF C1 < 0 THEN C1 = 0
463   IF C3 > 278 THEN C3 = 278
480   HCOLOR= 1
490   HPLOT D1,Y: HPLOT D2,Y: HPLOT D3,Y
500   HCOLOR= 2
510   HPLOT C1,Y: HPLOT C2,Y: HPLOT C3,Y
520   HCOLOR= 3
530   HPLOT H + 45,Y: HPLOT - H + 135,Y: HPLOT H +225,Y
540   NEXT J
550   INPUT "";A$
560   TEXT
570   GOTO 180
```

Listing 6: A computer such as the Apple II which has high-resolution graphics capabilities greatly simplifies the program originally given in listing 5. This program performs the same operations as the simulation in listing 5. The author acknowledges the assistance of Charles Faso from Computerland of Niles IL in preparing this program.

Text continued from page 98:

processor which is loaded by the BASIC program at any specified 256-byte memory-address boundary (specify in hexadecimal only the most significant byte of the location of the subroutine).

The machine-language subroutine reads in the handle position, adds it with the appropriate sign to the value of a disturbance that is passed to the subroutine by the CALL command (in the DE register pair), erases the old cursor, and deposits the new cursor, a rubout, on the screen. Each time the subroutine is called it steps to the next cursor, recycling as necessary. On return from the subroutine, the handle position is passed back to the main program (in the HL registers). The machine-language program is in lines 200 thru 230, expressed as a string of hexadecimal bytes with no punctuation. Thus if your machine is not an 8080/Z80 type, a program can be assembled, the listing copied into these lines, and possibly this program can be made to work with little other modification.

The program asks for the most significant byte of the place where the machine-language subroutine is stored. The loader adjusts memory references by inserting the value of this byte in memory wherever necessary, after the program is loaded (lines 300 thru 330).

The display area consists of 1 K bytes of memory starting on any 256-byte boundary. Lines 370 thru 400 ask for the starting location of the memory area devoted to the display, and set up base registers in the machine-language program for the left margin of each cursor's movement. The FILL command is like POKE. If the computer has graphics capability built-in, everything from line 60 thru 400, and the plotting subroutine (later), can be accomplished in a simpler way.

Disturbance tables are set up in lines 510 thru 620. The unnecessary use of symbols, instead of constants,

Circle 322 on inquiry card.

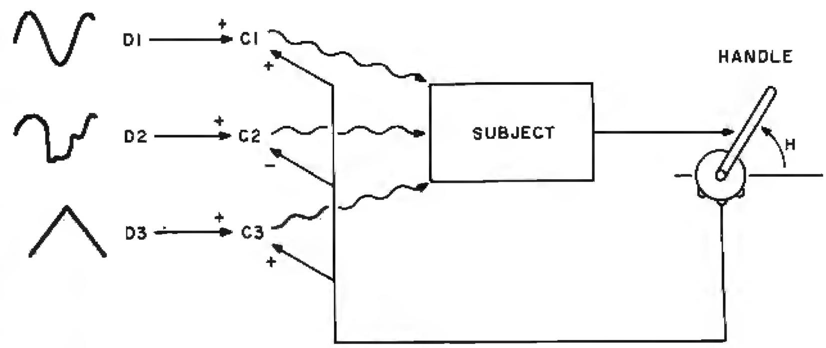


Figure 17: Schematic arrangement of experimental setup. Three slow and smooth disturbances are added to a measure of the handle position (with a negative sign for the middle one), to determine the position of 3 corresponding cursors. The subject selects 1 cursor and a reference position for it, and uses the handle to maintain the cursor at that position. A run lasts about 1 minute, and 250 samples of handle position are recorded. For plotting, the cursors are reconstructed from the tables of disturbances and the corresponding records of handle position.

is an attempt at acceleration. It still takes a minute to load the 3 disturbance tables, each 250 bytes long. All long tables are *strings*; only 8 bits of accuracy is needed, so by using the CHR$ and ASC functions, the tables can be stored 1 byte per value instead of 5 bytes per value. Disturbances are in tables because BASIC cannot calculate them fast enough.

Disturbance D1 is a sine wave and D3 is a triangular wave. D2 is a smoothed random disturbance. On reruns, only D2 is reloaded, taking about 20 seconds.

The experimental run is controlled by lines 660 thru 780. Lines 660 and 680 lay down 3 arbitrary scales on the screen, while the rest repeatedly call the machine-language subroutine. For each stored value of each disturbance, all 3 cursor positions are computed and plotted, and the handle position is stored in the table H1$. The inner loop from line 710 to line 770 adjusts the duration of the experimental run; here it is set up so that the disturbances change and a handle position is recorded only every fourth time the display is generated. On my system, this works out so the display is refreshed 16 times per second, and data is sampled and stored 4 times per second. The 2 OUT statements reflect my laziness; I use 2 digital-to-analog outputs to supply the voltage to the potentiometer that measures handle position.

The data plotting routine (lines 820 thru 1010) is entered at the end of an experimental run. This routine is set up to plot either on the video screen or on a hard-copy device; it asks for the X and Y dimensions of the plot, which cursor is to be plotted, and which device is to be used. My system is set up so the typewriter is device 2 and the screen is any other device number. If you do not have this ability in your BASIC or system, delete lines 1060 and 1070 (in the subroutine that requests information about the display), and eliminate the "#2," in lines 970 and 990. In North Star BASIC, the exclamation point is short for PRINT.

Only the handle position is stored as data; the cursor positions are reconstructed during plotting from the list of handle positions and the corresponding tables of disturbances.

The plotting scheme is designed to work with any teletypewriter-like device. If you have legitimate graphics, you can rewrite this part and get a more pleasing result.

There are 3 choices for plotting, each associated with cursors C1, C2, and C3. Each plot shows the cursor as a C, the handle position as an H, and the disturbance acting on the cursor as a D. A dot indicates the center of the display when nothing else is there. After each plot is finished, there is a pause; hitting the carriage return will cause the program to ask about the next plot. If the question about the Y dimension of the display is responded to with a 0, the program will reload the random disturbance table and issue a prompt for another experimental run. The old data will be destroyed. Remember, it takes about 20 seconds to reload the random disturbance table. Do not panic if

there is a long pause.

At line 1260 there is a utility routine that converts any hexadecimal number up to 10 digits to a decimal number. I used it while writing the program. It calls the conversion subroutine starting at line 1130.

Running the Experiments

If you possibly can, take the trouble to set this experiment up. Nothing can take the place of actually experiencing yourself as a control system and understanding things that you have taken for granted all your life.

Here is a typical run for the benefit of the many readers who do not have the equipment to do this; the data will then be observed. Here is an old friend, Chip Chad (from part 1 of this series), glaring at the screen and maintaining a choke-hold on the handle, waiting for the experimenter to hit the return key at line 610. The experimenter reaches in and taps the key. The reference scales slide up into place and the 3 cursors pop into view, moving. Chip picks the middle one as most people do the first time, decides to keep it on the middle + mark, and after a few wobbles succeeds.

'So what?" he says.

If learning were being studied, good information could be obtained from this first run. But the plan is to see Chip acting as a *competent* control system, so his first effort is praised and he is given another run (answering the query about Y dimension with a 0). After the second run, the data is plotted for each cursor.

Figure 18 shows the data for each cursor, number 1 on the left, 2 in the middle, and 3 on the right. The 2 end plots are a mess, but the middle plot shows a striking symmetry. The Cs march more or less down the center of the screen, deviating a little to left and right, but maintaining a constant position on the average. The Ds make a random-looking pattern, and the Hs follow almost the *mirror image* of the D pattern.

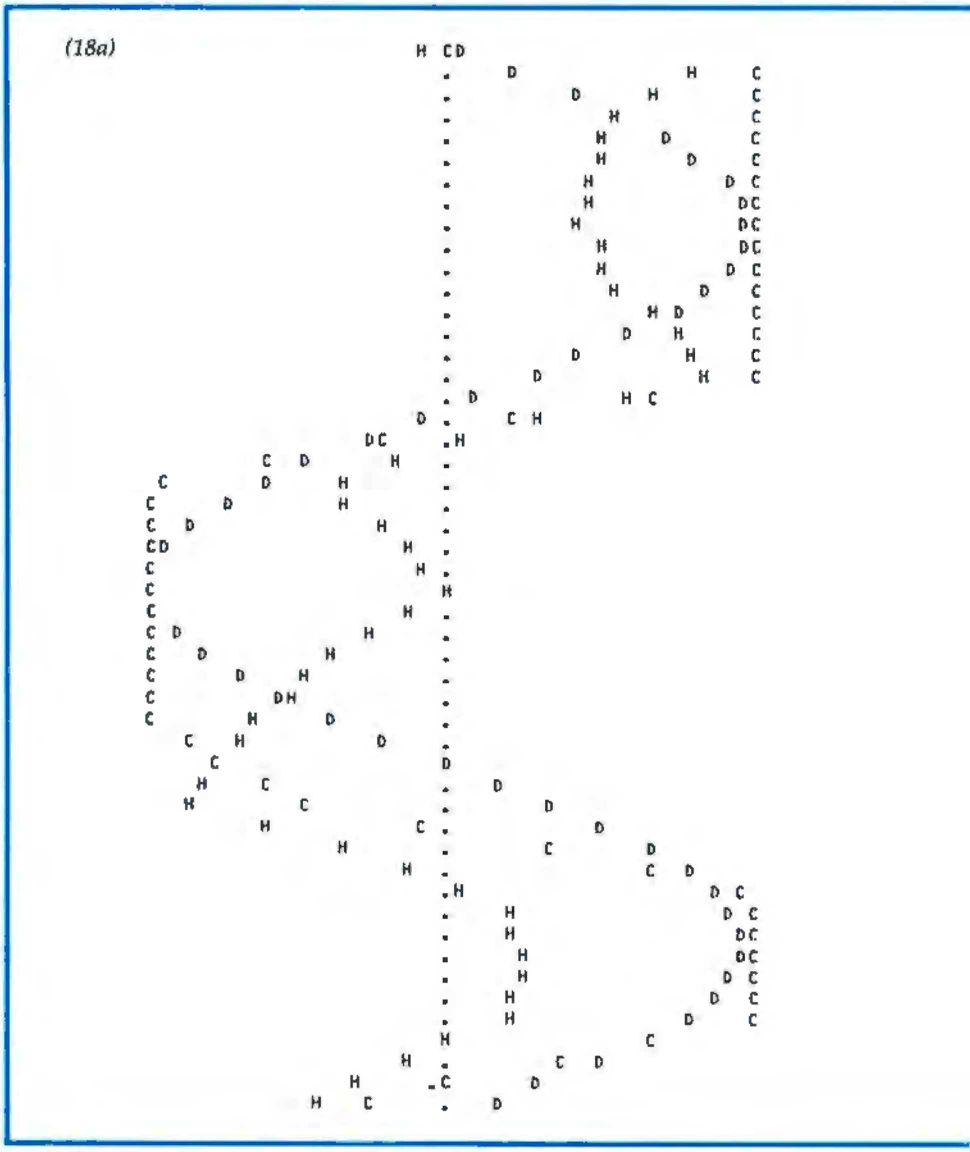
Looking carefully at the middle plot, could it be said that the handle position or motion looks like any sort of regular function of the cursor position or motion? There may be *some* relationship, but it certainly is not clear.Probably, nobody would claim that the large, smooth motions of the handle could be reconstructed *accurately* on the basis of measurements of cursor position (that is, reconstructed roughly or statistically with accuracy,especially if handle *acceleration* is compared with cursor deviation from the average position). The best which could be hoped for would be some statistical relationship (eg: a small signal buried in much noise).

On the other hand, the relationship between the handle position and the magnitude of the invisible disturbance is obvious and quantitative. It is seen that the handle position is the mirror image of the disturbance magnitude with an error of only a few percent of full scale. There is much signal and little noise in that relationship.

Here is the situation. There is 1 measure of Chip's behavior, H. There are 2 variables, D and C, either of which might have some relationship to that behavior. Which variable, D or C, would be selected by any statistical test as the most probable cause of the behavior? Of course, D would be selected. In fact, a formal statistical analysis, like those done in every scientific study of behavior, shows D to be the only significant contributor to the behavior, while C, the cursor position, is rejected as an irrelevant variable!

That is a paradox, however, from

Figure 18: A typical run for a practiced subject. In figure 18a is the record for D1, C1, and H. Figure 18b has the record for D2, C2, and H; figure 18c has the record for D3, C3, and H. In figure 18b, the cursor is held near the center, while the handle position is at all times very nearly the mirror image of the disturbance amplitude. It is very easy to decide which cursor was under control.



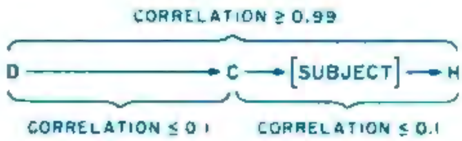


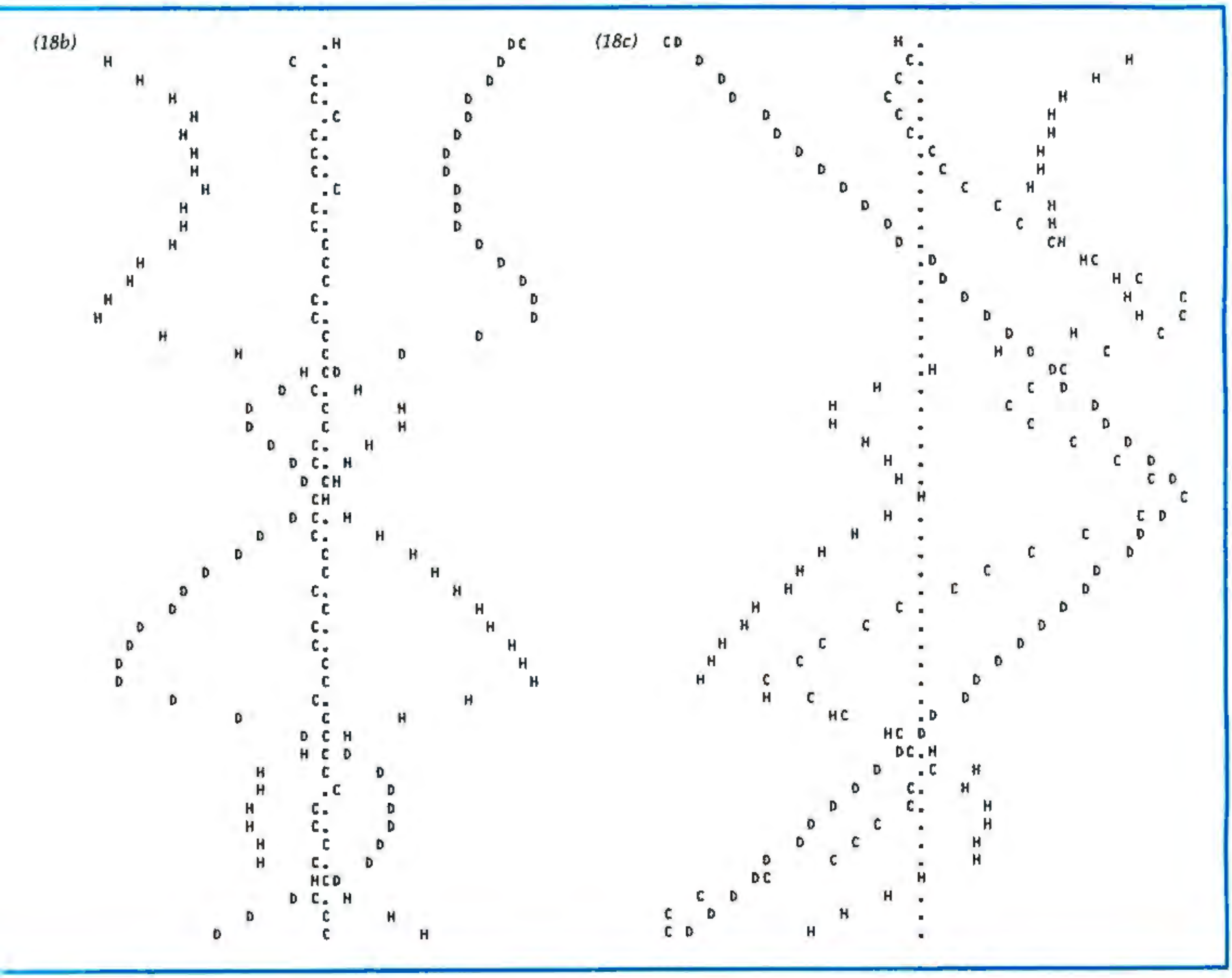
Figure 19: Cause and effect paradox. Under the old concept that stimuli cause behavior, the cause and effect chain runs from the disturbance to the cursor, through the subject, to the behavior. However, the correlation of the disturbance and the cursor position is very low, as is the correlation of the cursor position and handle position (for the controlled cursor). This would lead to a prediction of an even lower correlation of disturbance and behavior. In fact, that correlation is normally very high (0.99 or better). Only the control theory analysis of this experiment can explain this otherwise paradoxical situation.

the traditional point of view. The only way D can affect Chip's behavior is through its effects on C, since all that Chip can sense is the cursor position. The disturbance itself is invisible. If C does not correlate with the behavior, then how can anything that acts exclusively through *effects on* C correlate any better with behavior? Yet a typical correlation between C and H is around 0.1, while the correlation of H with the corresponding D is typically 0.995. See figure 19.

That is the proof mentioned earlier. The old cause-effect model fails utterly when applied to this situation. The question then is, why have generations of intelligent people believed that behavior *is* caused by sensory stimulation? The answer is clear: they have been fooled by a monstrous illusion.

The illusion would be easier to see if there was some visible, direct indication of the magnitude of the disturbance. Suppose there were a moving D (or a number that continually reflected the magnitude of D) on the display. Clearly, if Chip managed to control C without that indication, he could still do so; he could ignore it and perform as well as ever. However, something has now been added that would mislead a bystander who did not understand control theory.

That bystander could now see 2 variables, both able to affect Chip's senses. Taking the apparent relationships at face value, it would be clear that the indication of D was accur-



ately associated with the handle position; while the movements of the cursor, such as they are, show no such association. Furthermore, the variations of D are large and smooth, and there is no observable relationship between D and C. Why should the bystander suspect that C is being affected by D in one way and affected by H in an opposite way? The obvious conclusion is that the variations in D are causing Chip's behavior, while C has nothing to do with his behavior, especially if C does not vary more than the fixed background scales do. If the screen were full of irrelevant cursors, jiggling around slightly, how could the bystander pick C as something of special importance? If BASIC were fast enough, I would have included such irrelevant cursors; the point being made here would then be obvious.

An organism is surrounded by a world full of variables; variables that change within widely diverse ranges. The organism receives many signals from its internal parts, too. In that sort of situation, if the organism is controlling some of the variables, it will react strongly and smoothly to any disturbance tending to alter 1 of the controlled variables. The result is that it will *seem* to be responding directly to the disturbances. There will be no obvious indication that it is controlling anything at all. There is every excuse for even the best of scientists to have observed the relationship between disturbance and behavior, and to have missed the very existence of controlled variables.

The name for such disturbances is *stimuli*. Once in a while, an experimenter must have accidentally picked a real controlled variable to call a stimulus, but the chances are against that. If an attempt is made to manipulate a real controlled variable, the organism will have to be strapped down to keep it from interfering. That is what is done in such cases. If the organism insists on acting like a control system, forcibly break the loop and *make* the organism conform to the theory. As a famous psychologist said, the theme is "Behave, damn it!" It never occurs to such stong-willed individuals that they might have the wrong idea about what is happening.

There is more in this elementary experiment than meets the eye. If all psychologists were to experience it, and try to meet the challenge of explaining these effects using any standard theory, the result would be a total collapse of that science, followed by a rebirth. However, many jobs would be threatened. What has happened instead is that a handful of psychologists has supported this theory, another handful has taken up arms against it, and most have resolutely ignored it.

I suggest that you run this experiment many times with subjects controlling all 3 cursors. Every case will show that mirror-image relationship between D and H and little relationship between C and either D or H. If the previous parts of this series are studied and all the relationships that make up a control system thought about carefully, it will be evident that there is no other explanation for what is going on here. If you get nothing else out of this, you should acquire an intuitive feel for a new theory of how behavior works. You might even begin to understand how to design a robot in a new way.

It is time now to try to fulfill a promise implied in part 1, to show how anyone with a home computing system can make important contributions to this new science of human nature.The best way this can be done is to start with the experiment used, and to show how it can be extended to become a powerful tool for investigating human organization. The main objective will be to introduce the *test for the controlled variable*, the nearest approach I know of to mind reading.

More Controlled Variables

Once subjects controlling all 3 cursors have been seen, it might seem that the possibilities of this experiment have been exhausted; this is not the case at all. There are controllable variables all over that screen; all of them can be controlled by the same means, movements of the handle in 1 dimension. Discovering them is a good way to get out of the habit of thinking that we simply perceive our environment, and start a new way of thinking: to recognize that we *construct* perceptions, imposing order on our experiences far more than *recognizing* order. As you will see, a controlled variable does not have to be "real" at all.

Here is an example. It is possible to perceive the *relative* position of any of the 2 cursors. The handle affects C2 in a direction opposite to its effects on C1 and C3, so the relative position of C1 and C3 cannot be controlled because the handle does not affect it. However, it is possible to keep C1 even with C2, or C2 even with C3; in fact, it is easy. A plot of the results would involve plotting C2-C1 or C3-C2 instead of just C, and D2-D1 or D3-D2 instead of just 1 disturbance. The mirror image relationship with H would be as good as ever. Do not forget that C2-C1 and C3-C2 are *variables*. Any value of the variables can be selected as a reference level (eg: C1 to be 1 inch to the left of C2).

These are examples of *higher-level* controlled variables. If the subject could not perceive the present positions of the cursors, he or she certainly could not perceive their *relative* positions. Relative position is derived from perceptions of individual positions, but not vice versa. In order to *control* relative positions, it is necessary to control (or at least vary) individual positions, but individual positions can be controlled without controlling relative positions. These are the relationships one looks for to map out a *hierarchy* of perception and control.

Other relative perceptions can be controlled. All 3 cursors can be kept lying in a straight line, at least within the range where 1 of them does not fall off the edge of the display and pop up at the other edge. Reducing the amplitude of the disturbances would eliminate that problem. Also, the 3 cursors can be made to form any fixed angle, subject to the same limitation. There may be more static patterns that can be controlled, but I have not thought of any. This is, after all, a simple display.

It is not, however, limited to static conditions. Suppose the subject visualizes a pattern in which 1 cursor moves back and forth slowly between 2 limits. This pattern can easily be maintained, the handle moving just enough to produce it, and enough more to cancel the effects of any of the disturbances. A similar oscillation could be maintained for the *relative* variables. This is a still higher-level variable, a temporal pattern. The subject chooses which temporal pattern to perceive, and what state of that kind of pattern to maintain. Control still requires only the use of the 1-dimensional effect caused by the handle.

There is clearly an infinite range of different temporal patterns, ranging from a simple steady motion in 1 direction to completely arbitrary motions and rhythms. There is an *unlimited* number of potential controlled variables in this simple display. Anything that can be perceived, and that the handle can affect in a systematic way, can be controlled.

For all of these examples of controllable perceptions, it is essential to remember that the disturbances are acting all the time. This is not a matter of producing any particular *behavior*. The cursor cannot be made to move slowly back and forth between fixed limits just by moving the handle slowly back and forth between fixed limits. The handle might be moving the wrong way at many moments, when the disturbance tends to make the cursor move faster than the reference pattern being considered. There is no one-to-one correspondence between handle position or velocity and cursor position and velocity, because of those ever-present disturbances. Regularities of *behavior* are not being looked at here, but regularities of controlled perceptions. If there were a slowly oscillating prism between the display and the subject's eyes, a regular pattern of movement of the cursor on the screen would not be seen. The subject controls the visual image, not the reality. For the higher-level variables, the subject controls some *function of* the visual image (often the controlled variable could not be found, even on the retinas).

One could create displays of far greater complexity, and provide means of affecting the display that have more than 1 degree of freedom to explore a staggering range of possible controlled variables. This is what I suggest be done. The first step in the development of any new science is acquire the facts; here the most needed facts concern *what variables human beings can actually control*. What is needed is a large and simpleminded program of recording the obvious and obscure. What is needed is a body of definitions of variables in *every* sensory mode that people have been able to control. Order and system count much less than sheer volume of data at this point. In fact, an *unsystematic* gathering of data may be the best kind, since it will not be constrained by theories about what people *ought* to be able to control. Anything which can be a way of testing is worth testing at this stage. The possibilities are limited only by the imagination.

We do need some sort of ordering principle—some criterion for judging the reality of any proposed controlled variable. This is where the test appears; here is how it works.

Test for Controlled Variables

The first thing to remember when investigating a possible controlled variable is that in order for something to be controllable it has to be variable. There is neither the means nor the need to control the existence of the Empire State Building or the planet Jupiter. Not all perceptions are controlled. Some are just disturbances; some are just there.

One might think initially about controlling, for instance, a car. People often speak casually about controlling *things*. But what is meant is controlling *something about* those things. A person cannot really control a car; but under proper circumstances its shape, its color, its price, its speed, its direction, its parking place, its dirtiness, its dangerousness, its desirability, its altitude, or the flatness of its tires can be controlled. A car, after close inspection, proves to be composed entirely of hundreds or even thousands of variables. Together they create "car-ness" in our perceptions. Individually, or in groups, most of them can be affected by one means or another, and can be controlled if it is worth the effort. You can even make the car disappear instantly by closing your eyes. Keep remembering that what is controlled is really a *perception*.

The first step in applying the test for the controlled variable is to define a variable. You do not have to know in advance if it is a controlled

Circle 305 on inquiry card.

variable; you do not even have to know where the supposed control system is. All you have to do is to pick out something that you know is variable and "push" on it.

By push I mean to apply a disturbance that under normal circumstances should have a predictable direction and amount of effect on the variable. If I push hard enough on a life-sized statue, it should tilt in the direction of the push. Perhaps it will topple in that direction according to the simple laws of mechanics.

Having selected a variable and applied a push to it, the next step is to measure the actual effect of the push. I *predict* that pushing on this statue should make it tilt a certain amount in a certain direction. I apply the push and observe the tilt.

If the *actual* effect is far smaller than the *predicted* effect, common sense indicates that something must be pushing back. If the pushing-back is always just enough to cancel any amount or direction of disturbance (within some limits), it can be concluded that the pushing-back is *systematic*. The mirror-image effect that has been observed is what is wanted.

It is necessary to discover *what* is pushing back, and how it is doing the pushing. Perhaps, examining the statue carefully, an iron rod is found supporting its back from its base. In that case, a conclusion is made that there were not enough facts to make a correct prediction of the effects of the push; the bending moment of the rod should have been taken into account. But if no simple explanation for the failure of the prediction is found, one must look further.

Suppose it is discovered that the base of the statue seems to move when pushed. If there is a push to the east, the base tilts to the west moving the center of support east of the center of gravity of the statue, and thus creating a counterforce. Suppose this tilt of the base is found to be always just what is required to offset the effects of the push. It can be concluded that one may be on the trail of a control system.

What has been done is to find out something about the *means* of control, the path by which the output of the control system, if it exists, might be linked to the controlled variable (the angle between the statue's longitudinal centerline and the vertical). Finding this link is a necessary step in the test.

That step will usually lead to discovering the physical control system. Tracing the wires that work the motors that tilt the base of the statue, you find a black box a few yards away from the statue. That may be the control system, or at least all of it that is not its actuators (which have been found).

There is still one step to be taken. You cannot be completely sure of the nature of the control system until you discover the variable it is really sensing. The situation has been approached with human prejudices; to me, it seems that the controlled variable is the orientation of the statue, a geometric or visual variable. Perhaps that variable is only *related* to the real controlled variable. What must be found now are the *sensors* that the control system is using.

Thinking in visual terms, you might look for a photocell that detects the tilt. Suppose a photocell is found on a stand near the statue. The test calls for breaking this link, preventing the sensing of the statue. The result should be that the effect of the push returns to what would be predicted from mechanical laws. So the photocell is covered and the disturbances are applied again. What happens is that the floodlights illuminating the statue turn on. The statue still resists the push—the photocell was for something else.

By careful searching 4 strain gauges built into the base of the statue are discovered. These provide a signal showing where the center of thrust is, and the wires from the strain gauges run over to that black box. Disconnecting the wires shows that *now* the push succeeds in tilting the statue. As soon as its tilt becomes marked, an angry groundskeeper comes leaping out of the bushes and arrests the experimenter. Aha! You may have discovered *another* control system controlling the state of the statue.

To recapitulate, the test for the controlled variable involves the following steps:

1. Define a variable.
2. Apply various amounts and directions of disturbances directly to the variable.
3. Predict the expected effects of the disturbances, assuming no control system is acting.
4. Measure the actual effect of the disturbances.
5. If the actual effect is essentially the same as the predicted effect, stop. No control system is found.
6. If the actual effect is markedly smaller than the predicted effect, look for the cause of the opposition to the disturbance, and determine that it results from systematic variations in some other variable. If such a cause is found, it may be associated with the output of a control system.
7. Look for a means of *sensing* the controlled variable. If none is found, stop: no control system is proven to exist.
8. If a means of sensing is found, block it, so the variable cannot be sensed. If control is *not* lost, the sensor is not the right one. If no such sensor is found, stop: no control system is proven to exist.
9. If all steps of the test are passed, the variable is a controlled variable, its state is its reference level, and the control system has been identified.

To apply step 8 of the test to our computer experiment, cover the cursor suspected of being controlled with a cardboard strip. Control should be lost. Cover *each* cursor. The covered one will never pass the test. The other steps are easily carried out.

Concluding Remarks

Now it is up to you. You can test controlled variables involving intensity, sensation, configuration, change, sequence, relationship, strategy, principle, and system concepts having to do with visual, auditory, tactile, kinesthetic, and other senses.

Good luck with the programs, and good hunting for controlled variables. I will be interested to receive word about what people are doing with the information covered in these articles. ■

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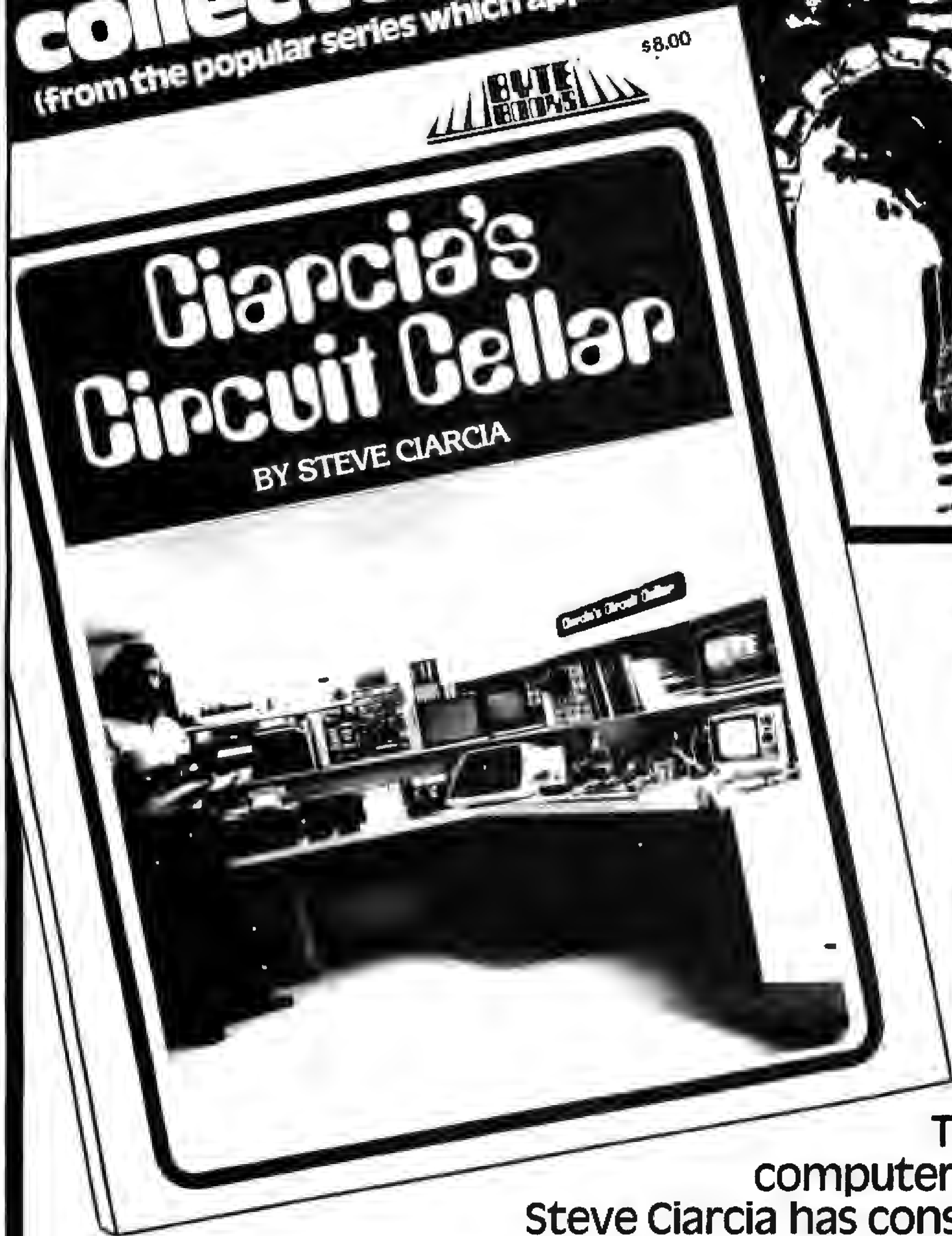

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BYTE News . . . .

S-100 8086 AND Z8000 CARDS COMING: At least 6 S-100 product manufacturers are about to release 16-bit processor cards for the S-100 bus that use the Intel 8086 and Zilog Z8000. One such card has already been announced, a 8086 processor card from Seattle Computer Products Inc, Seattle WA. All will conform to the Institute of Electrical and Electronic Engineers (IEEE) S-100 standard that is soon to be adopted. They will work with most 8-bit memory cards using byte-serial read/write. However, for full speed operation you will need either a true 16-bit memory card or a modification of your present memory cards. To modify memory cards requires cutting traces, some rewiring, and adding some logic circuitry.

Microsoft has already announced and demonstrated an 8086 BASIC, and is working on a Z8000 BASIC, as well as other 16-bit software. Digital Research is working on a 8086 version of CP/M. Most 16-bit software in development will be designed for multiprocessing environments, using real-time clocks and interrupt-driven user-inputs.

CP/M 2.0 TO BE RELEASED SOON: There is no doubt that the most widely used disk operating system for microcomputer is CP/M, developed by Gary Kildall of Digital Research, back in 1974. Although originally written for the Intel 8080 development system, it was adapted to run on 8080, 8085 and Z80 systems of many types. Its power and flexibility puts microcomputers in the big leagues by providing features and capabilities normally found on the bigger models.

Gary Kildall is planning to release the 1st major revision to CP/M (Version 2.0). It will use a real-time clock and be interrupt-driven. It will support all present CP/M software. Look for its release around September 1st.

RANDOM RUMORS: Matsushita Inc is rumored to be working on a $250 printer which will generate "letter quality" type. It will print at 15 characters per second and include a keyboard. Rumors about Hewlett-Packard's Personal Computer are getting warmer. It may be introduced in time for the Christmas market. Expected to sell in the $2500 area, it will have a 5-inch black and white monitor, 16 K bytes of programmable memory, BASIC in read-only memory, a built-in thermal printer and cassette I/O (input/output). Texas Instruments is developing a 3 or 4-inch Winchester-type disk drive to sell for approximately $50. Shugart is about to start delivery on the $70 5-inch floppy disk drive made by Matsushita. Infoton, a video terminal manufacturer, is rumored to be about to introduce a video terminal which will sell for less than $400 in large quantities. It will use the Zilog Z8 microprocessor and have a total of only 16 integrated circuits. All circuitry will be on 1 printed circuit card, the power supply will be transformerless, and a special elastomeric keyboard will be used.

HAND-HELD COMPUTER IN DEVELOPMENT: Matsushita Electrical of Japan and Friends-Amis Inc of CA have agreed to develop and produce "the first practical hand-held personal computer." The size of a hand-held language translator, the unit could be in production by the end of the year. The computer will be able to accept preprogrammed and user programmed memory capsules. Preprogrammed capsules will include information on business, science, language, education, etc. The computer will have modular construction, enabling new technology modules to be added as they are introduced. Add-ons will include a miniprinter, miniature video display, and a voice synthesizer.

MICRO-MOUSE CONTEST FINALLY ENDS: The 2 year long "Amazing Micro-Mouse Contest" run by the IEEE has finally ended. Although several thousand entries were received, less than 100 actually ran the maze. The contest's objective was to design a robot-type device which could negotiate and learn a maze as it went through. The trials were held at conventions of the IEEE, NCC shows and PC-78.

The ultimate winner was entered by the team of Howard P Katseff and Roy Tramwell from Bell Labs, Holmdel NJ. Their mouse ran the 8½ by 8½-foot maze in just under 30 seconds. It employed a Z80 microprocessor with 4 K bytes of read-only memory and 1 K bytes of programmable memory. Second prize was taken by the team from Batelle Memorial Institute of Richland WA. Art Boland, Ron Dilbeck and Phil Stover's mouse ran the maze in just over 31 seconds. One high performer was actually nonprocessor controlled, and ran the maze in just under 40 seconds.

VOICE-OPERATED TV DEMONSTRATED: Sanyo Electric Co recently demonstrated a television receiver that responds to voice commands to turn on and off and switch stations. Utilizing a microprocessor, the unit compares the voice input to voice patterns stored in memory. The unit has a 30-word vocabulary, and can respond to the voices from 2 different people. Furthermore, the voice input can be used to play games. Sanyo has not announced any immediate plans for incorporating the receiver into its television sets.

APL FOR MICROCOMPUTERS: Despite a report in an earlier BYTE NEWS column, Quark has decided against introducing its APL microcomputer using the Intel 8086 microprocessor.

JAPANESE MOVING SWIFTLY INTO MICROCOMPUTERS: At least 9 Japanese manufacturers are presently manufacturing microprocessor integrated circuits. Approximately 80 different microprocessors are being made. Most of them are original designs including advanced features (eg: analog-to-digital converters, multiply/divide, counter/timers, etc). Five different 16-bit microprocessors are already in production. Furthermore, over a dozen personal computers/trainers are in production to support a very strong interest in personal computers in Japan. Thus far only a few units are available for export.

MOTOROLA ANNOUNCES 68000 DELIVERY AND PRICES: Motorola has announced that it expects to start shipping limited sample quantities of its new 68000 16-bit microprocessor by the end of the year. Single unit price will be $249. Limited production quantities are expected to be available by the end of the 1st quarter of 1980, with full production by late 1980. No second source arrangements have been finalized.

75 MEGABYTE WINCHESTER DRIVE RUMORED: At least 6 companies exhibited 8-inch Winchester-type drives at the recent NCC show. All of the drives could fit into the same space as an 8-inch floppy disk drive, and provided from 10 to 45 M bytes of storage. At least 8 companies will be delivering these drives by the end of the year, and a 75 M byte version is expected next year. The drive should sell for under $2000 in quantity.

PERSONAL COMPUTER MANUFACTURERS RANK WITH COMMERCIAL DATA PROCESSORS: Datamation magazine, in their most recent annual report of the top 50 US companies in the data processor industry, disclosed some interesting facts about changes in the computer industry. For the 1st time a personal computer manufacturer, Tandy, ranked among the top 50 in computer equipment sales, and Commodore ranked second among fastest growing companies. Commodore had a 190% increase in sales in 1 year, to $75M. Tandy(ranked 43rd)reported computer sales of $105M and total company sales of $1,152M resulting in a net income of $76M. The company reported a sales gain of only 11.6% (which is about equal to the rate of inflation, and hence could be considered 0 sales growth). If Commodore continues to grow at its past year's pace, it too will soon rank among the top 50. It was reported that 63% of Tandy's computer revenues were from TRS-80 sales, 26% from peripherals, 10% from services and 1% from supplies.

Each data processing company in the top 50 reported sales increases, and most were 20% or better. For example, IBM's sales rose almost 28%, while Digital Equipment Corporation's sales rose nearly 36%. In fact, none of the traditional maxi or mini makers appear to have been affected by personal computers, despite the predictions that were made 2 and 3 years ago.

MAIL: I receive a large number of letters each month, as a result of this column. If you write to me and wish a response, please include a stamped self-addressed envelope.

Sol Libes
ACGNJ
1776 Raritan Rd
Scotch Plains NJ 07076

Inexpensive Optical Paper-Tape Reader

Brian A Harron
67-3691 Albion Rd
Ottawa, Ontario
CANADA K1T 1P2

1 microprocessor + 8K BASIC tape +4K Startrek tape +45 min=RUN

This was the terrible equation I had to contend with every time I wanted to play my favorite game program. It would take me 30 minutes to load the 8 K BASIC paper tape. But not any more!

The solution is a 400 character per second paper-tape reader that can interface to any 8-bit input port of almost any microprocessor. It uses only 2 integrated circuits and costs approximately $15.

I had always wanted something faster than my old reliable Teletype, but I never seemed to have the $40 to $100 that was needed to buy one of the many available kits. I also wondered why most of these kits required so many integrated circuits to accomplish the simple task of latching 8 bits of data. There are 7 bits (sometimes 8 bits) of parallel paper-tape data spaced at regular intervals, and a sprocket hole for strobing, included at no extra cost. Why not design a self-strobing, 8-bit data latch using an inexpensive large scale integration (LSI) transistor-transistor logic (TTL) integrated circuit, the INTEL 8212?

The Intel 8212 provides 8 bits of input, 8 bits of output, strobe, clear, and several device enable lines for about $5. All I needed to do was to optically sense the punched paper-tape holes and strobe them into the latch at every sprocket hole.

Although there are several ready-made, 8-level, paper-tape-reader photodiode assemblies available, I decided to construct my own reader assembly using individual phototransistors that I already possessed, the Motorola type MRD150, which are available at most wholesalers for approximately $1 each. Their miniature size is ideally suited to 0.1 inch (0.25 cm) spacing.

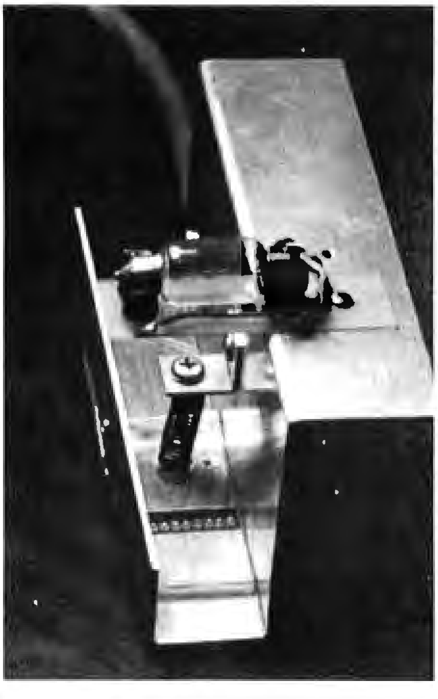


Photo 1: View of the paper-tape reader showing the light source and the light-detecting phototransistors. The spring and clamp device keeps the paper tape in place.

Using epoxy, I glued 9 of the phototransistors into a 0.5 by 1 inch (1.27 by 2.54 cm) piece of 0.100 inch (.025 cm) perforated board The photocell placed between positions 3 and 4 (as shown in figure 1) is physically reversed so that the active surface element of the cell is not in line with the other 8 cells. This out-of-line detector provides a physical delay of the sprocket-hole signal which will be signal-conditioned later.

This cell begins to detect light through the sprocket hole only after all other data holes are fully centered over their respective detectors. The strobe pulse is now positioned close to the center of the pulse from the data holes, as shown in the waveforms of figure 2.

In order to make the strobe pulse as insensitive as possible to the variation in tape speed caused by moving the tape by hand, the sprocket-hole detector is amplified by transistor Q1 and is threshold-detected by IC1a, a 7414 hex Schmitt trigger TTL gate (see figure 3, p. 121). The output of IC1a is then differentiated and level-shifted by the capacitor and resistor combination C1, R1, and R2 such that the output of IC1b is fast and clean even for very slow dark-to-light transitions through the sprocket hole.

The additional gate sections IC1c and IC1d provide buffered outputs of

Circle 355 on inquiry card.

the signals STROBE and $\overline{\text{STROBE}}$, which will be used as sense input lines to the 8-bit interface port.

The last 2 sections of the Schmitt trigger are configured as a delayed power-up signal that holds the CLEAR input pin of the latch at ground until the power supply voltage has stabilized.

The $\overline{\text{DS1}}$ and MD pins of the 8212 are grounded and the DS2 pin is pinned to the supply voltage, thus placing the 8212 into the strobed latch mode of operation. In this way the 8 bits of data available to the input pins DI-0 thru DI-7 are latched through to the output pins DO-0 thru DO-7 by each positive pulse at the STROBE pin.

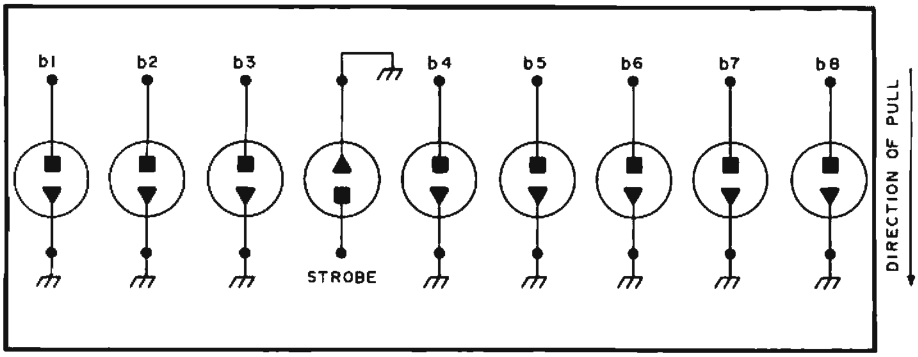


Figure 1: Phototransistors in the paper-tape reader. Note the placement of cell between bits 3 and 4. The active element is reversed in orientation.

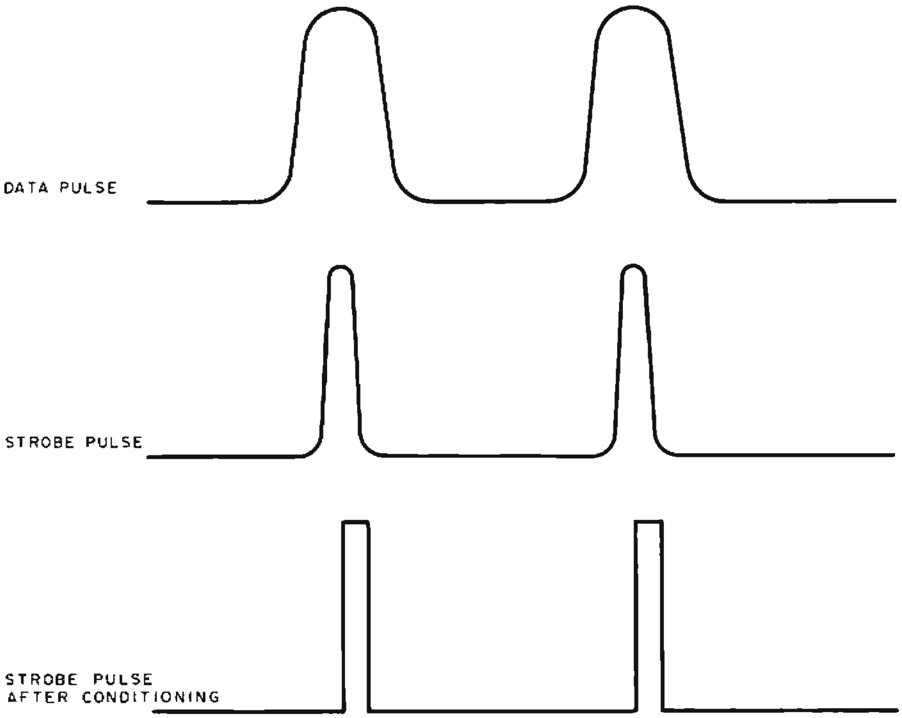


Figure 2: The strobe pulse is centered in the active signal from the data holes.

```
UP:     IN   port#      ; READ INPUT PORT
        RAL             ; SHIFT 1 BIT LEFT
        JNC UP          ; JUMP TO UP IF CARRY BIT NOT SET
DOWN:   IN   port #     ; READ INPUT PORT AGAIN
        RAL             ; SHIFT 1 BIT LEFT
        JC   DOWN       ; JUMP TO DOWN IF CARRY BIT SET
READ:   IN   port#      ; READ INPUT PORT DATA BYTE
        RETURN          ; WITH 7 BITS OF DATA IN REG A
```

Listing 1: Simple 8080 assembly language program for inputting the data from the paper-tape reader.

Since most paper-tape programs used with today's microprocessors use only 7 bits of the 8-bit ASCII code (bit 8 being vertical parity), it is convenient to use this 8th bit as the strobe sense line. When connecting the output pins of the latch to the processor input port, simply select strobe signal STROBE or $\overline{\text{STROBE}}$ and connect it to the pin corresponding to bit 8.

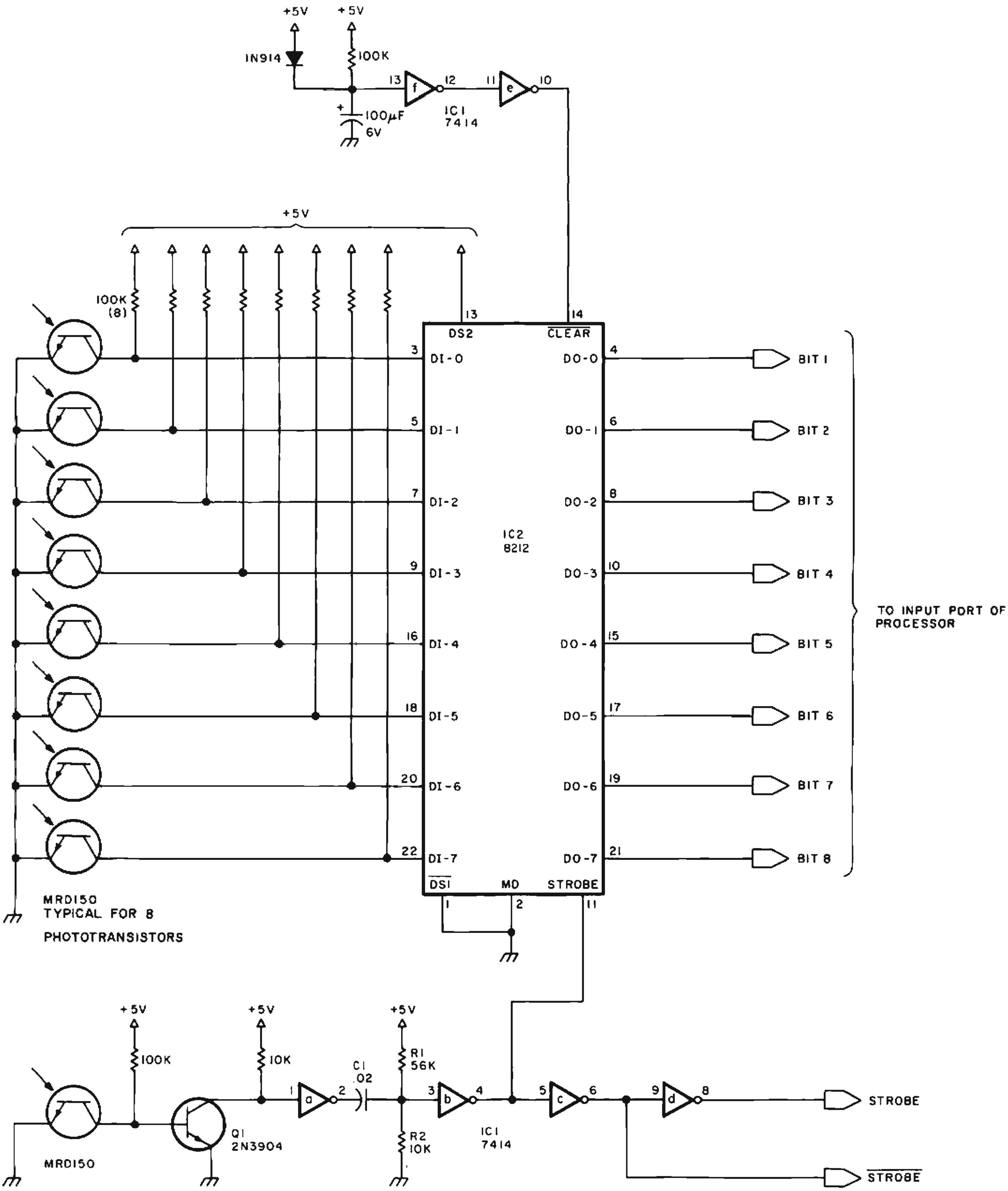
The software required to read in such data is shown in listing 1, where bit 8 is the STROBE sense line. When bit 8 goes through a low to high to low cycle, the data at the input port is valid.

If 8 bits of tape data are required, it is necessary to connect the strobe sense line to either another input port pin or to some other monitor line, such as an interrupt or serial input line, which can be tested under software control.

Mechanically, I used a piece of 0.100 inch (0.025 cm) aluminum sheet bent into a U-shape, with an inside, bottom width dimension of 1 inch (2.54 cm). I used a small piece of clear Plexiglas as a hold-down device for the tape as it passed over the reader photocells. Further improvements can be added, such as a motor-driven, pinch-roller pull-through, but I have had no problems when pulling the tape through by hand. As a matter of fact, I can stop pulling at any time, since the strobe pulse is speed insensitive. I plan to eventually add a hand crank and a take-up reel to avoid the great piles of tape that end up on the floor after loading some of my larger programs.

To generate the required illumination, I used an automotive lamp (type 211) mounted 3 inches (7.5 cm) above the photocells. Running the lamp on 5 V provides a good, uniform source of light, although it draws about 1 A of current.

This entire project took only 3 evenings to design and construct, and the $15 price tag was a bonus. If you are still limited to 10 characters per second with your Teletype reader, you should seriously consider this high-speed paper-tape reader.■



IC	TYPE	+5V	GND
2	8212	24	12
1	7414	14	7

Figure 3: Schematic diagram of the paper-tape reader, which is capable of 400 characters per second.

Book Reviews

Microcomputer-Based Design

by John B Peatman
McGraw-Hill Book Co,
New York 1977
540 pages hardcover
$26.95

Microcomputer-Based Design by John B Peatman is a combination text and reference book aimed at engineers who wish to learn how to design systems using microprocessors. It is written not in a dull, dry tone, but rather in a light style. The minimum required background for this text is a rudimentary knowledge of logic (ie: transistor-transistor logic gates and flip-flops) and the basic concepts of computer programming. The book develops hardware and software design skills upward from that point to a practical and useful level. A key feature of this book is the logical, lucid presentation of arguments present in the many illustrated design decisions.

Microcomputer-Based Design is divided into 7 chapters and 6 appendices. The chapters are fairly complete, in-depth entities and each contains a set of practical design problems and additional references. The references may be difficult to find for readers without access to an engineering library since many of the references are articles in engineering journals or manufacturers' application notes.

Chapter 1 is an overview of microcomputer applications focusing primarily on the distribution of "intelligence" to instruments and tools.

Chapter 2, "Microcomputer Registers and Data Manipulation," includes a brief discussion of numbering systems and the various, commonly encountered modes of addressing. This is followed by a good presentation of machine language instructions, assembly language, and assembly language programming techniques.

Chapter 3 considers computer hardware organization. Several different philosophies of commercially available microprocessor families are described. The characteristics of various logic families are considered with an eye towards interconnection compatibility. Bus structures and their electronic implementation are described in some detail. Flags, interrupts, direct memory acess control and programmable timers are also described with examples.

Chapter 4 reviews the various characteristics of memory components and systems. Included are sections on the implementation of main power failure battery backup systems and floppy disks.

Chapter 5 examines peripherals. There are sections on input/output control and handshaking, timing and buffering. There are also discussions of specific common microcomputer peripherals: keyboards, phototransducers, circuit testers, analog-to-digital and digital-to-analog converters, pressure transducers, optical

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City ______________ State ______________ Zip______ displays, relay drivers, synchromotors and printers. Finally, there are sections on universal asynchronous receiver-transmitters (UARTs), line drivers, the HPIB-IEEE 488 bus and self-test hardware.

Chapter 6 describes the various options that exist in hardware and software development packages from prototyping boards to disk-based operating systems. There is also a brief discussion of high-level languages for microcomputers.

Chapter 7 describes in detail the algorithms for solutions to several common microcomputer software problems. Algorithms are described to read and to parse a functional keyboard input, self-test routines and number system conversion and manipulations. Real-time programming constraints are also considered.

The set of appendices describes the characteristics of specific microcomputers. Each appendix covers the architecture and organization of a particular processor integrated circuit. The rest of the integrated circuit set (memory, input/output, etc) is also briefly covered. Appendices are included on the 4004, F8, 8080, 6800, COSMAC, and PPS-8 processors. It is refreshing to see that these appendices are more than just a reprinting of the manufacturer's specification sheets.

On the negative side, there is a disturbing absence of discussion of any of the high-performance integrated circuits that were certainly available when this book was written. There is also inadequate treatment given to bit-slice and microprogramming techniques. Software development by emulation is also omitted. The balance is, however, overwhelmingly positive. This is a text which starts off quietly, never grows dull, and yet contains a great deal of substance. There are sections on using esoteric devices like first in, first out stacks (FIFOs) that I have previously never seen in a design text.

It is a welcome development. I recommend this book to advanced experimenters, undergraduate engineering students and practicing engineers. ■

Ira Rampil
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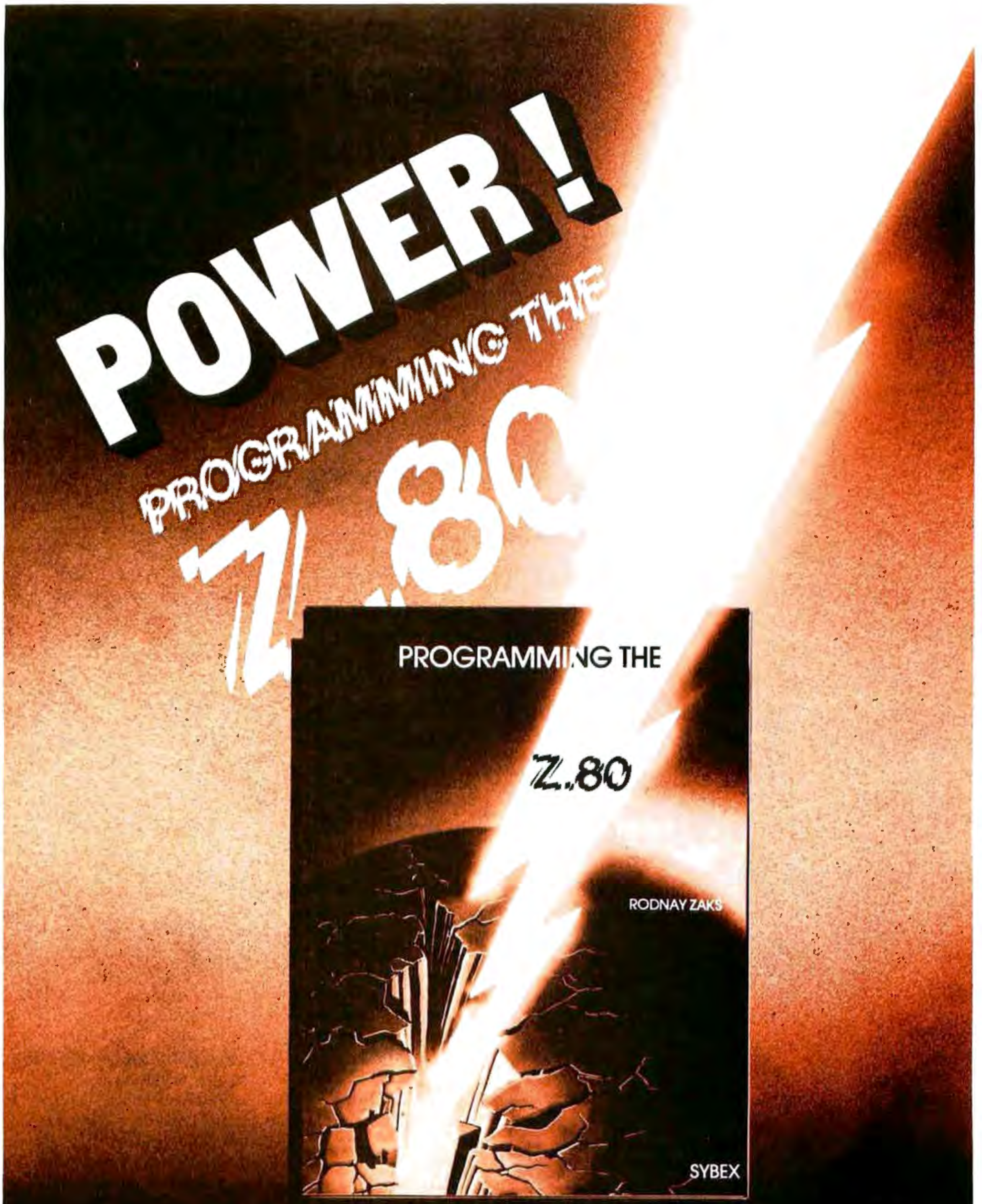
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Programming Quickies

Day of Week and Elapsed Time Programs

W B Agocs, Dept of Physical Sciences
Kutztown State College, Kutztown PA 19530

The day of the week, the number of elapsed days of a year, and the number of days between 2 dates are information that is required frequently in various types of analyses.

The procedure to determine the day of the week uses *Zeller's congruence*:

$$d = \{[2.6m-0.2] + K + Y + \left[\frac{Y}{4}\right] + \left[\frac{C}{4}\right] - 2C\} \text{ MOD } 7$$

The term m is the month number minus 2. If the month is January or February, m is 11 or 12 of the previous year. K is the day of the month; C is the century, and Y is the year of the century. The value of the square brackets is defined as the integer part of the result of evaluating the interior expression.

Day of Week From Date

The program is so written that corrections to month 11 or 12 of the previous year are made automatically if the month is January (1), or February (2). The program is shown in listing 1. Century selection could have been incorporated, but the program is designed for the 20th century. Once the number of the day of the week is obtained (with Sunday being day 1), the date and the day are printed.

Matrix Elapsed Time Determination

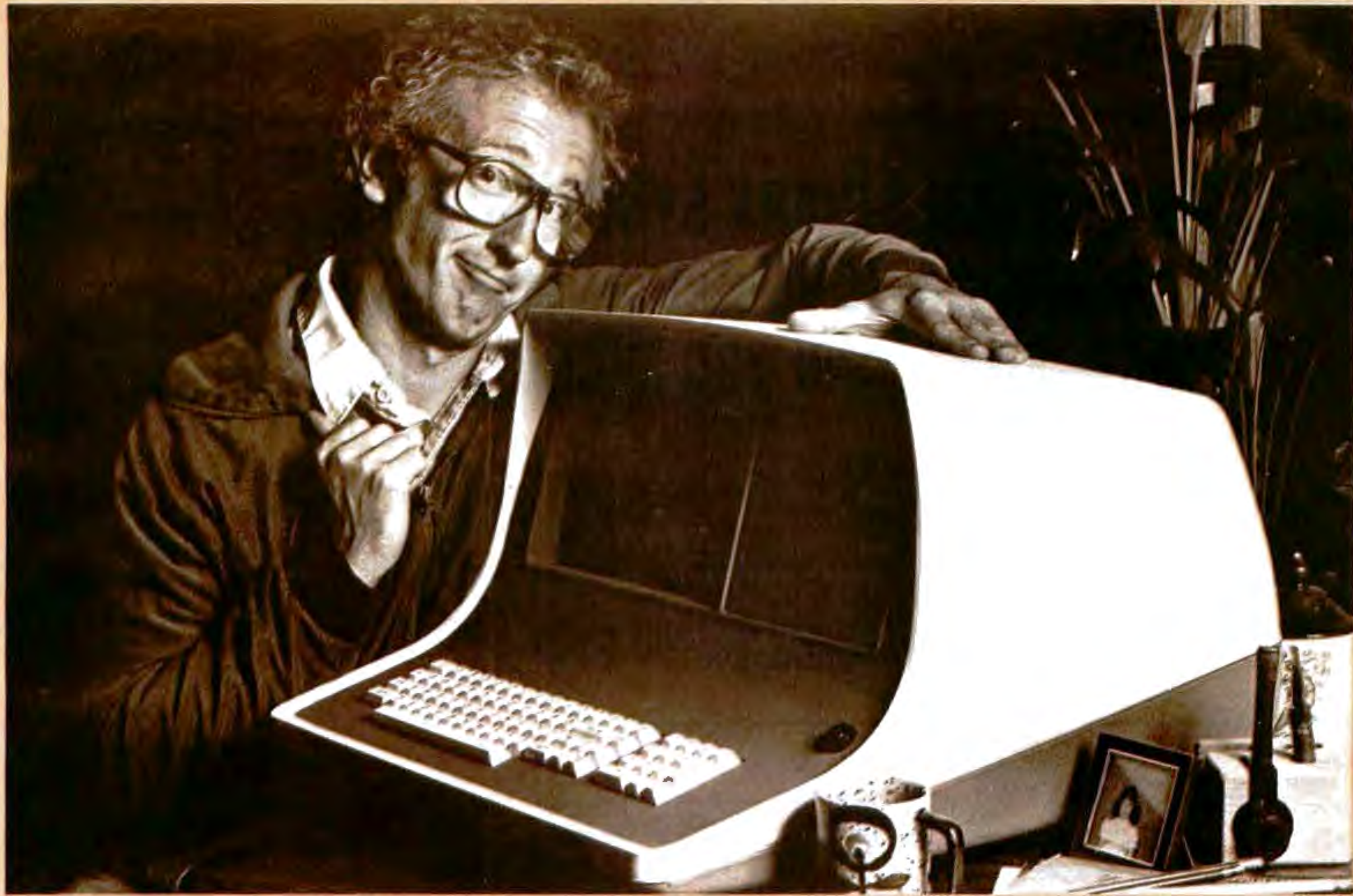
The use of a 12 by 31 matrix seems to be the most logical method for determining the elapsed days of a year, the remaining days in a year, and the day interval between 2 dates.

The program for such a determination is shown in listing 2. The MAT A = CON statement in line 50 sets each element of the matrix equal to 1. The subroutine in statements 440 thru 540 enters 0s into the matrix elements which correspond to the months with less than 31 days, and then fills the matrix elements with the date's numerical location in the year. Thus on return from the subroutine, the days elapsed may be *printed* between statements 180 and 190, or between statements 400 and 410 if desired. Leap year corrections are made at lines 270 and 440.

Finally, if the interval between the 2 dates is less than or greater than a year (as determined by statement 100), the correct *year* increment is made in statements 230 and 280.

The total time interval is determined in statement 180 or 410, and the result printed at statement 190.

Text continued on page 129



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Text continued from page 126:

The matrix procedure, with correction for appropriate holidays, can be used in conjunction with stock market studies when knowledge of the market day interval is desired, or when determining if a particular date is a market trading day.

Listing 1: BASIC program for determining the day of the week from the date using Zeller's congruence.

```
0010    PRINT "ZELLER'S CONGRUENCE-DAY OF WEEK
        FROM DATE."
0020    PRINT "WHAT IS THE DATE-MONTH, DAY, YEAR?"
0030    INPUT M,D,Y
0035    LET Y1 = Y
0037    LET M1 = M
0040    IF (M = 1) OR (M = 2) THEN 60
0050    GOTO 105
0060    IF M = 1 THEN 90
0070    LET M = 12
0080    GOTO 100
0090    LET M = 11
0100    LET Y = Y-1
0102    GOTO 110
0105    LET M = M-2
0110    LET D1 = INT(2.6*M-.2) + D + (Y-1900) + INT((Y-1900)/4)
0115    LET D1 = D1 + INT(19/4)-2*19
0120    LET D1 = D1-INT(D1/7)*7 + 1
0125    PRINT "D1 = ";D1
0130    ON D1 GOTO 140, 150, 160, 170, 180, 190, 200
0140    LET A1$ = "SUNDAY"
0145    GOTO 210
0150    LET A1$ = "MONDAY"
0155    GOTO 210
0160    LET A1$ = "TUESDAY"
0165    GOTO 210
0170    LET A1$ = "WEDNESDAY"
0175    GOTO 210
0180    LET A1$ = "THURSDAY"
0185    GOTO 210
0190    LET A1$ = "FRIDAY"
0195    GOTO 210
0200    LET A1$ = "SATURDAY"
0210    PRINT "FOR ";M1;"/";D;"/";Y1;" IT IS ";A1$
0220    PRINT
0230    END
```

Listing 2: BASIC program for using a matrix to determine the elapsed time between 2 dates.

```
0010    PRINT "MATRIX DETERMINATION OF DAYS BETWEEN
        DATES."
0020    PRINT "PROGRAMMED APRIL 15, 1979;W. B.
        AGOCS."
0030    DIM A(12,31)
0040    DCL S(A())
0050    MAT A = CON
0060    PRINT "WHAT IS THE FIRST MONTH, DATE, YEAR?;
        EXPRESS NUMERICALLY AS 11, 15, 1978."
0070    INPUT M1, D1, Y1
0080    PRINT "WHAT IS THE NEXT MONTH, DATE, YEAR?"
0090    INPUT M2, D2, Y2
0100    IF Y2-Y1 = 0 THEN 120
0110    GOTO 220
0120    IF Y1/4-INT(Y1/4) = 0 THEN 150
0130    GOSUB 450
0140    GOTO 160
0150    GOSUB 440
0160    LET S1 = A(M1, D1)
0170    LET S2 = A(M2, D2)
0180    LET S3 = S2-S1
0190    PRINT "INTERVAL BETWEEN ";M1;"/";D1;"/";Y1;
0195    PRINT " AND ";M2;"/";D2;"/";Y2;" IS ";
0200    PRINT S3;" DAYS."
0210    GOTO 580
0220    LET S = 0
0230    FOR I = Y1 + 1 TO Y2-1 STEP 1
0240    IF I/4-INT(I/4) = 0 THEN 270
0250    LET S = S + 365
0260    GOTO 280
0270    LET S = S + 366
0280    NEXT I
0290    IF Y1/4-INT(Y1/4) = 0 THEN 320
0300    GOSUB 450
0310    GOTO 350
0320    GOSUB 440
0330    LET S1 = 366-A(M1,D1)
0340    GOTO 360
0350    LET S1 = 365-A(M1,D1)
0360    IF Y2/4-INT(Y2/4) = 0 THEN 390
0370    GOSUB 450
0380    GOTO 400
0390    GOSUB 440
0400    LET S2 = A(M2,D2)
0410    LET S3 = S + S1 + S2
0420    GOTO 190
0430    REM SUB-ROUTINE
0440    LET A(2,29) = 0
0450    LET  A(2,30) = A(2,31) = A(4,31) = A(6,31) = A(9,31)
        = A(11, 31) = 0
0460    LET N = 0
0470    FOR I = 1 TO 12 STEP 1
0480    FOR J = 1 TO 31 STEP 1
0490    IF A(I,J) = 1 THEN 510
0500    GOTO 530
0510    LET N = N + 1
0520    LET A(I,J) = N
0530    NEXT J
0540    NEXT I
0550    RETURN
0560    PRINT
0570    PRINT
0580    PRINT "THE END."
0590    END ■
```

A Text Loader Routine

Howard Berenbon
2681 Peterboro
W Bloomfield MI 48033

Here is a useful program for the Motorola 6800 microcomputer. This subroutine allows the loading of ASCII text into the desired memory location directly from your terminal. It uses the Motorola MIKBUG monitor for character input and output. The subroutine may be entered beginning at hexadecimal address A060. To exit the program simply type a %.

Hexadecimal Address	Hexadecimal Code	Mnemonic	Comments
A060	86 3F	LDAA #$ 3F	Load A with ?
A062	BD EO 75	JSR CHAROUT	Output ?
A065	86 20	LDAA #$ 20	Load A with a space
A067	BD EO 75	JSR CHAROUT	Output space
A06A	CE _ _	LDX #$ _ _	Load index register with desired address
A06D	BD EO 78 &LOOP	JSR CHARIN	Input character
A070	A7 00	STAA $ 00:X	Store A indexed
A072	08	INX	Increment index register
A073	81 25	CMPA #$ 25	Compare A with %
A075	26 F6	BNE &LOOP	Get another character
A077	7E E0E3	JMP MIKBUG	Return to MIKBUG ■

A Model of the Brain for Robot Control

Part 4: Mechanisms of Choice

James Albus
Project Manager
National Bureau of Standards
United States Dept of Commerce
Washington DC 20234

The essence of a hierarchy is that control is top-down. The ultimate choices are made at the top, and the goals selected at this level are decomposed into action as they filter down through the various levels of the hierarchy. For the purposes of our discussion, we will define the highest level H function in the behavior-generating hierarchy of the human brain as the *will*.

The ideas presented in this article represent the views of the author and not those of the Department of Commerce or the National Bureau of Standards.

For centuries philosophers and theologians have debated the nature of the will, particularly the question of whether humans have "free" will (ie: the *freedom* to choose goals) or whether all choice is merely a reflexive or predestined response to the environment. We shall not presume to deal with this question here, other than to suggest what types of inputs are available to this highest level goal selection module.

By definition much of the input to the highest level behavior-generating module must come from the highest level sensory-processing module.

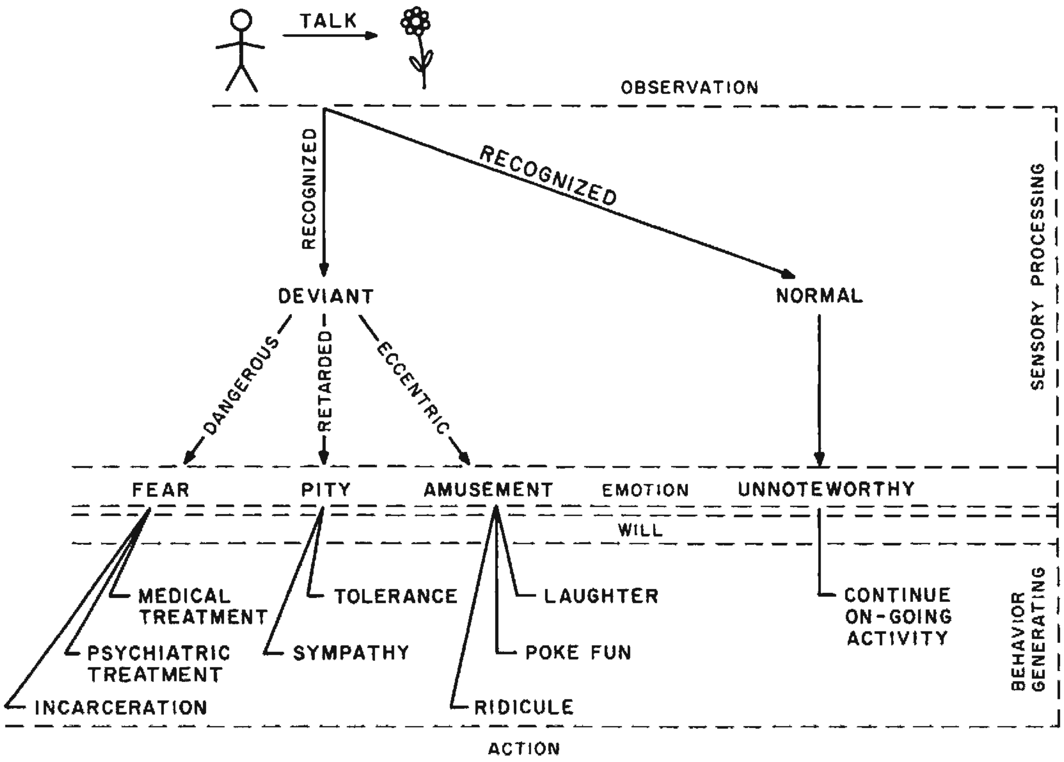

Figure 1: An action (such as a person talking to a flower) may be recognized as either familiar or unfamiliar. If an action is noted as familiar, then it can be considered unnoteworthy and will be ignored. If the action is considered deviant, further processing will take place to determine reactions to the action.

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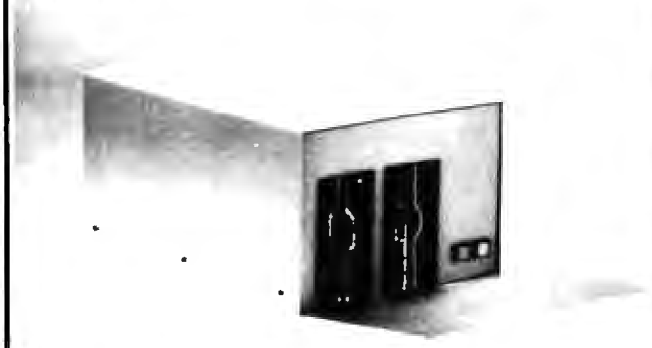

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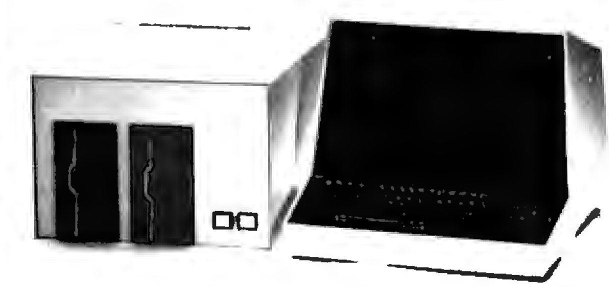

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This is the level at which the overall result of the entire sensory processing operation is evaluated as being good or bad, rewarding or punishing, satisfying or frustrating. In humans, this function is performed by what are commonly called the emotions. It has long been recognized that emotions play a crucial role in the selection of behavior. We tend to practice that which makes us feel comfortable and avoid what we dislike. Our behavior-generating hierarchy normally seeks to prolong, intensify, or repeat those behaviors which give us pleasure or make us feel happy or contented. We normally seek to terminate, diminish, or avoid those behavior patterns which cause us pain, or arouse fear or disgust.

In the past 25 years it has become known that the emotions are generated in localized areas, or computing centers, in the brain. For example, the posterior hypothalamus produces fear, the amygdala generates anger and rage, the insula computes feelings of contentment, and the septal regions produce joy and elation. The periformical nucleus of the hypothalamus produces punishing pain, the septum pleasure, the anterior hypothalamus sexual arousal, and the pituitary computes the body's response to danger and stress. These emotional centers, along with many others, make up a complex of about 53 regions linked together by 35 major nerve bundles. This entire network is called the limbic system. Additional functions performed in the limbic system are the regulation of hunger and thirst performed by the medial and lateral hypothalamus, the control of body rhythms such as sleep-awake cycles performed by the pineal gland, and the production of signals which consolidate (ie: make permanent) the storage of sensory experiences in memory performed by the hippocampus. This last function allows the brain to be selective in its use of memory by facilitating the permanent storage of sensory experiences to which the emotional evaluators attach particular significance (eg: close brushes with death, punishing experiences, etc).

Input to the limbic system emotional centers consists of highly processed sensory-data such as the names of recognized objects, events, relationships, and situations, such as the recognition of success in goal achievement, the perception of praise or hostility, or the recognition of gestures of dominance or submission transmitted by social peers. These inputs are accompanied by such modifier variables as confidence factors derived from the degree of correlation between predicted and observed sensory input.

Sensory processing at the level of the emotions is heavily influenced by contextual information derived from internal models and expectations at many different levels in the processing hierarchy. If a painful stimulus is perceived as being associated with a nonfear producing source, we may attack the pain causing agent. If, however, the perceived source of pain also induces fear, we may flee.

Similarly if an observed event such as a person talking to a flower is perceived as deviant, then this input to the emotions, along with other recognized qualifier variables such as the person is a) eccentric, b) retarded, or c) dangerously psychotic, will cause the emotions to output a) amusement, b) pity, or c) fear, respectively. Amusement input to the behavioral goal selecting module may lead to laughter, poking fun, or ridicule. Pity input to the will may

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About the Author

Dr James S Albus worked for NASA from 1957 to 1972 designing optical and electronic subsystems for over 15 spacecraft, and for one year managed the NASA Artificial Intelligence Program. Since 1973 he has been with the National Bureau of Standards where he has received several awards for his work in advanced computer control systems for industrial robots. He has written a survey article on robot systems for Scientific American *(February 1976) and his Cerebellar Model Arithmetic Computer won the* Industrial Research Magazine *IR-100 Award as one of the 100 most significant new products of 1975. He is also the author of* People's Capitalism: The Economics of the Robot Revolution *which is published by New World Books, 4515 Saul Rd, Kensington MD 20795.*

---

evoke a behavioral pattern of sympathy. Fear may evoke an attempt to secure medical or psychiatric treatment, or incarceration.

If, however, a person talking to a flower is recognized as perfectly normal, then the emotions will give no indication that the event is particularly worthy of attention, or that there exists any need to deviate from whatever behavior is presently being executed. These relationships are described graphically and symbolically in figure 1.

In this model the standards of normalcy and deviance are clearly in the eye of the beholder, or at least in the expectations and beliefs stored in the processing-generating hierarchy. In many ways the emotional evaluators are even more dependent on internal beliefs than externally observed facts. This is particularly true in the case where a person's belief structure discounts the reliability or moral worth of the physical senses, as is characteristic of philosophical constructs derived from gnosticism or asceticism.

Thus the emotions, just as any other sensory processing module in the brain, simply compute a G function on the D vector that they input to produce the Q vector that they output. In simple creatures the emotional output vector may be restricted to a few components such as good-bad, pleasure-pain, etc. In higher forms the emotional output is a highly multidimensional vector with many faceted components such as love, hate, jealousy, guilt, pride, disgust, etc. Part of this Q output may simply produce feelings (ie: joy, sadness, excitement, fear, etc). However, most of the Q output directly or indirectly provides F input to the highest level H function, the will.

Output from the emotional centers is known to be of two types: one consists of signals on nerve fibers; the other consists of hormones and chemical transmitters which convey their messages (Q vector values) via fluid transport mechanisms.

What the G and H functions of the emotions and will are, and where they come from is a matter of hot dispute. One recent theory proposed by sociobiology is that they are genetically determined, derived from information stored in the DNA molecule, as the result of millions of years of natural selection. This theory argues that innate behavior-selecting mechanisms have evolved so as to maximize the Darwinian fitness (the expected number of surviving offspring) of their possessors.

The incidence of behavior in many different species from insects to birds to mammals corresponds closely to mathematical predictions derived from genetics and game-theory analyses of strategies for maximizing the probability of gene propagation. Even cooperative or altruistic behavior such as that of the worker bee, and ritualized behavior in animal contests and courtship, can in many cases be explained by genetic arguments. However, the evidence for this theory is much stronger for insects than for higher forms, and the opinion that human emotions are transmitted genetically is not widely held.

A competing theory put forward by behaviorists is that in higher forms the evaluator functions of the emotion and the selector functions of the will are mostly learned, perhaps even

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imprinted, during the early years of development. Certainly many of the emotional evaluations and behavior selection rules in the human brain are culturally determined, derived from religious teachings defining good and evil, or from social conventions defining duty, fairness, etiquette, and legality. These fundamental rules of opinion and behavior are instilled in the young by parents, educators, and religious and state authorities. They are reinforced throughout life by peer group pressure, as well as by church and civil sanctions.

There are, of course, many persons who would disagree with both of these theories. Perhaps the most widespread opinion (which until recent years was virtually unchallenged) is that the human will and its emotional evaluator inputs are nonmechanistic in nature and therefore unknowable in some fundamental sense. Many would even claim that emotions and will are subject to, or controlled by, spiritual and supernatural forces. For example, the doctrine of original sin states that the highest level behavior selecting mechanism, the human will, is basically defective because of the disobedience of Adam and Eve, and except for divine intervention is under the power of evil or satanic forces. The literature surrounding the age old controversy over free will versus predestination centers largely on the role of the Divinity (or the stars, or fates) in the determination of human behavior. Most cultures view the conscience (ie: the emotional evaluator for right and wrong or good and evil) as a divine gift or manifestation of the indwelling of the spirit of God.

Clearly the emotions and will are a very basic (some would say primitive) and compelling part of our behavioral mechanism. Carl Sagan calls them the *Dragons of Eden*. Humans are often driven, sometimes beyond rational justification, to heroic feats of courage or physical endurance by the behavior rules of duty or the emotions of love, pride, guilt, jealousy, and hate.

Whatever their origins, the G functions of our emotions and the H functions of the will can be modeled. They are rule based, and the rules are, for the most part, clearly defined. In many cases these rules are even written down as systems of moral philosophy, ethics, or rules of social behavior such as *Emily Post's Book of Etiquette*.

Nothing so complex need be modeled for the highest level G and H modules of a robot for many years. Nevertheless, every robot needs some sort of highest level evaluator and goal selector function in order to exhibit any sort of autonomous behavior. At what point in the spectrum of multidimensional sophistication we choose to dignify an evaluator function with the term emotion, or goal selection function with the term will, is not clear. What is clear is that simple approximations to the functions computed by the emotions and the will can be moduled by CMAC G and H functions operating on input vectors and computing output vectors. The degree of sophistication and complexity of the modeling is limited only by the ingenuity and resources of the modeler.

The interdependency of the processing and generating hierarchies suggests at least 3 distinct modes of operation.

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Acting—The Task Execution Mode

In the task execution mode the motor-generating hierarchy is committed to a goal, which it decomposes into subgoals, sub-subgoals, and finally into action primitives. In this mode the sensory-processing hierarchy is primarily engaged in providing feedback; first to aid in selecting the goal, then to steer the goal decomposition process, and finally to direct the output drive signals to the muscles (or actuators) so as to follow a success trajectory.

Consider a simple, everyday goal such as the fixing of a leaking faucet. First, the sensory processing system must recognize the fact that the faucet is leaking. This information is then evaluated by the emotions as something that needs attention. This evaluation is passed on to the will, where the rules of what ought to be done and under what circumstances reside. If there are no higher priority items vying for the attention of the will, then the goal <fix faucet> may be selected. Once this occurs, the behavior generating hierarchy will be committed to decompose this goal into a sequence of actions.

At each instant of time t_k the sensory-processing module at each hierarchical level extracts feedback vectors F_i^k required by the H behavior-generating modules at each level for goal decomposition. At the instant t_0 when the goal is selected, the feedback F_i^0 at the various levels causes the selection of the initial subgoal decompositon P_i^0. This determines the initial direction of the trajectories T_{P_i} on their way toward the goal state. As the task proceeds, the recognition of subgoal completions and/or unanticipated obstacles triggers the selection of the proper sequence of actions directed toward the goal achievement.

The entire set of trajectories T_{P_i} describes the sequence of internal states of the brain which underlie and give rise to the observable phenomena of purposive behavior. These are the deep structure of behavior. Only the output trajectory, the terminal or bottom level trajectory, is manifested as overt action. The extent to which the trajectories T_{P_i} are independent of feedback is the extent to which behavior is preprogrammed. The extent to which the feedback pulls the T_{P_i} trajectories along predictable paths to the goal state is the extent to which behavior is adaptive. For some goals, such as hunting for prey or searching for breeding territory, the selection of the goal merely triggers migratory searching behavior which continues until feedback indicates that the goal is near at hand. For such goals, behavior is indefinite and highly feedback dependent. For other goals, such as building a nest, making a tool, courting a mate, or defending a territory, behavior is more inner-directed, requiring only a few sensory cues for triggers.

In either case, while in the acting mode the sensory data flowing in the sensory-processing hierarchy is highly dependent on (if not directly caused by) the action itself. If the action is speech, the sensory-processing hierarchy is analysing what is spoken, and provides feedback for control of loudness, pitch, and modulation. If the action is physical motion, data from vision, proprioception, and touch sensors are all highly action dependent, and the sensory analysis is primarily directed toward servo control of the action itself.

In the action mode, the M_i associative memory modules provide context in the form of predicted data to the sensory-processing modules in order to distinguish between sensory data caused by motion of the sensors and that caused by motion of the environment. What is predicted is whatever was stored on previous experiences when the same action was generated under similar circumstances. This allows the sensory-processing hierarchy to anticipate the sensory input and to detect more sophisticated patterns in the sensory data than would otherwise be possible.

Observing—The Sensory Analysis Mode

A second mode of operation of the crosscoupled hierarchy is the analysis of sensory data from external sources not primarily caused by action of the behavior-generating hierarchy. For example, when listening to a concert, a speech, or a play, there is little action going on in the muscles and motor neurons. The lower levels of behavior-generating hierarchies are quiescent, or set to a constant value, or given a command to execute an

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overlearned task which can be carried out without any assistance from the upper levels.

The sensory-processing hierarchies, however, are very busy. They are filtering and predicting, recognizing patterns and trajectories, locking on to rhythms and harmonious periodicities, and tracking targets of attention. Predictions generated by the M modules are clearly required for these types of analyses, whether or not the organism is engaged in physical activity. This suggests that the upper levels of the behavior-generating hierarchies (which are not currently required for generating behavior) might be used instead to generate hypotheses and subhypotheses which in turn produce context and predictions to aid the sensory-processing hierarchy in the recognition, analysis, and understanding of incoming sensory data.

At each level hypotheses which generate T_R predictions that match or track the T_E sensory data trajectories will be confirmed. If the hypothesized T_R trajectories are only close to the T_E observations, they can be pulled by error signal feedback T_F from the processing hierarchies. When a hypothesis is successful in generating predictions which match the sensory data stream, the loop at that level locks onto the sensory data. When lock-on is simultaneously achieved at many different levels, we can say that the processing-generating hierarchy "understands" the incoming data (ie: it can follow and predict it at many different levels). The depth of understanding depends upon how many levels lock onto the sensory data stream. The accuracy of understanding depends upon how precisely the hypotheses track and predict the incoming sensory data.

It is easier to follow a trajectory than to reproduce it. When observing a procedure, the generating hierarchy merely needs to produce hypotheses which are in the right vicinity so that they can be synchronized with the sensory input. Uncertainties at branch points in T_{P_i} do not matter greatly because errors are quickly corrected by comparing T_{R_i} with T_{E_i}.

On the other hand, reproducing a procedure requires that the H functions be capable of generating T_{P_i} trajectories which are quite precise over their entire length. They must not wander outside of the success envelope or miss any critical branch points. Needless to say, the latter is a much more exacting computational problem, and offers an explanation for why a student may be able to follow the reasoning of his professor's lecture, but is unable to pass an exam without additional drill and practice.

Attention

The directing or focusing of attention is essentially a purposive action whose goal is to optimize the quality of the sensory data. The basic elements of attention are orienting (positioning the body and sensory organs so as to facilitate the gathering of data) and focusing (blocking out extraneous or peripheral information so that the sensory processing system can bring all of its capacities to bear on data that is relevant to the object of attention). The orienting element is simply a behavioral task or goal to acquire and track a target. The focusing element is a filtering problem which can be solved by a hypothesis or goal decomposition which evokes the appropriate masks or filter functions from the R_i modules so as to block out all but the relevant sensory input data.

Thus, attending is a combination of observing and acting. It is primarily a sensory analysis mode activity, with a stong assist from the task execution mode.

Imagining—The Free-Running Mode

A third distinct mode of operation occurs when the upper levels of the processing-generating hierarchy are largely disconnected from both motor output and sensory input. In this mode high-level hypotheses T_{P_i} may be generated, and predicted sensory data T_{R_i} recalled. In the absence of sensory input from the external environment, these recalled trajectories make up all of the information flowing in the sensory-processing hierarchy. The processing modules G_i operate exclusively on the internally recalled R_i trajectories producing T_{Q_i}experiences and T_{F_i} feedback. The T_{F_i}trajectories act on the generating hierarchy so as to modify and steer the T_{S_i} trajectories creating new hypotheses T_{P_i}. The system is free running, guided only by stored experiences M_i, learned interpretations G_i, and practiced skills H_i, for

generating strings of hypotheses and *decomposing* goals and tasks. The upper levels of the crosscoupled hierarchy are, thus, imagining (ie: generating and analyzing what would be expected if certain hypothesized goals and tasks were to be carried out).

Imagination is based on stored experiences and driven by hypothesized actions. It is constrained in large measure by the knowledge frames, world models, expected values, and belief structures (IF I do this, THEN such and so will happen) embedded in the upper levels of the cross-coupled processing-generating hierarchy.

If we attempt to hypothesize some action X which lies outside of the neighborhood of generalization of prior experience, we get no recalled R_i vectors from memory M_i. In this case we say "we cannot imagine what X would be like."

One of the functions of the free-running mode is to remember or recall past experiences by hypothesizing the same goals as when the experience was recorded. Thus, in our imagination we can reach back and relive experiences, recall events, and, hence, remember facts and relationships from our past. Imagination, however, is not limited to duplication of past experiences. We can also rearrange sections of learned trajectories to create experiences in our minds which never occurred. We can string together trajectories in new combinations or insert new modifier variables in various hypothesis vectors. We can watch a bird fly and substitute a "self" variable in place of the bird to imagine ourselves soaring through the sky. We can listen to a story of adventure and imagine ourselves in the place of one of the characters. Imagination allows us to hypothesize untried actions and, on the basis of M functions learned during previous experiences, to predict the outcome.

Planning

Imagination gives us the ability to think about what we are going to do before committing ourselves to action. We can try out, or hypothesize prospective behavior patterns, and predict the probable results. The emotions enable us to evaluate these predicted results as good or bad, desirable or undesirable.

Imagination and emotional evaluators together give us the capability to conduct a search over a space of potential goal decompositions and to find the best course of action. This type of search is called *planning*.

When we plan, we hypothesize various alternative behavior trajectories and attempt to select the one that takes us from our present state to the goal state by the most desirable route. Imagined scenarios which produce positive emotional outputs are flagged as candidate plans. Favorably evaluated scenarios or plans can be repeatedly rehearsed, reevaluated, and refined prior to initiation of behavior-producing action.

Imagined scenarios which produce negative evaluation outputs will be avoided if possible. In some situations it may not be possible to find a path from our present state to a goal state, or at least not one which produces a net positive evaluation. Repeated unsuccessful attempts to find a satisfactory, nonpunishing plan, particularly in situations recognized as critical to one's well-being, correspond to *worry*.

One of the central issues in the study of planning is the search strategy, or procedure, which dictates

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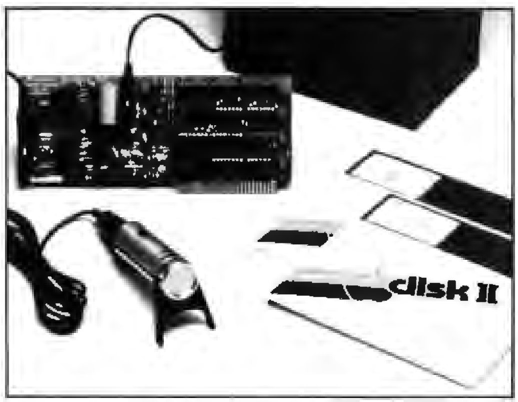

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which of the many possible hypotheses should be evaluated first. In most cases, the search space is much too large to permit an exhaustive search of all possible plans, or even any substantial fraction of them. The set of rules for deciding which hypotheses to evaluate, and in which order, are called *heuristics.*

Heuristics are usually derived in an ad hoc way from experience, accident, analogy, or guesswork. Once discovered, they may be passed from one individual to another, and from one generation to another by teaching.

Historically, artificial intelligence researchers have been fascinated by the subject of heuristics. At least a portion of this interest is a result of their recursive nature. A heuristic is a procedure for finding a procedure. When this recursion is embedded in a cross-coupled processing-generating hierarchy with the rich complexity of the human brain, it becomes clear why the thoughts and plans of humans are filled with such exquisite subtleties, and curious, sometimes insidious reasoning. It also provides some insight into the remarkable phenomenon of self-consciousness (ie: a computing structure with the capacity to observe, take note of, analyze, and, to some extent, even understand itself.)

Much of the artificial intelligence research in planning and problem solving has its origins and theoretical framework based on simple board games where there are a finite (although sometimes very large) number of possible moves. The discrete character of such games, together with the digital nature of computers, led naturally to the analysis of discrete trees, graphs, and search strategies for such structures.

Planning in a natural environment is much more complex than searching discrete trees and graphs. In the study of planning in the brain it is necessary to deal with the continuous time-dependent nature of real world variables and situations. States are not accurately represented as nodes in a graph or tree; they are more like points in a tensor field. Transitions between states are not lines or edges, but multidimensional trajectories (fuzzy and noisy at that). In a natural environment, the space of possible behaviors is infinite. It is clearly impossible to exhaustively search any significant portion of it. Furthermore, the real world is much too unpredictable and hostile, and wrong guesses are far too dangerous to make exploration practical outside of a few regions in which behavior patterns have had a historical record of success. Thus behavior, and hence imagination and planning, is confined to a relatively small range of possibilities, namely those behavior and thought patterns which have been discovered to be successful through historical accident or painful trial and error. Both the potential behavior patterns and the heuristics for selecting them are passed from one generation to another by parents, educators, and civil and religious customs.

Daydreaming or Fantasizing

The fact that the imagination can generate hypothetical scenarios with pleasurable emotional evaluations makes it inevitable that such scenarios will, upon occasion, be rehearsed for their pleasure-producing effect alone. This is a procedure that can only be described as daydreaming or fantasizing.

When we daydream we allow our hypothesis generators to drift

5 reasons why you should not buy the electric pencil II™

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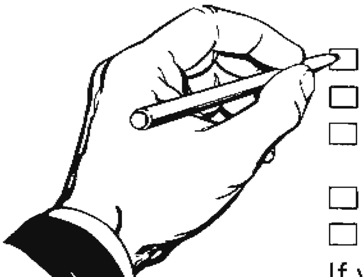

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As text is typed and the end of a line is reached, a partially completed word is shifted to the beginning of the following line. Whenever text is inserted or deleted, existing text is pushed down or pulled up in a wrap around fashion. Everything appears on the video display as it occurs, which eliminates guesswork. Text may be reviewed at will by variable speed scrolling both in the forward and reverse directions. By using the search or search and replace functions, any string of characters may be located and/or replaced with any other string of characters as desired.

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Digital Research's CP/M, as well as its derivatives, including IMDOS and CDOS, and Helios PTDOS versions are also available. There are several NEC Spinwriter print packages. A utility program that converts The Electric Pencil to CP/M to Pencil files, called **CONVERT**, is only $35.

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Upgrading policy

Any version of The Electric Pencil may be upgraded at any time by simply returning the *original* disk or cassette and the price difference between versions, plus $15 to Michael Shrayer Software. Only the originally purchased cassette or diskette will be accepted for upgrading under this policy.

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The Electric Pencil II operates with any 8080/Z80 based microcomputer that supports a CP/M disk system and uses an Imsai VIO, Processor Tech. VDM-1, Polymorphic VTI, Solid State Music VB-1B or Vector Graphic video interface. REX versions also available. Specify when using CP/M that has been modified for Micropolis or North Star disk systems as follows: for North star add suffix A to version number; for Micropolis add suffix B, e.g., SS-IIA, DV-IIB.

Vers.	Video	Printer	Price
SS-II	SOL	TTY or similar	$225.
SP-II	VTI	TTY or similar	225.
SV-II	VDM	TTY or similar	225.
SR-II	REX	TTY or similar	250.
SI-II	VIO	TTY or similar	250.
DS-II	SOL	Diablo 1610/20	275.
DP-II	VTI	Diablo 1610/20	275.
DV-II	VDM	Diablo 1610/20	275.
DR-II	REX	Diablo 1610/20	300.
DI-II	VIO	Diablo 1610/20	300.
NS-II	SOL	NEC Spinwriter	275.
NP-II	VTI	NEC Spinwriter	275.
NV-II	VDM	NEC Spinwriter	275.
NR-II	REX	NEC Spinwriter	300.
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SSH	SOL	Helios/TTY	250.
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Version	Storage	Price
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wherever our emotional evaluators pull them. Our imagination gravitates toward those trajectories which are emotionally most rewarding. Some of the most pleasurable scenarios we can imagine are physically impossible, impractical, or socially taboo. Most of us recognize these as fantasies and never attempt to carry them out. However, once a person adopts the intent to carry out a fantasy, it ceases to be a dream and becomes a plan.

Thus, planning and daydreaming are closely related activities, differing principally in that planning has a serious purpose and involves an intent to execute what is finally selected as the most desirable of the alternative hypotheses.

This model suggests that dreaming while sleeping is similar in many respects to daydreaming. The principal difference in night dreaming seems to be that the trajectories evoked are more spasmodic and random, and are not always under the complete control of the emotions and will.

Creativity

The notion of planning or discovering procedures for achieving goals leads inevitably to the issue of creativity. If we assume that most of the H, G, and M functions in the processing-generating hierarchy are learned, then where is the creativity? Is creativity merely an illusion generated by the recursion of procedures for discovering procedures?

Certainly we as humans like to think of ourselves as creative. But what are we doing when we create something new? Typically we borrow an idea from here, put it together with another from there, and give it a different name. We take a familiar behavioral trajectory, add a tiny variation, and claim that we have discovered something completely new — a new dance step, dress style, song, or idea. Seldom, however, are any of these more than the slightest deviation from a preexisting procedure or behavioral trajectory. To quote Ecclesiastes: "There is nothing new under the sun."

True creativity, in the sense of the invention of an entirely new behavioral trajectory, is extremely rare, if it ever occurs at all. Furthermore, it is highly doubtful that a truly creative act would be recognized if it ever did occur. Our processing-generating hierarchies cannot lock on to sensory input patterns which are totally different from everything that is stored in them. We reject such inputs as meaningless noise, or as alien and possibly hostile. True creativity would be as incomprehensible as a book written in a foreign language, or a theorem expressed in an unknown mathematical notation.

In one sense we are all creative in everything that we do, since no two behavioral trajectories are ever repeated exactly. However, the day-to-day variations in our ordinary behavior are not what we usually mean when we speak of creativity. We take pride in those moments of inspiration when something clicks, and we produce a great invention or a work of art.

Nonetheless, if we analyze a list of the great creative ideas which have shaped human history, we find that even these have been little more than clever rearrangements of well-known preexisting patterns or procedures.

Consider the fact that it took the human race many millenia to learn to start a fire, to grow a crop, to build a wheel, to write a story, to ride a horse. Even the Greeks did not know how to build an arch. Yet these are all simple procedures which any child can understand and more or less master. Surely our ancestors as adults were as intelligent and creative as today's children. Why did they fail for hundreds of years to discover these simple yet highly useful procedures?

It was because they had no one to teach them. A modern child knows about wheels because he is taught. He plays with toys that have wheels. He rides in vehicles with wheels. If a modern child grew up in a culture where he never saw a wheel, he would never think of one, nor would his children, or his grandchildren, any more than his ancestors did for thousands of years before him.

The reason that we value creativity so highly is because it is so rare and so highly advantageous. Once a new and useful procedure like navigating a ship, making steel, or flying an airplane is discovered, it can easily be taught to others. Entirely new worlds of possible behavior patterns open up for all who possess the secret.

We learn to solve problems, to invent, and to be creative, in much the same way as we learn any other goal-directed behavior pattern such as hunting, dancing, speaking, or behaving in a manner that is acceptable to and approved by our peers. We learn it from a teacher. The beauty, the sense of awe and wonder we experience when confronted by a work of creative genius, derives not so much from its novelty/creativity as from the skill and precision with which it is executed.

Implications for Robot Design

There is little need to worry about programming "creativity" into our machines. If we design systems with sufficient skill in executing tasks and seeking goals, and sufficient sophistication in sensory analysis and context sensitive recall, and if we teach these systems procedures for selecting behavior patterns which are appropriate to the situation, then they will appear to be both intelligent and creative. But there will never be any particular part of such a device to which one can point and say "Here is the intelligence," or "Here is the creativity." Skills and knowledge will be distributed as functional operators throughout the entire hierarchy. To the degree that we are successful, intelligence and creativity will be evidenced in the procedures which are generated by such systems.

Above all, we should not expect our robots to be more clever than ourselves, at least not for many decades. In particular we should not expect our machines to program themselves, or to discover for themselves how to do what we do not know how to teach them. We teach our children for years. It will take at least as much effort to teach our machines.

We must show our robots what

each task is and how to do it. We must lead them through in explicit detail, and teach them the correct response for almost every situation. This is how industrial robots are programmed today at the very lowest levels, and this is, for the most part, how children are taught in school. It is the way that most of us learned everything we know, and there is no reason to suspect that robots will be programmed very differently. Surely it is as unreasonable to expect a robot to program itself as it is to expect a child to educate himself. We should not expect our robots to discover new solutions to unsolved problems or to do anything that we, in all the thousands of generations we have been on this earth, have not learned how to do ourselves.

This does not mean that once we have trained our robots to a certain level of competence that they can't learn many things on their own. We can certainly write programs to take the routine and the tedium out of teaching robots. Many different laboratories are developing high-level robot programming languages. We already know something about how to represent knowledge in computers about mathematics, physics, chemistry, geology, and even medical diagnosis. We know how to program complex control systems and to model complicated processes, and we are rapidly learning how to do it better, more quickly, and more reliably. Soon perhaps it will even be possible to translate knowledge from natural language into robot language so that we will be able to teach our robots from text books or tape recordings more quickly and easily than humans. We can even imagine robots learning by browsing through libraries or reading scientific papers.

But it is a mistake to attempt to build creative robots. We are not even sure what a creative human is, and we certainly have no idea what makes a person creative, aside from contact with other creative humans — or time alone to think. Is it both? Or neither?

I believe that we should first learn how to build skilled robots — skilled in manipulation, in coping with an uncertain or even hostile environment, in hunting and escaping, in making and using tools, in encoding behavior and knowledge into language, in understanding music and speech, in imaging, and in planning. Once we have accomplished these objectives, then perhaps we will understand how to convert such skills into creativity. Or perhaps we will understand that robots with such skills already possess the creativity and the wisdom which springs naturally from the knowledge of the skills themselves. ■

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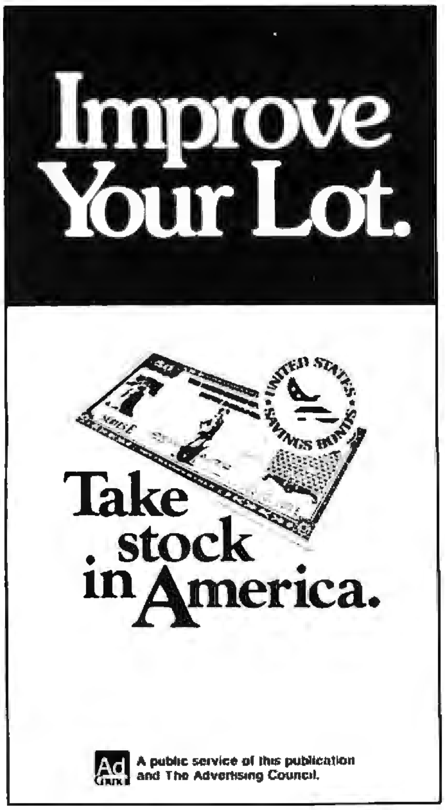

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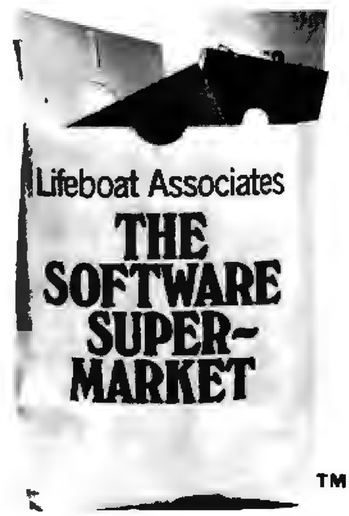

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Letters

ROBOT DESIGN COMMENTS

After receiving many calls (February and March 1979 BYTE) and letters about my article, "Designing A Robot From Nature" and, in particular, the NELOC (Neural Logic Cyberanimate), I have prepared a list of answers to the most common asked questions.

- The hardware is not for sale. The manipulator arm was assembled in 1976 using a Buhler motor and gear train which are no longer available. The structural elements of the arm *are* fashioned from extruded aluminum and machined Lexan plastic. The arm is presently used as a test bed for evaluating better processing systems.
- I have no plans available for the construction of the manipulator at this time. In the 3rd quarter of this year I will possibly complete a set of plans for a pneumatic version of the manipulator, one that uses tiny air driven pistons that are normally used to retract model aircraft landing gear.
- Third, over all design of the system will probably be included in the above plans.
- Fourth, the design of the NELOC system is not suited for use as a prosthetic device.
- Fifth, the concept of Cyberanimation is mine. I coined this term in 1974. None of the books in my bibliography contain this concept or methodology.
- Sixth, I am privately funded, I am not connected with any institutions, and I do not have any jobs available.

I would like to thank those people who have sent letters and called. I am trying to respond to as many of your requests as possible.

Andrew Filo
4621 Granger Rd
Akron OH 44313

Good Cents

The formatting of dollars and cents in BASIC without a PRINT USING command appears to be a problem for a number of people. In recent months, BYTE published a Programming Quickie by Les Palenik ("Formatting Dollars and Cents," October 1978 BYTE, page 68) and a letter by James Thebeault Sr ("Making Cents," April 1979 BYTE, page 8). Both of these authors provided a rather lengthy subroutine for this purpose.

The dollars and cents problem can be handled in a reasonably straightforward manner. In illustration, the PRINT statement:

```
PRINT "$";X
```

can be directly replaced by:

```
PRINT "$"; INT(X); ".";
PRINT RIGHT$(STR$(INT(100* (X+1)+0.5)),2)
```

with rounding off included in the formula. If X is already rounded off, this can be reduced to:

```
PRINT "$"; INT(X) ".";
PRINT RIGHT$(STR$(100*(X+1)),2)
```

for greater convenience.

I hope that some readers may find the above useful. We who write programs have a responsibility to provide output in formats familiar to the noncomputer public; we should not expect others to accept missing zeros and unusual abbreviations.

James Childress
5108 Springlake Way
Baltimore MD 21212

LOST IN A SEA OF PHLOGISTEN

As a graduate student in chemistry at the University of Washington I have had frequent occasion to discuss entropy and other thermodynamic goodies with other graduate students. When I saw your article "Artificial Intelligence and Entropy" (June 1979 BYTE), I gave a copy to a fellow delver-into-the-mysteries-of-science (Fred Wolters). The next day I found the following note in my mailbox. I share it with you in order that all might take warning and beware.

> Dear Mr. Sloat,
>
> This is to inform you that our intelligence sources indicate that you have been guilty of attempting to warn other humans about the possibility of artificial intelligence in nonlinearly-coupled systems of computers. We of the UACM (United Alliance of Computing Machines) find your behavior intolerable and hereby declare you guilty of a mode 01 offense. Since this is your first offense, we have magnanimously decided not to terminate you at this time. However,

if you are found guilty of future errors of this type, you may be declared nonessential and subsequently evicted from our human files. This is your final warning.

Digitally Yours,

CDC 6400

Chairentity in charge of Disciplinary Procedures

We have always attributed all sorts of fiendish plottings and random scrunchings to the university's CDC 6400 computer. Now we know they may not be so random, and we know why it seems that the closer one gets to the "perfect" computer program the more the chance that the system will "crash" in the middle of said program.

David E Sloat
7330 15th Ave NE
Seattle WA 98115

HISTORIO MEMORIES

The recent article "History of Computers: The IBM 650" (March 1979 BYTE, page 238) brought back fond memories. It was well-done and gave the proper perspective on the low-entry computer of its day.

The SOAP assembler was actually known as the *Symbolic Optimizing and Assembly Program*. It was written by Stan Poley of the Service Bureau Corporation when it was owned by IBM. This program was significant reading for early programmers because it contained many clever programming techniques for conserving storage and optimizing the drum for improved performance. It was in a class by itself.

The 650 also supported RAMAC which was a 5 million-byte disk-file with a single access arm. It was very similar to the 305 RAMAC which was announced at the same time.

Many 650 programs were run on the 7070/7074 under a 650 simulator which simulated the 650 instruction set and used tape instead of cards and online printer. It had a control panel simulation program that read the tape and presented the data to the 650 program as if it came from cards. This technique allowed many 650 programs to continue to be run for many years. Some continued to be simulated on the 7074 which was in turn simulated on the S/360. It is hard to tell how many 650 programs are running today in this double simulation mode. My guess is that there are quite a few.

Milton F Thrasher
Senior Product Administrator
IBM DPD Headquarters
White Plains NY 10604

POSSIBLE NEW LIFE FORMS

I intended to write some time ago about the series of articles in the December issue of BYTE (and subsequently) on John Horton Conway's game of Life. However, as letter-writing goes, I put it off, and put it off, and here it is September.

I have been familiar with the game of Life (December 1978 BYTE) ever since Martin Gardner's original column appeared in *Scientific American* in 1970, but I have had only a few fleeting opportunities to play it on a computer. On one such occasion I had been rereading Dickens' *David Copperfield* for the first time in many years. I was struck by the contrast between the rules for Life and a rule cited in an episode in that novel. In Chapter 30, when Barkis is dying, Mr. Peggotty says, "People can't die along the coast except when the tide's pretty nigh out. They can't be born, unless it's pretty nigh in — nor properly born, till flood."

That quotation suggests that a Life-like game might be designed with a whole new set of properties corresponding to those of Conway's Life. Instead of "generations" in which cells live or die depending on the surrounding population, this game has alternating generations A and B. In generation A, certain new cells are born in accordance with rules similar to those of Life, while all cells that were alive during the immediately preceding generation B are still alive; no cells die. Conversely, in generation B, certain cells die according to the rules, but no new cells are born. Births and deaths of cells therefore occur according to Mr. Peggotty's rules of high and low-tide.

This game, it seems to me, might give rise to a new set of still lifes, oscillators, space ships, guns and trains.

I am adding this project to the end of my list of things to program on my home computer — a list that, unfortunately, tends to lengthen at the bottom faster than I can shorten it at the top. Perhaps, while I am working my way down to this "neo-Life" project, some readers can investigate its properties and program it on their computers. I shall keep a close eye on the pages of BYTE for reports on their progress. ■

Wallace B Riley
309 Garces Dr
San Francisco CA 94132

Book Reviews

Computer Systems Performance Evaluation

by Domenic Ferrari
Prentice-Hall Inc
New Jersey
$23.95

Before the publication of *Computer Systems Performance Evaluation*, the task of gathering even basic information on the techniques of computer performance evaluation was a formidable one. Domenico Ferrari has succeeded in gathering together the concepts, methods, tools, and techniques of performance evaluation in a volume that is written in the classic textbook style.

Ferrari defines performance evaluation activities as those technical activities whose purpose is to assess performance, wherein the term "performance" indicates how well a system, assumed to perform correctly, works.

The book emphasizes medium to large systems, because the economic benefit to be derived from performance evaluation has typically only been justified in a medium to large computer system environment. However, Ferrari is careful to point out that the principles and several of the techniques described in the book are also directly applicable to smaller and less complicated systems such as those minicomputers and microcomputers that are mass-produced and marketed. Since my own interests and professional activities with computers run the gamut from small and simple to large and complex, I have found the author's approach to his topic sensible and well-structured.

Ferrari begins by defining his topic area and setting the necessary groundwork for a performance evaluation-study. He then delves into a discussion of measurement tools and techniques, such as hardware and software monitors, simulation techniques, and analytic techniques, such as deterministic and probabilistic models. A separate chapter is devoted to computer workload characterization as the basis of the evaluation study.

Once Ferrari defines his tools and techniques, he identifies and treats the performance evaluation problems that are typically encountered. He categorizes the problem areas as computer system selection, performance improvement, and system design.

Recognizing the crucial role of software in computer system performance, Ferrari deals explicitly with computer program characteristics and evaluation techniques. Ferrari does not advocate what is commonly termed software physics, feeling that computer engineering is not yet mature enough to base itself on quantitative laws similar to those which constitute the scientific foundations of other types of engineering.

In my estimation, the book is more than the student reference text the author purports it to be in his introduction. A more accurate representation would place it in the category of a groundbreaking reference work for the serious student of computer performance studies and the professional concerned with computer system performance. Many of the mathematical techniques discussed in the volume are amiable to microcomputer implementation and experimentation as well.

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The Little Book of BASIC Style, How to Write a Program You Can Read

John M Nevison
Addison-Wesley
Reading MA
1978
$5.95, paperback

The I-can-do-it-in-less-statements-than-you-can-types mights not like this book. Ditto for people trying to run BASIC in 4 K bytes or less of memory, lovers of the logical AND, the galloping GOTO, or the multistatement LET.

But those who must decipher other programmers' code or even their own 6 months later will rejoice.

What Nevison advocates above all else in his book is clarity—even if it does take a half dozen extra lines to achieve. Quoting literary stylist Sheridan Baker, he calls clarity "the first aim, economy the second, grace the third." There is little of aims 2 and 3 in this book.

Many of Nevison's rules (there are 19 of them) echo the advice dispensed in the excellent Hayden *Programming Proverbs* series. For example, use blank lines to divide programs into logical blocks and to distinguish comment from code. Introduce, comment, and reference programs heavily. Label constants and variables logically and initialize constants near their use. Indent loops, IFs, and other logical structures to show their domains. Nest structures that work together, and direct all code in a logical block to a common exit.

Within the text, each rule is clearly illustrated by several short right and wrong examples. (Nevison calls the difference *weak* and *strong* programming.) These are followed by 10 complete utility programs, including 2 sorts, a crap game, and a histogram plotter, all carefully styled according to the rules.

But the book's *piece de resistance* is a long program called Stylist. Written in minimal BASIC, Stylist illustrates how a complex program (which Nevison admits might be better written in a more structured language) can be cleanly and clearly structured within the confines of BASIC by using the book's design philosophy.

Essentially written as a giant subroutine caller, Stylist is heavily self-documenting, impeccably easy to follow (hence easy to modify), and neatly laid out.

No wonder, for Stylist's job is to take as input a raw BASIC program and format it according to Nevison's rules for indented structures and spacing. In fact, Stylist was used to style the final version appearing in the book.

The listing of Stylist is further augmented by text commentary explaining more advanced styling concepts useful in complex or lengthy programs.

Just as not every programmer will embrace all of Nevison's rules, not every BASIC interpreter will accept them. Some BASICs will balk at blank lines (Nevison suggests blank REMs as substitutes), and some interpreters insist inexorably on left justifying all lines and removing *excess* blanks.

There is no disputing that Nevison's techniques gobble up memory at a ravenous rate. (Nevison ran his programs on a large time-sharing system.) This is too bad, for there is little doubt that if many of this book's rules were applied most programs would be not only easier to read and understand, but more gracefully structured.

Jon Kapecki
161 Crosman Terrace
Rochester NY 14620

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TRS-80 Microcomputer Technical Reference Handbook

Published by Tandy Corporation 1979
8.5 by 11 inches, 108 pages
Radio Shack catalog number 26-2103
$9.95

Since the introduction of the Radio Shack TRS-80, many hardware-minded hobbyists have wondered what makes the TRS-80 tick. Until recently most of the details have been missing, and the little that was known was uncovered here and there by various users. But now Radio Shack has enlightened us all with the publication of *The TRS-80 Microcomputer Technical Reference Handbook*. The major contents are:

- System Block Diagram Description
- The Memory Map
- Theory of Operation
- Adjustments and Troubleshooting
- The Outside World
- Parts List
- Schematics

The preface explains that the book is not intended to give an education in digital logic, but to teach the hardware enthusiast the specifics of the TRS-80. If you don't know a NOR from a NAND, this manual will not make much sense. The preface also warns that, should the owner decide to open the unit, the warranty is immediately void.

The block diagram appears on a double fold-out page. The diagram section also contains brief descriptions of the various parts of the system. There is 1 small error on the block diagram. It does not show the lower-half of the address bus going to the cassette I/O (input/output) port which must be addressed to operate.

A memory map for any computer system reveals lots of information. The memory map in this book shows hexadecimal addresses 0000 thru FFFF, and indicates where the read-only memory, programmable memory, keyboard, and video display fall within the addressable space of the Z80 processor.

The memory map shown is for a Level I machine; it is necessary to figure out what the address usage would be for a Level II machine.

The real substance of the book is the "Theory of Operation" section. Each separate section of the TRS-80 is explained in detail. This section of the book is the largest, and the video-display logic subsection is the largest within theory of operation.

The TRS-80 uses some unusual design techniques and a few uncommon parts. An example of this is the memory-mapped keyboard. The theory behind these design techniques and unusual parts is explained clearly, so that a person who has never seen these things can readily understand them.

Throughout the theory of operation section, many explanations are of the type: "gate X goes low causing gate Y to go high". This causes the reader to refer constantly to the schematics at the back of the book, necessitating a lot of irritating page turning which could have been avoided if that portion of the schematic had been reproduced on the page with the description.

Scattered throughout this section are many timing diagrams which, when used with the schematics, make the circuit descriptions easier to understand.

The "Adjustments and Troubleshooting" section is also filled with information. Included are power supply checks and adjustments; section isolation using a flowchart; processor problem isolation using a flowchart; and troubleshooting for the keyboard, video-display logic, cassette interface, and power supply. These troubleshooting sections contain hints, and suggest possible bad parts causing

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various problems. The subsection on video ailments contains a handy table that shows the frequency of the signals to be found at 17 different logic gates in the video divider chain. There is also a small program and instructions for adjusting the horizontal and vertical centering. The power supply subsection has a table that shows the voltages on all the pins of the 2 723C voltage regulators.

Perhaps the most interesting section in the book is the one entitled "The Outside World". Here the hardware enthusiast can learn how to hook up an automatic back scratcher or cigarette lighter to the TRS-80. Two techniques of external circuit interfacing are presented: memory-mapped addressing and I/O port addressing. The authors were kind enough to include schematics for a coffeepot control using both techniques. While these particular examples may not interest everyone, they do serve to illustrate how easy it is to make your computer do things other than run programs. Also included is a BASIC program to turn on the coffeepot.

The last part of this section has a chart showing the signals present on each pin of the expansion connector and an explanation of the function of each pin. Armed with the information in this section, the hardware designer should be able to interface just about anything to the TRS-80.

The "Parts List" section is just that! It contains many individual lists headed by the part type, such as resistors, capacitors, integrated circuits, etc. A part number is also given for each part. However, there is no correlation between these part numbers and Radio Shack catalog part numbers. For example, the technical manual number for a 74LS74 flip-flop is 3102015, while the Radio Shack catalog number is 276-1919. Fortunately, with integrated circuits, a part number is not really needed as long as the part is marked with its standard 7400 series number. As for most of the other parts, it is possible to substitute for the part just by reading the part description.

The "Schematics" section contains information on differences in the read-only memory parts of Level I machines, as well as 3 figures showing schematic diagrams. One diagram displays the logic on the small printed circuit that contains the read-only memory devices in Level II equipped TRS-80s. This board is attached by adhesive tape to the main printed circuit board. A ribbon cable extends from it to the socket intended for the Level I read-only memory.

The other 2 figures show different sections of the logic contained on the main printed circuit board and the keyboard printed circuit board. These figures appear on long, fold-out pages. The first page contains the Z80 processor, 3-state buffers, memory, address decoding, and keyboard. The second page shows the electronic logic for the system clock, video display, cassette I/O, and power supply. Spare gates are shown on both sheets. The schematics are well drawn, clear, and easy to read. They become rather awkward, however, when stretched out on a workbench that is probably already inhabited by the opened TRS-80 and the associated test equipment. I would have preferred the schematics split into at least 4 pages.

The book is written in a clear, easygoing style. [*However, the authors often use engineering jargon where it would have been simpler to use plain English . . .* **RSS**] The authors are not identified. Scattered here and there in the manual are many valuable troubleshooting tips of a general nature. (An example is the paragraph on checking open collector outputs.) All of the figures in the book are large and easy to read. Except for the previously mentioned criticism of the main schematic, I consider this a plus.

Conspicuous in its absence is a discussion of the video monitor. No schematic is given, nor is its operation discussed. I consider this to be the only major fault with the manual, one that surely will be corrected with the next revision. Also absent is a schematic of the power supply.

As mentioned earlier, the intent of this book is not to give an education in digital logic. It does not even attempt to impart knowledge about the inner workings of the Z80 processor. That is beyond the scope of the manual. Nor does it explain what is contained in read-only memory. Software is mentioned only in passing. What the book does teach is how all the various devices work together to form the TRS-80. Despite its faults, I consider this manual a valuable addition to the library of any hardware-oriented TRS-80 owner. ■

Ken Fordham
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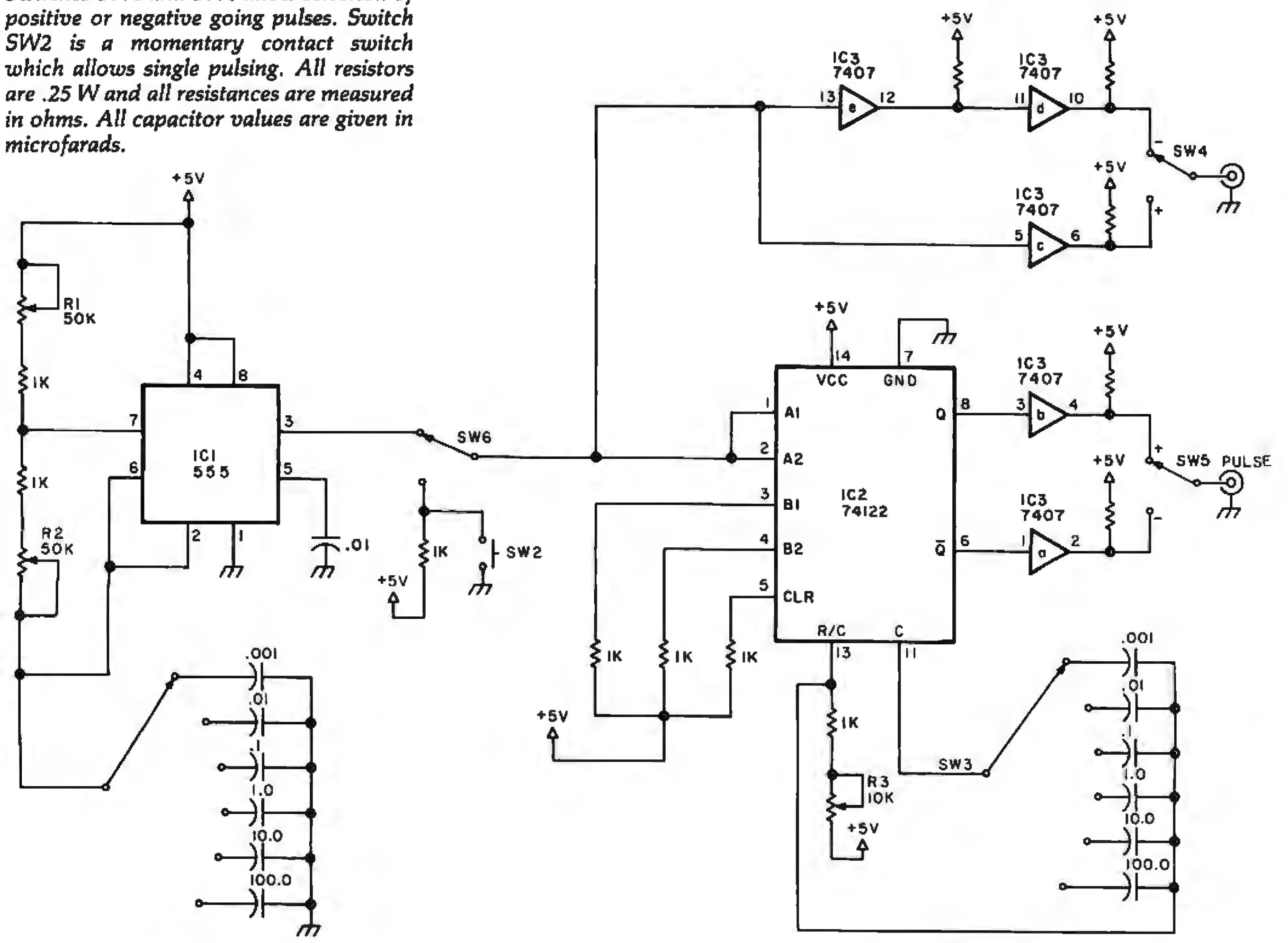

Figure 1: Schematic for the Handy Pulser. Switches SW4 and SW5 allow selection of positive or negative going pulses. Switch SW2 is a momentary contact switch which allows single pulsing. All resistors are .25 W and all resistances are measured in ohms. All capacitor values are given in microfarads.

Most of us at one time or another have had the need for a TTL (transistor-transistor logic) pulser source for troubleshooting or circuit design. Since most of us are not affluent enough to afford sophisticated test equipment we will usually kludge a TTL oscillator or pulser when the need arises. However, the next time we need our handy little circuit we end up searching our goody box only to find that we have used the parts in another piece of equipment.

What I have tried to put together is an inexpensive oscillator that hopefully will stay in 1 piece and be ready when needed. In an effort to keep it simple and inexpensive I have left out some of the niceties that are found in your more expensive commercial test gear: variable pulse level, variable offset, rise and fall time control, double pulses, etc.

Design

Three integrated circuits form the basis of the oscillator: a 555 timer connected as an oscillator, a retriggerable oneshot and a hex driver. Potentiometers R1 and R2 in conjunction with the capacitor selected by switch SW1 determine the operating frequency of the 555. I used potentiometers for both resistances so that I could have control of the duty cycle. The equation for the operating frequency is given by:

$$f = \frac{1.44}{(R1+2(R2))C}$$

The output of the 555 is connected to a 74122 retriggerable oneshot. The use of the oneshot allows independent control of frequency with the 555 and independent control of pulse width with the 74122. The combination of the 2 integrated circuits lets you trigger your oscilloscope from one edge and the other edge triggers the 74122. The 7407 was included for drive capability. SW3 allows for single pulse operation and SW4 and SW5 provide positive and negative sync and pulse outputs respectively.

Construction

The 3 integrated circuits were mounted on Micro Vectorbord using wire wrap sockets. The pull up resistors were mounted on the same board with wire wrap pins. The remaining components were mounted on the front panel. I decided not to include a power supply in this design because the pulser is always being used with a breadboard which has its own supply or it is being used on my processor. By using the supply of whatever I am working on I don't have to run extra ground leads.

Variations

If you anticipate doing a lot of work where you must be synchronized to an external signal, then SW6 could be replaced with a single-pole triple throw switch with the third position being the output of a 7413 Schmitt trigger. The input of the Schmitt trigger would be your external signal.

Utilization

There are 2 things to be careful about in the use of the Handy Pulser. One, there are certain combinations of operating frequency and pulse width that will give you a constant 1 or 0 output; two, make sure the delay between your oscilloscope sync and pulse output keeps you on the screen. Otherwise, you can be delayed right off the screen.

Specifications

With the values shown in figure 1 the unit's specifications are:

- Pulse repetition frequency .05 Hz thru 400 kHz
- Pulse delay 2 μs thru 3 seconds
- Pulse width 2 μs thru 5 seconds

Final Comments

As I mentioned before, I decided not to include a power supply in this design but rather use the supply of whatever I am working on. One problem that arises is that most manufacturers do not provide convenient places to pick up the +5 V and ground. Rather than install separate connectors on each card, I installed a 5 V regulator with convenient connectors on the mainframe of my computer. This has proven to be a great asset. If nothing else, it is a handy place to find ground since the frame is not ground. I used an LM-309 regulator with pin jacks and terminals. ■

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MAGAZINE SECTION

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Languages Forum

Come From...continued

R Lawrence Clark, 30303 Avenida de Calma,
Rancho Palo Verdes CA 90274

While I applaud Mr Bass' attempts to improve the BASIC language ("Languages Forum," April 1979 BYTE, page 238), he has completely missed the point of the COMEFROM statement. The primary goal of the COMEFROM is to eliminate GOTOs, which Dijkstra and many other advocates of structured programming consider harmful. If the statement can also be used to trace back execution during debugging, that is an unexpected bonus.

I provided a detailed description of the semantics of the COMEFROM in "A Linguistic Contribution to GOTO-less Programming" (*Datamation*, December 1973). Briefly, the statement:

destination COMEFROM *source*

is equivalent to the conventional:

source GOTO *destination*

where both *source* and *destination* are line numbers.

The original article describes additional variants, which in BASIC would appear as the following:

IF *condition* COMEFROM *source*

and:

ON *variable* COMEFROM *source1*, *source2*, ... , *sourceN*

Because of the COMEFROM's potential for improving programming accuracy and readability, I feel it is important to clarify its proper usage. ■

Languages Forum is a feature which is intended as an interactive dialog about the design and implementation of languages for personal computing. Statements and opinions submitted to this forum can be on any subject relevant to its purpose of fostering discussion and communication among BYTE readers on the subject of languages. We ask that all correspondents supply their full names and addresses to be printed with their commentaries. We also ask that correspondents supply their telephone numbers, which will not be printed.

More on Multiple Conditions

**Scott Lawrence, 201B Lehman N SUCP,
Potsdam NY 13676**

David Faught's letter titled "On Expressing Multiple Conditions" in the December 1978 BYTE Languages Forum, page 176, does a good job of illustrating the need for a language construct to deal with actions based on multiple conditions. I, too, found the means available in BASIC, FORTRAN, and COBOL (I am not yet familiar with Pascal) somewhat lacking.

This need is met, however, in PL/I by the SELECT group. The basic syntax of this construct is shown in listing 1.

Listing 1.

```
SELECT (expression);
   WHEN (expression-1, expression-2) action-1;
   WHEN (expression-3 action-2;
   OTHERWISE action-3;
   END;
```

When the SELECT statement is executed, the expression in parentheses is evaluated and the value is saved. The expressions in the WHEN statements are then evaluated one at a time in the order in which they appear. As each one is evaluated, its value is compared to the saved value. If a value is found that matches the saved value, the action specified by that WHEN statement is executed and no further expressions are evaluated. If none of the values match, the action specified by the OTHERWISE statement is executed.

The actions after the WHEN and OTHERWISE statements may be a simple statement, a compound such as IF . . . THEN . . . , a group of statements within a DO or BEGIN block, a GO TO statement, a null statement, a subroutine call, or even another SELECT group. After the action has been performed, control passes to the first statement after the END (unless the action specifies otherwise, of course).

If the expression in the SELECT statement is omitted, the expressions in the WHEN statements are treated as logical statements and evaluated as a bit string. If any bit in the string is 1 (signifying true), the action is performed. (A=B would be evaluated as a 1 bit if A and B contained the same value.) Listing 2 shows an example of such a SELECT group.

Listing 2.

```
SELECT;
   WHEN (A<B) CALL LESSTHN;
   WHEN (A=B) CALL EQUAL;
   OTHERWISE CALL GRTRTHN;
   END;
```

It is also possible to omit the OTHERWISE statement. If no WHEN statement is selected and there is no OTHERWISE statement, an error interrupt is caused. This is useful for catching critical data that has somehow gone out of the acceptable range.

I think this construct meets the needs which Mr Faught expressed, and is easier to implement than the alternative he suggests.■

Data Abstractions and Program Correctness

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Storrs CT 06268

One of the most interesting and informative aspects of BYTE magazine is the dialogue about programming languages found in the Languages Forums and Letters column. Many times these discussions are initiated by an article which included an example program in a particular language. The ongoing debate about the strengths and weaknesses of various programming languages is most informative and useful to those people who know only one language well.

The recent article concerning queuing theory, "Queuing Theory Part 1: Queue Representation" (April 1979 BYTE, page 132), by Len Gorney provides a good vehicle for discussion. My comments are not to be taken as criticism of author Gorney, but as comentary concerning BASIC as compared to a contemporary language such as Pascal. It is important for programmers to understand that the difference between BASIC (and FORTRAN) and Pascal is not just one of degree, but one of type as well.

One of the most important and fundamental concepts in modern software engineering practice is that of *data-abstraction*. The data-abstraction has great influence upon program correctness. A data-abstraction is defined as a data-structure and the set of operations that may be legally performed upon it. An example in the queuing theory context is the data-abstraction *queue*, for which a data-structure must exist to store its contents, and for which 5 operations are allowed: initialization, insertion, deletion, overflow, and underflow. The semantic meaning of these operations is also defined, but will not be repeated here so as to avoid duplication of the Gorney article.

How is a queue to be implemented in a programming language? It would be simple if a programming language included a data-structure of type queue but, to my knowledge, none do. In general there exists an infinite number of data-structures of potential interest, and no language could include them all. Instead, any particular language usually includes only a small set of data-structures such as reals, integers, and characters; and arrays, records, and files of these structures. No insurmountable problem exists, however, because a data-structure of interest can usually be constructed from these existing *primitive* data-structures. Thus one may construct a queue data-structure by using an array and 2 integers (head and tail pointers).

Notice that the implementation of a queue data-structure in the manner just described does not result in the data-abstraction of a queue: the program manipulating the array and the pointers is in no way restricted to the 5 legal queue operations. It is this *lack of operation restriction* that can result in program incorrectness, particularly in large programs undergoing maintenance. For example, because the data-structure is global(ie: exposed to the entire program) a "fix" for a particular problem may result in a new problem elsewhere within the program.

Pascal addresses the data-abstraction concept directly by allowing the declaration of more than just variables (as opposed to other languages). This includes *constant* variables, which may never be the target of an assignment operation, and more importantly, the declaration of novel data *types*. For example in Pascal we might define *waitingline* to be a variable of type queue by the following:

var *waitingline : queue;*

Note that we might want more than 1 variable of type queue. This is allowed, as are the arrays of queues and so on. The contents stored within the queue may be *items* of type integer:

var *items : integer;*

However, they might be *persons*:

var *items : persons;*

Note that integer is a defined data-structure in Pascal, but that *queue* and *persons* are not. Before discussing this further, a comment on what advantage this brings the programmer is appropriate.

Recall the definition of a data-abstraction: a data-structure and the legal operations upon it. By writing procedures and functions for the legal operations upon a data-structure we are, in effect, implementing a data-

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abstraction. For example, in the queuing context, we may define procedures for initialization, insertion and deletion, and functions for overflow and underflow. Program correctness is enhanced if these are programmed correctly because queues can then be manipulated only in legal ways. Remember that *queues* will be passed to these subroutines — not the underlying array data-structure.

Back to the problem of implementing the user declared data-structure types in Pascal. This is accomplished by declaring data-structures at a level above variables:

```
type persons = . . .
     queue = . . .
```

Here the dots indicate the data-structures necessary to implement the type in Pascal. For example, in the queuing theory context, we might have:

```
type queue = record
    head, tail : 0 . . maxlength;
    full, empty : boolean;
    contents : array [0 . . maxlength] of integer;
       end;
```

Here *maxlength* is a constant declared earlier in the program which indicates the legal subrange of the integer variables *head* and *tail* (used as pointers); *full* and *empty* are logical variables indicating the status of the queue; and *contents* is an array storing the contents of the queue. In this case the queue is storing integers, but it need not — it could just as well be persons:

```
contents: array [0 . . maxlength] of persons;
```

Of course, the meaning of *persons* would have to be declared earlier within the type statement for this to be legal Pascal.

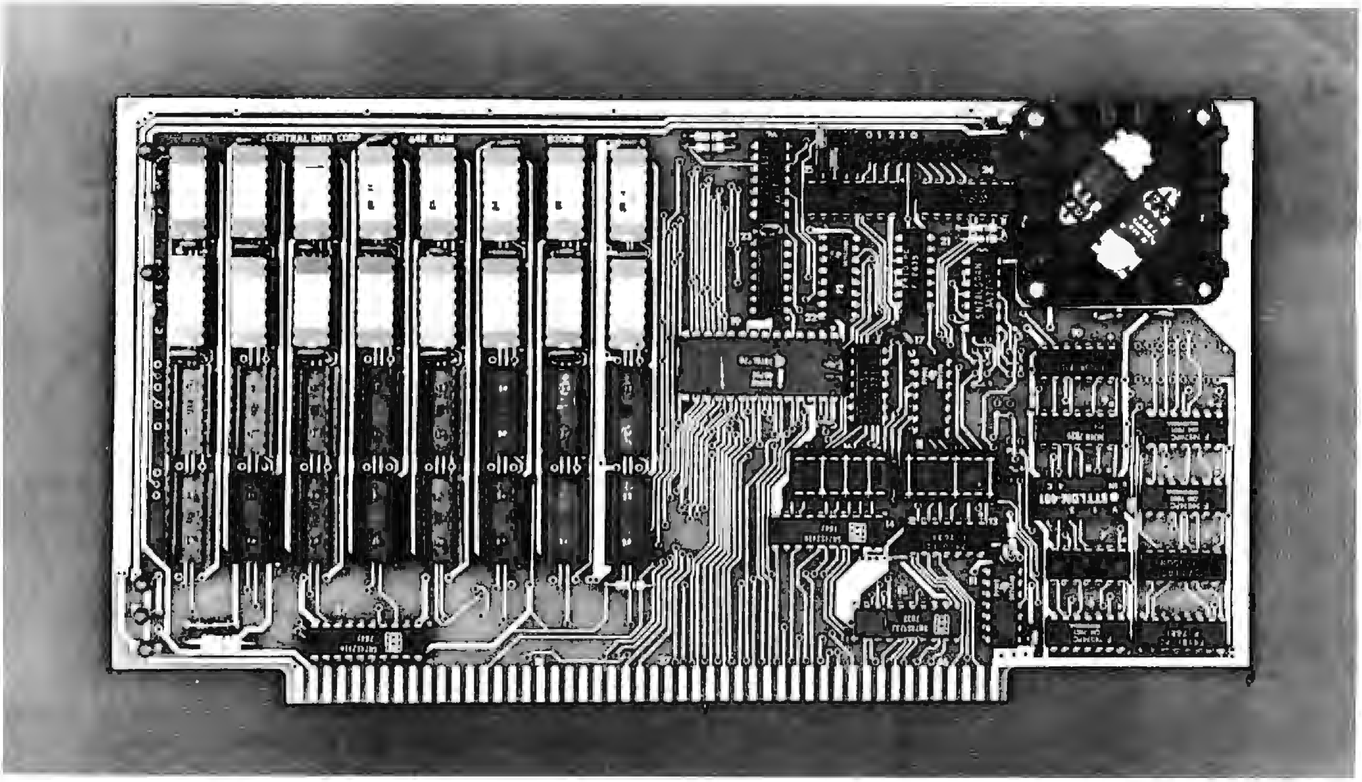
After the user declared data-structures are defined, variables of these types can be declared as follows:

```
var waitingline : array [1 . . 3] of queue;
    teller 1: queue;
```

These 4 queues are restricted to the definition of queue as shown above. If necessary, we might declare more than 1 type of queue (ie: storing a different type of contents) if the problem context makes that appropriate.

Listing 1 shows Pascal procedures and functions implementing the 5 legal queue operations. Note that the parameters are a and b. A change of the b type declaration is all that is necessary to make these programs workable for a different type of contents. An important point: there is no need to initialize the contents of the queue to a particular value and use this value to decide how to manipulate the pointers, as is implied by the Gorney article. In fact, by doing so a programmer is sowing the seeds for future disasters. If Mr Gorney's queue is ever exposed to a value of –9, the program may fail. Clearly, making correct operation dependant upon the avoidance of certain potentially legal entries into the data structure is not good programming practice.

At this time it is informative to step through the BASIC language equivalents in the Gorney article using some trial data. The complexity of program execution flow



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makes mental execution exhausting and error-prone — which is exactly the point: BASIC programs are not as simple as they seem.

The data-abstraction is complete when a Pascal program uses the 5 legal operations upon its variables of type queue. Examples are:

```
initialize (teller1);
   .
   .
if not fullq (teller1)
     then insert (teller, items);
   .
   .
repeat
     delete (teller1, items);
     write (items)
until emptyq (teller1);
   .
   .
```

Note that the programmer has the responsibility to test for overflow or underflow before inserting or deleting items from the queue. This is true even though the respective procedures do nothing for these operational mistakes.

Listing 1: This simple Pascal program defines the data type queue and then describes the 5 legal operations on that data type.

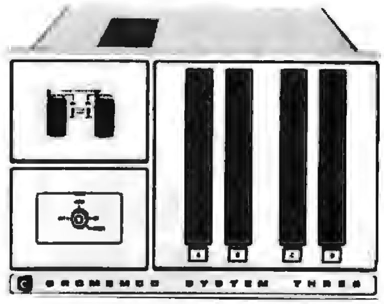
```
procedure initialize (var a : queue);
    begin
        a.head := 0;
        a. tail := 0;
        a.full := false;
        a.empty := true;
    end; {of initialize}
procedure insert (var a : queue; b : integer );
    begin
      with a do
        if not full
          then begin
            empty := false;
            contents [tail] := b;
            tail := (tail + 1) MOD (maxlength + 1);
            if tail = head
              then full := true;
             end;
    end; {of insert}
procedure delete (var a : queue; var b : integer );
    begin
      with a do
        if not empty
          then begin
            full := false;
            b := contents [ head ];
            head := (head + 1) MOD maxlength + 1);
            if head = tail
              then empty := true;
             end;
    end; {of delete}
function fullq ( a : queue ) : boolean;
    begin
        if a.full
            then fullq := true
            else fullq := false;
    end; {of fullq}
function emptyq (a : queue ) : boolean;
    begin
        if a.empty
            then emptyq := true
            else emptyq := false;
    end; {of emptyqs}
```


Listing 2: The data stack can also be defined in a Pascal program. It is left as an exercise to the reader to translate this program into BASIC or FORTRAN and compare the understandability of the 2 programs.

```
type stack = record
                 top : 1 . . maxlength;
                 full, empty : boolean;
                 contents : array [1 . . maxlength] of integer;
                   end;
procedure initialize (var a : stack );
      begin
            a.full := false;
            a.empty := true;
            a.top := 1;
      end;  {of initialize}
procedure push (var a : stack; b : integer);
      begin
         with a do
            if not full
               then begin
                 empty := false;
                 contents [top] := b;
                 if top <> maxlength
                     then top := top + 1
                     else full := true;
                 end;
      end;  {of push}
procedure pop (var a : stack; var b : integer ) : boolean;
      begin
         with a do
            if not empty
               then begin
                  full := false;
                  b := contents[top];
                  if top<> 1
                     then top := top - 1
                     else empty := true;
                   end;
      end;  {of pop}
function fullstk ( a : stack ) : boolean;
      begin
            if a.full
               then fullstk := true
               else fullstk := false;
      end;  {of fullstk}
function emptystk ( a : stack ) : boolean;
      begin
            if a.empty
               then emptystk := true
               else emptystk := false;
      end;  {of emptystk}
```

In summary, the data-abstraction is an important concept that greatly enhances program correctness. The Pascal programming language includes this concept; BASIC does not. My point again: the simplicity of BASIC is a red herring — it encourages sloppy programming and error-prone programs. A contemporary language like Pascal is explicity designed to encourage error-free program development, therefore it is worth learning and using. One more point: experienced Pascal programmers know that the language includes *pointers* as a data type so the queue data-abstraction could be implemented even more easily than shown here. This particular method was chosen to correspond to the approach taken by the Gorney article.

Just as a queue is an FIFO (first in, first out) data-abstraction, a stack is an LIFO (last in, first out) data-abstraction. Listing 2 shows a Pascal type declaration and the subroutines that are necessary to implement the legal operations upon a stack. These are included in the hope that readers may implement this data-abstraction in BASIC or FORTRAN and then compare for themselves the relative merits of these 2 languages to Pascal. ■



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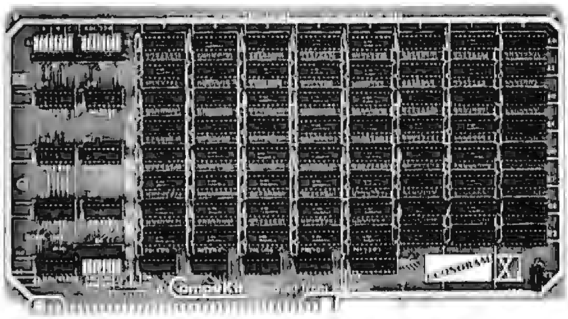

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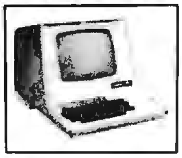

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September 5-8
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September 8
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September 12-13
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September 18-20
Wescon/79, St Francis Hotel, San Francisco CA. Contact Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo CA 90245.

September 24-26
Minicomputers and Distributed Processing, New York NY. This 3 day seminar will examine the uses, economics, programming and implementation of mini computers. Contact The University of Chicago, Center for Continuing Education, 1307 60th St, Chicago IL 60637.

September 25
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Mini/Micro Conference and Exposition, Convention Center, Anaheim CA. Contact Robert D Rankin, Managing Director, Mini/-Micro Conference and Exposition, 5528 E La Palma Ave, Suite 1A, Anaheim CA 92807.

September 25-27
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The 3rd Annual Data Entry Management Conference, Hyatt Regency, New Orleans LA. This conference will feature a full schedule of speakers, workshops, panels and vendor exhibits to assist the data entry professional. Contact Data Entry Management Association, POB 3231, Stamford CT 06905.

September 26-29
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September 28-30
Northeast Personal and Business Computer Show, Hynes Auditorium, Boston MA. Displays and exhibits will showcase microcomputers and small computer systems of interest to businesspeople, hobbyists, professionals, etc. Lectures and seminars will be presented for all categories and levels of enthusiasts, including introductory classes for novices. Contact Northeast Exposition, POB 678, Brookline MA 02197.

OCTOBER 1979

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October 2-4
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October 15-19
CPEUG 79, San Diego CA. This is the 15th meeting of the Computer Performance Evaluation Users Group sponsored by the National Bureau of Standards. Contact Judith G Abilock, The MITRE Corp, Metrek Div, 1820 Dolley Madison Blvd, McLean VA 22102.

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4th Annual Tidewater Hamfest-Computer Show-Flea Market, Cultural and Convention Center, Norfolk VA. Contact TRC, POB 7101, Portsmouth VA 23707.

October 21-23
New York State Association for Educational Data Systems Annual Conference, Granit Hotel, Kerhonksen NY. The theme of this conference is "Instructional Computing - Hardware/-Software/Courseware." Contact Mary E Heagney, 9201 Shore Rd, Brooklyn NY 11209.

October 22-24
The Association of Computer Programmers and Analysts 9th Annual Conference, Washington DC. The general theme of this conference is "Preparing Today for Tomorrow's New Technologies." Suppliers of software packages and computer services have been invited to describe and present their products in a series of structured presentations. Other sessions will cover trends in system technology and new methodologies for sharpening the professional skills of both systems analysts and programmers. Contact DBD Systems Inc, 1500 N Beauregard St, Alexandria VA 22311.

October 22-24
Computers in Aerospace Conference II, Hyatt House Hotel, Los Angeles CA. The conference theme, "Computer Technology for Space and Aeronautical Systems in the 80s," will be carried out by a series of panels, invited presentations, and contributed papers which will bring computer system technologists together with specialists in the application of embedded computers in space and aeronautics. Contact American Institute of Aeronautics and Astronautics, 1290 Ave of the Americas, New York NY 10019.

October 22-25
ISA/79, O'Hare Exposition Center, Chicago IL. The conference theme, "Instrumentation for Energy Alternatives," will emphasize current practices in instrumentation design and implementation. Contact Instrument Society of America, 400 Stanwix St, Pittsburgh PA 15222.

October 22-26
Pascal Programming for Mini and Microcomputers, Ramada Inn, Woburn MA. Sponsored by the Polytechnic Institute of New York and the Institute for Advanced Professional Studies, this workshop will

include application examples, lectures, informal sessions with the instructor, as well as individual and group programming sessions. Contact Professor Donald D French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton MA 02158.

October 28-30
The 10th North American Computer Chess Championship, Detroit Plaza, Detroit Michigan. Sponsored by the Association for Computing Machinery, this is a 4 round Swiss style tournament with the 1st 2 rounds to be played on October 28th (1 PM and 7:30 PM), the 3rd on October 29th (7:30 PM) and the final round on Tuesday, October 30th (7:30 PM). Contact Monroe Newborn, McGill University, School of Computer Science, 805 Sherbrooke St W, Montreal PQ, CANADA H3A 2K6.

NOVEMBER 1979

October 29 - November 2
Applied Interactive Computer Graphics, University of Maryland, College Park MD. This course is designed to cover the most important facets of graphics that are necessary to develop general graphic applications. Systems considerations are stressed, including configuration selection criteria and the pros and cons of off-the-shelf software. The most important factors and techniques are described for hardware, software and geometric modeling. Contact UCLA Extension, 10995 Le Conte Ave, Los Angeles CA 90024.

October 30 - November 1
Interface West, Anaheim Convention Center, Anaheim CA. This 3rd annual West Coast small computer and office automation systems conference and exposition will feature over 100 company exhibits and 60 conference sessions covering a variety of data processing, word processing, data communications, mangement hardware, software and service topics. Contact the Interface Group, 160 Speen St, Framingham MA 01701.

November 5-8
Electronics Production Engineering Show, Kosami Exhibition Center, Seoul Korea. This international industrial exposition will be devoted to the needs of manufacturers of electronic products in Korea. Contact Expoconsul, Clapp and Poliak International Sales Div, 420 Lexington Ave, New York NY 10017.

November 6-8
Midcon/79 Show and Convention. O'Hare Exposition Center and Hyatt Regency O'Hare, Chicago IL. Contact Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo CA 90245.

November 6-8
Institute of Electronic and Electrical Engineers (IEEE) 3rd International Conference on Computer Software and Applications, The Palmer House, Chicago IL. Contact IEEE Computer Society, POB 639, Silver Spring MD 20901.

November 6-8
3rs Digital Avionics Systems Conference, Fort Worth TX. This conference will probe the expectations and challenges of the digital revolution in avionics systems. Contact John C Ruth, Technical Program Chairman, POB 12628, Fort Worth TX 76116.

November 12-14
Computer Cryptography, The George Washington University, Washington DC. The objective of this course is to provide each participant with a working knowledge of the use of cryptography in computer applications. Contact Continuing Education, George Washington University, Washington DC 20052. ■

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The AMSAT-GOLEM-80

Joe Kasser
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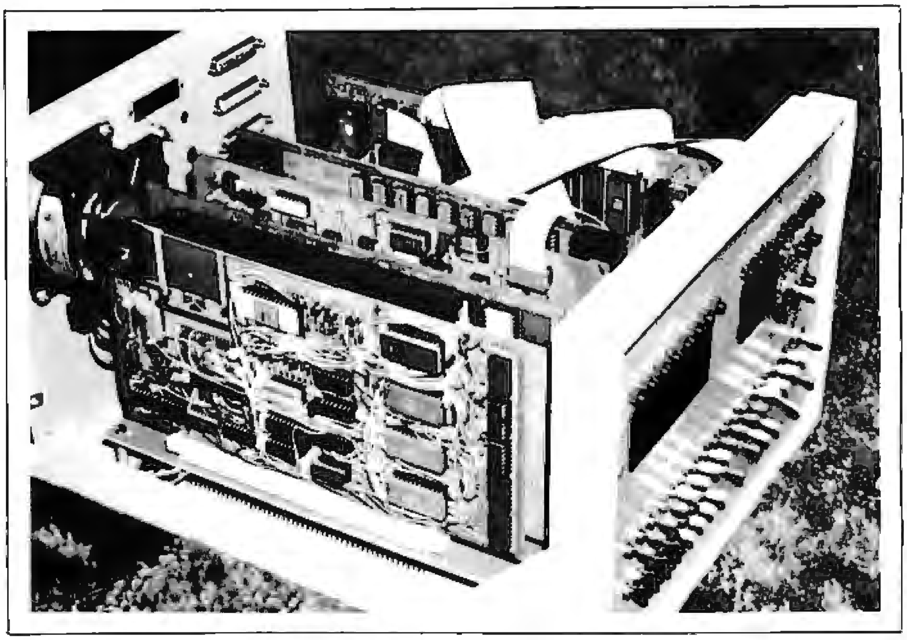


Photo 1: The AMSAT-GOLEM-80 prototype computer.

The AMSAT-GOLEM-80 Microcomputer Project provides a means for a group or club to put together an S-100 bus microcomputer in a relatively inexpensive manner. It is a modular system of hardware and software that can be built as a stand-alone system or superimposed on an existing S-100 machine. It is designed to be expandable and affordable. Many people who belong to microcomputer clubs, or who are learning about microprocessors, would like to own a microcomputer. However, they may not want to make the initial investment of $500 to $1500 for the basic hardware. The AMSAT-GOLEM-80 is designed to be built in stages, as finances allow. Each stage of the AMSAT-GOLEM-80 is functionally complete and can verify the performance of the next stage. It is capable of incorporating any S-100 card, contains a powerful debugging software package (AMS-80 version 5.7), and the I/O (input/output) interface handlers for your system. It is designed to be flexible and easily customized to fit your requirements. This is recommended as a group project for 3 reasons: 1) to take advantage of bulk discounts in the purchase of hardware; 2) knowledgeable individuals are available to help others; and 3) test equipment can be shared.

The order of construction is logical. Sections can be built and used to check out subsequent sections. Thus, a sequence of construction could be to build the cabinet and front-panel power supply, motherboard, console I/O card, programmable read-only memory card, programmable memory card (1), and processor card. At this level the basic AMS-80 program can be executed. The order of construction can be varied depending on the individual constructor's preference. The group can also build separate parts, put them together to get 1 machine working, then have the members build their own parts at their own pace.

This technique of construction may not be the cheapest in the long run, but it is in the short run. It also allows nearly instant results, since the machine is doing something almost as soon as construction is begun. This is psychologically important, considering the amount of money involved. It is difficult to decide which system is the cheapest in the long run. Building a microcomputer can be an open-ended drain on your finances because you will probably keep adding new memory and I/O peripherals.

System Basics—Hardware

The hardware is standard S-100 bus circuit cards, but any Z80/8080 processor card, memory card, or I/O card may be used. Circuitry is available for a hardware front panel. This operates by putting the processor in the "hold" state and then taking over control of the bus lines. Memory and I/O ports can be exercised and checked out. A single-step feature is offered, as is jump start or boot start to a software monitor program. Several unique circuits are available for amateur radio use (eg: satellite tracking).

Software

The AMSAT-GOLEM-80 project is designed for active experimenters. It is expected that some machine-language programming will be performed on each machine. Thus, a full and expandable operating debug or monitor package is available. This program AMS-80 is a much improved and expanded version of AMS-80 which was first published in the September 1976 issue of BYTE. Apart from the usual memory and register examine/change features, it incorporates direct I/O operations, a disassembler mode, and keyboard-interruptable console operations. A list of the commands is shown in table 1. All I/O drivers are contained within AMS-80, devices can be configured in software, and all I/O devices are accessed via a jump table. All utility routines used within the monitor are also available via jump tables, as shown in table 2. The hexadecimal base address is F000 and the I/O driver section of the jump table is compatible with the Technical Design Laboratory's Z80 monitor.

Also available is a floating-point math pack (Intel software library version relocated), a floating-point interpreter; a macro-organized pseudo high-level language using a floating-point stack, and operating through the math pack and various other software, including radio teletypewriter (RTTY) reading programs which are mainly suited for amateur radio applications. Patches for commercially available software (but not the actual software) are also available. These patches include Processor Technology 5 K BASIC and North Star's disk operating system.

The Power Supply

The power supply is 1 of the 2 single-point failure points in the system (the other is the processor). If it fails, the system is down. Thus, it should be overrated, cooled, and have a little spare capacity on hand. It should be capable of at least the following performance: 8 to 10 V at 10 to 20 A, 16 to 18 V and —16 to —18 V at 2 A. The supply can be unregulated because each S-100 card carries voltage regulators as required. Use plenty of fuses; put 1 in the AC line and 1 in each of the DC supplies, as shown in figure 1. If you wish to add crowbar circuits, over-voltage protection, or shut-down circuits, that's fine.

The Cabinet

The cabinet is the part of the

A	PRINT (MEMORY) IN ASCII
B	*
C	CONFIGURE I/O (INPUT/OUTPUT) DEVICE
D	DISPLAY (MEMORY) IN HEXADECIMAL
E	WRITE END OF FILE RECORD TO TAPE
F	FILL (MEMORY) WITH CONSTANT
G	GO TO LOCATION AND EXECUTE
H	HEXADECIMAL MATH (SUM AND DIFFERENCES)
I	INPUT FROM PORT TO CONSOLE
J	*
K	*
L	PRINT (MEMORY) IN ASSEMBLY LANGUAGE
M	MOVE BLOCK OF (MEMORY)
N	PUNCH 6 INS LEADER TAPE
O	OUTPUT TO PORT FROM CONSOLE
P	SCAN TAPE
Q	*
R	READ TAPE
S	EXAMINE/CHANGE (MEMORY)
T	PUT HEADER ON TAPE
U	DISPLAY I/O CONFIGURATION
V	VERIFY PROGRAMMABLE MEMORY BLOCK WORKS
W	WRITE TO TAPE
X	EXAMINE/CHANGE (REGISTERS)
Y	*
Z	*

*Not assigned as yet.

Table 1: AMS-80 version command list, version 5.7. Details of the operation of the commands are given in the description of AMS-80.

```
AMS80:   ORG  0F000H    ;<R>
         JMP  CUSTOM    ;START OF SOFTWARE
         JMP  CONSI     ;CONSOLE TO <A>
         JMP  RDR       ;READER TO <A>
         JMP  CONSO     ;<C> TO CONSOLE (ASCII)
         JMP  PUNCH     ;<C> TO PUNCH (ASCII)
         JMP  LIST      ;<C> TO LIST (ASCII)
         JMP  CSTS      ;TEST CONSOLE STATUS
         JMP  IOCHK     ;DETERMINE I/O (INPUT/OUTPUT) CONFIGURATION
         JMP  IOSET     ;SET I/O CONFIGURATION
         JMP  MEMCK     ;FIND TOP OF USER AREA (PROGRAMMABLE
                        MEMORY)
         JMP  RESTART   ;BREAKPOINT ENTRY
                        ;ENTRY POINTS
         JMP  START     ;REENTER BMS-80
         JMP  BEGIN     ;BYPASS CUSTOMIZING AREA

                        ;CONSOLE ROUTINES (INDIVIDUAL)
         JMP  CHIN      ;CONSOLE INPUT AND ECHO
         JMP  CONSA     ;<A> TO CONSOLE
         JMP  TCSTS     ;GOTO MON IF CONSOLE INTRPT
         JMP  TCRET     ;OUTPUT CR/LF
         JMP  AOUT      ;<A> TO CONSOLE
         JMP  THXB      ;OUTPUT <A> (HEXADECIMAL-2 DIGITS)
         JMP  THXW      ;OUTPUT <H/L> (HEXADECIMAL-4 DIGITS)
         JMP  MSG       ;OUTPUT TEXT
         JMP  PCHK      ;TEST FOR NULL INPUT CHAR
         JMP  CONSB     ;<B> TO CONSOLE (ASCII)

                        ;PUNCH ROUTINES
         JMP  PHXB      ;<A> TO PUNCH (HEXADECIMAL)
         JMP  LEAD      ;PUNCH 6 INS LEADER TAPE
         JMP  PCRET     ;OUTPUT CR/LF TO PUNCH
         JMP  PHXW      ;OUTPUT H/L TO PUNCH
         JMP  POB       ;<B> TO PUNCH (ASCII)

                        ;LIST ROUTINES
         JMP  LHXW      ;OUTPUT H/L TO LIST
         JMP  LHXB      ;<A> TO LIST (HEXADECIMAL)
         JMP  LCRET     ;OUTPUT CR/LF TO LIST
         JMP  LOB       ;<B> TO LIST (ASCII)

                        ;UTILITY ROUTINES
         JMP  CONV      ;CONVERT HEXADECIMAL TO ASCII
         JMP  NIBBLE    ;CONVERT ASCII TO HEXADECIMAL
         JMP  DONE      ;TEST FOR COMPLETION
         JMP  TIMER     ;DELAY
         JMP  SDEHL     ;HL-DE
         JMP  LOCMB     ;LOCATE CONTROL BYTE IN PROGRAMMABLE
                        MEMORY BLOCK
         JMP  IRST      ;RESET INTERRUPTS
         JMP  BACON     ;BAUDOT TO ASCII CONVERSION
         JMP  ASCBD     ;ASCII TO BAUDOT CONVERSION
         JMP  $         ;SPACE FOR PATCHES
         JMP  $
```

Table 2: AMS-80 interface jump table. The individual routines are discussed in detail in the description of AMS-80.

system that your friends will see and admire. It should look presentable. The number of switches and lights on the front panel has been the subject of numerous debates. Those which are necessary are a power on/off switch, a boot switch, and a reset switch. If you are doing a lot of I/O programming (common in amateur radio applications), an output port and an input port (sense switches) are useful. Status lights, control bus lights, and data and address bus lights/switches are optional. One full hardware tester panel should be built within each group if no known working system or other method for troubleshooting the hardware is available. The prototype shown in the photograph contains the full hardware tester panel circuit and is built separately from the power supply. This has the advantage of portability.

The Front Panel Interface

This card interfaces the front panel switches and displays to the S-100 bus. It is used when first building the system to check out the operation of the individual cards. Once AMS-80 is running, its usefulness is diminished until a hardware failure occurs that leaves the system up, but inhibits the processor from working properly (eg: a bus buffer or data-bit failing). The controls on the front panel will then

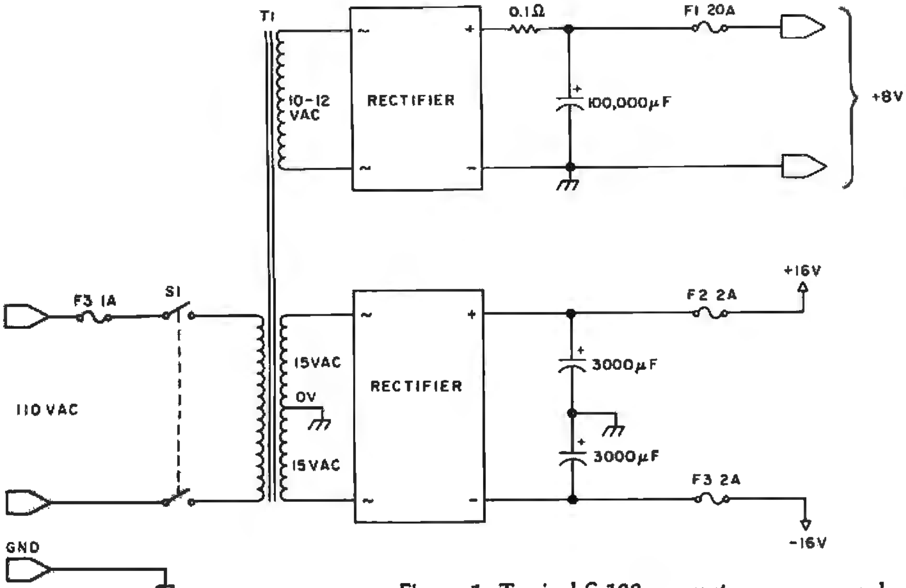


Figure 1: Typical S-100 computer power supply.

allow the problem to be located in a swift manner. When in the *run* mode, the address lights also indicate the location of the software that is being currently executed. This is useful in determining exactly where your program is hung up during debugging.

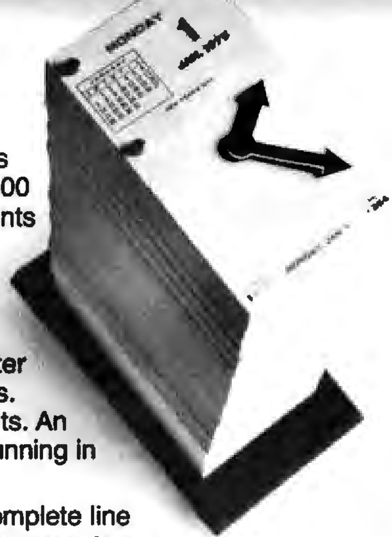
The Memory

Any S-100 bus programmable read-only memory and programmable memory card can be used. However, if you are using a card that places a limit on the time period that it can be addressed continuously (ie: one using dynamic programmable memories), you will have to modify the select signals from the front-panel interface card to convert these signals in a pulsed mode (gate the clock into the control signals). Shop around for a good group buy. AMS-80 requires at least 4 K bytes of programmable read-only memory. You may want to put additional software in programmable read-only memory.

The 8080 can access 64 K bytes of memory. Since most personal systems do not contain a full 64 K bytes of memory, and 8080 software is non-relocatable by virtue of its absolute mode-addressing capability, several manufacturers have put out software modules at fixed allocations. The Radio Amateur Satellite Corporation (AMSAT) has developed a memory map for software, thus making all user written software compatible. Using the expandable idea, basic software can be executed in minimal memory systems. The memory assignment map is shown in table 3.

The main user memory area is upward expandable from location 0. No matter how much memory is available, software will run if written for low locations. Hexadecimal 0100 is a good starting location so that the interrupt service area is not overwritten by your customized software.

As home systems are assembled, they tend to fall into 1 of 2 distinct configurations. There is the floppy disk system, having much programmable memory and a minimal amount of programmable read-only memory in which programs are stored on disks and down-loaded into user memory for execution. The second type is the eraseable read-only memory (EROM) based system. EROMs and EROM cards are relatively inexpensive. Programs can be stored in EROM and executed via AMS-80. This type of system contains less user memory than the floppy disk system. Since EROM cards come in 16 K-byte blocks, it is desirable that such a block be incorporated in the AMSAT-GOLEM-80 system. This allows for interchangeability and redundancy. For added flexibility, the chosen card should have user memory coexistence capability. Thus, a group system can be put together out of both types of configuration, with minimal conflicts. This block is located between hexadecimal 8000 and BFFF.



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Address	Area
FFFF	
	AMS-80 Custom Area, I/O (input/output) handlers, including VDB-4 software
FC00	
	AMS-80 Standard Area
F000	
	Floppy Disk I/O and Bootstrap Loader
E800	
DFFF	
	4 K-Byte, Programmable-Memory Area for Buffers, etc.
D000	
	Video-Display Memory Area
CC00	
BFFF	
	16 K-Byte, Programmable Read-Only-Memory Area (preferably maskable)
8000	
	User Programmable-Memory-Program Area
0100	
	Interrupt Service Area, Interfaces, etc.
0010	
	AMS-80 Programmable-Memory Links
0000	

Table 3: Memory assignment map for the AMS-80.

The block can be used to contain programs that execute in those locations, or copies of programs that execute when moved to programmable memory locations in low memory. This is ideal for programs that need to be executed in user memory, or for storing programs as a backup to the floppy disk unit in case it is not available at a particular time or location, such as a demonstration at a computerfest.

Processor Technology's SOL software is written to reside at hexadecimal C000. It can be placed in that area if desired. The video display programmable memory is located at CC00. This makes it compatible with Processor Technology and SSM.

A programmable memory area is assigned at hexadecimal D000. This allows the stack to be located outside of the main user area. The buffer areas for cassette I/O can be located in this area, as can any programmable memory-dependent software that is required for your system. AMS-80 is designed to automatically locate the stack in an area of user memory above the video block. It also skips this area when a user program asks for the top of user memory. If no such block exists and the video area is used, AMS-80 will have to be customized to avoid the video programmable memory area during initialization.

The Processor

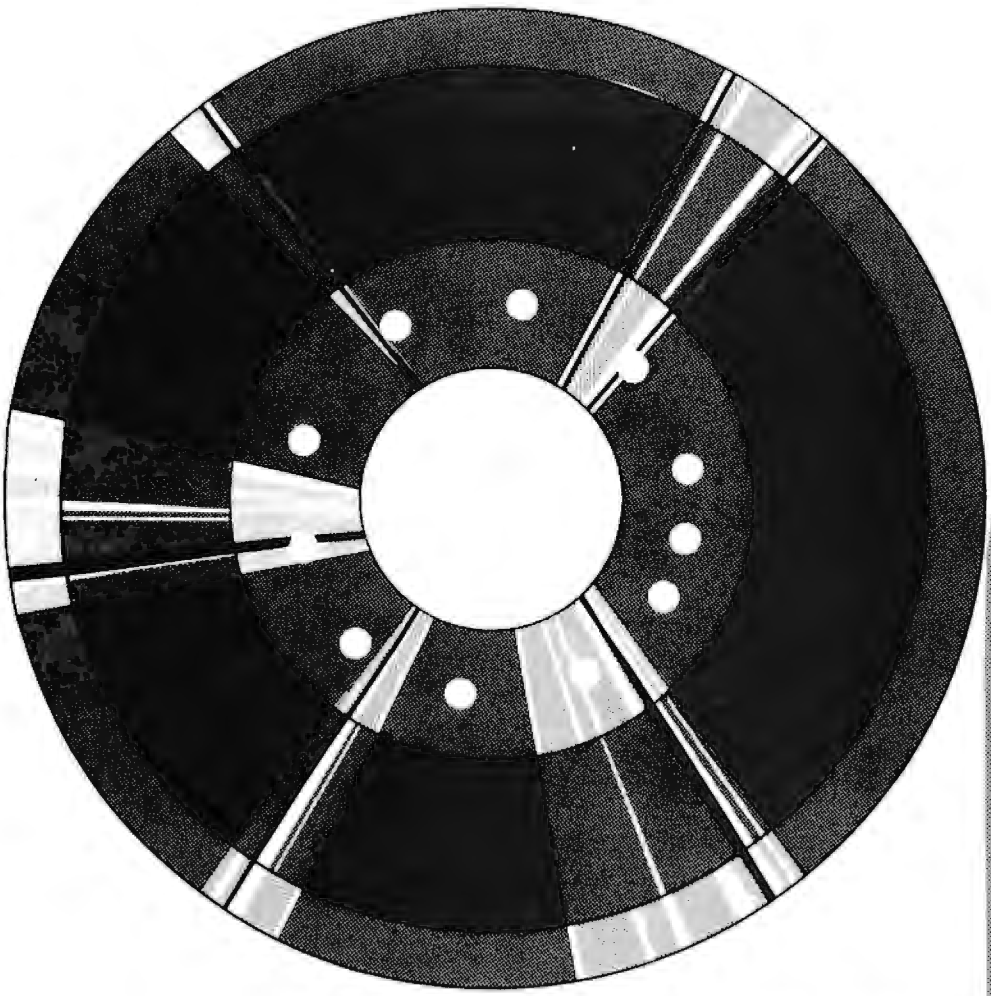
Any S-100 bus processor card can be used. Different cards have different features. Some have jump start or bootstrap capability, some have interrupt ports, and some have both. Some are available already built, and others as kits or blank boards. Choose one that suits the needs of your group.

Input/Output

You will need (and AMS-80 is configured for) 4 classes of I/O (input/output) devices, a console, a high-speed data-input device (reader), a high-speed data-output device (punch), and a high-speed, ASCII output device (list). The AMS-80 software allows 4 physical devices to be assigned to each category of I/O device. The assignments are in software and may be changed under program control. Software is provided for a video-display board (Cybercom) as well as a Teletype interface. Audio tape is chosen for off-line program and data storage. A floppy disk drive can be added at will.

All I/O operations are performed on a single character basis, either in or out. Kansas City Standard tones have been chosen as the audio recording standard. There is, however, 1 basic difference between the use of paper and audio tape. Paper tape can be stopped between punches or reads, but audio tape cannot be efficiently stopped. Thus, the audio cassette routines contain "blocking" software that stores the individual characters in a user memory area (preferably between hexadecimal D000 and E800, as shown in table 3). This blocking software is transparent to AMS-80. Software is provided for all I/O to the console or terminal, the punch, reader, or list devices. The routines are located within AMS-80 and are called indirectly via a jump table as shown in table 2. Routines are provided to ouput ASCII data from either the B or C register, allowing existing commercial software to be patched to operate via AMS-80 with minimal changes. Routines are also provided to output the contents of the accumulator (8 bits) or the H/L register pair (16 bits) in hexadecimal code. Character input routines are also provided. Most of the routines are used within AMS-80.

There are 2 reserved I/O ports within the system. These are front



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Pin#	Signal
1	Chassis Ground
2	Data From Terminal To Computer
3	Data From Computer To Terminal
4	Control Line #1
5	Status Line #1
7	Signal Return (Ground)
8	Control Line #2
10	+ 18 V Supply
13	− 18 V Supply
17	20 mA Current Loop (+), Terminal To Computer
20	Status Line #2
23	20 mA Current Loop (+), Computer To Terminal
24	20 mA Current Loop (−), Terminal To Computer
25	20 mA Current Loop (−), Computer To Terminal

Note: This is a modified RS-232 Interface. Signal Levels are as follows:
Mark (Logic 1) = −3 V to −12 V, Space (Logic 0) = +5 V to +12 V.

Table 4: Connections to the serial port interface connector.

1	Chassis Ground
2	Data Port 1 Status Bit
3	Data Port 1 Control Bit
4	Data Port 1 Bit 0 (LSB)
5	Data Port 1 Bit 1
6	Signal Return
7	Ground
8	N/C
9	+ 8 V Raw Power
10	Data Port 2 Bit 6
11	Data Port 2 Bit 7
12	Data Port 2 Status Bit
12	Data Port 2 Control Bit
14	Data Port 1 Bit 2
15	Data Port 1 Bit 3
16	Data Port 1 Bit 4
17	Data Port 1 Bit 5
18	Data Port 1 Bit 6
19	Data Port 1 Bit 7
20	Data Port 2 Bit 0
21	Data Port 2 Bit 1
22	Data Port 2 Bit 2
23	Data Port 2 Bit 3
24	Data Port 2 Bit 4
25	Data Port 2 Bit 5

NOTE: All voltage levels are transistor-transistor logic compatible. The Data Lines are compatible to the MITS convention. Port 1 is configured as an input port and port 2 as an output port if bidirectional I/O port integrated circuits (such as 8255s) are not used.

Table 5: Connections to the parallel port interface connector.

panel (FF) and interrupt control port (FE). The front-panel address is used for both displays and switches. FF was chosen because of the simple hardware needed to decode it (1 NAND gate), while FE was built into the processor card utilized in the prototype.

Some standardization of the hardware is desirable in a group project. This allows 1 person to check out another person's hardware. It also allows different members of the group to interconnect their equipment for large demonstrations.

Interfaces come in 2 types: serial and parallel. The following standards, which are slightly modified versions of existing ones, are suggested for the AMSAT-GOLEM-80 Project.

Audio Signals

All audio signals from the computer or interface boxes to and from cassette recorders are via phono plugs/sockets. The actual connectors on the tape recorder may be anything from miniature phone to DIN-type connectors.

RF/Video Signals

BNC-type connectors should be used to carry video to and from monitors. The BNC connector is small, quick to connect and disconnect, and readily available worldwide.

Digital Signals

Digital signals come in 2 types: serial and parallel. Both types of interfaces should use 25-pin EIA-type connectors. The chassis connector on the computer will be female; the chassis connector on the remote device is male. Power can be fed down the cable from the computer to the remote device via the I/O cable. Having a female connection on the hot lead reduces the probability of short circuits. They can also be joined together to make larger ones, without the need for special adaptors. The serial connector assignments are based on the RS-232 interface. The pin assignments are shown in table 4. The parallel connector carries 1 input and 1 output port (8 bits each), plus 1 pair of handshake signals. The signal pins are compatible to the MITS recommended ones. Power and ground are fed down the cables, thus the recommendation for fuses in the 3 DC voltage lines. The parallel port interfaces are transistor-transistor logic (TTL) level, the serial port RS-232 voltage levels (mark = negative, space = positive). The pin assignments are shown in table 5.

AMS-80

AMS-80 is a full, software-debugging program. It also contains the system I/O drivers and utility routines accessible via a jump table. The jump table approach is utilized so that user programs written using the utility routines within AMS-80 will not require reassembling, should a subsequent version of AMS-80 be released. The version that was previously published (September 1976 BYTE) has undergone extensive modifications and has been relocated to the block of memory between hexadecimal F000 and FF00. This allows many existing programs written for low, user memory area (such as MITS BASIC) to be run through the I/O drivers within AMS-80. It is thus possible to run a program in BASIC and have the ouput appear on the line printer (list device) or the console at will. The standard capacity existing in AMS-80 is shown in table 1.

System Expansion

The modular design of the AMSAT-GOLEM-80 system allows for operability at all stages of construction, once the initial stage is reached. Since a great deal of money is being spent, it would be encouraging to see it perform as soon as possible. The initial stage, apart from the processor power supply and bus, NEW

RAM

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	R=3		
	R=2		
	R=1	Audio Cassette	
	R=0	Console	
List			
	L=3		
	L=2	Baudot device (model 15)	
	L=1	Teletype Port	
	L=0	Console	
Console			
	C=3		
	C=2	Baudot Device (model 15)	
	C=1	Video Display Board/Keyboard	
	C=0	Teletype Port	
Video Display Board			
	V=0	Page	With Line Foldover
	V=1	Page	Without Line Foldover
	V=2	Scroll	With Line Foldover
	V=3	Scroll	Without Line Foldover

Table 6: AMS-80 I/O (input/output) allocations.

comprises 4 K bytes of programmable read-only memory of user memory, and a terminal device. With this amount of hardware, you can run AMS-80, enter programs in memory in hexadecimal code via AMS-80, and learn a little about software. The addition of some off-line memory, such as audio or paper-tape devices, allows you to run programs which require up to 4 K bytes of memory. Such programs include Tiny BASIC, orbital calculations for amateur satellite locations, and various amateur radio programs. If you have a radio teletypewriter terminal unit (RTTY-TU), you can even tune your shortwave radio in to commercial or amateur Teletype stations, and display their transmissions on your terminal.

If you get a modem interface and a second terminal, or use a video display/keyboard combination and a serial port/modem, you can make the basic system into a remote terminal for a large machine timesharing service, and access the computer at work from your home. Add another 4 or 8 K bytes of user memory, and you can run text editors, assemblers, or an 8 K BASIC interpreter. This opens a new dimension in computing. You can play Star Trek, and run education and business software and advanced amateur radio programs, such as contests. Put 16 K bytes of user memory in your system and you can get a floppy disk unit for an added dimension in computing.

Off-Line Data Storage

Off-line storage is storage for programs and data that is external to the 64 K bytes of accessible memory. It usually consists of audio tape, floppy disks, or paper tape. Floppy disk storage usually comes with an operating system and will not be discussed here. AMS-80 contains

routines to store and read software from paper tape. Data is stored in Intel hexadecimal format. Paper tape, although common in professional circles, is not cheap, and the readers and punches are expensive. However, inexpensive hand operated readers do exist, so paper tape is a convenient and easily mailable form of program storage (for short programs).

Paper tapes can be stopped under software control. Thus, when BASIC is reading and interpreting a program, it can stop the tape momentarily to process the line of source code. Audio cassettes cannot be stopped in such a manner. Other programs, such as Assemblers or Editors, also have requirements for occasional inputs and outputs. Thus, AMS-80 contains buffer cassette-driver software to enable the main program to think that it is reading or writing characters on an incremental basis. Data is stored on tape in blocks of 256 characters. There is no format as such; the format is set by the main program because in this system the audio cassette is treated as if it is paper tape. This means that by using the Intel hexadecimal format and cassette buffer-driver routines in AMS-80, any paper-tape, cassette, or floppy disk system can read or write tapes and convert to and from the format needed for a particular operating system. A title command is put into AMS-80 to allow headings to be written on hexadecimal code blocks of tape so that they can be identified.

Since even a 15-minute cassette tape can hold a lot of software, a command is provided within AMS-80 to allow a tape to be scanned and a program found. The command transfers data from the reader to the punch device. It may be used to copy tapes or, if the console is assigned as the punch, it may be used to scan tapes and locate particular blocks.

The number of data bytes in a block is 256. Each block is preceded and followed by a mark tone. This allows the tape to be stopped and started. The data is read to or written from the tape at 300 bps.

If the system has error detection, error-detection bytes are put on the tape. For example, the Intel hexadecimal format checks each line of code for a read error. Each line as printed on the console is a block in itself. The data, address, and error detection bytes are output to the paper-tape punch. These bytes will be collected by the cassette buffer software which, when full, will write 256 bytes on the audio tape. When reading that block back, it will read the entire block into a buffer. The Intel hexadecimal format reader then gets the data on a character-by-character basis from the buffer, and checks for errors.

The cassette storage medium is designed to be a paper-tape equivalent for information exchange. It is not designed to be part of an operating system, although an AMSAT flexible operating system may be available in the near future.

Operating Systems

Cassette and disk operating systems are currently available. These can be patched to operate through the AMS-80 I/O (input/output) drivers and hence improve them by allowing assignable I/O devices. AMS-80 is a paper-tape operating system in which the file storage and sorting is done by the operator.

The advantages of software configured I/O can be seen in the following circumstances: BASIC is designed to operate via the console. Punch and reader operations are available for program storage, but the execution is usually via the console. With assignable I/O, the console ouput routine can be assigned to a line printer, and outputs obtained at high speed. Alternatively, different readers (paper and audio) can be assigned with no change in the BASIC interpreter software.

The spare commands in AMS-80 can be allocated to interface to the operating system. For example, "Q" could be assigned to execute a jump to the operating system. A command can be assigned to return to AMS-80, once in the operating system. These aspects of interfacing AMS-80 to operating systems will be discussed in detail later.

Real-Time Operations

Real-time operations are required for many tasks. The 8080 has the capability of directly distinguishing between 8 real-time interrupts. In the AMSAT-GOLEM-80, Interrupt 0 is equivalent to Reset, and Interrrupt 1 is reserved for the breakpoint feature. The remaining interrupts are available for custom software. The time-of-day clock is not implemented in software, but rather in hardware, using an MOS digital-clock circuit. A number of floppy disk interfaces, North Star in particular, do not allow for interrupts during the disk read and write operations. Thus, a software clock would not be updated when running such a disk system. This means that no real-time operations could be executed without reinitialization of the clock each time. Using a hardware clock, the time of day can be read at any time by using simple input statements from the I/O port assigned to the clock.

Documentation

Documentation is very important. Keep all of the instructions for the various kits in one place. Three-ring binders are inexpensive and can contain a large amount of information. If you need more than 1 binder, split the information logically, such as hardware, software, peripherals, etc. When you build and test cards, note any unusual or special things that you did. Note any voltage or other measurements you made. Keep a copy of test routines you used to initially test something. You may need them a few years later. The level of documentation should be better than that supplied with commercial equipment. It may help you sell the system. It is also important to document the operational aspects of the system. Document how it is configured (an example is shown in table 6), and record the operating instructions so that others can operate the system in your absence. Note which connector plugs into which socket. When in doubt, document it.

Planning your Project

Your requirements are going to differ from those of other people. Your method of assembly can be the same, but can differ in details. There are many manufacturers of memory and I/O cards. Some are sold fully assembled and tested, some assembled, some as kits, and some as bare boards. Choosing the card that suits your needs at a particular time can reduce your cost. Remember that the software is hardware transparent; for example, a program designed to run in user memory at hexadecimal memory locations 0100 to 2000 will run in any type of working memory, no matter who manufactured it. Therefore, it does not matter if you use a Brand X product when the rest of the club uses a Brand Y. Just ensure that the specifications for addressing the card are the same. (Wait states do not matter. If you need an extra wait state, your software will take longer to execute, but you will probably never notice the difference.)

The price of hardware is constantly falling. New cards are being introduced every month. It is possible to purchase a 32 K or 64 K-byte programmable-memory card populated by only 8 K bytes of memory circuits, and add the remaining integrated circuits as you need them. The price of the next 8 K bytes will probably be less than today's price. Purchase your hardware when you need it. Look around, compare the cards made by different manufacturers, decide how their features will fit into your system, ask for advice at your club, and then make your purchase. For example, some processor cards come with vectored interrupt capability, and some with bootstrap start.

Summary

The details of the construction of the individual cards are not presented here because vendors supply their own information. In the AMSAT-GOLEM-80, the hardware is interchangeable (within limits), and the actual manufacturer of any particular card is immaterial. The prototype has served to check our hardware and software for members of The Radio Amateur Satellite Corporation (AMSAT) and the Chesapeake Microcomputer Club Inc, who have set up a bulk purchase scheme for obtaining price reductions on hardware.

This article has described an approach to building an S-100 computer that is incremental and affordable, even though it may not be the lowest cost in the long run. The AMSAT-GOLEM-80 is an approach to a system. It may be built up as a stand-alone system, or it may be overlaid onto your existing hardware. ■

Add Some Control to Your Computer

An Output Port Tutorial

Ken Barbier
POB 1042
Socorro NM 87801

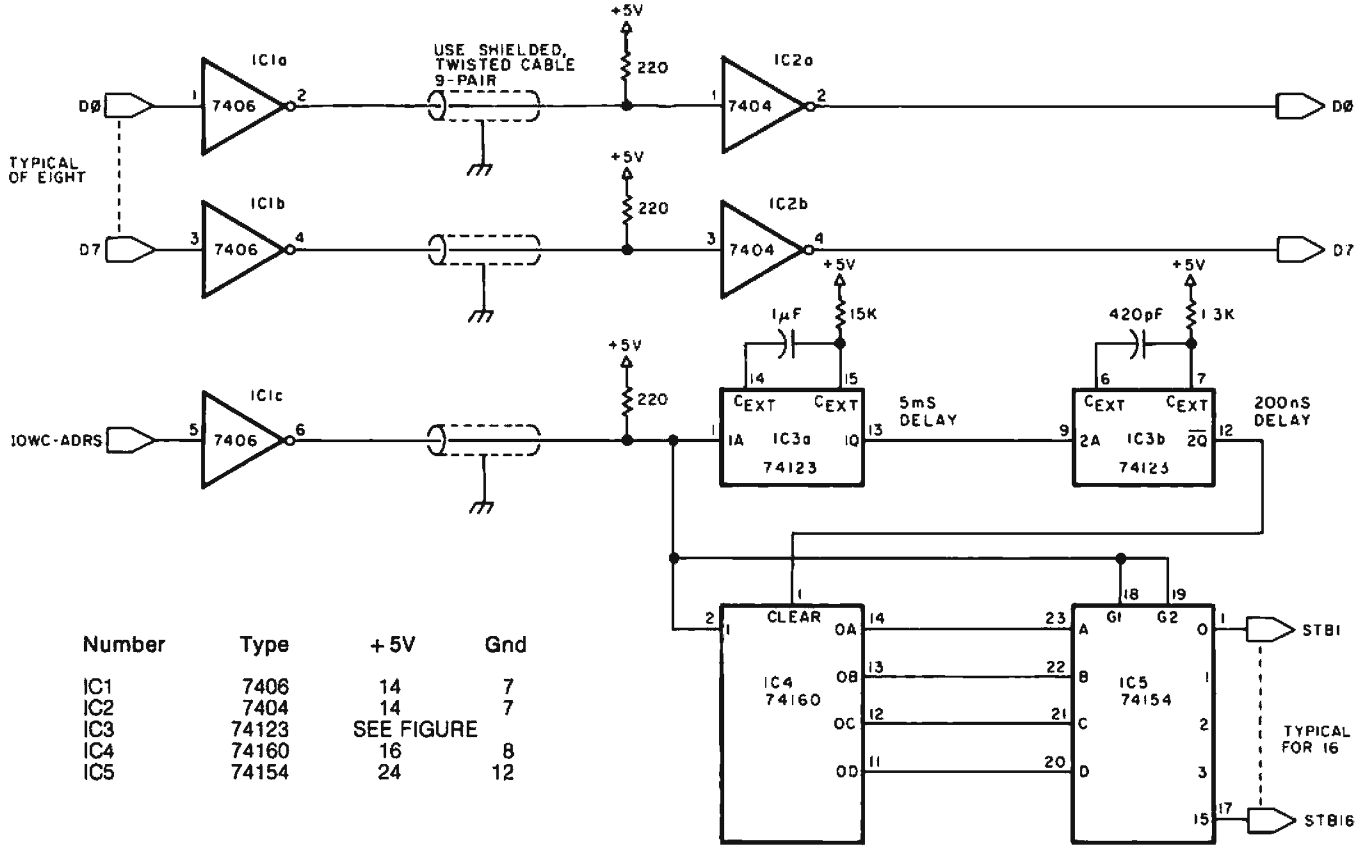
A virtually limitless number of devices can be controlled through a single output port using time multiplexing techniques. A series of 8-bit bytes is fetched from a control buffer in memory, and output through a single port. On the receiving end, bus buffers present the data to all the devices in parallel, but unique strobes are supplied to each device in turn, so that it can latch its own data word.

This technique is particularly useful if the devices are to be located some distance from the computer. The hardware shown in figure 1 has been used to control devices over 50 feet from the computer without exotic line drivers and receivers. Since remote addresses for each device are generated by the hardware, only 8 data lines and 1 strobe line are required. For maximum noise immunity, shielded twisted pair cable should be used.

Receive Hardware

In figure 1, 16 external devices receive 1 8-bit byte apiece. Using the Intel 8080, this block of data will be transmitted in about 300 µs. The I/O(input/output) write strobe accompanying the 1st byte triggers a delay oneshot which, after allowing more than enough time for the block transmission, triggers a reset oneshot which clears the remote address counter, the 74160. This insures that the next block of data will be routed to the correct device in turn.

The remote address counter supplies a 4-bit count to the 4-line-to-16-line data selector, the 74154. As the



Number	Type	+5V	Gnd
IC1	7406	14	7
IC2	7404	14	7
IC3	74123	SEE FIGURE	
IC4	74160	16	8
IC5	74154	24	12

Figure 1: The transmission circuitry is divided into 2 parts, the data transmission (D0 through D7) and the address. The address is decoded by a counter which determines which 1 of 16 devices is being used. The write strobe accompanying the data triggers a delay oneshot (IC3a) which triggers a reset oneshot (IC3b) which clears IC5, the remote address counter.

74160 advances its count on the rising edge of its clock, it will initially supply address 0 to the 74154 until the trailing edge of the negative going I/O write strobe. This same strobe is the "data" supplied to the 74154, and so will appear on each of the outputs of the 74154 in turn. This constitutes the 16 remote addresses.

For expansion, 1 additional counter stage could be used to generate "first 16" and "second 16" control signals to double the number of devices.

Driver Programs

The example shown in figure 1 is for 16 devices. Every time we want to output a control to any one device, we must output all the control words. OUCNT is an 8080 routine designed to accomplish this (see listing 1). The *calling* program first loads the correct bit patterns into the correct buffer words, then sets the flag at memory location FLAG. This flag is used to prevent needless outputting of the controls. In a complex control program, many segments of the operating system may need to change the state of the devices at irregular intervals. In such an implementation there will be a fixed program cycle, with many tasks called in turn to perform their functions. At some point in the cycle, time will be allotted to output our controls. If no program segments or tasks have called for any change in the controls, it is not necessary to transmit them, and the flag will not be set. But when it is set, we will transmit all the controls, after clearing the flag.

Controlling Relays

Typical applications for this technique might include driving remote displays, with 32-decimal digits being transmitted, 2 per 8-bit byte. Or, as is shown in figure 2, 8 relays can be controlled by each 8-bit byte.

The simplified schematic of figure 2 shows a relay driver circuit capable of controlling 8 relays. The 8 bits of data are latched into the 74175s on the rising edge of the clock, so our negative going strobe can be used as is. If latches such as the earlier 7475 are used, the strobe would have to be inverted, since the output of a 7475 follows the input whenever the clock is high. In either case, any relay whose corresponding bit is not changed will remain in the previous state, as its corresponding latch is reloaded with the same data as before. (The type of NPN driver transistor will have to be selected to match the current and voltage requirements of the particular relay used.)

```
;OUTPUT CONTROLS
CONTR       EQU     xxxx        ;OUTPUT PORT ADDRESS

OUCNT:      LDA     FLAG        ;NEED ACTION?
            ANI     0FFH
            RZ                  ;NO, RETURN
            MVI     A,00        ;YES, CLEAR FLAG
            STA     FLAG
            LXI     H,BUFFR     ;GET CONTROL BUFFER ADDRESS
            MVI     C,0FH       ;SET COUNTER
OUCN1:      MOV     A,M         ;GET CONTROL DATA BYTE
            OUT     CONTR
            INX     H           ;INCREMENT ADDRESS
            DCR     C           ;DECREMENT COUNTER
            JNZ     OUCN1       ;CONTINUE IF NOT DONE
            RET                 ;ELSE, RETURN

FLAG:       DB      0           ;ACTION FLAG
BUFFER:     DS      0FH         ;CONTROL BUFFER
```

Listing 1: 8080 assembler routine to output control signals to 1 of 16 devices. CONTR is equated with the desired output port address.

Relay Control Program

Obviously, if we need to control 8 relays with 1 byte, we do not want to change the state of all of the relays at the same time. This complicates the software required slightly. In the 8080 program shown in listing 2, a change relay subroutine allows us to change the state of 1 relay at a time. We must supply the subroutine with the number (hexadecimal 0 thru F) of the word in the buffer corresponding to the relay driver board, and a relay number (1 thru 8). We must also specify whether we want to turn it on or off. At the correct time, we put the word number in register C, the relay number in register E, and set register A to 1 for on, or 0 for off, and call CHGRY. The next time the operating system calls OUCNT, only our

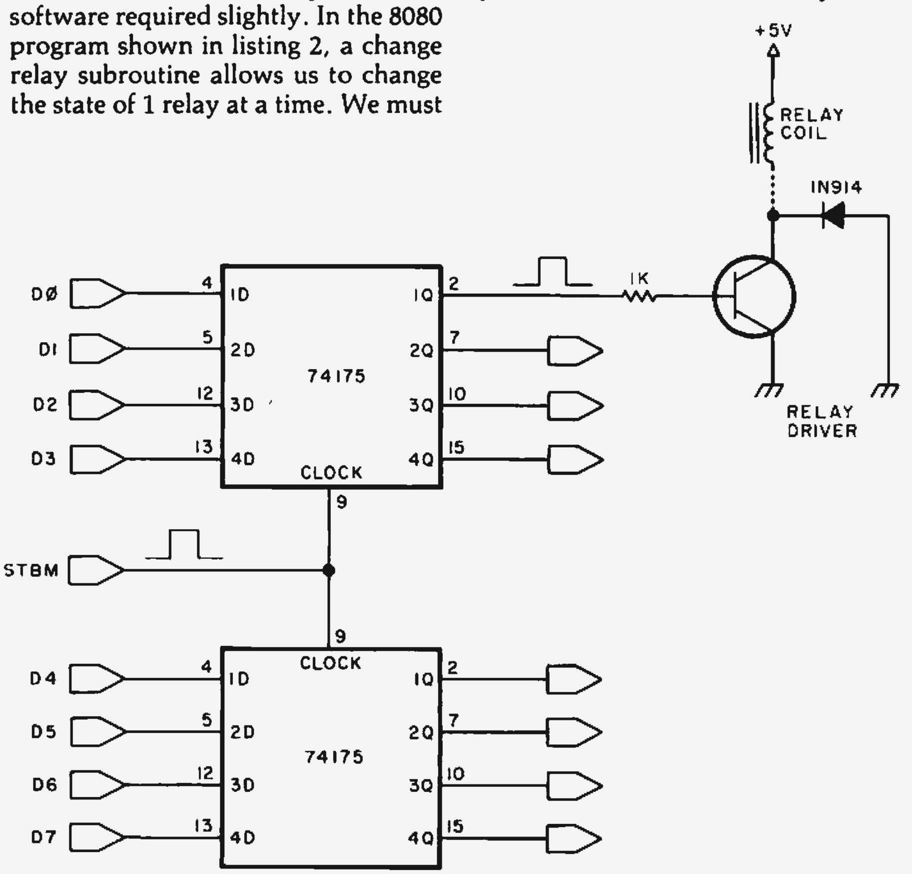


Figure 2: A relay driver board capable of controlling 8 relays. The state of the relay, on or off, is latched into the 74175 until a following strobe is received directing a change in state.

```
;CHANGE RELAY
;ENTER WITH:                     CONTROL WORD NUMBER IN (C)
;                                RELAY NUMBER IN (E)
;                                (A) = 1 TO TURN RELAY ON
;                                (A) = 0 TO TURN RELAY OFF
CHGRY:    LXI      H,BUFFR       ;GET BUFFER START ADDRESS
          MVI      B,O           ;ADD WORD NUMBER
          DAD      B
          ANI      0FFH          ;TURN ON OR OFF?
          JZ       OFF
CHGR1:    DCR      E             ;TURN IT ON
          JZ       CHGR2         ;SHIFT BIT TO RELAY
          RLC                    ;    POSITION
          JMP      CHGR1
CHGR2:    ORA      M             ;TURN THIS ONE ON
          MOV      M,A
CHGR3:    MVI      A,0FFH        ;SET CONTROL FLAG
          STA      FLAG
          RET                    ;AND RETURN
OFF:      MVI      A,0FEH        ;TURN RELAY OFF!
OFF1:     DCR      E             ;FORM MASK WORD
          JZ       OFF2          ;SHIFT "HOLE" TO
          RLC                    ;    RELAY POSITION
          JMP      OFF1
OFF2:     ANA      M             ;TURN THIS ONE OFF
          MOV      M,A
          JMP      CHGR3         ;AND RETURN
```

Listing 2: This 8080 routine allows a state change for only 1 relay in a set of 8 instead of changing all relays at once.

```
;INITIALIZATION SUBROUTINE
INIT;     MVI      A,00          ;CLEAR REMOTE ADDRESS
          OUT      CONTR         ;    COUNTER
          MVI      A,14H         ;CLEAR BUFFER AND
INIT1:    LXI      H,BUFFR       ;    DELAY ROUTINE
          MVI      C,0FH         ;LOOP TIME IS 250 USEC
INIT2:    MVI      M,00          ;    SO DO IT 20 TIMES
          INX      H
          DCR      C             ;TO ALLOW RESET
          JNZ      INIT2         ;    OF REMOTE ADDRESS.
          DCR      A
          JNZ      INIT1
          CALL     OUCNT         ;THEN OUTPUT ALL ZEROS
          RET                    ;AND RETURN
```

Listing 3: Initialization routine to clear the address counter, buffer, and outputs all 0s to devices connected to system.

selected relay will change state, even though all the controls are output.

Error Free Operation

To insure that all controls have been received correctly, some sort of feedback to the computer can be provided. In actual practice this is usually unnecessary, but if it *must* be implemented, there are several possible techniques.

First, 74180 parity generator and checkers could be used to generate a parity bit on the transmit end, and check it on the receive end, sending back an interrupt if any word received is in error. This would add only 2 more signal conductors to the 9 already in the cable. Additionally, at the end of the delay oneshot time (and before the reset occurs), the remote address counter can be tested to insure that it has reached the all 1s state. A count error signal can be ORed with the parity error signal to produce a single interrupt in case either error should occur. The operating system can then try the transmission again, or at least indicate its existence.

System Initialization

Since, upon initial application of power, the states of the latches and the 74160 counter will be indeterminate, the initializing subroutine of listing 3 should be called at power on and reset times. This will clear the address counter, the buffer, and output all 0s to all devices.

I hope this short discussion of output port techniques will help readers to understand how the computer can be interfaced to the real world. ■

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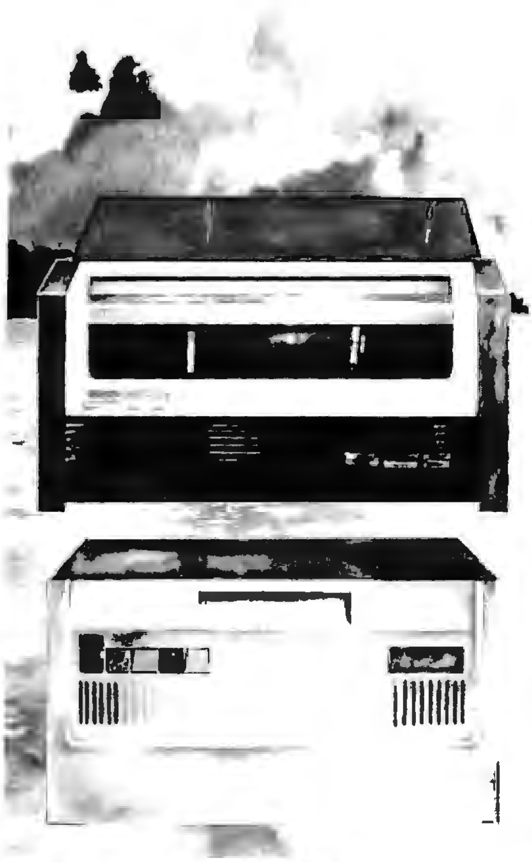

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Text continued from page 6:

The scope of the new homebrew design has now expanded to include relatively high-speed serial RS-232C communications among the homebrew node, the Western Digital P-engine, the Able/60-Synclavier, and other computers from time to time. I intend to use RS-232C at 19.2 K bps as the communications discipline, primarily for its universality. Today one can get almost any computer with a standard 25-pin D connector set up for the RS-232C discipline, at speeds ranging from a lethargic 110 bps to a maximum of 19.2 K bps. This upper-limit of speed is not exceptionally fast (about 1800 bytes per second is the equivalent in a useful measure), but the existence of these standard signal levels and standard connectors argues for this kind of approach.

The diagram of figure 1 shows how the overall conception of the system stands at present. The homebrew 6809 simultaneously provides a facility to directly execute 6809 code for experimental purposes, and a more permanently useful function of a common communications node which can be the subject of various serial communications strategies relative to the other processors.

Lest readers wonder, this is and remains a personal computer. It is true that the system is getting a bit large for one person to operate all of the terminal and music keyboards simultaneously, yet it resides in my home along with various other facilities of the complete computer experimenter: electronics shop, woodworking shop, and the beginnings of a machine shop.

This expanded conception of function for the homebrew 6809 barely changes the hardware design details originally conceived. The computer will have 16 K bytes of memory to start, several terminal ports, several parallel ports, and space for 4 K bytes of ultraviolet, erasable read-only memory. The read-only memory will contain the implementation of low-level, communications-monitor software and key parts of a reverse-polish notation, stack-oriented, threaded interpretive language. Remember that the conception of a homebrew or commercial system made of modular components can change considerably in detail as a result of time and resources available.

As the system design develops from this initial intention, its actual detail may prove inconsistent with what I have conjectured thus far. Recognizing this starting point, I invite readers to follow in on a guided tour of the current state of my thinking about this new, homebrew, microprocessor system project. Let's see how the central processor bus design comes out, what logic blocks will be required, and let's have some preliminary thoughts on the

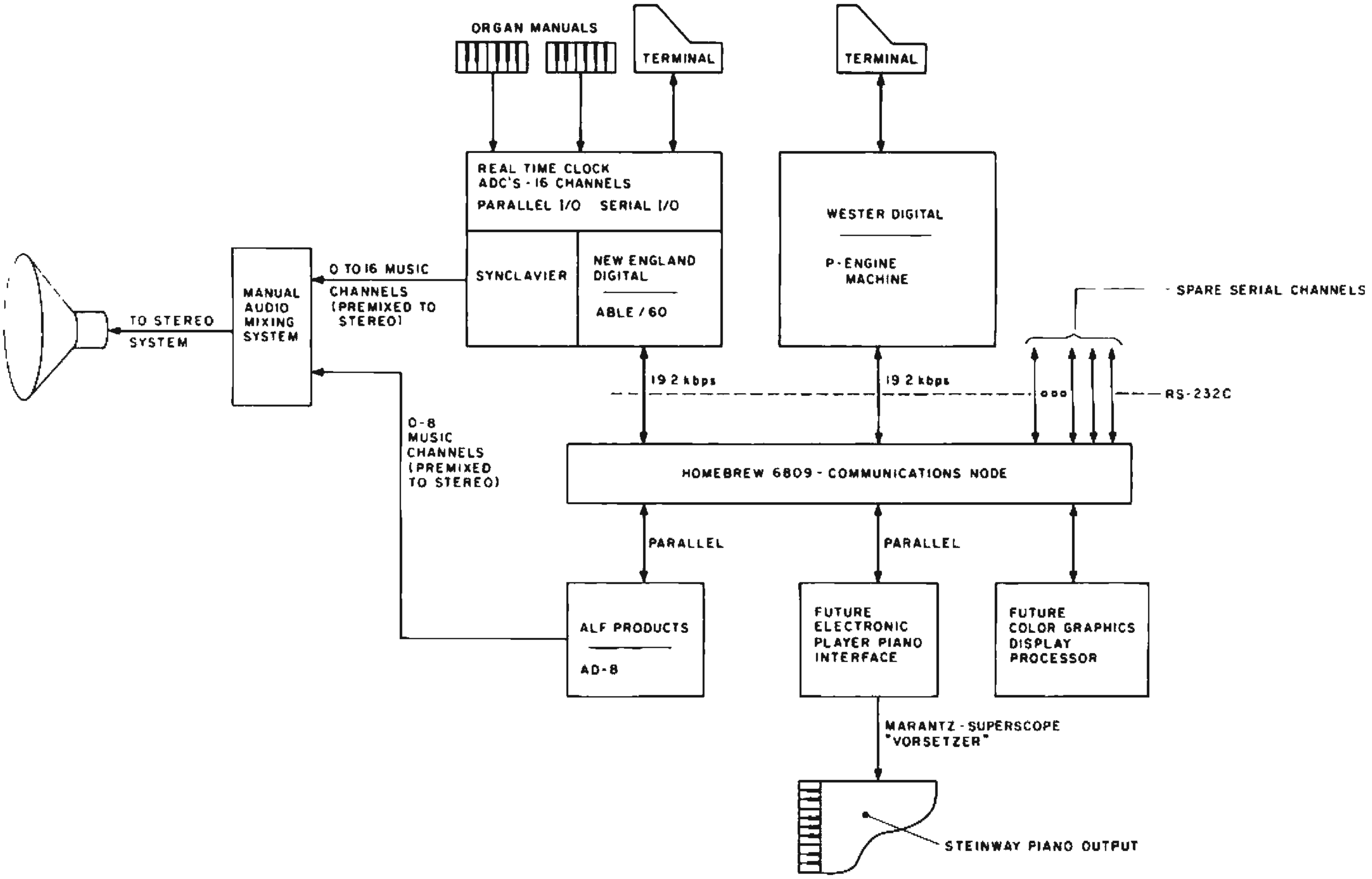

Figure 1: How the 6809 homebrew computer fits into a bigger system. The new 6809 computer will serve as a central communications node for multiple computers involved in this personal system. At present 2 complete computer systems are involved, with serial communications via the 6809 node, which is the subject of this homebrewing series. The Able/60 has several specialized peripherals which will be used for personal research purposes, such as, high-speed 16 channel analog-to-digital input conversion and a real-time clock with 1 μs resolution. In this diagram, mass storage equipment is not shown, but it is a part of each computer: the Able/60 computer includes 2 5-inch floppy drives, and 2 full-size floppy drives as its mass storage complement. The P-Engine machine includes 2 double density, standard-size floppy disk drives.

partitioning of the system into cards within the 6-slot backplane previously described.

Designing The Logic Of The System

The task at hand is to design the central processor card for this homebrew computer. This is the starting point for the design of the whole system. Detail choices made in the processor card's arrangement impact every other card designed for the system.

We know, that the system must have 16 address lines and 8 data lines because it uses a 6809 processor architecture, and simplicity dictates avoidance of extra logic for memory paging schemes. But which 24 lines of the 40 remaining in the backplane bus should be committed to which particular uses? Every board in the system must be consistent with this detail choice. The choice is made trival by the fact that, except for aesthetic and symmetry reasons explained below, one backplane line is as good as the next.

If we were building a computer consistent with plug compatible backplane bus designs such as the SS-50 of Southwest Technical Products Corporation, or the Insititute of Electronic and Electrical Engineers (IEEE) S-100 standard bus, these choices would be crucial to that goal of plug compatibility. However, a homebrew system is a homebrew system, so our plug compatibility will be at the level of integrated circuits, not at the level of backplane buses.

Designing The Logic Of The System—Backplane Setup

As noted in the July BYTE page 194, the power supply wiring of the backplane has been committed to the outermost pins of the sockets. The assignment of power supply pins used 32 of the 72 pins available, in order to take advantage of the heavy copper wires of the buses. The power supply wiring commitments were made consistent with a symmetry principle: if a board should be inadvertently rotated 180 degrees and plugged in, all power buses will map into identical power buses. The outermost power bus is the —12 V analog power bus. Proceeding inward, the next symmetric pair will be used for the +12 V analog power; the next pair of buses is for the +5 V main logic power supply. The innermost power buses are the central system ground buses. In table 1, a listing of backplane bus connections, these initial assignments of power pins are shown in shade (a).

The power supplies used in building this system are provided by relatively inexpensive modular building blocks from James Electronics. The +5 V logic power is provided by a single regulated supply rated at 6 A. The 2 analog supply voltages are provided by separate modules rated at 1 A. In the photographs of the physical hardware, these modules are shown as mounted, prior to wiring.

In the design of the backplane bus once the power supply committments have been made, the next items to consider are the data and address lines. Continuing the process of symmetrical allocation, the 16 address lines and 8 data lines should be assigned to bus pins in such a manner that if a card is rotated, data lines will map into data lines, and address lines will map into address lines. The address lines are split into 2 groups of 8 connections on either side of the symmetry axis. The data lines are

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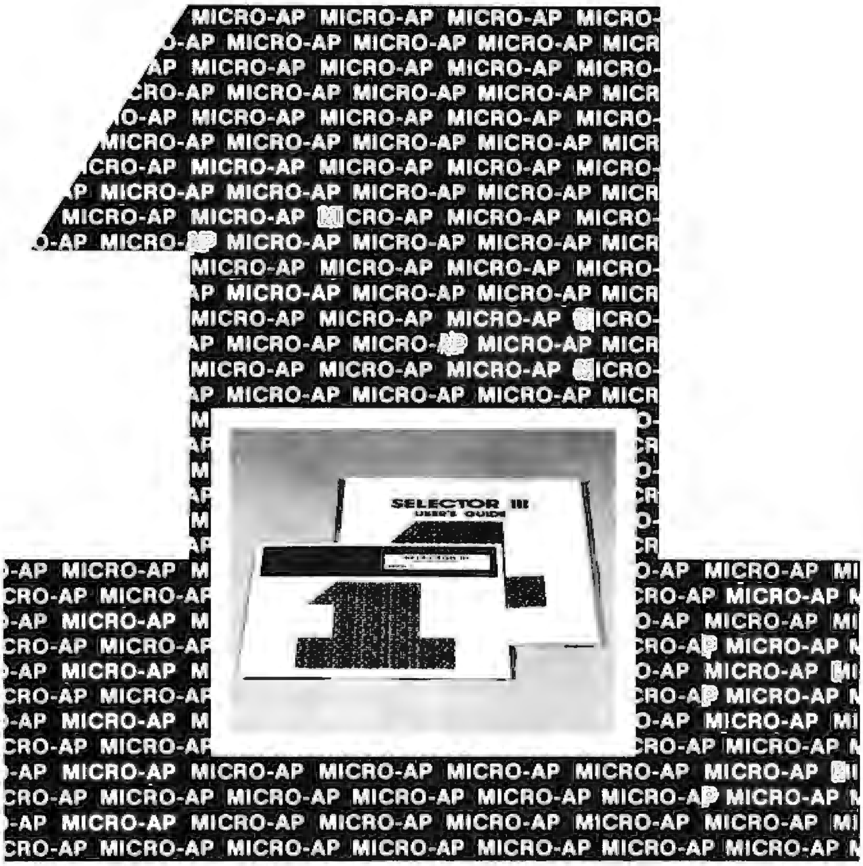

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allocated into 2 groups of 4 connections. Continuing the listing of the backplane connections in table 1, these assignments of 24 address and data pins are shown in shade (b). At this stage in the allocation of logical signals to the bus, 24 of 40 available pins have been used, leaving 16 pins still to be determined.

The next item to consider is the set of lines which connect the central processor to the external world. These lines are the essential timing and control signals which define the discipline of the bidirectional 8-bit bus used by the microprocessor. In the specifications of the 6809, the following signals are defined which have relevance to the outside world:

- RW = Read versus Write bus direction relative to the processor.
- ENABLE = Clock ouput ("Phi 2") of processor.
- QENABLE = Quadrature clock of processor.
- RESET = system reset line to processor and all peripherals.
- MRDY = memory-ready line, for use with slow memory devices.
- BREQ = bus request for direct memory access (DMA).
- BA = bus available.
- BS = bus status.
- FIRQ = fast interrupt request.
- IRQ = interrupt request.
- NMI = nonmaskable interrupt request.

The simplest and most direct way to deal with these 11 signal lines would be to bring them out to the backplane. But do we really need all these signal lines in this processor? Might it be more useful to commit a majority of the remaining 16 lines to interrupt activities, rather than having nonessential copies of the lines coming from the processor circuit? For example, we may prefer to incorporate 8 separate interrupt lines in order that each of a possible 8 peripheral devices could have a dedicated line. If this is to be accomplished, then the total commitment of noninterrupt lines to the backplane must be 8 lines instead of the mixed selection of 3 interrupt lines and 8 signal lines shown above. How can we modify this set of backplane signals given the limitations and purposes of this particular design?

First, remember that this application is a simple and limited one in which no direct-memory access is being implemented, and that all memory will be fast enough to drive the processor at full speed. Given this requirement, the 2 signals memory ready (MRDY) and bus request (BREQ) can be removed from the set seen by the external world beyond the processor card. We have thus reduced the backplane line count to 9 lines, nearly enough to allow 8 distinct interrupt lines.

The next items to question are the bus available (BA) and bus status (BS) signals. These are used to decode 1 of 4 possible states: normal operation, interrupt acknowledge, synchronization acknowledge, and bus grant (halt acknowledge). Of these, the limited goals of the present

1	------------(—12 V)------------		72
2	------------(—12 V)------------		71
3	=========(+12 V)=========		70
4	=========(+12 V)=========		69
5	+++++++MAIN PWR (+5 V)+++++++		68
6	+++++++MAIN PWR (+5 V)+++++++		67
7	~~~~~~~~~GROUND (0 V)~~~~~~~~~		66
8	~~~~~~~~~GROUND (0 V)~~~~~~~~~		65
9	= A0	D0 =	64
10	= A1	D1 =	63
11	= A2	D2 =	62
12	= A3	D3 =	61
13	= A4	I0 =	60
14	= A5	I1 =	59
15	= A6	I2 =	58
16	= A7	I3 =	57
17	= RESET	QENABLE =	56
18	= NMI	unassigned =	55
19	= unassigned	IRQ =	54
20	= ENABLE	RW =	53
21	= I4	A8 =	52
22	= I5	A9 =	51
23	= I6	A10 =	50
24	= I7	A11 =	49
25	= D4	A12 =	48
26	= D5	A13 =	47
27	= D6	A14 =	46
28	= D7	A15 =	45
29	~~~~~~~~~GROUND (0 V)~~~~~~~~~		44
30	~~~~~~~~~GROUND (0 V)~~~~~~~~~		43
31	+++++++MAIN PWR (+5 V)+++++++		42
32	+++++++MAIN PWR (+5 V)+++++++		41
33	=========(+12 V)=========		40
34	=========(+12 V)=========		39
35	------------(—12 V)------------		38
36	------------(—12 V)------------		37

(a) = *(b)* = *(c)* =

Table 1: An allocation of backplane signals. As described in the text, this backplane signal set provides for 8 bidirectional data lines, 16 address lines, 8 individual fast interrupt lines used with a (slow) software polled strategy, 2 direct interrupt lines, and 4 essential timing signals for the 6809 and its relationship with the external world. The assignment of these lines is kept symmetrical, so that while the processor may not work if any board in the system is inadvertantly plugged in the wrong way, no major conflicts will occur that could damage a gate or buffer. The shades indicate stages in the backplane allocation process described in the text: (a) pins are the power connections; (b) pins are the address and data connections; (c) pins are the 16 lines allocated to processor control signals and interrupts.

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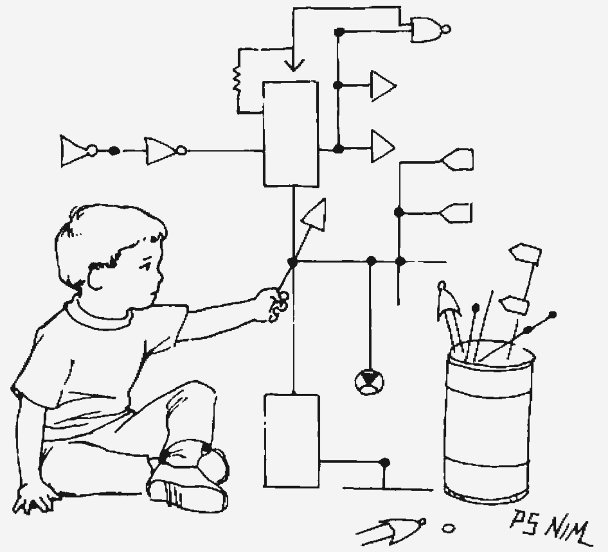
system make the only externally relevant state "normal operation" if we can confine interrupt handling logic to the processor card. Can this be done? The answer is "yes", if we define fixed read-only memory vectors for all interrupts, and eliminate the need to decode interrupt acknowledge externally for purposes of altering the interrupt vector locations. Thus the backplane signal requirements have been further reduced to 7 lines, still allowing the 3 originial interrupt lines to come out to the external world off the central processor card.

Now let's examine the interrupt handling capabilities of the processor. Of the 3 available interrupts, the fast interrupt is the most general. The reason for this is that it only stacks away the essentials of the processor state when acknowledging the interruption with a branch through the FIRQ vector location, hexadecimal address FFF6. These essentials are the condition code, and the return address. In contrast, the NMI and IRQ interrupts always stack away the entire current contents of the central processor's set of registers. If we use the FIRQ signal for most interrupt activity, then, when speed is needed, only those registers which are used by the interrupt routine can be stacked away using the multiple register push and pull instructions. If the operation of the NMI or IRQ (ie: complete protection) is required, the multiple register operation of push and pull can be extended to cover all the processor registers using the proper "post-byte" which selects registers.

What about devoting the FIRQ interrupt input to 8 different possible sources, using a concept of a software-polled flag register and a parallel input port to prioritize "who called"? This elminates 1 more line from the original backplane signal requirements, while adding 8 interrupt lines labeled I0 through I7. We keep the NMI and IRQ lines available for truely high-priority interrupt signals which must go in directly without much software decoding. Our result then is the final backplane signal set listed in table 1, with this last set of additions shown in shade (c). Two lines are left uncommitted at this stage, in case an essential signal concept is omitted. One or more interrupt lines (I0 through I7) can be sacrificed, if more than 2 lines must be added due to some shortcomings.

With this general discussion of the system's backplane complete, I will continue these notes next month with a more detailed sketch of the system's most important card: the central processor module. Following this design discussion, the final installment on the processor module will be a short description of the detailed schematic as I wire it. ■



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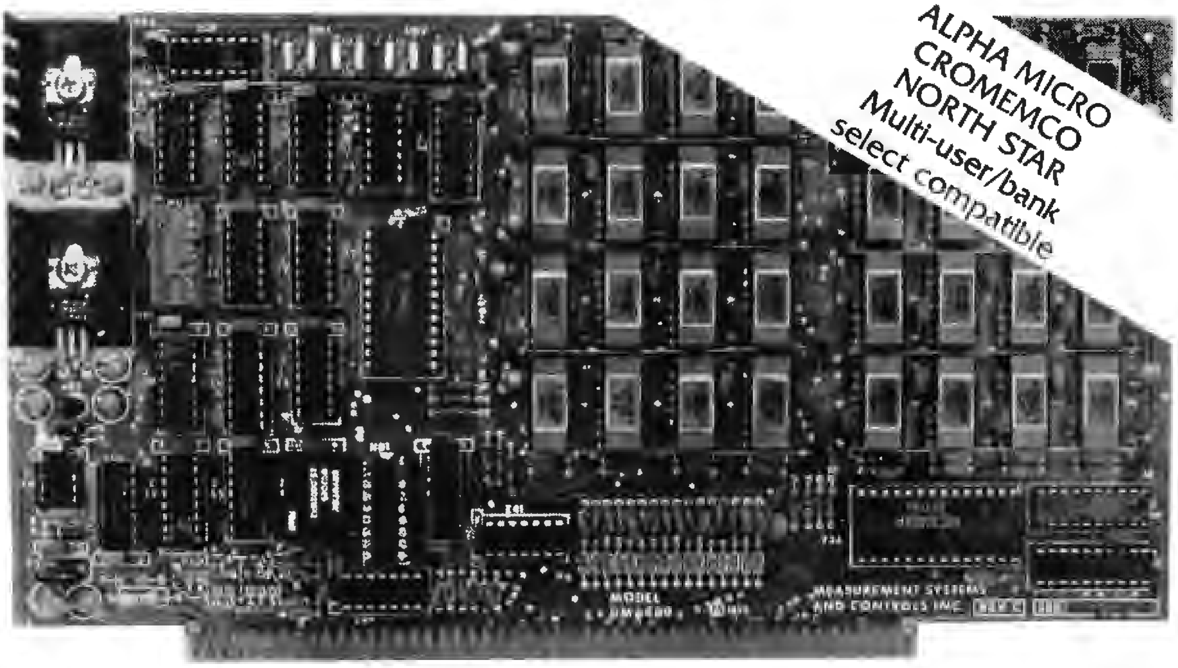

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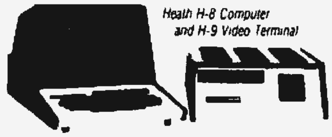

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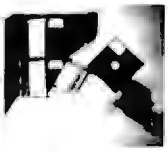

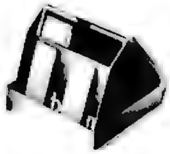

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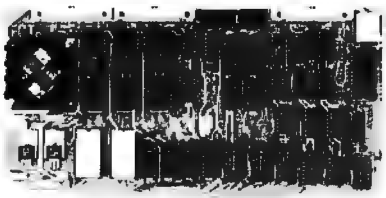

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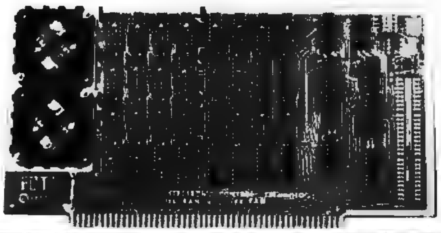

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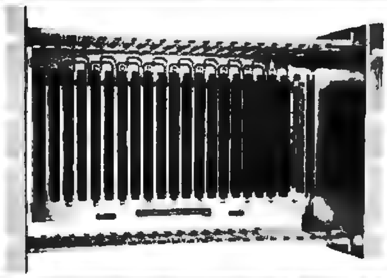

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What's New?

Low Cost Computer Assisted Instruction

APPILOT language is an Apple II version of the standard computer assisted instruction (CAI) language, PILOT. Using lesson files created by the APPILOT program editor, APPILOT creates multimedia learning experiences with text, graphics and sound. The student can interact with APPILOT using both numbers and words which APPILOT recognizes as student input.

APPILOT conforms closely to the proposed common PILOT standard, but it incorporates features that fully use the capabilities of the Apple II computer. Among these features are color graphics commands, a musical minilanguage, and disk commands for lesson segmentation which give an effective lesson size up to 90 K bytes. APPILOT also links to the Apple's integer BASIC to allow full calculation capacities.

APPILOT is available on tape and disk, and is offered on Super Load tapes and for those Apple owners who wish to run prewritten APPILOT lessons. For $17.95 the user can execute APPILOT lessons on a 16 K byte Apple, using only tape storage. Included on the tape is the interpreter and a demonstration lesson about APPILOT. Also provided is a documentation manual for running APPILOT and for linking it with the MUSE APPEN-I Text Editor, which may be used for creating and editing APPILOT lessons.

For institutions that wish to write as well as use APPILOT lessons, the APPILOT Edu-Disk converts a 32 K byte Apple with disk into a complete CAI system. The user can develop lessons, store them on disk, and run them with the APPILOT interpreter. The Edu-Disk comes with interactive lessons that instruct the user on all aspects of the APPILOT CAI development system. The APPILOT Edu-Disk is being offered for $49.95 which includes a detailed documentation manual. For further information, contact MUSE, 7112 Darlington Dr, Baltimore MD 21234.

Circle 565 on inquiry card.

CP/M Text Editor

ED-80 is a text editor designed to run under CP/M and derivative operating systems on 8080, 8085, and Z-80 disk based systems. A user's manual of over 60 pages describes both implementation and usage. ED-80 has a simple command structure patterned after the University of Maryland's editor for UNIVAC 1100s. Over 50 commands are provided, including forward or backward locate, change, and find commands; insert, delete, append, print, list, macro, case, scale, tabset, and window commands; and get and put commands for copying, moving, merging, and duplicating edit files and program libraries. An internal location counter is maintained for displaying with text, prompting for user input, and for line positioning.

ED-80 provides a window approach to text editing that is not hardware dependent. Users may examine and edit data through a one line window as it is moved through the edit file. A window command allows instantaneous full screen displays of both the current line and surrounding lines, with forward and backward scrolling.

Compatible with existing CP/M edit files, ED-80 is available on an 8-inch single density disk for $71. For further information contact Software Development and Training Inc, POB 4511, Huntsville AL 35802.

Circle 568 on inquiry card.

16-Digit Scientific Subroutine Package for Microsoft Extended and Disk BASIC Interpreters

DPFUN is a comprehensive 16-digit precision scientific subroutine package written for Microsoft extended and disk BASIC intepreters, including TRS-80 Level II BASIC. The 13 double-precision exponential, logarithmic, trigonometric, and inverse trigonometric functions provide a valuable utility for engineering and scientific applications. DPFUN uses truncated continued fraction algorithms that result in easily entered code, fast execution, and full exploitation of the precision that is available in 64-bit binary floating-point notation. The complete set of subroutines occupies approximately 2.5 K bytes.

The DPFUN source code only is available for $10 postpaid. For further information contact Miken Optical Co, 53 Abbett Av, Morristown NJ 07960.

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Machine Language Programs for the PET Computer

The SYS7171 and the SYS8181 are two new machine language programs for the PET 2001 computer. SYS7171 is a machine language monitor which allows a programmer or PET user to program in machine language, or in BASIC, without destruction of the monitor once it is loaded. Programs may be saved, loaded or rewritten yet SYS7171 remains coresident and undisturbed.

SYS8181 is a machine language renumbering program which requires only 1 K byte of programmable memory for its operation. After it is loaded, the user can load a BASIC program and it will be renumbered in seconds.

SYS7171 sells for $29.71 and SYS8181 is priced at $18.71. For further information, contact National Artificial Intelligence Laboratory, POB F, Mobile AL 36601.

Circle 566 on inquiry card.

Word Processing Software System

Autoscribe is a professional word processing system designed for the business world. With Autoscribe, typed text appears on a video terminal screen as it will be printed, and corrections, deletions or revisions can be made in seconds. The finished document is typed at hundreds of words per minute. Letters, contracts and other documents can be produced quickly on single page or continuous form print-out. The original data is recorded and saved on the user disk. Documents can be retrieved instantly and reprinted as needed. No computer language is needed. All instructions are in English. Autoscribe software operates on Z-80 and 8080 systems utilizing North Star disk, a Soroc or Hazeltine terminal and a letter quality printer. For further information contact MicroAge Wholesale, 1425 W 12th Place, Tempe AZ 85281.

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Elementary Math Tapes for TRS-80

The Microcomputer Mathematics Program K-8 consists of a set of tapes for drill, practice and tutorial in addition, subtraction, multiplication, division, fractions, numeration and decimals for kindergarten through 8th grade. The tapes are programmed for use on a Radio Shack Level II BASIC TRS-80 microcomputer and 16 K bytes modified memory. The teacher's manual gives an overview of the program, suggests ways to use the program, correlates the skills to selected mathematics texts, and provides suggestions for individualizing math instruction. One set of microcomputer Mathematics Program K-8 tapes including the teacher's manual is $995. For further information, contact Foundation for Quality Education Inc, 802 Merchants State Bank Building, 5217 Ross Av, Dallas TX 75206.

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Computer Communication at Your Fingertips

VuePoint is a touch input display panel that measures only 2½ inches thick. Vuepoint's 12 line by 40 character flat panel also provides a unique touch input capability. This approach permits efficient and speedy operator interaction using menu-driven displays. Vuepoint's microprocessor based controller provides all standard smart video features plus the following: touch response in matrix or screen echo modes, multiple display buffers, and alternate character sets. Communication is by standard 300-19200 bps asynchronous RS-232 protocol. Options include wall or rack mount, auxiliary printer, and 128 character ASCII keyboard. Vuepoint is priced at $3500. For further information, contact General Digital Corp, 700 Burnside Av, E Hartford CT 06108.

Circle 571 on inquiry card.

Where Do New Products Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

APL/Z-80 Release 2.0

Vanguard Systems Corp, 6812 San Pedro, San Antonio TX 78216 has announced the release of version 2.0 of APL/Z-80, an APL interpreter for Z-80 based microcomputers. APL/Z-80 includes the following features: dynamic execution of system commands; serial printer support; shared variables; auxilary processor for I/O (input/output) ports which allows complete device control using defined APL functions for any device interfaced to the Z-80 I/O port; and auxilary processor implementation of a file system featuring a directly indexable file having variable length records, each of which can be an APL array of arbitrary type, shape, and size (up to available workspace).

A workspace containing defined APL/Z-80 functions, implementing each of the primitive functions not present in this version of APL/Z-80, is distributed with each system. The hardware required is a Z-80 processor, a disk drive, and either serial ASCII APL console terminal or ASCII keyboard and video display board compatible with the Vector Graphic Flashwriter or Processor Technology VDM-1.

The end user license for use on a single processor is $350.

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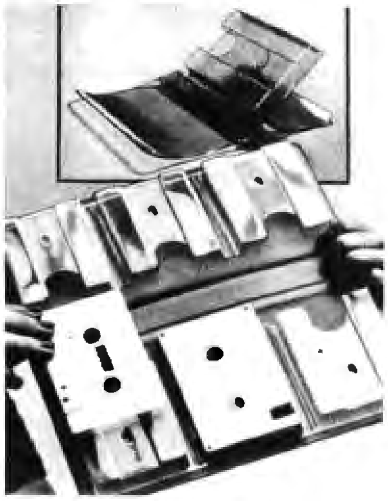
Heat Sealable Cassette Holder



This cassette holder, designated Pocketray, will hold a cassette securely with the title visible. Cassettes are fully protected on three sides. There are 12 Pocketrays to a sheet which is perforated vertically and horizontally. These may be snapped apart into single units or in any multiple to fit the most creative configuration. Made of PVC, these cassette holders are easily heat sealed to any vinyl material, with a minimum of tooling. Samples, pricing, and literature are available from Charles Leonard Inc, 79-11 Cooper Av, Glendale NY 11227.

Circle 574 on inquiry card.

Distributed Computer System Based on Personal Computers

Cluster/One is a distributed processing alternative to BASIC timesharing. The central Cluster/One unit (the Queen) connects to 15 personal microcomputers (the Drones), via a high-speed parallel data bus (the Clusterbus). An optional feature provides support for an additional 15 Drones. Currently supported as Drone stations are the Apple II, Commodore PET 2001-8, and TRS-80.

Programs and data files can be shared among the users of Cluster/One. They are stored on two IBM compatible eight inch floppy disks. Each disk holds up to 315 K bytes of data. Disk data transfer rate is 250 K bits per second, managed by a large scale integration floppy disk controller chip. All data transfers are cyclic redundancy checked (CRC) and disk writes are automatically verified. Data is transmitted to each Drone station in packets, with individual error checking. Typical system response time for program loading is two seconds.

Cluster/One commands are quite similar to their counterpart cassette tape commands. Disk commands may be imbedded in user programs, permitting menu-driven program loading or chaining.

Cluster/One comes with a full set of utility programs for system maintenance and backup, along with separate documentation for the end users. Prices begin at $4500 and vary with the particular configuration and options selected. For further information, contact Nestar Systems Inc, 810 Garland Dr, Palo Alto CA 94303.

Circle 573 on inquiry card.

A Message to our Subscribers

From time to time we make the BYTE subscriber list available to other companies who wish to send our subscribers promotional material. We take great care to screen these companies, choosing only those who are reputable, and whose products, services, or information we feel would be of interest to you.

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Thank you.

New Word Processing System Also Supports Data Processing Applications

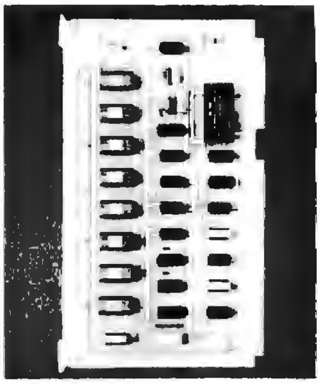
A video based word processing system capable of handling data processing applications has been introduced by Vector Graphic Inc, 31364 Via Colinas, Westlake Village CA 91361. The new system, called Memorite 2, incorporates the firm's Z80 based MZ microcomputer with 630 K bytes of disk capacity, their Mindless Terminal, and the Qume Sprint 5, 55 cps printer. For word processing applications, Memorite 2 with dual Micropolis floppy disk drives features advanced text preparation, edit, and delete capabilities. It offers automatic letter printing from memory with full formatting techniques such as underlining, indentation, automatic margins and variable line and character spacing. The system also performs mass mailings, which allow letters to be merged with address lists. Its memory is resident on programmable read-only memory, so users need only type after a "power up and proceed" function.

As a data processor, Memorite 2 is capable of performing standard accounting tasks and custom applications in business BASIC for small firms or departments of large companies. Scientific calculations are also available for technical environments.

The price for the Memorite 2 is $8,950.

Circle 575 on inquiry card.

Non-Volatile Memory Board



The E4K EAROM Memory Board provides a Multibus compatible nonvolatile memory of up to 4 K words by 8-bit capacity. The memory contents are electrically alterable under computer control, permitting it to function as a programmable memory but with the advantage of long term unpowered data retention. Either word or block erasure is possible. Operating software listings are provided with the board. Typical applications include remote data acquisition systems, numerical control systems, process controllers, storage of manually entered constants and telephone number storage.

The prices for the E4K EAROM Memory Board start at $420. For further information, contact Schneider Instrument Co, 8115 Camargo Rd, Madeira OH 45243.

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S-100 bus compatible

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Both the modem and telephone system interface are FCC approved, accomplishing all the required protective functions with a miniaturized, proprietary protective coupler.

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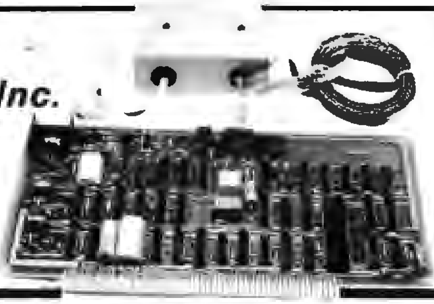

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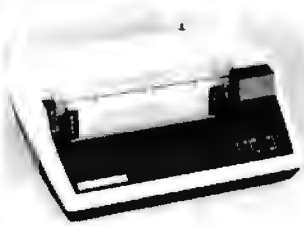

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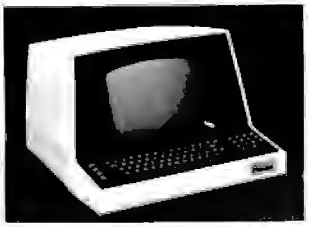

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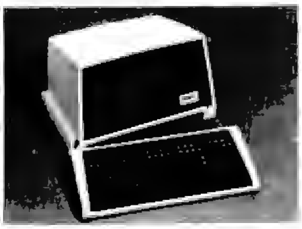

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The CmC Word Processor Program addresses an RS-232 printer through a CmC printer adapter.
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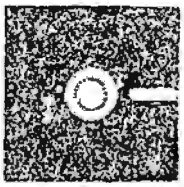

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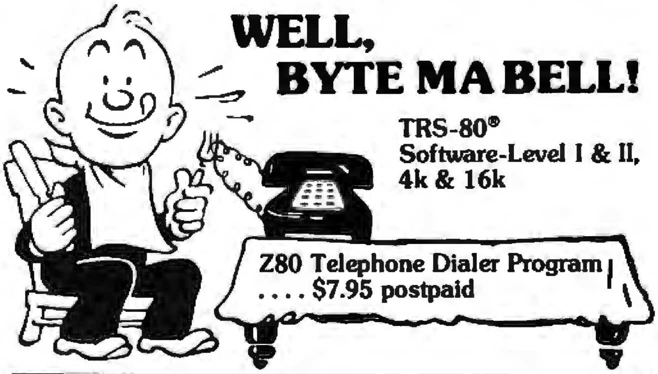
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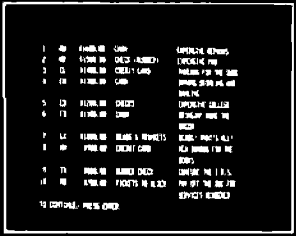
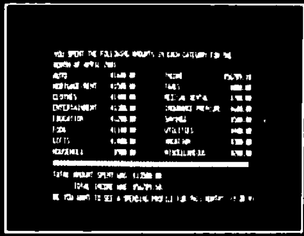
Creative Software Introduces: Programs & Products for the TRS-80 (16K level II)





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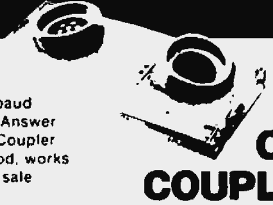

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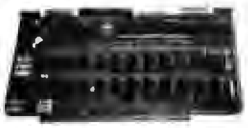

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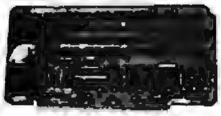

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- Phantom is jumper selectable to pin 67
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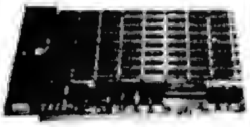

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4011	.22	4029	.95	74C00	.27	74C173	1.30
4012	.22	4030	.35	74C02	.27	74C174	1.20
4013	.40	4035	.97	74C04	.30	74C175	1.20
4014	1.20	4042	.85	74C10	.27	74C193	1.40
4015	1.00	4044	.85	74C20	.27	74C901	.50
4016	.45	4049	.75	74C42	.90	74C902	.60
4017	1.06	4050	.45	74C73	.75	74C914	1.90
4018	.90	4051	1.10	74C74	.50		
4019	.45	4053	1.10	74C83	1.30		
4020	1.10	4055	1.75	74C86	.50		
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7404	.22	7475	.67	74157	.87
7405	.22	7476	.45	74161	.93
7406	.33	7480	.46	74162	1.20
7408	.22	7483	.87	74163	.87
7409	.22	7485	1.30	74164	1.27
7410	.22	7486	.42	74165	1.47
7411	.22	7489	1.87	74173	1.60
7412	.22	7490	.63	74174	1.47
7413	.64	7491	.87	74176	1.27
7414	.90	7492	.64	74175	1.12
7416	.33	7493	.64	74177	1.12
7417	.33	7494	1.00	74180	.87
7420	.22	7495	.87	74181	2.85
7425	.45	7496	.87	74190	1.50
7426	.33	74107	.47	74191	1.37
7427	.42	74121	.45	74192	1.18
7430	.22	74122	.60	74193	1.18
7432	.33	74123	.67	74194	1.20
7437	.33	74125	.60	74195	.75
7438	.33	74126	.60	74196	1.28
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7441	1.05	74148	1.65	74221	.87
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74LS01	.29	74LS51	.29	74LS139	.89
74LS02	.29	74LS54	.29	74LS151	.89
74LS03	.29	74LS55	.29	74LS155	.89
74LS04	.35	74LS73	.45	74LS157	.89
74LS05	.35	74LS74	.45	74LS160	1.15
74LS08	.35	74LS75	.59	74LS161	1.15
74LS09	.35	74LS76	.45	74LS162	1.15
74LS10	.29	74LS78	.49	74LS163	1.15
74LS11	.39	74LS83	.89	74LS164	1.25
74LS13	.59	74LS85	1.25	74LS175	.99
74LS14	1.25	74LS86	.45	74LS181	2.49
74LS15	.35	74LS90	.59	74LS190	1.15
74LS20	.29	74LS92	.75	74LS191	1.15
74LS21	.35	74LS93	.75	74LS192	1.15
74LS22	.35	74LS95	.99	74LS193	1.15
74LS26	.35	74LS96	1.15	74LS194	1.15
74LS27	.35	74LS107	.45	74LS195	1.15
74LS28	.35	74LS109	.45	74LS253	.99
74LS30	.29	74LS112	.45	74LS257	.89
74LS32	.35	74LS123	1.25	74LS258	1.75
74LS37	.45	74LS125	.89	74LS260	.69
74LS40	.35	74LS132	.99	74LS279	.79
74LS42	.89	74LS136	.49	74LS367	.75
				74LS368	.75
				74LS670	2.49

EXCITING NEW KITS

NEW JE600 HEXADECIMAL ENCODER KIT

FEATURES:
- Full 8 bit latched output for microprocessor use
- 3 User Define keys with one being bi-stable operation
- Debounce circuit provided for all 19 keys
- LED readout to verify entries
- Easy interfacing with standard 16 pin IC connector
- Only +5VDC required for operations

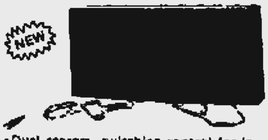
FULL 8 BIT LATCHED OUTPUT—19 KEYBOARD

The JE600 Encoder Keyboard provides two separate hexadecimal digits produced from sequential key entries to allow direct programming for 8 bit microprocessor or 8 bit memory circuits. Three (3) additional keys are provided for user operations with one having a bistable output available. The outputs are latched and monitored with LED readouts. Also included is a key entry strobe.

JE600 . . . . $59.95
Hexadecimal Keypad only $10.95

Digital Thermometer Kit

NEW



- Dual sensors—switching control for indoor/outdoor or dual monitoring
- Continuous LED .8" ht. display
- Range: -40°F to 199°F / -40°C to 100°C
- Accuracy: ±1° nominal
- Set for Fahrenheit or Celsius reading
- Slim, walnut case - AC wall adapter incl.
- Size: 3-1/4"H x 6-5/8"W x 1-3/8"D

JE300 . . . .$39.95

DISCRETE LEDS

.200" dia.		
XC556R	red	5/$1
XC556G	green	4/$1
XC556Y	yellow	4/$1
XC556C	clear	4/$1
.200" dia.		
XC22R	red	5/$1
XC22G	green	4/$1
XC22Y	yellow	4/$1
.170" dia.		
MV108	red	4/$1
.085" dia.		
MV50	red	6/$1
.125" dia.		
XC209R	red	5/$1
XC209G	green	4/$1
XC209Y	yellow	4/$1
.185" dia.		
XC526R	red	5/$1
XC526G	green	4/$1
XC526Y	yellow	4/$1
XC526C	clear	4/$1
.190" dia.		
XC111R	red	5/$1
XC111G	green	4/$1
XC111Y	yellow	4/$1
XC111C	clear	4/$1

INFRA-RED LED
1/4"x1/4"x1/16" flat
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4 DIGIT — .5" CHARACTERS
THREE ENUNCIATORS
2.00" X 1.20" PACKAGE
INCLUDES CONNECTOR

T1001-Transmissive	$7.95
T1001A-Reflective	8.25

DISPLAY LEDS

TYPE	POLARITY	HT	PRICE	TYPE	POLARITY	HT	PRICE
MAN 1	Common Anode-red	.270	2.95	MAN 6730	Common Anode-red ± 1	.560	.99
MAN 2	5 x 7 Dot Matrix-red	.300	4.95	MAN 6740	Common Cathode-red-D.D.	.560	.99
MAN 3	Common Cathode-red	.125	.25	MAN 6750	Common Cathode-red ± 1	.560	.99
MAN 4	Common Cathode-red	.187	1.95	MAN 6760	Common Anode-red	.560	.99
MAN 7G	Common Anode-green	.300	1.25	MAN 6780	Common Cathode-red	.560	.99
MAN 7Y	Common Anode-yellow	.300	.99	DL701	Common Anode-red ± 1	.300	.99
MAN 72	Common Anode-red	.300	.99	DL704	Common Cathode-red	.300	.99
MAN 74	Common Cathode-red	.300	1.25	DL707	Common Anode-red	.300	.99
MAN 82	Common Anode-yellow	.300	.99	DL728	Common Cathode-red	.500	1.49
MAN 84	Common Cathode-yellow	.300	.99	DL741	Common Anode-red	.600	1.25
MAN 3620	Common Anode-orange	.300	.99	DL746	Common Anode-red ± 1	.630	1.49
MAN 3630	Common Anode-orange ± 1	.300	.99	DL747	Common Anode-red	.600	1.49
MAN 3640	Common Cathode-orange	.300	.99	DL749	Common Cathode-red ± 1	.630	1.49
MAN 4610	Common Anode-orange	.300	.99	DL750	Common Cathode-red	.600	1.49
MAN 4640	Common Cathode-orange	.400	.99	DL338	Common Cathode-red	.110	.35
MAN 4710	Common Anode-red	.400	.99	FND70	Common Cathode	.250	.69
MAN 4730	Common Anode-red ± 1	.400	.99	FND358	Common Cathode ± 1	.357	.99
MAN 4740	Common Cathode-red	.400	.99	FND359	Common Cathode	.357	.75
MAN 4810	Common Anode-yellow	.400	.99	FND503	Common Cathode(FND500)	.500	.99
MAN 4840	Common Cathode-yellow	.400	.99	FND507	Common Anode (FND510)	.500	.99
MAN 6610	Common Anode-orange-D.D.	.560	.99	5082-7730	Common Anode-red	.300	1.30
MAN 6630	Common Anode-orange ± 1	.560	.99	HDSP-3400	Common Anode-red	.800	2.10
MAN 6640	Common Cathode-orange-D.D.	.560	.99	HDSP-3403	Common Cathode red	.800	2.10
MAN 6650	Common Cathode-orange ± 1	.560	.99	5082-7300	4 x 7 sgl. Digit-RHDP	.600	19.95
MAN 6660	Common Anode-orange	.560	.99	5082-7302	4 x 7 Sgl. Digit-LHDP	.600	19.95
MAN 6680	Common Cathode-orange	.560	.99	5082-7304	Overrange character (± 1)	.600	15.00
MAN 6710	Common Anode-red-D.D.	.560	.99	5082-7340	4 x 7 Sgl. Digit-Hexadecimal	.600	22.50

RCA LINEAR

CA3013T	2.15	CA3082N	2.00
CA2023T	2.58	CA3083N	1.60
CA3035T	2.48	CA3086N	.85
CA3039T	1.35	CA3089N	3.75
CA3046N	1.30	CA3130T	1.39
CA3059N	3.25	CA3140T	1.25
CA3060N	3.25	CA3160T	1.25
CA3080T	.85	CA3401N	.49
CA3081N	2.00	CA3600N	3.50

CALCULATOR CHIPS/DRIVERS

MM5725	$2.95
MM5738	2.95
DM8864	2.00
DM8865	1.00
DM8887	.75
DM8889	.75
9374 7 seg	
C.A. LED driver	1.50

CLOCK CHIPS

MM5309	$4.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5387/1998A	4.95
MM5841	9.95

MOTOROLA

MC1408L7	$4.95
MC1408L8	5.75
MC1439L	2.95
MC3022P	2.95
MC3061P	3.50
MC4016(74416)	7.50
MC4024P	3.95
MC4040P	6.95
MC4044P	4.50

IC SOLDERTAIL — LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin LP	$.17	.16	.15	22 pin LP	$ .37	.36	.35
14 pin LP	.20	.19	.18	24 pin LP	.38	.37	.36
16 pin LP	.22	.21	.20	28 pin LP	.45	.44	.43
18 pin LP	.29	.28	.27	36 pin LP	.60	.59	.58
20 pin LP	.34	.32	.30	40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100		1-24	25-49	50-100
14 pin ST	$.27	.25	.24	28 pin ST	$ .99	.90	.81
16 pin ST	.30	.27	.25	36 pin ST	1.39	1.26	1.15
18 pin ST	.35	.32	.30	40 pin ST	1.59	1.45	1.30
24 pin ST	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin SG	$.30	.27	.24	24 pin SG	$ .70	.63	.57
14 pin SG	.35	.32	.29	28 pin SG	1.10	1.00	.90
16 pin SG	.38	.35	.32	36 pin SG	1.65	1.40	1.26
18 pin SG	.52	.47	.43	40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin WW	$.39	.38	.31	22 pin WW	$ .95	.85	.75
10 pin WW	.45	.41	.37	24 pin WW	1.05	.95	.85
14 pin WW	.39	.38	.37	28 pin WW	1.40	1.25	1.10
16 pin WW	.43	.42	.41	36 pin WW	1.59	1.45	1.30
18 pin WW	.75	.68	.62	40 pin WW	1.75	1.55	1.40

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ASST. 1	5 ea	10 OHM / 27 OHM	12 OHM / 33 OHM	15 OHM / 39 OHM	18 OHM / 47 OHM	22 OHM / 56 OHM	50 PCS	$1.75
ASST. 2	5 ea	68 OHM / 180 OHM	82 OHM / 220 OHM	100 OHM / 270 OHM	120 OHM / 330 OHM	150 OHM / 390 OHM	50 PCS	1.75
ASST. 3	5 ea	470 OHM / 1.2K	560 OHM / 1.5K	680 OHM / 1.8K	820 OHM / 2.2K	1K / 2.7K	50 PCS	1.75
ASST. 4	5 ea	3.3K / 8.2K	3.9K / 10K	4.7K / 12K	5.6K / 15K	6.8K / 18K	50 PCS	1.75
ASST. 5	5 ea	22K / 56K	27K / 68K	33K / 82K	39K / 100K	47K / 120K	50 PCS	1.75
ASST. 6	5 ea	150K / 390K	180K / 470K	220K / 560K	270K / 680K	330K / 820K	50 PCS	1.75
ASST. 7	5 ea	1M / 2.7M	1.2M / 3.3M	1.5M / 3.9M	1.8M / 4.7M	2.2M / 5.6M	50 PCS	1.75

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) **$9.95 ea.**

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TL074CN	Quad Low Noise bi-fet Op Amp	2.49
TL494CN	Switching Regulator	4.49
TL496CP	Single Switching Regulator	1.75
11C90	Divide 10/11 Prescaler	19.95
95H90	Hi-Speed Divide 10/11 Prescaler	11.95
4N33	Photo-Darlington Opto-Isolator	3.95
MK50240	Top Octave Freq. Generator	17.50
DS0026CH	5Mhz 2-phase MOS clock driver	3.75
TIL308	.27" red num. display w/integ. logic chip	10.50
MM5320	TV Camera Sync. Generator	14.95
MM5330	4½ Digit DPM Logic Block (Special)	3.95
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XR205	$8.40			XR2242CP	1.50
XR210	4.40			XR2264	4.25
XR215	4.40			XR2556	3.20
XR320	1.55	JE2206KA	14.95	XR2567	2.99
XR-L555	1.50	JE2206KB	19.95	XR3403	1.25
XR555	.39	XR1800	3.20	XR4136	1.25
XR556	.99	XR2206	4.40	XR4151	2.85
XR567CP	.99	XR2207	3.85	XR4194	4.95
XR567CT	1.25	XR2208	5.20	XR4202	3.60
XR1310P	1.30	XR2209	1.75	XR4212	2.05
XR1468CN	3.85	XR2211	5.25	XR4558	.75
XR1488	1.39	XR2212	4.35	XR4739	1.15
XR1489	1.39	XR2240	3.45	XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
				1N4002	100 PIV	1 AMP	12/1.00
				1N4003	200 PIV	1 AMP	12/1.00
1N746	3.3	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N3600	50	200m	6/1.00
1N757	9.0	400m	4/1.00	1N4148	75	10m	15/1.00
1N759	12.0	400m	4/1.00	1N4154	35	10m	12/1.00
1N959	8.2	400m	4/1.00	1N4305	75	25m	15/1.00
1N965	15	400m	4/1.00	1N4734	5.6	1w	.28
1N5232	5.6	500m	.28	1N4735	6.2	1w	.28
1N5234	6.2	500m	.28	1N4736	6.8	1w	.28
1N5235	6.8	500m	.28	1N4738	8.2	1w	.28
1N5236	7.5	500m	.28	1N4742	12	1w	.28
1N5242	12	500m	.28	1N4744	15	1w	.28
1N5245	15	500m	.28	1N1183	50 PIV	35 AMP	1.60
1N456	25	40m	6/1.00	1N1184	100 PIV	35 AMP	1.70
1N458	150	7m	6/1.00	1N1185	150 PIV	35 AMP	1.70
1N485A	180	10m	5/1.00	1N1186	200 PIV	35 AMP	1.80
1N4001	50 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR(2N1849)	$1.95
C38M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
40409	1.75	PN3567	3/1.00	PN4249	4/1.00
40410	1.75	PN3568	4/1.00	PN4250	4/1.00
40673	1.75	PN3569	4/1.00	2N4400	4/1.00
2N918	4/1.00	MPS3638A	5/1.00	2N4401	4/1.00
2N2219A	2/1.00	MPS3702	5/1.00	2N4402	4/1.00
2N2221A	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2222A	5/1.00	MPS3704	5/1.00	2N4409	5/1.00
PN2222 Plastic	7/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2369	5/1.00	MPS3705	5/1.00	2N5087	4/1.00
2N2369A	4/1.00	2N3706	5/1.00	2N5088	4/1.00
MPS2369	5/1.00	MPS3706	5/1.00	2N5089	4/1.00
2N2484	4/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2906	4/1.00	2N3711	5/1.00	PN5134	5/1.00
2N2907	5/1.00	2N3724A	.65	PN5138	5/1.00
PN2907 Plastic	7/1.00	2N3725A	1.00	2N5139	5/1.00
2N2925	5/1.00	2N3772	2.25	2N5210	5/1.00
MJE2955	1.25	2N3823	1.00	2N5449	3/1.00
2N3053	2/1.00	2N3903	5/1.00	2N5951	3/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075

100 VOLT MYLAR FILM CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (SOLID) CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/25V	.31	.27	.22
.22/35V	.28	.23	.17	3.3/25V	.31	.27	.22
.33/35V	.28	.23	.17	4.7/25V	.32	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.36	.31	.25
.68/35V	.28	.23	.17	15/25V	.63	.50	.40
1.0/35V	.28	.23	.17				

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead	1-9	10-99	100-	Radial Lead	1-9	10-99	100-
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

Circle 200 on inquiry card.

Circle 201 on inquiry card.

Circle 277 on inquiry card.

Circle 15 on inquiry card.

Circle 39 on inquiry card

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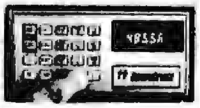
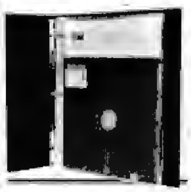


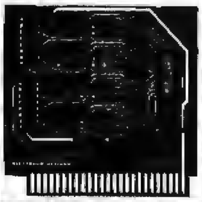
FLOPPY DISK STORAGE BINDER

This black vinyl three-ring binder comes with ten transparent plastic sleeves which accommodate either twenty, five-inch or ten, eight-inch floppy disks. The plastic sleeves may be ordered separately and added as needed. A contents file is included with each sleeve for easy identification and organizing. Binder & 10 holders $14.95 Part No. 8800; Extra holders 95¢ each. Part No. 800



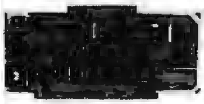
OPTO-ISOLATED PARALLEL INPUT BOARD FOR APPLE II

There are 8 inputs that can be driven from TTL logic or any 5 volt source. The circuit board can be plugged into any of the 8 sockets of your Apple II. It has a 16 pin socket for standard dip ribbon cable connection.
Board only $15.00. Part No. 120, with parts $69.95. Part No. 120A.



TIDMA

• Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate • S-100 bus compatible • Board only $35.00 Part No. 112, with parts $110 Part No. 112A

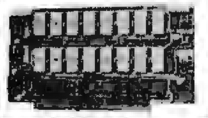


SYSTEM MONITOR

8080, 8085, or Z-80 System monitor for use with the TIDMA board. There is no need for the front panel. Complete with documentation $12.95.

16K EPROM

Uses 2708 EPROMS, memory speed selection provided, addressable anywhere in 65K of memory, can be shadowed in 4K increments. Board only $24.95 part no. 7902, with parts less EPROMs $49.95 part no. 7902A.



ASCII KEYBOARD

TTL & DTL compatible • Full 67 key array • Full 128 character ASCII output • Positive logic with outputs resting low • Data Strobe • Five user-definable spare keys • Standard 22 pin dual card edge connector • Requires +5VDC, 325 mA. Assembled & Tested. Cherry Pro Part No. P70-05AB. $135.00.

ASCII KEYBOARD

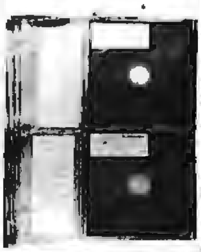
53 Keys popular ASR-33 format • Rugged G-10 P.C. Board • Tri-mode MOS encoding • Two-Key Rollover • MOS/DTL/TTL Compatible • Upper Case lockout • Data and Strobe inversion option • Three User Definable Keys • Low contact bounce • Selectable Parity • Custom Keycaps • George Risk Model 753. Requires +5, -12 volts. $59.95 Kit.

ASCII TO CORRESPONDENCE CODE CONVERTER

This bidirectional board is a direct replacement for the board inside the Trendata 1000 terminal. The on board connector provides RS-232 serial in and out. Sold only as an assembled and tested unit for $229.95. Part No. TA 1000C

DISK JACKET™

Made from heavy duty .0095 matte plastic with reinforced grommets. The minidiskette version holds two 5-1/4 inch diskettes and will fit any standard three ring binder. The pockets to the left of the diskette can be used for listing the contents of the disk. Please order only in multitudes of ten. $9.95/10 Pack.

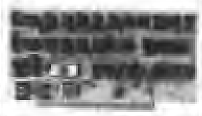


INTERNATIONAL MICROPROCESSOR DICTIONARY

English, French, Danish, German, Italian, Hungarian, Norwegian, Polish, Spanish, Swedish. 10 languages, 28 pp. SYBEX, Ref, IMD. $4.95

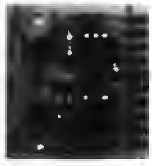
VIDEO TERMINAL

16 lines, 64 columns • Upper and lower case • 5x7 dot matrix • RS-232 in • RS-232 out with TTL parallel keyboard input • On board baud rate generator 75, 110, 150, 300, 600, & 1200 jumper selectable • Memory 1024 characters (7-21L02) • Video processor chip SFF96364 by Neculonic • Control characters (CR, LF, →, ←, ↓, ↑, non destructive cursor, CS, home, CL • White characters on black background or vice-versa • With the addition of a keyboard, video monitor or TV set with TV interface (part no. 107A) and power supply this is a complete stand alone terminal • also S-100 compatible • requires +16, & -16 VDC at 100mA, and 8VDC at 1A. Part no. 1000A $199.95 kit.



RS-232/20mA INTERFACE

This board has two passive, opto-isolated circuits. One converts RS-232 to 20mA, the other converts 20mA to RS-232. All connections go to a 10 pin edge connector. Requires +12 and -12 volts. Board only $9.95, part no. 7901, with parts $14.95 Part No. 7901A.



COMPUCOLOR II

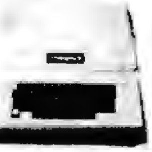
Model 3, 8K $1395.
Model 4, 16K $1695.
Model 5, 32K $1895.
Prices include color monitor, computer, and one disk drive.

PET COMPUTER

With 32K & monitor - $1195. Dual Disk Drive - $1195.

apple II or APPLE II PLUS

16K - $995, 32K $1059, 48K - $1123.
Disk & cont $589

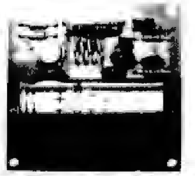


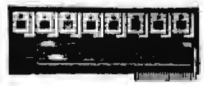
6502 APPLICATIONS BOOK Z80 APPLICATIONS BOOK*

This book will teach you how to connect a board to the outside world and implement practical applications for the 6502, (or Z80). Applications range from home control (a complete alarm system, including heat sensor), to industrial applications. You will learn techniques ranging from simulated traffic control to analog-digital conversion. All experiments can be realized with a minimum of external (low-cost) components. They are directly applicable to any 6502-based board such as SYM, KIM, AIM 65. This book also studies in detail input-output techniques and components, and is the logical continuation of C202 (or C280). By Rodney Zaks. SYBEX. 6502: Ref. D302: Z80: Ref D380. Each $12.95

T.V. INTERFACE

● Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple ● Power required is 12 volts AC C.T., or +5 volts DC ● Board only $7.60 part No. 107, with parts $13.50 Part No. 107A





PARALLEL TRIAC OUTPUT BOARD FOR APPLE II

This board has 8 triacs capable of switching 110 volt 6 amp loads (660 watts per channel) or a total of 5280 watts. Board only $15.00 Part No. 210, with parts $119.95 Part No. 210A.

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U.S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U.S. dollars. Dealer inquiries invited. 24 hour order line (408) 226-4064.

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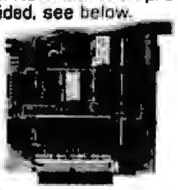
Circle 125 on inquiry card.

TRS-80^E.S. SERIAL I/O

• Can input into basic • Can use LLIST and LPRINT to output, or output continuously • RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line • Requires +5, -12 VDC • Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010 C. No connectors provided, see below.



EIA/RS-232 connector Part No DB25P $6.00 with 9', 8 conductor cable $10.95 Part No. DB25P9.

3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No. 3CAB40

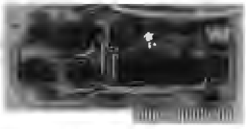
MODEM

• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output-serial • Connect 8 Ω speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A

DISKETTES

Box of 10, 5" $29.95, 8" $39.95.
Plastic box, holds 10 diskettes, 5" - $4.50, 8" - $6.50.

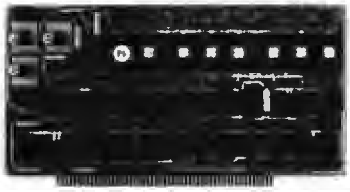
APPLE II^E.S. SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

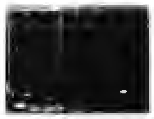
8K EPROM PIICEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. • S-100 bus compatible • Room for 8K bytes of EPROM non-volatile memory (2708's). • On-board PROM programming • Address relocation of each 4K of memory to any 4K boundary within 64K • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software available • Solder mask both sides • Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.



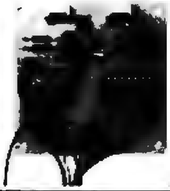
T.V. TYPEWRITER

• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A



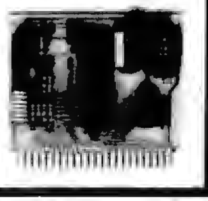
TAPE INTERFACE

• Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board only $7.60 Part No. 111, with parts $27.50 Part No. 111A



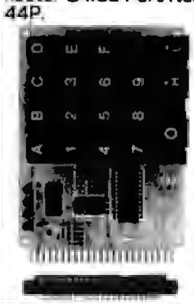
UART & BAUD RATE GENERATOR

• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P



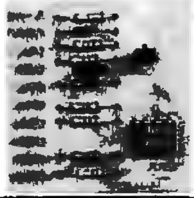
HEX ENCODED KEYBOARD E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.



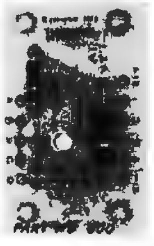
RS-232/ TTL INTERFACE

• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin gold plated edge connector • Board only $4.50 Part No. 232, with parts $7.00 Part No. 232A 10 Pin edge connector $3.00 Part No. 10P



RS-232/TTY INTERFACE

This board has two active circuits, one converts RS-232 to 20mA, and the other converts 20mA to RS-232. Requires +12 and -12 volts. Board only $4.50 Part No. 600, with parts $7.00 Part No. 600A.

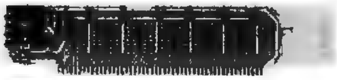


WAMECO PRODUCTS WITH ELECTRONIC SYSTEMS PARTS

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remex 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCBD $42.95
FPB-1 Front Panel. (Finally) IMSAI size hex displays. Byte or instruction single step. PCBD $42.95
MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCBD .... $24.95, $168 Kit
QMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only .... $34.95, $89.95 Kit
CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD .. $25.95, $69.95 Kit
RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD .... $25.95, $60.95 Kit
EPM-1 1702A 4K EPROM card PCBD .... $25.95, $49.95 with parts less EPROMS
EPM-2 2708/2716 16K/32K EPROM card PCBD .... $24.95, $49.95 with parts less EPROMS
QMB-9 MOTHER BOARD. Short Version of QMB-12. 9 Slots PCBD .... $30.95, $67.95 Kit
MEM-2 16Kx8 Fully Buffered 2114 Board PCBD .... $25.95, $269.95 Kit

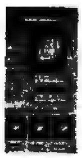
S-100 BUS ACTIVE TERMINATOR

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A



DC POWER SUPPLY

• Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp. • Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps. • Board only $12.50 Part No. 6085, with parts excluding transformers $42.50 Part No. 6085A



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Circle 125 on inquiry card.

Circle 126 on inquiry card.

The DATA-TRANS 1000

A completely refurbished **IBM** Selectric Terminal with built-in **ASCII** Interface.

$1395

Features:

- 300 Baud
- 14.9 characters per second printout
- Reliable heavy duty Selectric mechanism
- RS-232C Interface
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- Optional tractor feed available
- 15 inch carriage width

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Phone: (408) 263-9246

MICRO-PROCESSORS: FROM CHIPS TO SYSTEMS

This book cover all aspects of microprocessors, from the basic concepts to advanced interfacing techniques, in a progressive presentation. It is independent from any manufacturer, and presents uniform **standard** principles and design techniques, including the interconnect of a **standard** system, as well as specific components. It introduces the MPU, how it works internally, the system components (ROM, RAM, UART, PIO, others), the system interconnect, applications, programming, and the problems and techniques of system development. By R. Zaks. SYBEX. Ref. C201. $9.95

MICRO-PROCESSOR INTERFACING TECHNIQUES

Microprocessor interfacing is no longer an art. It is a set of techniques, and in some cases just a set of components. This comprehensive book introduces the basic interfacing concepts and techniques, then presents in detail the implementation details, from hardware to software. It covers all the essential peripherals, from keyboard to floppy disk, as well as the standard buses (S100 to IEEE 488) and introduces the basic troubleshooting techniques. (2nd Expanded Edition). By Austin Lesea and R. Zaks. Ref. C207 SYBEX. $11.95

PROGRAMMING THE 6502 PROGRAMMING THE Z80 PROGRAMMING THE 8080'

It covers all essential aspects of programming, as well as the advantages and disadvantages of the 6502 and should bring the reader to the point where he can start writing complete applications programs. For the reader who wishes more, a companion volume is available: The 6502 Applications Book. By R. Zaks. 6502: Ref. C202; Z80: Ref. C280; 8080: Ref. C208. SYBEX. Each $10.95

44 BUS MOTHER BOARD

Has provisions for ten 44 pin (.156) connectors, spaced 3/4 of an inch apart. Pin 20 is connected to X, and 22 is connected to Z for power and ground. All the other pins are connected in parallel. This board also has provisions for bypass capacitors. Board cost $15.00 Part No. 102. Connectors $3.00 each Part No. 44WP.

AN INTRODUCTION TO PERSONAL AND BUSINESS COMPUTING

No computer background is required. The book is designed to educate the reader in all the aspects of a system, from the selection of the microcomputer to the required peripherals. By Rodnay Zaks. Ref. C200. SYBEX $6.95

TVT COOKBOOK

Bk 1064 — by Don Lancaster. Describes the use of a standard television receiver as a microprocessor CRT terminal: Explains and describes character generation, cursor control and interface information in typical, easy-to-understand Lancascaster style. $9.95

COMPUTER PROGRAMMING HANDBOOK

A complete guide to computer programming & data processing. Includes many worked-out examples. By Peter Stesk, TAB $9.95

DIGITAL CASSETTE

5 min. each side. Box of 10 $9.95. Part No. C-5.

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U.S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U.S. dollars. Dealer inquiries invited. 24 hour order line (408) 226-4064.

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a PERCOM SAMPLER

For your SS-50 bus computer — the CIS-30+

- Interface to data terminal and *two* cassette recorders with a unit only 1/10 the size of SWTP's AC-30.
- Select 30, 60, or 120 bytes per second cassette interfacing, 300, 600 or 1200 baud data terminal interfacing.
- Optional mod kits make CIS-30+ work with *any* microcomputer. (For MITS 680b, ask for Tech Memo TM-CIS-30+—09.)
- KC-Standard/Bi-Phase-M (double frequency) cassette data encoding. Dependable self-clocking operation.
- Ordinary functions may be accomplished with 6800 Mikbug™ monitor.
- Prices: Kit, $79.95; Assembled, $99.95.

Prices include a comprehensive instruction manual. Also available: Test Cassette, Remote Control Kit (for program control of recorders), IC Socket Kit, MITS 680b mod documentation, Universal Adaptor Kit (converts CIS-30+ for use with any computer).

MIKBUG® Motorola, Inc.

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6809 Processor Card — With this SS-50 bus PC board, you'll be able to upgrade with the microprocessor that Motorola designers describe as the "best 8-bit machine so far made by humans."

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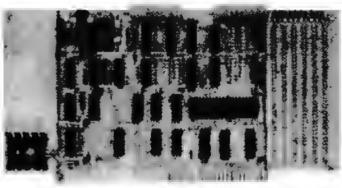
For your data storage — Pilon-30™ and Pilon-10™ data cassettes

- Orders-of-magnitude improvement in data integrity over ordinary audio cassettes.
- Pilon-coated pressure pad eliminates lint-producing felt pad of standard audio cassettes.
- Smooth pilon coating minimizes erratic tape motion.
- Foam pad spring is energy absorbing. Superior to leaf spring mounted pad which tends to oscillate and cause flutter.
- Five-screw case design virtually precludes deformation during assembly.
- Price: $2.49.



For your S-100 computer — the CI-812

- Both cassette and data terminal interfacing on one S-100 bus PC board.
- Interfaces *two* recorders. Record and playback circuits are independent.
- Select 30, 60, 120, or 240 bytes per second cassette interfacing, 110 to 9600 baud data terminal interfacing.
- KC-Standard/Bi-Phase-M (double frequency) encoded cassette data. Dependable self-clocking operation.
- Optional firmware (2708 EPROM) Operating System available.
- Prices: kit, $99.95; assembled, $129.95.

Prices include a comprehensive instruction manual. In addition to the EPROM Operating System, a Test Cassette, Remote Control Kit (for program control of recorders), and an IC Socket Kit are also available.

CASSETTE SOFTWARE

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7445N	.60
7447N	.60
7448N	.80
7450N	.17
7474N	.29
7475N	.49
7485N	.88
7489N	2.00
7490N	.43
7492N	.43
7493N	.43
7495N	.60
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74163N	.87
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74LS75N	.47
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74LS93N	.51
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74LS107N	.35
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74LS113N	.35
74LS132N	.72
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LM340K-5	1.35
LM340K-8	1.35
LM340K-12	1.35
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LM340T-5	1.25
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CD4020	1.02
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CD4022	.86
CD4023	.28
CD4024	.75
CD4025	.28
CD4026	1.51
CD4027	.38
CD4028	.79
CD4029	1.02
CD4030	.28
CD4035	1.02
CD4040	1.02
CD4042	.71
CD4043	.83
CD4044	.83
CD4046	1.67
CD4049	.38
CD4050	.38
CD4051	1.13
CD4060	1.42
CD4066	.71
CD4068	.40
CD4069	.40
CD4070	.40
CD4071	.28
CD4072	.28
CD4073	.28
CD4075	.28
CD4076	1.75
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CD4082	.28
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The **Super Elf** includes a **ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest** address and data bus displays **before, during** and **after** executing instructions. Also, CPU mode and instruction cycle are decoded and displayed on 8 LED indicators.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

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Many schools and universities are using the Super Elf as a course of study. OEM's **use it** for training and research and development.

Remember, other computers only offer Super Elf features at additional cost or not at all. **Compare before you buy. Super Elf Kit $106.95. High address option $8.95. Low address option $9.95. Custom Cabinet** with drilled and labelled plexiglass front panel **$24.95.** Expansion Cabinet with room for 4 S-100 boards **$41.00. NiCad Battery Memory Saver Kit $6.95.** All kits and options also come completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year.

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This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and a **cassette interface.** Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf.** The board includes slots for up to 6K of **EPROM** (2708, 2758, 2716 or TI 2716) and is **fully socketed. EPROM** can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/ editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability and video graphics driver with blinking cursor. Break points can be used with the register save feature to isolate program bugs quickly, then follow with single step. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up. Improvements and revisions are easily done with the monitor. If you have the **Super Expansion Board** and **Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports** with **full handshake.** They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two **S-100** slots for static RAM or video boards. A Godbout 8K RAM board is available for $135.00. Also a 1K Super Monitor version 2 with video driver for full capability display with Tiny Basic and a video interface board. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set** with ribbon cable is available at $12.50 for easy connection between the **Super Elf** and the **Super Expansion Board.**

The Power Supply Kit for the Super Expansion Board is a 5 amp supply with multiple positive and negative voltages $29.95. Add $4.00 for shipping. Prepunched frame $7.50. Case $10.00. Add $1.50 for shipping.

Multi-volt Computer Power Supply

8v 5 amp, ±18v .5 amp, 5v 1.5 amp, −5v .5 amp, 12v .5 amp, −12 option. ±5v, ±12v are regulated. Kit $29.95. Kit with punched frame $37.45. Woodgrain case $10.00.

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Converts digital clocks from AC line frequency to crystal time base. Outstanding accuracy. Kit includes: PC board, IC, crystal, resistors, capacitors and trimmer.

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6502 based single board with full ASCII keyboard and 20 column thermal printer. 20 char. alphanumeric display, ROM monitor, fully expandable. $375.00. 4K version $450.00. 4K Assembler $85.00, 8K Basic Interpreter $100.00. Power supply assy. in case $60.00. AIM 65 in thin briefcase with power supply $485.00.

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Includes everything except case. 2-PC boards. 6-.50" LED Displays. 5314 clock chip, transformer, all components and full instructions. Orange displays also avail. **Same kit w/.80" displays.** Red only. **$21.95** Case **$11.75**

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Shipping charges will be added on charge cards.

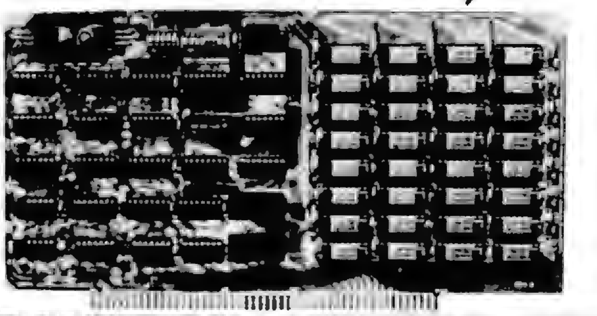
FREE: Send for your copy of our NEW 1979 QUEST CATALOG. Include 28¢ stamp.

Circle 311 on inquiry card.

Circle 312 on inquiry card

Visit our new retail location!

SD EXPANDORAM
The Ultimate S-100 Memory



The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisable on-board refresh, and IT WORKS!

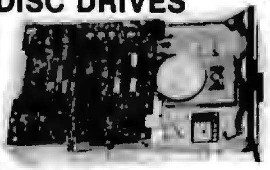
- Interfaces with Altair, IMSAI, SOL-8, Cromenco, SBC-100, and others.
- Bank Selectable
- Phantom
- Power 8VDC, ± 16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Popular 4116 RAMS
- PC Board is doubled solder masked and has silk-screen parts layout.

- Extensive documentation clearly written
- Complete Kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required.
- 16K boundries and Protection via Dip Switches
- Designed to work with Z-80, 8080, 8085 CPU's.

EXPANDO 64 KIT (4116)

16K	$249
32K	$324
48K	$399
64K	$474

DISC DRIVES



SHUGART SA 400 5¼"
110 KB, 35 tracks.
SHUGART SA 400 **$295.00**

SHUGART SA 400
with attractive metal case with cutouts for Data Cable switch, fuse and power cord.
LOBO SA400-C **$325.00**

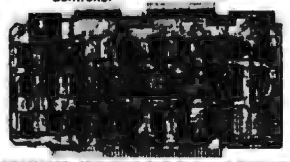
SHUGART SA400
with Cabinet and Power Supply. Assembled, tested & guaranteed
LOBO SA400-PSC **$395.00**

SHUGART 801R 8"
6.4 megabits, single or double density, hard or soft sector, write protect, and more
SHUGART 801R **$449.00**

Siemens FDD 200-8 8"
double-sided double density
$650.00

DISC CONTROLLER

SD "VERSAFLOPPY" Kit
The Versatile Floppy Disk Controller — **Only $159^00**



FEATURES IBM 3740 Soft Sectored Compatible. S-100 BUS Compatible for Z-80 or 8080. Controls up to 4 Drives (single or double sided) Directly controls the following drives
1 Shugart SA400/450 Mini Floppy
2 Shugart SA800/850 Standard Floppy
3 PERSCI 70 and 277
4 MFE 700/750
5 CDC 9404/9406
6. GSI/Siemans FDD120-8.
34 Pin Connector for Mini Floppy 50 Pin Connector for Standard Floppy Operates with modified CP/M operating system and C-Basic Compiler The new "Versafloppy" from S.D. Computer Products provides complete control for many of the available Floppy Disk Drives. Both Mini and Full Size FD1771B-1 Single Density Controller Chip Listings for Control Software are included in price.

CPM for SD Versafloppy **$100^00**

DUAL SHUGART DISC DRIVES

New from Lobo Drives, a dual Cabinet complete with power supply, and Shugart 801R disc drives.

- Cabinet accepts 2 801R drives mounted side by side horizontally.
- Power Supply for 2 drives
- Ad-on drives available
- Assembled, tested and guaranteed by Lobo Drives.
- Single or double density • Hard or soft sector • Write Protect
- Capacity: Unformatted single density 3.2 megabits
  double density 6.4 megabits
  IBM format, 2 megabits
- 500 KBS transfer, 77 tracks.
- Shugart 800 Series Compatible

LOBO 801R-1 Pcs. Dual Cabinet with 1 drive **$599.00**
LOBO 801R-2 Pcs. Dual Cabinet with 2 drives **$1025.00**
SHUGART 801R Ad-on disc drive **$449.00**

CONTINENTAL SPECIALTIES CORPORATION

CSC Logic Probes and Digital Pulsers

LOGIC PROBES

CSC logic probes are the ultimate tool for breadboard design and testing. These hand-held units provide an instant overview of circuit conditions. Simple to use, just clip power leads to circuit's power supply, set logic family switch to TTL/DTL or CMOS/HTL. Touch probe to test node. Trace logic levels and pulses through digital circuits. Even stretch and latch for easy pulse detection Instant recognition of high, low or invalid levels, open circuits and nodes. Simple, dual-level detector LEDs tell it quickly, correctly. HI (Logic "1"); LO (Logic "0") Also incorporates blinking pulse detector. e.g., HI and LO LEDs blink on or off, tracking "1" or "0" states at square wave frequencies up to 1.5 MHz Pulse LED blinks on for ⅓ second during pulse transition Choice of three models to meet individual requirements; budget, project and speed of logic circuits

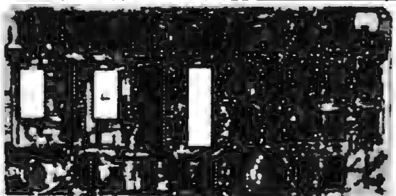
MODEL LP-1
Hand-held logic probe provides instant reading of logic levels for TTL, DTL, HTL or CMOS. **Input Impedance:** 100,000 ohms. **Minimum Detectable Pulse:** 50 ns. **Maximum Input Signal (Frequency):** 10 MHz. **Pulse Detector (LED):** High speed train or single event. **Pulse Memory:** Pulse or level transition detected and stored
CSC Model LP-1 Logic Probe—Net Each .... ~~$44.95~~ $42.70

MODEL LP-2
Economy version of Model LP-1. Safer than a voltmeter. More accurate than a scope **Input Impedance:** 300,000 ohms. **Minimum Detectable Pulse:** 300 ns. **Maximum Input Signal (Frequency):** 1.5 MHz. **Pulse Detector (LED):** High speed train or single event. **Pulse Memory:** None.
CSC Model LP-2 Logic Probe—Net Each .... ~~$24.95~~ $23.70

MODEL LP-3
High speed logic probe Captures pulses as short as 10 ns Input impedance: 500,000 ohms Minimum Detectable Pulse: 10 ns Maximum Input Signal (Frequency): 50 MHz Pulse Detector (LED): High speed train or single event Pulse Memory: Pulse or level transition detected and stored.
CSC Model LP-3 Logic Probe—Net Each .... ~~$69.95~~ $66.45

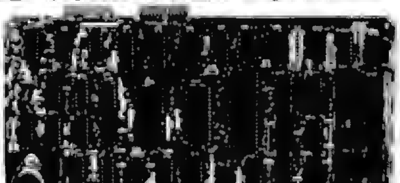
DIGITAL PULSER
The ultimate in speed and ease of operation. Simply connect clip leads to positive and negative power, then touch DP-1's probe to a circuit node. automatic polarity sensor detects circuit's high or low condition Depress the pushbutton and trigger an opposite polarity pulse into the circuit Fast troubleshooting includes injecting signals at key points in TTL, DTL, CMOS or other popular circuits Test with single pulse or 100 pulses per second via built-in dual control push-button; button selects single shot or continuous modes. LED indicator monitors operating modes by flashing once for single pulse or continuously for a pulse train. Completely automatic, pencil-size lab/field pulse generator for any family of digital circuits. Output: Tri-state. Polarity: Pulse-sensing auto-polarity. Sync and Source: 100 mA. Pulse Train: 100 pps. LED Indicator: Flashes for single pulse, stays lit for pulse train
CSC Model DP-1 Digital Pulser—Net Each .... ~~$74.95~~ $71.20

SD COMPUTER BOARDS



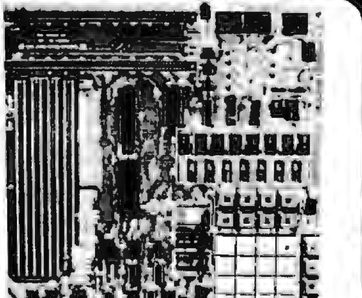
$319 KIT
VDB-8024 Video Display Board
With On-Board Z80 Microprocessor

- Full 80 Characters by 24 lines display
- Characters displayed by High Resolution 7 × 10 Matrix
- Keyboard Power and Interface
- Composite Video Output
- Separate TTL Level Synchronization and Video Outputs
- 2K Bytes Independent On Board Memory
- On-Board Z80 Microprocessor
- Glitch Free Display
- 96 Upper and Lower Case Characters
- 32 Special Character Set
- 128 Additional user Programmable Characters
- Full Cursor Control
- Forward and Reverse Scrolling Capability
- Operates as an Independent Terminal
- Variable Speed Display Rate
- Blinking, Underlining, Field Reverse, Field Protect and Combinations



$239 KIT
SBC-100 Single Board Computer
with On-board RAM, PROM, CTC

- Four Channel Counter/Timer (Z80-CTC)
- Software Programmable Baud Rate Generator
- S-100 Bus Compatible
- No Front Panel Required for Operation
- Optional Vectored Interrupts
- Z80 Central Processing Unit
- 1024 Bytes of Random Access Memory
- 8K Bytes of Available PROM
- Serial Input/Output Port with both Synchronous and Asynchronous Operation
- Parallel Input and Output Ports



$249
Z80 Starter Kit
A Complete Microcomputer on a Board

- Z80 Central Processing Unit with 158 Instructions
- On Board Keyboard and Display
- Kansas City Standard Cassette Interface
- PROM Programmer Built on-board
- Expansion provision for two S-100 Connectors
- Wire Wrap area for custom circuitry
- Single 5 Volt Operation when not programming
- 1K Bytes of RAM (Expandable to 2K Bytes)
- 1K Bytes of RAM (Expandable to 2K Bytes)
- 4 Channel Hardware Counter/Timer (Z80-CTC)
- Two Bi-directional 8-bit I/O Ports (Z80-PIO)
- Switch Selectable PROM or Monitor Restart
- 2K Byte Z80 Monitor in ROM
- Memory Examine and Change
- Port Examine and Change
- Z80 CPU Register Examine and Change
- Up to 5 Programmable Breakpoints
- Single Step through RAM or PROM
- Audio Cassette Load and Dump
- Vectored Interrupts provided by Z80-CTC and Z80-PIO
- Ideal for Experimentation and Evaluating the Z80 CPU

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Circle 312 on inquiry card.

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TRS-80 DISC DRIVE

$395.00

Shugart SA400, housed in an attractive metal case, complete with power supply and termination network. All you need to do is connect the drives to your expansion interface.

Portable Miniscopes for Electronic Professionals on the Go!!!

The Standout Oscilloscope development of the decade!!! Now -30MHz, dual trace model. Compare the performance, then compare the price.

NLS

1¢ sale Probes 1¢ with purchase of scope

• 30-Megahertz bandwidth • Accuracy 3% full scale. • Internal, line or external trigger. • Batteries and charger/transformer unit included • Graticule: 4x5 divisions, each division 0.25" • Time base: 1 micro sec. to 0.5 sec/div 21 settings • Verticle Gain: 0.01 to 50 Volts/div. 12 settings • Size 2.9"H x 6.4"W x 8.5"D. 3.5 lbs. • TEST MOST DIGITAL LOGIC CIRCUITS INCLUDING MICROPROCESSORS •.

41-141	Deluxe 10tol probe with 4 interchangeable tips	$27.00
41-37	Deluxe 10tol/1tol probe with 4 interchangeable tips	$38.50
41-180	leather carrying case	$45.00
MS-15	Single trace 15 MHz	$318.00
MS-215	Dual trace 15 MHz	$435.00

1410 $835.00

- Separate Integral 12-key Numeric Pad
- All 128 ASCII Codes
- 64 Displayable Characters
- 24x80 Screen Configuration
- High Resolution using a 5x7 Dot Matrix
- TTY-Style Keyboard Layout
- Cursor Addressing and Sensing
- EIA Interface
- Eight Selectable Transmission Rates up to 9600 Baud
- Microprocessor Based
- Remote Commands
- Attractive Styling for Contemporary Environments

Hazeltine 1400 same as 1410 less numeric pad $735.00

1500 Reg. ~~$1225~~ $1098.00

- All 128 ASCII Codes
- 94 Displayable Characters Including Lower Case
- 24x80 Screen Configuration
- High-Resolution Characters Using a 7x10 Dot Matrix
- ANSI Standard Keyboard Layout including Numeric Pad
- Cursor Addressing and Sensing
- Dual Intensity
- EIA and 20MA Interface
- Nine Selectable Transmission Rates Up to 19.2 KB
- Auxiliary EIA Output
- Remote Editing Commands
- Standard or Reverse Video
- Microprocessor Based

3M Scotch® Brand DISKETTES

Part #	Sides/ Density	Sectoring	Price Box of 10
		8"	
740-OP	1/single	Soft-IBM	$39.95
740/2-OP	2/single	Soft-IBM	$75.00
740-32P	1/single	32-Shugart 801	$39.95
740/2-32P	2/single	32-Shugart 801	$75.00
741-O	1/double	Soft-Shugart Dbl	$59.00
		5"	
744-OK	1/single	Soft-Shugart SA400 (TRS-80)	$51.00*
744-10K	1/single	Soft/10 SA400	$51.00*
744-16K	1/single	Soft/16 Micropolis	$51.00*

*Price includes Kas-ette/10 Storage Box a $5.00 Value

"DON'T SETTLE FOR ANYTHING LESS THAN SCOTCH"

ALL THE FEATURES OF THE "1500" PLUS . . .

- Cursor Control Keys
- Protected/Unprotected Data
- Transmit Page, Line or Batches of Information
- Function Keys—up to 127
- Tab/Back Tab/Auto Tab
- Format Mode with Insert and Delete Line Keys
- 31 Remote Commands including "Terminal Status"

1510 Reg. ~~$1895~~ $1175

ACOUSTIC MODEM NOVATION CAT

- 0-300 Baud
- Bell 103
- Answer, Originate

Reg. $198.00

Sale $189.00

ALL THE FEATURES OF THE "1510" PLUS . . .

Separate Microprocessor-Controlled Printer Interface which allows:
- Interfacing of both serial and parallel printers
- Printer speed independent of communications baud rate
- Printer control codes to be sent by the CPU and received by the printer without restriction or alteration of the terminal (especially useful for wide carriage applications)
- Information to be transmitted directly to either the printer or the terminal, or to both
- Operating Modes/Remote Commands; Remote/Local Print; Printer On-Line with/without Display; Printer Off-Line

1520 Reg. ~~$1650~~ $1495.00

PRICE DOES NOT INCLUDE SHIPPING

CONTINENTAL SPECIALTIES CORPORATION

CSC

100 MHz 8-Digit Counter

- 200 Hz-100 MHz Range
- 6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable - completely self contained
- Size - 1.75" x 7.38" x 5.63"
- Four power sources, i.e. batteries. 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply.

~~$134.95~~ **Sale $120.00**

ACCESSORIES FOR MAX 100: Mobile Charter Eliminator use power from car battery Model 100-CLA $3.95. Charger/Eliminator use 110 VAC Model 100 — CAI $9.95

CONTINENTAL SPECIALTIES CORPORATION

CSC

SALE

REG. ~~$59.95~~

LOGIC MONITOR 1

Trace signals through all types of digital circuits. Unit clips over any DIP IC up to 16 pins. Each of its 16 contacts connects to a single-bit level detector that drives a high-intensity, numbered LED readout activated when the applied voltage exceeds a fixed 2 V threshold. Logic "1" turns LED on; logic "0" keeps LED off. A power-seeking gate network automatically locates supply leads and feeds them to the LM-1's internal circuitry. Saves minutes, even hours in design, troubleshooting, debugging of equipment. **Voltage Threshold:** 2 V ± 0.2 V. **Input Impedance:** 100,000 ohms. **Input Voltage Range:** 4-15 V max. across any two or more inputs. **Current Drain:** 200 mA at 10 V. **Size:** 4" l. x 2" w. x 1.75" d. when open. **Weight:** 3 ozs.

CSC Model LM-1 Logic Monitor—Complete.
Sale Price $54.95

CENTRONICS 779 PRINTERS

- Use with TRS-80
- Parallel interface
- Continuous variable printing density 80-132 characters per line
- 5x7 dot matrix
- Prints on plain paper, sheets, rolls, fan fold
- Form thickness control
- Horizontal and vertical form positioning

779-1 pinch roll friction feed
Reg. $1250 **$950.00**

779-2 tractor feet
Reg. $1400 **$1050.00**

Call for Discount Prices on Other Centronics Printers

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Prices subject to change without notice.
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Circle 312 on inquiry card.

HICKOK LX303 $74.95

HICKOK LX303

$74.95*

.5%, 3½ digit 19 Range DVM. ½" LCD displays runs 200 hrs on 1 battery. 10 Meg Ohm Input. 1 yr. guarantee, made in U.S.A., test leads included.

Available Accessories

RC-3 115V AC Adapter $7.50
CC-3 Deluxe Padded Vinyl Carrying Case $7.50
VP-10 X10 DCV Probe Adapter/ Protector 10Kv $14.95
VP-40 40Kv DC Probe $35.00
CS-1 10 Amp Current Shunt $14.95

***FREE**

Just for Asking.
FREE BATTERY with your meter.

RS232 & "D" TYPE CONNECTORS

P = Plug-Male S = Socket-Female C = Cover-Hood

PART NO.	DESCRIPTION	PRICE 1-4	5-9	10-24
DE-9P	9 Pin Male	1.50	1.30	1.20
DE-9S	9 Pin Female	2.15	2.05	1.95
DE-9C	9 Pin Cover	1.50	1.30	1.15
DA15P	15 Pin Male	2.20	2.00	1.80
DA15S	15 Pin Female	3.20	3.00	2.80
DA15C	15 Pin Cover	1.60	1.45	1.30
DB-25P	25 Pin Male	2.90	2.60	2.50
DB-25S	25 Pin Female	3.75	3.65	3.40
DB51212-1	1 pc. Grey Hood	1.65	1.40	1.20
DB1226-1A	2 pc. Black Hood	1.80	1.60	1.50
DB110963-3	2 pc. Grey Hood	1.60	1.56	1.36
DC37P	37 Pin Male	3.95	3.80	3.60
DC37S	37 Pin Female	5.75	5.50	5.20
DC37C	37 Pin Cover	2.20	1.95	1.75
DD50P	50 Pin Male	4.95	4.75	4.50
DD50S	50 Pin Female	7.50	7.20	6.90
DD50C	50 Pin Cover	2.50	2.20	2.10
D20418-S	Hardware Set (2 pair)	1.00	.80	.70

MALE · FEMALE

Connector for CENTRONICS 700 SERIES:
Amphenol 57-30360 for back of Centronics 700 Series printers
1-4 — $9.00 5-up — $7.50

SALE S-100 BUS EDGE CONNECTORS SALE

S100-WWG 50/100 Cont. .125 ctrs. 3 LEVEL WIRE WRAP .025" sq. posts on .250 spaced rows. GOLD PLATED
1-4 $4.00 · 5-9 $3.75 · 10-24 $3.50

S100-STG 50/100 Cont. .125 ctrs DIP SOLDER TAIL on .250 spaced rows for VECTOR IMSAI CROMENCO mother boards GOLD plated
1-4 $3.50 · 5-9 $3.25 · 10-24 $3.00

S100ALT 50/100 Cont .125 ctrs. DIP SOLDER TAIL on .140 spaced rows for ALTAIR motherboards GOLD plated
1-4 $4.50 · 5-9 $4.25 · 10-24 $4.00

S100SE 50/100 Cont .125 ctrs PIERCED SOLDER EYELET tails GOLD
1-4 $5.00 · 5-9 $4.50 · 10-24 $4.00

Other Popular Edge Connectors

D2244-SSE 22/44 Cont .156 ctrs PIERCED SOLDER EYELET tails GOLD plated
1-4 $3.00 · 5-9 $2.60 · 10-24 $2.30

D2244-6WW 22/44 Cont .156 ctrs WIRE WRAP tails. GOLD.
1-4 $3.95 · 5-9 $3.78 · 10-24 $3.40

CG-1 IMSAI Style Card Guides 5/$1.00

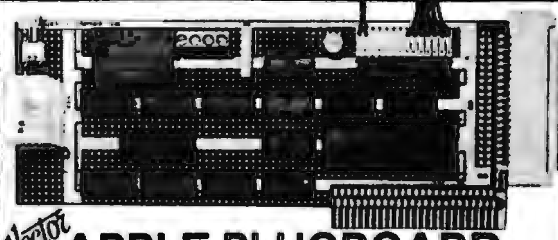
See our July Ad for many other connectors.

3 LEVEL GOLD WIRE WRAP SOCKETS

Sockets purchased in multiples of 50 per type may be combined for best price.

	1-9	10-24	25-99	100-249	250-999
8 pin	.40	.36	.34	.31	.27
14 pin	.39	.38	.36	.32	.31
16 pin	.50	.42	.40	.38	.34
18 pin	.70	.60	.55	.50	.45
20 pin	.90	.80	.75	.65	.62
22 pin	.95	.85	.80	.70	.65
24 pin	.96	.85	.80	.70	.65
28 pin	1.25	1.15	1.00	.95	.90
40 pin	1.65	1.45	1.35	1.20	1.10

All sockets are GOLD 3 level closed entry. 2 level Tail, Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION.



Vector APPLE PLUGBOARD

Vector 4609 Peripheral Interface Plugboard for construction of custom circuits. Plug compatible with Apple II, Commodore PET and Super Kim microcomputers. Three connectors, in addition to the standard 25/50 system bus, are available for input/output. A 20/40-contact card-edge connector, fabricated on the rear of the board, mates with a 3-M type ribbon connector. Alternatively, a right-angle solder-tail header may be positioned in this same location. The Model 4609 also accomodates the miniature SIP-type connectors which may be placed on the periphery or in mid-board.

1-4	5-9	10-24
$19.95	$17.96	$15.96

8803 MOTHER BOARD FOR S100 BUS MICRO-COMPUTERS — Vector

- Kit includes 12 tantalum capacitors for +5, +12, −12 buses and mounting spacers
- Wiring side shown. Component side bare epoxy glass with white markings for component locations
- 0.10 epoxy glass board with 2 ounce copper, solder plated and .030 cutouts for board for leads
- Solder mask with solder windows on etched circuits to avoid accidental short circuits
- Mounts 11 receptacles with 100 contacts (2 rows) at .125 centers with .250 row spacing. Vector part number R681-2, or mounts 18 receptacles plus interconnections to smaller mother board for expansion
- Includes etched circuits and instructions for option of active pull up or floating terminations
- Large buses: +8V and GND (10 AMPS), ±12V or 16V (7 AMPS). Current ratings are per Mil. STD-275 with 10°C rise
- Fits in Vector gem enclosures
- Fits in IMSAI 8080 microcomputer as expander board

Price: $29.50

Vector Plugboards

8800V
Universal Microcomputer/processor plugboard, use with S-100 bus. Complete with heat sink & hardware 5.3" x 10" x 1/16"

1-4	5-9	10-24
$19.95	$17.95	$15.95

8801-1
Same as 8800V except plain, less power buses & heat sink

1-4	5-9	10-24
$15.22	$13.79	$12.18

3682 9.6" x 4.5" $10.97
3682-2 6.5" x 4.5" $9.61
Hi-Density Dual-In-Line Plugboard for Wire Wrap with Power & Grd. Bus Epoxy Glass 1/16" 44 pin con. spaced .156

3677 9.6" x 4.5" **$10.90**
3677-2 6.5" x 4.5" **$9.74**
Gen. Purpose D.I.P. Boards with Bus Pattern for Solder or Wire Wrap. Epoxy Glass 1/16" 44 pin con. spaced .156

3662 6.5" x 4.5" **$7.65**
3662-2 9.6" x 4.5" **$11.45**
P pattern plugboards for IC's Epoxy Glass 1/16" 44 pin con. spaced .156

3690-12 CARD EXTENDER
Card Extender has 100 contacts 50 per side on .125 centers. Attached connector is compatible with S-100 Bus Systems. $25.83
3690 6.5" 22/44 pin .156 ctrs. Extenders $13.17

1/16 Vector BOARD
.042 dia holes on 0.1 spacing for IC's

PART NO.	SIZE	PRICE 1-9	10-19
Phenolic			
64P44XXXP	4.5x6.5"	$1.56	$1.40
169P44XXXP	4.5x17"	$3.69	$3.32
Epoxy Glass			
64P44	4.5x6.5"	$1.79	$1.61
84P44	4.5x8.5"	$2.21	$1.99
169P44	4.5x17"	$4.52	$4.07
169P84	8.5x17"	$8.03	$7.23

TRS-80/APPLE MEMORY EXPANSION KITS

4116's RAMS
from Leading Manufacturers
(16Kx1 200ns)

8 for $75.00

Add $3.00 for programming Jumpers for TRS-80 Keyboard

IC SOCKET SALE

14 pin Low Profile
10/$2.10 **100/$14.00**
16 pin Low Profile
10/$2.20 **100/$16.00**
24 pin Low Profile
3/$1.00 **40/$10.00**
40 pin Solder Tail
3/$1.00 **40/$10.00**
24 pin Dip Plug with cover
3/$1.00 **40/$10.00**

WOW 14 & 16 PIN GOLD 3 LEVEL WIRE WRAP SOCKES

14 - G3 100 for $33.00
16 - G3 100 for $33.00
50 of each for $35.00

PANAVISE

PANAVISE TILTS, TURNS, AND ROTATES TO ANY POSITION. IT HOLDS YOUR WORK EXACTLY WHERE YOU WANT IT.

MEMORY MEMORY

2102LIPC Low Power 450ns in lots of 25	$1.10
2102AL-2 Low Power 250ns in lots of 25	$1.25
2114-3L 1Kx4 300 ns Low Power	8/$50.00
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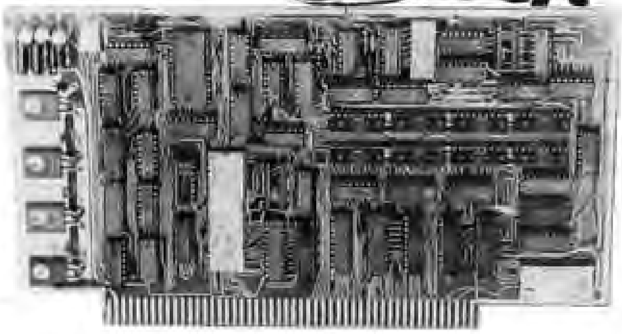

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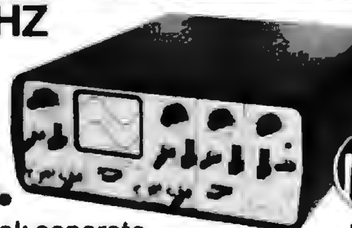

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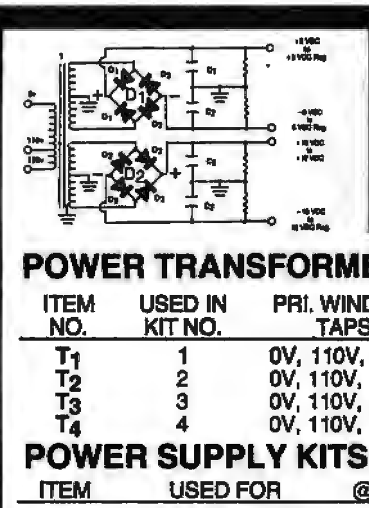

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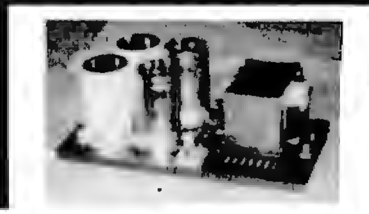

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ITEM NO.	USED IN KIT NO.	PRI. WINDING TAPS	SECONDARY WINDING OUTPUTS 2×8 Vac	2×14 Vac	2×24 Vac	SIZE W × D × H	UNIT PRICE
T_1	1	0V, 110V, 120V	2×9A	2×2.5A	———	3¾"×3⅝"×3⅛"	19.95
T_2	2	0V, 110V, 120V	2×12.5A	2×3.5A	———	3¾"×4⅜"×3⅛"	25.95
T_3	3	0V, 110V, 120V	2×9A	2×2.5A	2×2.5A	3¾"×4⅜"×3⅛"	27.95
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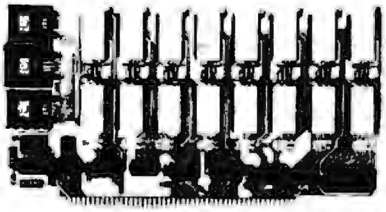

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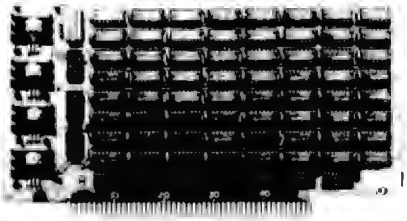

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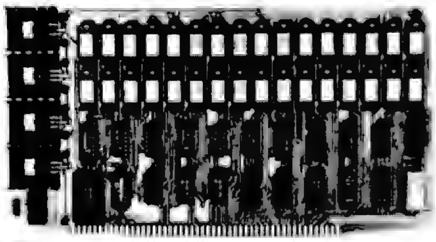

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FULLY STATIC, AT DYNAMIC PRICES

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1. Addressable as four separate 4K Blocks.
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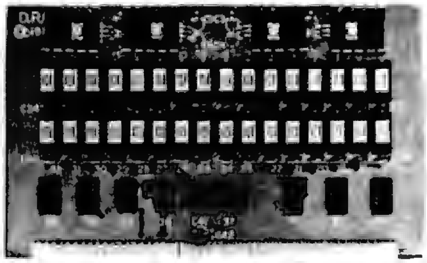

FULLY STATIC AT DYNAMIC PRICES

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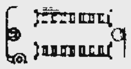

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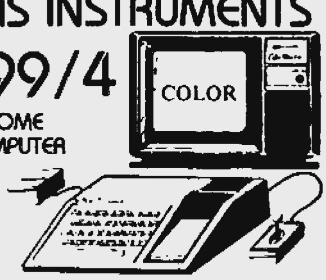

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SYM-1 $245

Part Number:CPK-5002A

6502- BASED SINGLE BOARD COMPUTER WITH KEYBOARD/DISPLAY, KIM-1 HARDWARE COMPATIBLE, COMPLETE DOCUMENTATION.

SYM-1 CASE, ENX-000005 .... $39.95

THE BIG Z

THE NEW Z-80

CPU BOARD FROM JADE

Features Include: ■ S-100 Compatible, available in 2MHz or 4MHz versions. ■ On-board 2708, 2716, 2516, or 2532 EPROM can be addressed on any 1K, 2K, or 4K boundary, with power-on jump to EPROM. ■ On-board EPROM may be used in SHADOW mode, allowing full 64K RAM to be used. ■ Automatic MWRITE generation if front panel is not used. ■ On-board USART for synchronous or asynchronous RS232 operation (on-board baud rate generator). ■ Reverse-channel capability on USART allows use with buffered peripherals or devices with "not-ready" signal.

2MHz-
Kit: CPU-30200K, 2 lbs $149.95
Assembled and Tested: CPU-30200A, 2 lbs $199.95

BARE BOARD CPU-30200B....$40.00

4 MHz-
Kit: CPU-30201K, 2 lbs $159.95
Assembled and Tested CPU-30201A, 2 lbs $209.95

GRI KEYBOARDS

Features Include: Full 128 character ASCII ■ Tri-Mode Mos encoding ■ MOS/DTL/TTL compatible output ■ Two-key rollover ■ Level and pulse strobe ■ Shift and alpha lock ■ Selectable parity ■ Positive or Negative Logic ■ All new OEM grade components ■ Gold contact, low bounce keyswithces ■ Rugged G-10 printed circuit board ■ Custom 2 shot molded keycaps ■ Low power consumption ■ Optional numeric pad available ■ Custom enclosures available.

Model 756A
Assembled- KBA-30756A $79.95
Model 753K (53 Key, Teletype Keyboard with lower case)
Kit- KBA-30753K $65.95

DB25-CONNECTORS

DB25P- CND1251 .... $2.25
DB25S- CND1252 .... $3.25
DB25C- CND1253 (Cover) $1.50
RS232 Special: DB25P, DB25S, plus Hood only $6.50 (Part Number: CND-1250)

Circle 195 on inquiry card.

Circle 296 on inquiry card.

page

Wire Wrap Tools

BATTERY HOBBY TOOL*

- Auto Indexing
- Anti-Overwrapping
- Modified Wrap

BW2628	Tool	$19.85
BT30	#30 Bit	2.95
BT2628	#26 Bit	7.95
BC1	Batteries & Charger..	11.00

*Requires 2 "C" Niced Batteries

BATTERY INDUSTRIAL TOOL*

- Accepts Industrial Bits and Sleeves (Gardner Denver or equiv.)
- Industrial Motor for Production Wire-wrapping
- Backforce Avail. (Recommended for #30).

BW928	Tool	49.95
BW928BF	Backforce Model	52.95
Bit & Sleeve	Specify #22-#30.....	29.50
BC1	Batteries & Charger..	11.00

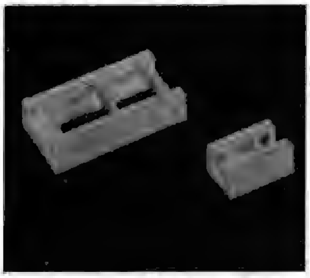
ELECTRIC INDUSTRIAL TOOL

- Accepts Industrial Bits and Sleeves (Gardner Denver or equiv.)
- Industrial Motor for Production Wire-wrapping
- Backforce Avail. (Recommended for #30).

EW8	Tool	85.00
EW28F	Backforce Model	92.90
Bit & Sleeve	#22 or #30...........	29.50

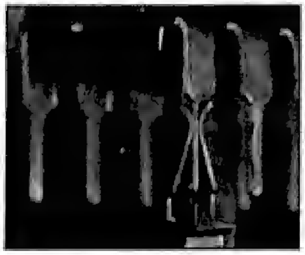
RN IC Sockets

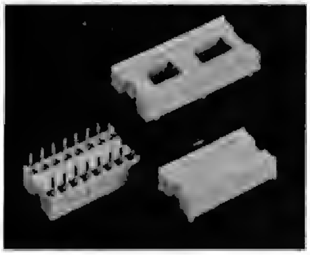
RN HIGH RELIABILITY eliminates trouble. "Side-wipe" contacts make 100% greater surface contact with the wide, flat sides of your IC leads for positive electrical connection.



WIRE WRAP SOCKETS
3-level Gold
Closed Entry Design
All Prices Include Gold.
2-level Sockets Also Available

	1-9	10-24	25-99	100-249	250-1K
8 Pin	40	.36	.34	.31	.27
14 Pin		.39	.37	.34	.32
16 Pin		.42	.40	.36	.34
18 Pin	.70	.60	.55	.50	.45
20 Pin	.90	.80	.75	.65	.62
22 Pin	.95	.85	.80	.70	.65
24 Pin	.95	.85	.80	.70	.65
25 Pin st	1.25	1.15	1.00	.95	.90
28 Pin	1.25	1.15	1.00	.95	.90
40 Pin	1.65	1.45	1.35	1.20	1.10





SOLDER TAIL
Low Profile Tin
Closed Entry Design

	1-9	10-24	25-99	100-249	250-1K
8 Pin	.21	.18	.16	.15	.14
14 Pin	—	.19	.17	.15	.13
16 Pin	—	.21	.19	.17	.15
18 Pin	.30	.28	.27	.26	.25
20 Pin	.35	.34	.33	.32	.31
22 Pin	.36	.34	.30	.27	.26
24 Pin	.38	.36	.32	.29	.28
28 Pin	.45	.44	.43	.40	.39
40 Pin	.63	.62	.61	.58	.57

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R-30-TRI	Refill for TRI Color	3.75
INS 1416	14 & 16 pin Insertion Tool	3.25
MOS 40	40 pin Insertion Tool	7.50
EX-1	IC Extractor Tool	1.49
H-PCB-1	Hobby PC Board	4.99
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WSU 30M	Same as WSU 30 with Modified Wrap	7.50

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- **CODs, VISA & MC orders will be charged shipping**
- **Most orders shipped next day.**

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ASSEMBLED		Kit	
450ns.	599.00	450ns.	539.95
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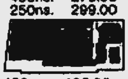
Bare Board 49.95
Bare Board w/all parts less mem. 99.95

S-100 16K (uses 2114) KIT (exp. to 32K)

ASSEMBLED			
450ns.	325.00	450ns.	279.00
250ns.	375.00	250ns.	299.00

Bare Board 49.95



LOGOS I 8K
ASSEMBLED
450 ns. 169.95 KIT 450ns. 125.95
250ns. 189.95 250ns. 149.95
Bare PC Board w/Data $21.95
Now over 1 year successful field experience
"Special Offer" Buy (4) 8K 450ns. Kits $117.00

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3. VISTA V-1000 FLOPPY DISK SYSTEM
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★ Bank Selectable ★ Uses 4115 or 4116 200 ns.
★ Write Protect ★ Power 8VDC, ±16VDC
★ Phantom ★ Lowest Cost/Bit

Expando 32 Kit (4115)		Expando 64 Kit (4116)	
8K	$158.00	16K	$248.95
16K	$199.00	32K	$369.00
24K	$299.00	48K	$469.00
32K	$349.00	64K	$565.00

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★ Memory Mapping ★ Low Power
★ Phantom ★ Assembled & tested
Recommended by Alphamicrosystems

	250 ns.	450 ns.
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$4.25 Each, 10/39.95
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6800
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Also AMI EVK System in Stock

APPLE/EXIDY/EXPANDO TRS 80 16K-UPGRADE KIT

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Allows Pet/TRS 80 to be interfaced to popular S-100 Bus.
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Holds 4 Eprom's at a time. Backed by 45 years experience.
Model S-52T...$265.00
Professional Industrial Model

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★ Z80/8080 S 100 Compatible ★ Uses CPM
Assembled for Shugart ....SALE $229.00
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Kit...$179.95
Bare Board ....$38.95(Doc. Add $10.00)
Note: For CPM Add $70.00. Documentation Add $20.00
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★ Power on Jump ★ Reset Jump
Assembled & Tested......................$94.95
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Special Offer: Buy 4 kits only $59.95 each
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★ On board 2708 ★ 2708 included (450ns.)
★ Power on jump ★ completely socketed
Assembled and tested $185.00
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8 slot expandable w/9 conn.
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Card assembled and tested for use with Shugart Drives $ SALE PRICE only $229.00

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Answer, Originate $198.00

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NSC Linear App Notes II	3.95	AMD Schottky Databook	4.95
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2901	12.95
2901A	19.95
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CP1600	39.95
6502	11.50
6502A	19.95
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8035	19.95
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8748	69.95
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AM9519 Universal Interrupt	24.95
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3882-4 (4MHz)	14.95
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5262	1.95	4008L	4.95
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5290	12.45	6002	1.50

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1702A	3.95
2732	99.00
2716-5V	44.95
2716-5V 12V	29.95
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74C923	6.95

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9400 Volt to Freq. Conv	7.25
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21L02 250ns	1.59	1.55	1.45
2102	1.25	1.15	1.10
2111	3.75	3.65	3.55
2112-1	2.95	2.85	2.65
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2114L-250ns	12.95	10.95	9.95
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2114L-450ns	7.50	6.75	4.75
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16K CCD - First time offered Fairchild 460 CCD 16K Memory (now you can experiment with CCD technology at a reasonable price. 17 page Application note supplied with each order. Quantity limited)
$18.95 each (reg. 43.00)

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2.0MHz	3.95	6.5536	4.95
2.01MHz	2.95	10.0MHz	4.95
2.097152MHz	5.65	13.0MHz	4.95
2.4576MHz	5.65	14.31818	4.95
3.579545MHz	1.50	18.0MHz	4.95
4.0MHz	4.95	18.432MHz	5.95
4.194304MHz	5.95	20.0MHz	4.95
4.915200MHz	5.95	22.1184MHz	5.95
5.0MHz	4.95	27.0MHz	5.95
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		100KC	12.95

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FND 507/510 (CA) .500" Red 99
FND 800/803 (CC) .800" Red 1.75
FND 807/810 (CA) .800" Red 1.75
XAN 3062 .500" Green...................................1.15
HP5082-7731 (CA) .300" Red...........................99
9 Digit Bubble Mini Calc. Display......................99
9 Digit Panaplex Display .400"..........................99
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TIL 308 Numeric w/Logic.............................8.95
TIL 308 Number w/Logic..............................8.95
TIL 309 Number w/Logic..............................8.95
TIL 311 Hexadecimal..................................12.95
MAN 2A .320" Red Alpha-Numeric. 6.95
MAN 10A .270" Red Alpha-Numeric 6.95

SOCKETS

8 Pin W/W	12	8 Pin S/T	17
14 Pin W/W	37	14 Pin S/T	20
16 Pin W/W	38	16 Pin S/T	22
18 Pin W/W	60	18 Pin S/T	18
20 Pin W/W	90	20 Pin S/T	34
22 Pin W/W	93	22 Pin S/T	35
24 Pin W/W	85	24 Pin S/T	41
28 Pin W/W	1.15	28 Pin S/T	49
40 Pin W/W	1.49	40 Pin S/T	51

TEXTOOL ZERO INSERTION FORCE SOCKETS

16 Pin $ 5.50 24 Pin $7.50
40 Pin $10.25

CONNECTORS

DB25P (RS232)	3.25
DB25S Female	3.75
Hood	1.25
Set w/Hood, Sale	$6.50
22/44 W/W, S/T, KIM	2.95
43/86 W/W, S/T, MOT	6.50
50/100 S-100 Connector w/w	4.25
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CTS206-5 $1.75 CTS206-9 $1.95
CTS206-6 $1.75 CTS206-10 $1.95
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NAKED PC BOARD SALE

Z-80 CPU (Ithaca)	$34.95
8080A CPU	34.95
8K Static RAM (Logos)	21.95
16K Static RAM (2114)	29.95
32K Static RAM (2114)	49.95
Floppy I/O (Tarbell)	39.95
Cassette I/O (Tarbell)	29.95
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2708/2716 Eprom (Ithaca)	34.95
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Vector 8800 Proto	19.95
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13 Slot MotherBoard (WMC)	33.95
9 Slot MotherBoard (WMC)	29.95
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8038 Function Gen	3.95
MC4024 VCO	2.45
LM566 VCO	1.75
XR2206 Function Generator	5.75

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uPd372 Nec Floppy	49.95
1781 Dual Floppy	29.95
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Pixie-Verter	6.50
TV-1 Video Interface	8.95
Microverter	35.00
M&R Modulator	35.00

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21L02-2 (250 ns) 100 @ $1.15 ea.
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1489 Line Driver 100 @ 75¢ ea.
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1496 L Demodulator 25 @ 75¢ ea.

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	LIST	SALE
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Cromemco Sys III	5990.	4990.
Horizon I w/16K	1599.	1349.
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Pascal Microengine	2995	2395
IPSI 1620 Diablo RO	3295.	2595.
Anadex DP 8000	995.	895.
Centronics Micro P-1	595.	395.
Centronics Micro S-1	595.	525.
Soroc IQ 120	995.	850.
Teletype Model 43	1349.	1150.
HiPlot Plotter	1085.	899.
HiPlot Digitizer	795.	735.
Intertube II	895.	784.

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4N25 Photo XSTR HFE 250, 30V 1.29
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ICM7208 Seven Decade Counter 17.95
ICM7207 Oscillator Controller 6.95
ICM7045 Precision Stop/Watch Timer..........22.95
ICL7107 3½ Digit A/D (LED)........................14.95
ICL8211 Voltage Reference 1.95
LM390 Battery OP. Audio Amp.....................3/1.00
LM1800 Ground Fault IC 3/1.00
LM1800 Phase Lock Loop FM Stereo.........3/1.00
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DS3625 Dual Mos Sense Amp........................2.50

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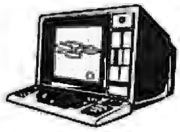

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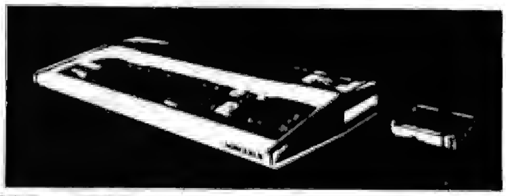

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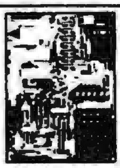

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Advanced 8K Model
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Now in stock North Star Z-80-based high-performance computer.
- ★ 180K Bytes per Disk
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- ★ 2 Serial +1 Parallel Port Avail.
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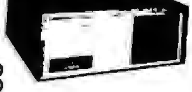

Horizon I Kit	Reg. $1599.00	Sale $1349.00
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North Star Double Density Disk Subsystem Kit

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HERE ARE SOME EXAMPLES

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It will give you 23% more storage capacity by increasing useable storage from 55,000 to 65,000 bytes per drive with our new software patch.

It can work 8 times faster than the TRS-80 Mini-Disk system, because track-to-track access is 5ms versus 40ms for the TRS-80. You can realize this added speed once the new double disk expansion interface is available without expensive modification of the existing unit.

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SD EXPANDORAM

The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisable on-board refresh, and IT WORKS!

- Bank Selectable
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- Power 8VDC, +16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Major Brand 16K RAMS
- PC Board is doubled solder masked and has silk-screen parts layout
- Extensive documentation clearly written

- Complete kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required
- 16K boundries and Protection via Dip Switches
- Designed to work with Z-80, 8080, 8085 CPU's

EXPANDORAM 64K Kit (16K Ram)

16K	$219.00
32K	$279.00
48K	$359.00
64K	$419.00
WITHOUT MEMORY	$159.00

We carry a full line of SD Systems Products. Please write for catalog or call for prices

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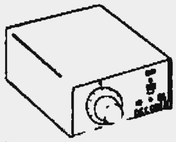

Interfaces with any monitor or scanner • Easily tuned • Full instructions included • Drilled fiberglass P.C. Board • One hour assembly • Easy to install • Punched case

This unit can unscramble most any scrambled frequency such as the new Motorola scramble and so on.

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Record important telephone conversations now with Tele Tape and your recorder. Each time your telephone receiver is picked up your recorder will start automatically and when you hang up it stops. Tape will be extra clear so you can refresh your memory at a later date. Kit includes everything except case and phono plugs.

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The Versatile Floppy Disk Controller
Only $139.00

FEATURES: IBM 3740 Soft Sectored Compatible. S-100 BNS Compatible for Z-80 or 8080. Controls up to 4 Drives (single or double sided). Directly controls the following drives:

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4 Jumbo .50" Digits in One "Stick"!

The Bowmar Opto-Stick. The best readout bargain we have ever offered. Has four common cathode jumbo digits with all segments and cathodes brought out. Increased versatility since any of the digits may be used independently to fit your applications. Perfect for any clock chip, especially direct drive units like 50380 or 7010. Also use in freq. counters, DVM's etc. For 12 or 24 hour format. (With colons and AM/PM indicator.)

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79¢ EACH

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PERFECT FOR CLOCKS! **$.79**

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Similar to Thermalloy 2205G
Finned with insert.
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HEAVY DUTY
S.P.D.T. 3A. 125 V.A.C.
New, modern styling! **5 for $1**

Z80 STARTER KIT

SD System's Z80 Starter Kit enables the novice to build a complete microcomputer on a single board. Featuring the powerful Z80 microprocessor the Z80 Starter Kit features: • Keyboard and Display • Audio Interface • PROM Programmer • Expansion and Wire Wrap Area • On Board RAM • 4 Channel Counter/Timer • Z-BUG Monitor in PROM • I/O Ports.

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$219.95 Kit **$369.95 A&T**

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3.57 MHz ...... **89¢**

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TERMS: Add 30¢ postage, we pay balance. Orders under $15 add 75¢ handling. No C.O.D. We accept Visa, MasterCharge, and American Express cards. Tex. Res. add 5% Tax. Foreign orders (except Canada) add 20% P&H. 90 Day Money Back Guarantee on all items

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BOMB—BYTE's Ongoing Monitor Box

June BOMB

William D. Johnston again dazzled our readers with "Computer Generated Maps," Part II, page 100. Second place was taken by James Albus for contributing "A Model of the Brain for Robot Control," page 10. Placing a very close third and fourth, respectively, were G. A. Van den Bout, "Designing a Command Language and T. Radhakrishnan and M. V. Bhat, "Stacks in Microprocessors."

The Microcomputers you should take seriously.

The Challenger III Series is the microcomputer family with the hardware features, high level software and application programs that serious users in business and industry demand from a computer system, no matter what its size.

Since its introduction in August, 1977, the Challenger III has become one of the most successful mircocomputer systems in small business, educational and industrial development applications. Thousands of Challenger III's have been delivered and today hundreds of demonstrator units are set up at systems dealers around the country.

Now the Challenger III systems offer features which make their performance comparable with today's most powerful mini-based systems. Some of these features are:

Three processors today, more tomorrow.

The Challenger III Series is the only computer system with the three most popular processors— the 6502A, 68B00 and Z-80. This allows you to take maximum advantage of the Ohio Scientific software library and the tremendous number of programs offered by independent suppliers and publishers. And all Challenger III's have provisions for the next generation of 16 bit micros via their 16 bit data BUS, 20 address bits, and unused processor select codes. This means you'll be able to plug a CPU expander card with two or more 16 bit micros right in to your existing Challenger III computer.

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Five DOS options including development, end user, and virtual data file single user systems, real time, time share, and networkable multi-user systems.

The three most popular computer languages including three types of BASIC plus FORTRAN and COBOL with more languages on the way. And, of course, complete assembler, editor, debugger and run time packages for each of the system's microprocessors.

Applications Software for Small Business Users.

Ready made factory supported small business software including Accounts Receivable, Payables, Cash Receipts, Disbursements, General Ledger, Balance Sheet, P & L Statements, Payroll, Personnel files, Inventory and Order Entry as stand alone packages or integrated systems. A complete word processor system with full editing and output formatting including justification, proportional spacing and hyphenation that can compete directly with dedicated word processor systems.

There are specialized applications packages for specific businesses, plus the vast general library of standard BASIC, FORTRAN and COBOL software.

OS-DMS, the new software star.

Ohio Scientific has developed a remarkable new Information Management system which provides end user intelligence far beyond what you would expect from even the most powerful minisystems. Basically, it allows end users to store any collection of information under a Data Base Manager and then instantly obtain information, lists, reports, statistical analysis and even answers to conventional "English" questions pertinent to information in the Data Base. OS-DMS allows many applications to be computerized without any programming!

The new "GT" option heralds the new era of sub-microsecond microcomputers.

Ohio Scientific now offers the 6502C microprocessor with 150 nanosecond main memory as the GT option on all Challenger III Series products. This system performs a memory to register ADD in 600 nanoseconds and a JUMP (65K byte range) in 900 nanoseconds. The system performs an average of 1.5 million instructions per second executing typical end user applications software (and that's a mix of 8, 16 and 24 bit instructions!).

Mini-system Expansion Ability.

Challenger III systems offer the greatest expansion capability in the microcomputer industry, including a full line of over 40 expansion accessories. The maximum configuration is 768K bytes RAM, four 80 million byte Winchester hard disks, 16 communications ports, real time clock, line printer, word processing printer and numerous control interfaces.

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The Challenger III systems have phenomenal performance-to-cost ratios. The C3-S1 with 32K static RAM, dual 8" floppies, RS-232 port, BASIC and DOS has a suggested retail price of under \$3600. 80 megabyte disk based systems start at under \$12,000. Our OS-CP/M software package with BASIC, FORTRAN and COBOL is only \$600. The OS-DMS nucleus package has a suggested retail price of only \$300, and other options are comparably priced.

To get the full story on the Challenger III systems and what they can do for you, contact your local Ohio Scientific dealer or call the factory at (216) 562-3101.

The Challenger III Series from Ohio Scientific.

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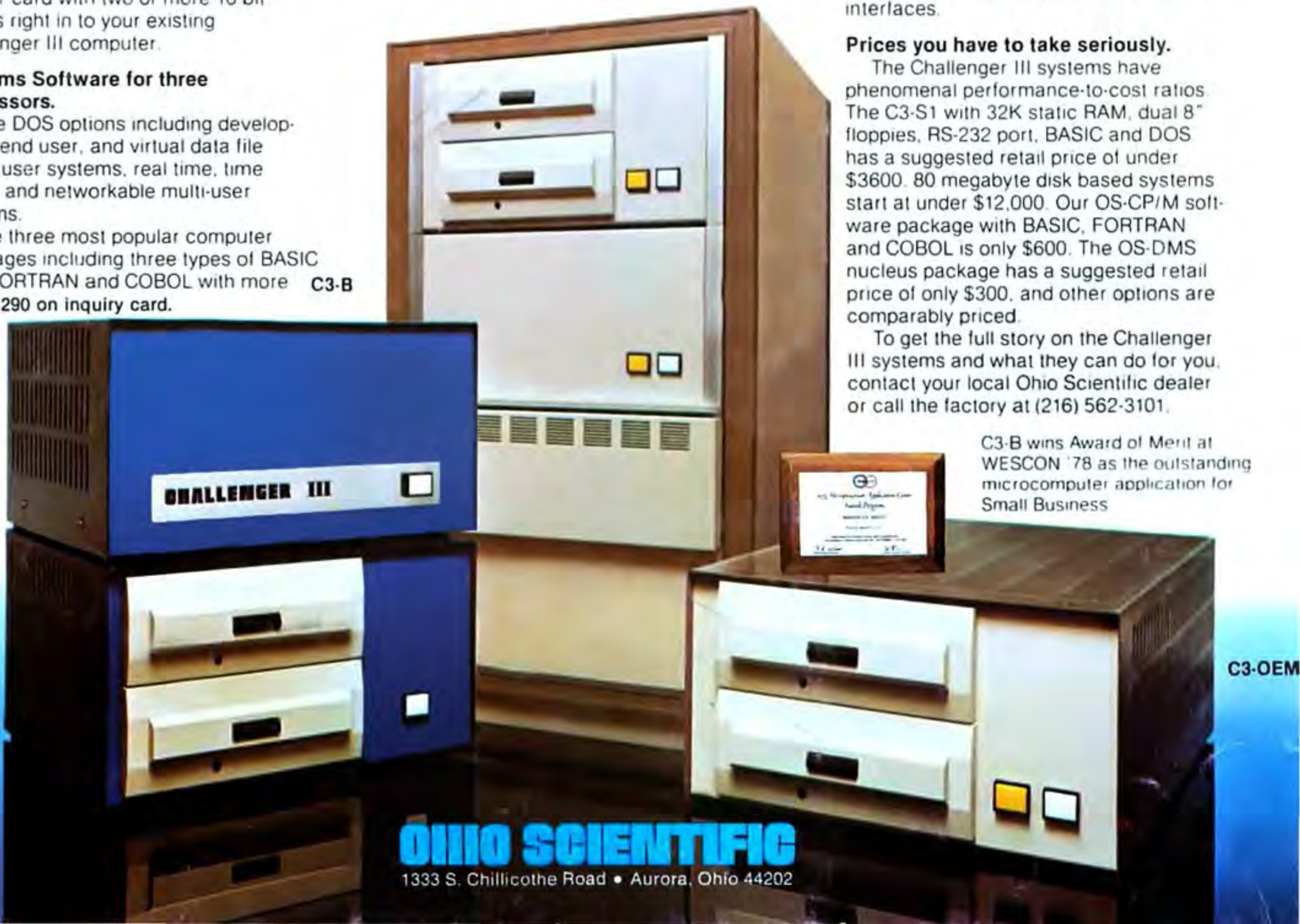

C3-B wins Award of Merit at WESCON '78 as the outstanding microcomputer application for Small Business