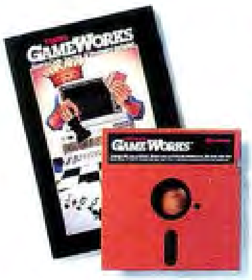
Extra All–IBM Edition

BYTE
THE SMALL SYSTEMS JOURNAL®

Inside the IBM PCs

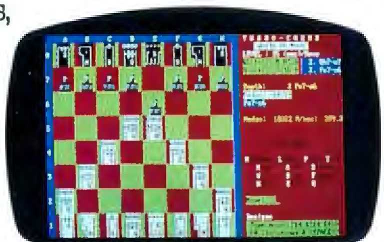
Third Annual Special Issue

EXTRA EDITION BYTE INSIDE THE IBM PCs Volume 10, Number 11



Turbo GameWorks™

Also recently released, Turbo GameWorks is what you think it is: "Games" and "Works." Games you can play right away (like Chess, Bridge and Go-Moku), plus the Works—which is how computer games work. All the secrets and strategies of game theory are there for you to learn. You can play the games "as is" or modify them any which way you want. Source code is included to let you do that, and whether you want to write your own games or simply play the off-the-shelf games, Turbo GameWorks will give hours of diversion, education, and intrigue. George Koltanowski, Dean of American Chess, and former President, United States Chess Federation, reacted to Turbo GameWorks like this, "*With Turbo GameWorks, you're on your way to becoming a master chess player*," and Kit Woolsey, writer, author, and twice Champion of the Blue Ribbon Pairs, wrote, "*Now play the world's most popular card game—Bridge . . . even program your own bidding or scoring conventions.*" Suggested retail: $69.95.



Turbo Graphix Toolbox™

It includes a library of graphics routines for Turbo Pascal programs. Lets even beginning programmers create high-resolution graphics with an IBM, Hercules,™ or compatible graphics adapter. Our Turbo Graphix Toolbox includes all the tools you'll ever need for complex business graphics, easy windowing, and storing screen images to memory. It comes complete with source code, ready to compile. Suggested retail: $69.95.

Recognition for Borland International has come from business, trade, and media, and includes both product awards and awards for technical excellence and marketing. Borland was named "Company of the Year" by PC Magazine; Sidekick, the #1 best seller for the IBM PC, was named "Product of the Year" by InfoWorld; Turbo Pascal was selected one of PC Week's Top 10 Products for 1984; SuperKey won one of PC Magazine's "Best of 1985" awards; Reflex, The Analyst was recognized in the "Software Products of the Year" awards by InfoWorld; and Reflex and SideKick were both nominated for British Micro Awards in 1986.

Turbo Database Toolbox™

A perfect complement to Turbo Pascal, because it contains a complete library of Pascal procedures that allows you to search and sort data and build powerful database applications. Having Turbo Database Toolbox means you don't have to reinvent the wheel each time you write a Turbo Pascal program. It comes with source code for a free sample database—right on disk. The database can be searched by keywords or numbers. Update, add, or delete records as needed. Just compile it and it's ready to go to work for you. Suggested retail: $69.95.

Technical Specifications:

TURBO PASCAL 3.0 Minimum memory:128K; includes 8087 and BCD features for 16-bit MS-DOS and CP/M-86 systems. CP/M-80 version minimum memory: 48K; 8087 and BCD features not available

TURBO DATABASE TOOLBOX Minimum memory: 128K. CP/M-80 minimum memory: 48K. Requires Turbo Pascal 2.0 or later.

TURBO GRAPHIX TOOLBOX* Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later, Turbo Pascal 3.0, and IBM CGA, Hercules Monochrome Card or equivalent.

TURBO TUTOR 2.0 Minimum memory: 192K. CP/M-80 version minimum memory 48K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0.

TURBO EDITOR TOOLBOX* Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0.

TURBO GAMEWORKS* Minimum memory: 192K. Requires PC/MS-DOS 2.0 or later and Turbo Pascal 3.0.

TURBO PROLOG* Minimum memory: 384K.

REFLEX: THE ANALYST* Minimum memory: 384K. Requires IBM CGA, Hercules Monochrome Card or equivalent. Works with Intel's AboveBoard-PC and -AT; AST's RAMpage! and RAMpage! AT; Quadram's Liberty-PC and -AT; Tecmar's 640 Plus; IBM's EGA and 3270/PC; AT&T's 6300 and many others.

REFLEX WORKSHOP* Minimum memory: 384K. Requires Reflex: The Analyst. Two disk drives or hard disk recommended.

TURBO LIGHTNING* Minimum memory: 256K. Two disk drives required. Hard disk recommended.

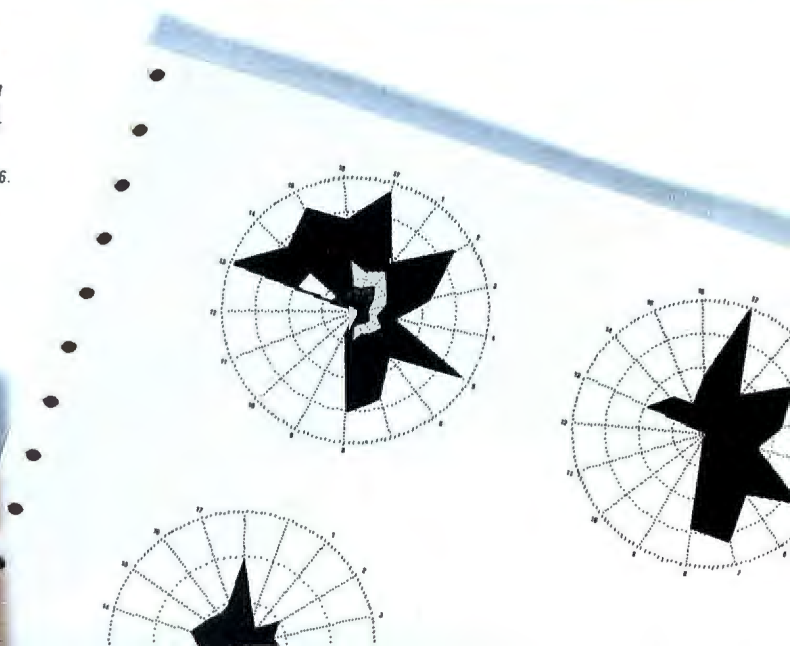
LIGHTNING WORD WIZARD* Minimum memory: 256K. Requires Turbo Lightning. Turbo Pascal 3.0 required to edit source code.

SIDEKICK* Minimum memory: 128K.

TRAVELING SIDEKICK* Minimum memory: 256K.

SUPERKEY* Minimum memory: 128K.

*For IBM PC, AT, XT, PCjr and true compatibles only, running PC/MS-DOS 2.0 or later.



COMPLETELY NEW VERSION!

Turbo Tutor® 2.0

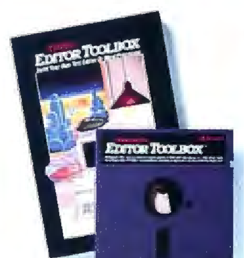
Just released (July '86), the new Turbo Tutor can take you from "What's a computer?" on through to complex data structures, assembly languages, trees, tips on writing long programs in Turbo Pascal, and a high level of expertise. Source code for everything is included. New split screens allow you to put source text in the bottom half of the screen and run the examples in the top half. There are quizzes that ask you, show you, tell you, teach you. You get a 450-page manual—which is not as daunting as it sounds, because unlike many software manuals, it was not written by orangutans. (With our all "almost-free" upgrade, you can upgrade to Turbo Tutor 2.0 by sending us your master diskettes, proof of purchase, and $10.00, which covers shipping and handling.) Suggested retail: $39.95.

NEW SPECIAL!

Turbo Pascal® 3.0

"*For the IBM PC, the benchmark Pascal compiler is undoubtedly Borland International's Turbo Pascal,*" says Gary Ray of *PC Week.* We and more than 500,000 other people around the world think Mr. Ray got that right.

Since launch, Turbo Pascal has become the *de facto* worldwide standard in high-speed Pascal compilers. Described by Jeff Duntemann of *PC Magazine* as the "*Language deal of the century,*" Turbo Pascal is now an even better deal than that—because we've *included* the most popular options (BCD reals and 8087 support). What used to cost $124.95 is now only $99.95! You now get a lot more for a lot less: the compiler, a completely integrated programming environment, and BCD reals and 8087 support—all for a suggested retail of only $99.95.



Turbo Editor Toolbox™

Recently released, we called our new Turbo Editor Toolbox a "construction set to write your own word processor." Peter Feldmann of *PC Magazine* covered it pretty well with, "*A 'write your own word processor' program for intermediate level programmers, with lots of help in the form of prewritten procedures covering everything from word wrap to pull-down windows.*" Source code is included, and we also include MicroStar, a full-blown text editor with pull-down menus and windowing. It interfaces directly with Turbo Lightning to let you spell-check your MicroStar files. Jerry Pournelle of *BYTE* magazine said, "*The new Turbo Editor Toolbox is the Turbo Pascal source code to just about anything you ever wanted a PC-compatible text editor to do.*" Suggested retail: $69.95.

Borland's Business Productivity Programs:

Reflex: The Analyst™ Analytical database manager. Provides complete new look at data normally hidden by programs like 1-2-3® and dBASE.® Best report generator for 1-2-3.

NEW! **Reflex Workshop™** Important new addition to Reflex: The Analyst. Gives you 22 different templates to run your business right.

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SuperKey® Keyboard enhancer. Simple macros turn 1000 keystrokes into 1. Also encrypts your files to keep confidential files confidential.

Borland's Electronic Reference Programs:

Turbo Lightning™ Works with all your programs and checks your spelling *while you type!* Includes 80,000-word Random House® Concise Dictionary and 50,000-word Random House Thesaurus. Forerunner of Turbo Lightning Library.

Lightning Word Wizard™ Includes ingenious crossword solver and six other word challenges. If you're into programming, Lightning Word Wizard is also a development toolbox and the technical reference manual for Turbo Lightning.

We frequently surprise people with inventive, imaginative software, and people frequently surprise us with the way *they* use it.

For example, you'll read on this page how Michael J. Watkins of the Petroleum Technology Center in Houston, Texas, used Turbo Pascal® (and Turbo Graphix Toolbox™ and Turbo Tutor®) to cut down the tedium and time in creating Circular Performance Profile Charts (CPPCs).

We didn't know they existed, but you learn something new every day!

Applications like CPPCs might not fit your exact needs, but at the same time they might stimulate fresh ideas in your mind about how you can put Turbo Pascal and the Turbo Pascal family to work for you.

And thank you for your interest in and support for Borland International.

Philippe Kahn,
President, Borland International

INSIDE STORIES!

■ Turbo Pascal 3.0, already described by *PC Magazine* as "*Language deal of the century*," is now an even better deal than that, because we've included the most popular options (BCD reals and 8087 support). What used to cost $124.95 is now only $99.95!

■ Completely new Turbo Tutor 2.0 now available. New software. New manual. New split screens. New quizzes. Only $39.95. Upgrades available under Borland's "Almost-Free" upgrade plan. Details inside.

LATE NEWS!

■ June/July Special Artificial Intelligence Issue of The *Micro Technical Journal* says, "*Turbo Prolog looks like it's going to be a winner, for both the beginner and professional programmer.*"

Turbo Pascal deliberately programmed to go around in circles

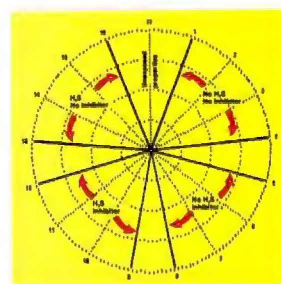
Circular charts (or CPPCs) are used by Michael J. Watkins of the Petroleum Technology Center in Houston, Texas, to plot a single performance property for a large number of elastomers, which have elastic, rubber-like properties.

Mr. Watkins wrote us saying, "*Because CPPCs condense a lot of data in one graphic, they can be very tedious and time-consuming to draw.*"

What he did to solve those problems was to write a Turbo Pascal program for IBM® personal computers to "*generate these charts quickly and easily.*"

He used Turbo Pascal "*because it has a companion set of very powerful graphics programs (Turbo Graphix Toolbox) which greatly simplifies the required programming.*

Turbo Pascal is not a difficult language to use and can be easily learned by persons who can program in FORTRAN or BASIC. An excellent tutorial (Turbo Tutor) is available for the novice or experienced programmer. The Turbo Pascal products are also very moderately priced."



"The computer is no better than its program."
Elting Morison, author of "Men, Machines and Modern Times"

Step-by-step tutorial, demo programs with source code included!

Borland's new Turbo Prolog is the powerful, completely natural introduction to Artificial Intelligence

Prolog is probably one of the most powerful computer programming languages ever conceived, which is why we've made it our *second* language—and "turbo-charged" it to create Turbo Prolog.

Our new Turbo Prolog, the natural language of Artificial Intelligence, brings supercomputer power to your IBM® PC and introduces you step-by-step to the fascinating new world of Artificial Intelligence. And does all this for an astounding $99.95.

Turbo Prolog is to Prolog what Turbo Pascal® is to Pascal!

Our Turbo Pascal astonished everyone who thought of Pascal as "just another language." We changed all that—and now Turbo Pascal is the de facto worldwide standard, with hundreds of thousands of enthusiasts and users in universities, research centers, schools, and with professional programmers, students, and hobbyists.

You can expect at least the same impact from Turbo Prolog, because while Turbo Prolog is the most revolutionary and natural programming language, it is also a complete development environment—just like Turbo Pascal.

Minimum memory: 384K

> "Turbo Prolog offers generally the fastest and most approachable implementation of Prolog."
> Darryl Rubin, AI Expert

Even if you've never programmed before, our free tutorial will get you started right away

You'll get started right away because we have included a complete step-by-step tutorial as part of the 200-page Turbo Prolog Reference Manual. Our tutorial will take you by the hand and teach you everything you're likely to need to know about Turbo Prolog and artificial intelligence.

For example: once you've completed the tutorial, you'll be able to design your own expert systems utilizing Turbo Prolog's powerful problem-solving capabilities.

Think of Turbo Prolog as a high-speed electronic detective. First you feed it information and teach it rules. Then Turbo Prolog "thinks" the problem through and comes up with all the reasonable answers—almost instantly.

If you think that this is amazing, you just need to remember that Turbo Prolog is a 5th-generation language—and the kind of language that 21st century computers will use routinely. In fact, you can compare Turbo Prolog to Turbo Pascal the way you could compare Turbo Pascal to machine language.

You get the complete Turbo Prolog programming system for only $99.95

You get a complete Turbo Prolog development system including:

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- The 200-page reference manual which includes the step-by-step Turbo Prolog tutorial.
- The free GeoBase™ natural query language database including commented source code on disk—ready to compile. GeoBase is a complete database designed and developed around U.S. geography. It includes cities, mountains, rivers, and highways, and comes complete with natural query language. Use GeoBase immediately "as is," or modify it to fit your own interests.

So don't delay—don't waste a second—get Turbo Prolog now. $99.95 is an amazingly small price to pay to become an immediate authority—an instant expert on artificial intelligence! The 21st century is only one phone call away.

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__	Turbo Pascal 3.0 w/8087 & BCD	99.95	$______
__	Turbo Pascal for CP/M-80	69.95	$______
__	Turbo Database Toolbox	69.95	$______
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__	Turbo Tutor 2.0	39.95	$______
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Prices subject to change without notice.

Turbo Prolog 1.0 Technical Specifications

Compiler: Incremental compiler generating native in-line code and linkable object modules. The linking format includes a linker and is compatible with the PC-DOS linker. Large memory model support. Compiles over 2500 lines per minute on a standard IBM PC.

Interactive Editor: The system includes a powerful interactive text editor. If the compiler detects an error, the editor automatically positions the cursor appropriately in the source code. At run-time, Turbo Prolog programs can call the editor, and view the running program's source code.

Type System: A flexible object-oriented type system is supported.

Windowing Support: The system supports both graphic and text windows.

Input/Output: Full I/O facilities, including formatted I/O, streams, and random access files.

Numeric Ranges: Integers: −32767 to 32T67; Reals: 1E−307 to 1E+308.

Debugging: Complete built-in trace debugging capabilities allowing single stepping of programs.

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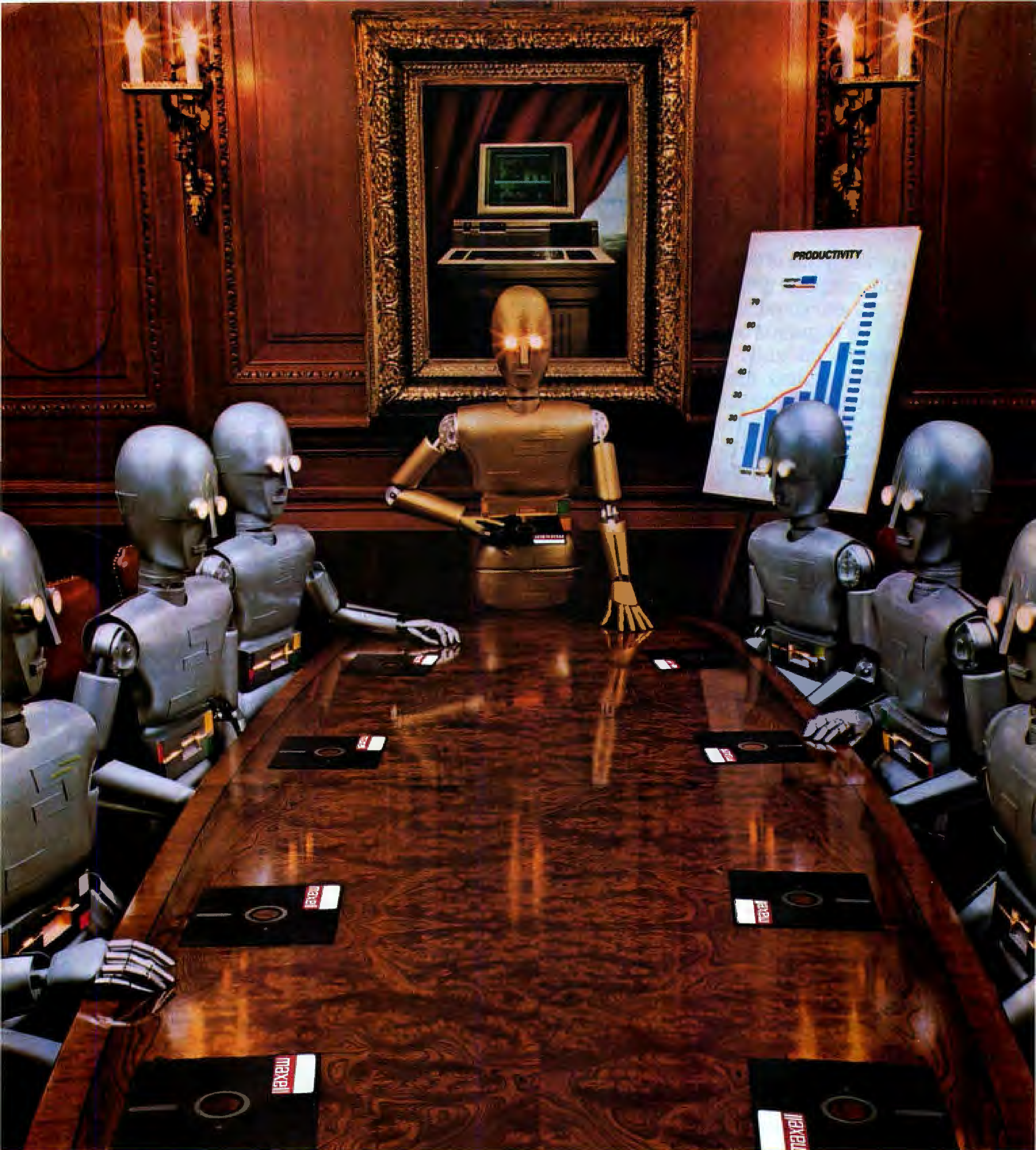
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COVER ILLUSTRATED BY ROBERT TINNEY

VOLUME 11, NUMBER 11, 1986

BYTE

Inside the IBM PCs

LISTINGS

ABC

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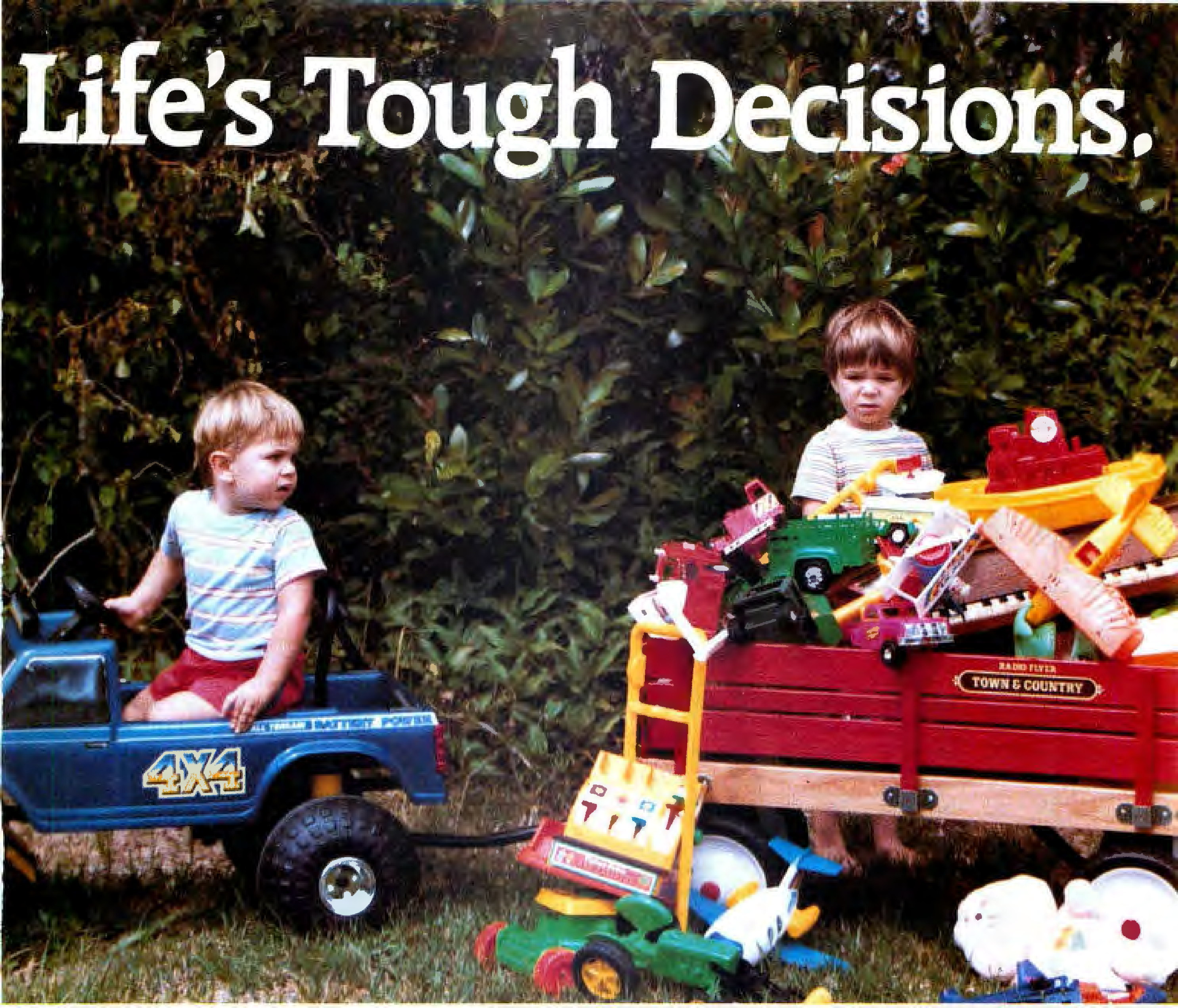
Life's Tough Decisions.



THE CHOICES.

Remember when your biggest problem was no storage space in your wagon? No room for your boats, trains, cars, and planes. Your choice was to either get rid of some toys or get a bigger wagon.

Now your *wagon* has turned into an IBM PC-XT. Your boats, trains, and cars are now database, spreadsheet, and word processing files. But your choice for more storage is still about the same: either get rid of some "toys" or get a bigger "wagon."

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EDITORIAL

The Struggle for Compatibility

The IBM Personal Computer, introduced in the fall of 1981, celebrates its fifth birthday this year. With the flattery quotient nearing 1.00, the folks in Boca Raton should be proud of their progeny as the homes and offices of customers around the world slowly fill with imitation PCs. 1986 is proving to be the Year of the Clone.

What makes building clones so easy? Why can anybody who feels like it put together a clone, rent a mailbox, and rake in a pile of cash?

The key to clone building is the use of standard parts and the availability of crucial system software, like Phoenix Technology's IBM PC–compatible BIOS and Microsoft's MS-DOS. While there are subtle incompatibilities from clone to clone, there are usually enough similarities from machine to machine to make most clones perform acceptably as copies of the PC. This is particularly true for application software written to make DOS and BIOS calls instead of directly addressing a machine's hardware.

Compatibility with the IBM PC has been a contraposition for IBM. Wide availability of machines that can all run the same software has prompted the creation of thousands of programs. The availability of this software has assured the sale of machines that will run all these great programs. IBM's problem has been that other companies can provide this now-standard computer more cheaply than IBM.

So the IBM PC created an archetype around which a flourishing industry has sprouted. Could this industry-building scenario work in reverse?

Toward a 32-Bit Bus Standard

This past spring, a group of hardware and software makers got together to talk about creating a bus standard for extending the IBM PC AT's 16-bit bus to 32 bits. The extra 16 bits would accommodate the Intel 80386 microprocessor as the engine for new computers and peripheral devices designed to work with the new 32-bit bus. The name chosen for this new bus is Personal Computer Extended Technology (PCET).

The PCET bus makes possible the construction of personal computers and peripheral devices based on the Intel 80386 processor in the absence of a standard 80386 machine from IBM. Many people speculate that IBM will either be late with an 80386-based machine or build an 80386 machine that uses a proprietary operating system (or maybe both). In any case, the PCET bus circumvents IBM by establishing a standard bus around which other manufacturers can build 80386 machines. A half dozen 80386 machines using the PCET bus would establish a standard that might survive, regardless of actions taken by IBM.

Since the PCET bus is an extension of the PC AT bus, machines built around this bus could use existing graphics and memory-expansion cards and existing versions of MS-DOS—and thousands of existing application programs. The PCET bus provides a painless way to build "turbo" ATs—machines that function like an AT but at two to three times the speed.

Once an existing base of turbo ATs develops, software houses can create new operating systems—or adapt existing ones like UNIX—to tap the potential of the 80386. Hardware companies can build graphics and memory boards for a new class of workstations that are based on the 80386.

Thus, a whole new genre of clones can be built, using standard, off-the-shelf parts along with adapted BIOS software and existing operating system and application programs. These new clones will actually predate the machine they are designed to replace! It seems that the personal computer world may take on an odd, ironic tilt.

PCET-bus-based machines may survive as a group only if IBM's 80386 machine is *not* an open-architecture machine. Tandy is gambling that IBM will make an 80386 machine that can be cloned. If this turns out to be the case, any company selling a PCET-bus computer should get in touch with an auctioneer.

The obvious question arises about whether or not people really need turbo ATs. Only 13 percent of the owners of IBM computers require the power of an AT. Maybe only 13 percent of AT owners will benefit from the power of a turbo AT. Even if this were the case, that would still create a niche for approximately 40,000 80386-based computers. But another problem is the issue of affordability. Is using an 80386 in a single-user machine a waste of hardware resources? Is it cost-effective?

Modifications are already available for Apple's Macintosh that permit the use of an MC68020 processor and MC68881 math coprocessor and the addition of up to 4 megabytes of RAM. These modifications, when coupled with a 1K- by 1K-pixel monitor, transform a Mac into a high-performance workstation. But the cost is high—$7000 to $9000.

Building similarly equipped turbo ATs may turn out to be just as expensive. At that price, buyers who need a full-fledged workstation (in contrast to the folks who want to run Lotus 1-2-3 faster) might look at Sun, Apollo,

(continued)

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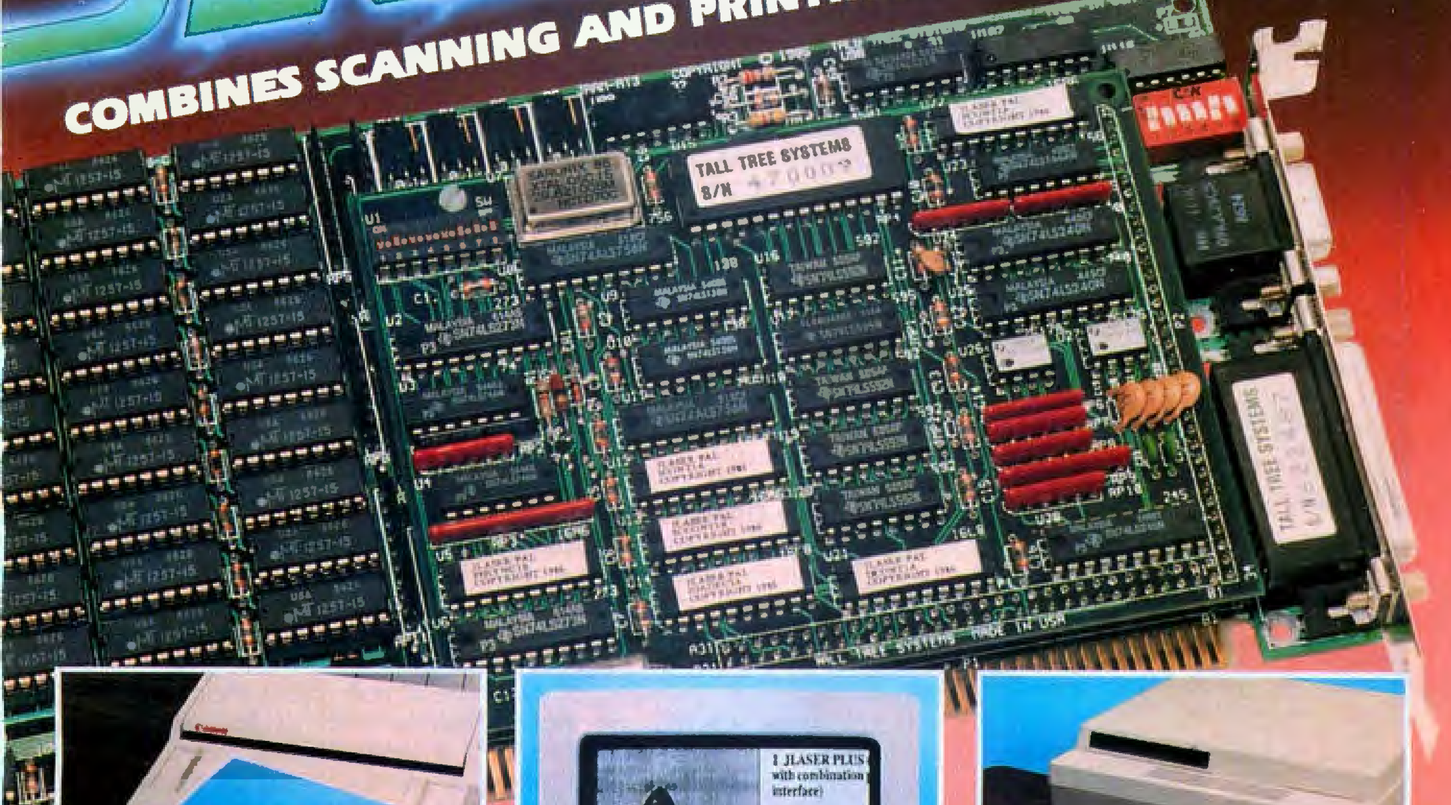

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1-2-3 faster) might look to Sun, Apollo, DEC, or IBM's RT PC for more stable hardware and software.

The one application area that can potentially benefit most from 80386 performance is graphics. Intel's new microprocessor can permit the creation of workstations with a great deal of graphics power. But the trend in graphics processing is to offload graphics to its own processor, either custom-built, as in the Amiga, or off-the-shelf parts, like the Texas Instruments TMS34010. There is also the problem of the 16-bit EGA standard and how it can be adapted to a 32-bit environment.

Technology Driven

Regardless of the *need* for 80386-based machines, technology has a way of evolving for its own sake. People need to find out what is possible, whether it be with airplanes or computers.

Therefore, the PCET-bus specification effort makes sense from a research and development point of view. It establishes a common starting ground for machine designs using a new processor.

The PCET-bus design goals seek to provide a high-speed bus for 32-bit memory and memory-mapped data transactions. The bus also needs to be flexible enough to permit 32-bit coprocessor cards to become alternate bus masters.

The PCET bus pipelines address and control information, making this information for a subsequent bus cycle available in the latter stages of the current bus cycle. The bus design calls for a default to two wait states but can be operated with one or no wait states by activating additional control signals.

Compatibility with the existing 16-bit PC AT bus is a must for the PCET bus to take advantage of existing graphics and memory standards. (An interesting outgrowth of the PCET-bus specification effort is that the committee first had to codify the AT bus.) A mix of 16- and 32-bit bus masters can drive the PCET bus to accommodate refresh, direct memory access, and other tasks.

The memory map for the PCET bus shows the entire 4-gigabyte address space of the 80386 as being available to the bus, except the 640K-byte to 1-megabyte area reserved for ROM and video devices.

Mechanically, the PCET bus extends the data lines of the PC AT bus by 40 pins. The data lines on the RT PC bus, already 40 pins instead of 36 as in the AT, also get another 40 pins.

We still need to ask some legitimate questions about the PCET bus. Is it possible to achieve nearly the same 80386 performance on a 16-bit bus feeding a 32-bit cache? Since 85 percent of all CPU operations are read operations, caching operands may allow an 80386 to operate almost as fast with a 16-bit bus as it would with a 32-bit bus for some applications.

Another question about a 32-bit standard bus: What if companies ignore it and create their own bus? There have been widespread reports of 80386-machine projects at Compaq and Zenith that will feature proprietary 32-bit bus designs. The PCET bus, no matter how elegant its design, will fade away like the dodo if everyone ignores it.

Another Round

Regardless of the creation of the PCET bus, there will be new machines built around the 80386. The early machines will be expensive and will have no software to fully exploit their power. They may serve as a bridge from the current PC world to a future 80386-machine-based environment. These new machines will undoubtedly raise a different set of compatibility problems with the machines and software that preceded them.

But we'll buy them anyway.

—G. *Michael Vose*
Senior Technical Editor

Look for IBM-related conferences and special events on BIX starting in late October. Current plans call for a special event on "System Software for the 80386," plus conferences on the RT PC and the PC Convertible.

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Inquiry 263

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Inquiry 66

IBM's PC XT *Model* 286 *runs on a* 6-MHz 80286.

IBM Introduces 80286-based XT

IBM's latest version of its PC XT, the Model 286, is based on an 80286 processor running at 6 MHz with no wait states and features more memory than earlier models of the XT and up to three internal drives.

Priced at $3995, the Model 286 comes standard with 640K bytes of memory that can be expanded to 12.6 megabytes, a half-height 1.2-megabyte 5¼-inch floppy disk drive, a 20-megabyte hard disk drive, and a serial/parallel adapter. The machine has eight expansion slots, five of which can accommodate 16-bit boards. Internal storage options include a 3½-inch 720K-byte floppy disk drive ($190), a second 5¼-inch floppy drive with a capacity of 1.2 megabytes ($275), and a 5¼-inch floppy drive that can handle 360K bytes ($225). The Model 286 also supports IBM's external 3½-inch floppy disk drive.

The computer uses a number of custom gate arrays to reduce chip count and board space requirements. Some of the chips are SIP (single in-line package), arranged vertically on the motherboard, thus further reducing the space requirements of the motherboard. The Model 286 has the same footprint as the IBM PC and XT.

According to the company, the machine's 80286 operates in real address mode for compatibility with the 8088 and in protected virtual mode, which supports multitasking and enables the processor to address up to 16 megabytes of real memory and 1 gigabyte of virtual memory. The computer requires DOS version 3.2 or XENIX version 2.0.

The older 6-MHz PC AT will be phased out, the company says, but IBM will continue to sell the 8-MHz version of the AT. Contact IBM Corp., Information Systems Group, 900 King St., Rye Brook, NY 10573, (914) 934-4488.

Inquiry 550.

AT&T's 32-bit Digital Signal Processor

AT&T has developed the WE DSP32, a 32-bit single-chip digital signal processor with floating-point capabilities. Applications for the chip include communications functions such as filtering, adaptive equalization, and echo canceling. The device can also be used for speech and image processing, as well as graphics simulation.

The chip has a clock rate of 16 MHz and executes its instruction cycle in 250 nanoseconds, or 8 million floating-point operations per second. On-chip memory consists of 2K bytes of ROM and 4K of RAM.

Software and hardware development tools that operate under MS-DOS and UNIX System V are available for use with the chip. A Support Software Library includes a high-level "C-like" syntax assembler and a simulator. A single-board development system permits real-time testing, debugging, and evaluation of hardware and software.

Sample OEM quantities of the WE DSP32 chip cost $175. Contact AT&T Technology Systems, 555 Union Blvd., Dept. 50AL203140, Allentown, PA 18103, (800) 372-2447.

Inquiry 551.

Object-oriented Programming Language

Actor is an object-oriented language that makes use of the Microsoft Windows interface. Because it's interactive, you can experiment at the keyboard with your programming ideas and watch the results.

The environment includes a workspace for communicating with the interpreter, a browser, an error manager, a window-based debugger, and a save facility. You can send messages to any object in the system to check status, change parameters, or learn about inherited behavior. A concurrent garbage collector is designed to free you from memory management duties. Actor contains classes that support list processing, pattern matching, parsing, and predicate logic.

The package sells for $495 and comes with source code (except for the assembly language kernel), tutorial, reference manual, and demo program. Contact The Whitewater Group Inc., 906 University Place, Evanston, IL 60201, (312) 491-2370.

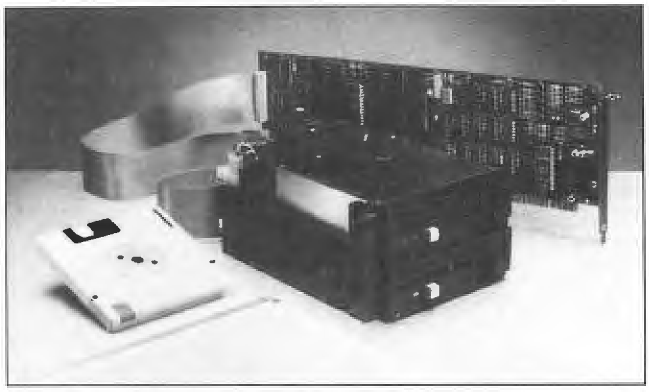
Inquiry 552.

(continued)

Two Removable-Cartridge Systems

Sysgen introduced the DuraPak, an internal storage subsystem with removable hard disk cartridges for IBM PCs, XTs, ATs, and compatibles. A single-drive, 15-megabyte DuraPak system sells for $1295, which includes a controller and installation hardware. A dual-drive, 30-megabyte DuraPak sells for $2095.

Each removable cartridge has a 15-megabyte capacity and measures 4¼ inches by 4⅜ inches. For more information, contact Sysgen Inc., 47853 Warm Springs Blvd., Fremont, CA 94539, (415) 490-6770.
Inquiry 553.



Sysgen's DuraPak uses 15-megabyte removable cartridges.

Data Technology's subsystem features 5¼-inch removable cartridges that can store 10 megabytes of data. The drive's average access time is 75 milliseconds, and its data transfer rate is 275K bytes per second. The cartridges consist of a flexible disk encased in a hard disk cartridge.

A single half-height subsystem retails for $1195; a dual configuration sells for $1995. The disks cost about $39 each. For more information, contact Data Technology Corp., 2775 Northwestern Parkway, Santa Clara, CA 95051, (408) 496-0434.
Inquiry 554.

System for Visual Artists

Time Arts, producers of the Lumena software for visual arts, has released another graphics package. EVA (Environment for Visual Art), based on a 512K-byte PC AT, combines raster and vector display technology and uses 32,000 on-screen colors. You can use the program to digitize images and then manipulate them with the AT. Time Arts says its package can also duplicate many of the video and film effects produced by more expensive systems.

With the digitizing tablet and pen, you have a selection of electronic brushes, colors, typefaces, and such capabilities as masking, automatic edge smoothing, texture rendering, and instant full-color tinting.

EVA uses two monitors: color for working with images, monochrome for keeping track of tools and system status. Images you develop on the 512 by 512 RGB screen can be increased to 2048 by 4096 resolution for direct transfer to a digital film recorder. With appropriate output devices, the system can also make its own color separations, 35mm slides, transparencies, video frames, tape sequences, and ink-jet, dot-matrix, and laser prints. Images can also be sent directly to Scitex graphics systems.

Pricing depends on output requirements, but the company says a complete system can cost $15,000. For more information, contact Time Arts Inc., P.O. Box 6476, 3436 Mendocino Ave., Santa Rosa, CA 95406-0476, (707) 576-7722.
Inquiry 555.

3-D Engineering and Animation on PC AT

Renaissance Graphics unveiled real-time three-dimensional solid-modeling and animation add-on boards for the IBM PC AT. The Renaissance Graphics System (RGS) boards allow for fully animated 3-D shaded objects at a resolution of 512 by 512 pixels, 256 simultaneous colors from a palette of 16.8 million, and flicker-free 60-Hz display on the PC AT.

The system includes three 68000 microprocessors operating at 12.5 MHz, a 68881 math coprocessor, and two video frame buffers. The boards also have a TI 34061 video controller and a 192K-byte ROM with firmware routines. Among the system's capabilities are hidden line and surface removal, flat or smooth shading, selectable light source, and anti-aliasing. Its z-axis clipping, infinite zoom, and roam enable the viewer to travel around in 3-D space, going behind or inside moving objects.

The RGS is designed for use with a high-resolution analog RGB monitor and will be bundled with a 3-D paint system. Standard NTSC, PAL, and SECAM video signals that can be genlocked (synchronized) to an external video source, along with film and slide recording, are also planned and will require additional hardware.

PC AT–based workstations using RGS boards will cost under $20,000 and, according to the company, will run five times faster than competing systems costing $60,000 or more. The recommended system includes an IBM PC AT with a 40-megabyte hard disk, high-resolution analog RGB monitor, and graphics tablet. The RGS cards, which are slated to be available in early 1987, occupy three slots in the PC AT. Contact Renaissance Graphics Inc., 1050 Walnut, Suite 325, Boulder, CO 80302, (303) 443-0191.
Inquiry 556.

CP/M on IBM PCs

Micro Solutions' UniDOS software lets IBM PCs and compatibles run 8-bit CP/M programs without additional hardware. The package emulates a Z80 microprocessor and provides an environment compatible with CP/M 2.2. You can run a CP/M program from DOS by typing its name. The two types of programs can reside on the same disk.

UniDOS retails for $69.95. Contact Micro Solutions Inc., Software Division, 125 South Fourth St., DeKalb, IL 60115, (815) 756-3411.
Inquiry 557.

(continued)

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Inquiry 243

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PC Convertible Add-ons

Alloy announced the StarBase subsystem, one of the first add-ons for the IBM PC Convertible. Priced at $1995, StarBase-II is a combination 20-megabyte hard disk and 5¼-inch floppy drive with a parallel printer port. StarBase-III, a second model of the subsystem, also includes a 40-megabyte tape drive and sells for $2495. Both units attach to the expansion connector on the rear of the computer. For more information, contact Alloy Computer Products Inc., 100 Pennsylvania Ave., Framingham, MA 01701, (617) 875-6100.
Inquiry 558.

STB released a memory board, called the C-Ram 384, for the IBM PC Convertible. The C-Ram 384 plugs into a single slot and offers 384K bytes of CMOS RAM, expanding the portable's 256K base memory to 640K. The board connects directly to the IBM memory cards that come as standard equipment in the computer. The C-Ram 384 sells for $495. Contact STB Systems Inc., 601 North Glenville, Suite 125, Richardson, TX 75081, (214) 234-8750.
Inquiry 559.


The StarBase subsystem for the PC Convertible.

Desktop Publisher

Studio Software has released a desktop publishing package called FrontPage for the IBM PC XT and AT. The program uses an icon-oriented display and comes with a font library and preformatted document layouts. Features include full hyphenation and justification, capability to mix type styles and sizes, and on-screen editing. You can import graphics files from spreadsheet, drafting, and drawing programs.

To use the software, you need at least 512K bytes of memory (640K is recommended), a math coprocessor, graphics card and monitor, and a laser printer (Apple LaserWriter, AST TurboLaser, HP Laserjet, or QMS PS 800). FrontPage has a suggested retail price of $695. Contact Studio Software, 17862-C Fitch Ave., Irvine, CA 92714, (800) 821-7816; in California, (714) 474-0131.
Inquiry 560.

Five Graphics Modes on One Chip

NSI Logic announced a chip that emulates five graphics display adapters for the IBM PC. These include IBM's Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), and Professional Graphics Adapter (PGA), as well as the Hercules Graphics Card. Although several graphics boards are available that can emulate a variety of standards, the chip, called the EVC-315, is one of the first that features PGA emulation. In addition to these five modes, the chip supports a double-scanning mode with a resolution of 640 by 400 pixels, which is compatible with software using the CGA's resolution of 640 by 200.

The EVC-315 chip also has a RAM-resident character generator that can store 256 characters (expandable to 512 or 1024 characters) with a maximum size of 32 by 8 pixels. It can drive monitors at bandwidths from 15.75 kHz to 38 kHz and, the company claims, it has a high graphics throughput.

Available to OEMs, the chip costs $65 per unit in a minimum quantity of 10,000. Contact NSI Logic Inc., Cedar Hill Business Park, 257-B Cedar Hill Rd., Marlboro, MA 01752, (617) 460-0717.
Inquiry 561.

Internal CD-ROM Drive from Panasonic

Panasonic announced a half-height CD-ROM disk drive that fits internally in IBM PC–compatible computers. The Model SQ-D1 drive can be installed in the computer's floppy or hard disk slot and can access up to 540 megabytes of data from a CD-ROM disk. With the addition of an SCSI port, a single computer can access as many as eight CD-ROM drives.

The drive provides a maximum access time of 650 milliseconds and a data transfer rate of 1 megabyte per second. The unit also has a built-in audio interface; the interface card for the IBM PC has a stereo port that can be connected to a standard stereo set.

The internal drive is priced at $1495; an external standalone version (SQ-D101) is also available and costs $1795. Contact Panasonic Industrial Co., One Panasonic Way, Secaucus, NJ 07094, (201) 348-7000.
Inquiry 562.

LAN Tester

The Smart LAN Performance Test program is a standardized test package that enables users to compare LANs in a simulated working environment. Innovative Software says test results measure throughput as well as the productivity levels you can anticipate in actual usage. The menu-driven package can be used on any LAN operating system compatible with IBM NETBIOS and DOS CALL 3.1 or later.

The tester chooses the application to be run on each workstation and the level of usage. The application runs in a loop on each station until stopped by the tester. After each workstation is "busied out," the tester can have Smart LPT perform timed tests. Smart LPT can be run on a single PC to establish a baseline timing for comparison. Results can be printed in a bar chart or spreadsheet.

The Smart LPT costs $49.95. Contact Innovative Software Inc., 9875 Widmer Rd., Lenexa, KS 66215, (800) 438-7627; in Kansas, (913) 492-3800.
Inquiry 563.

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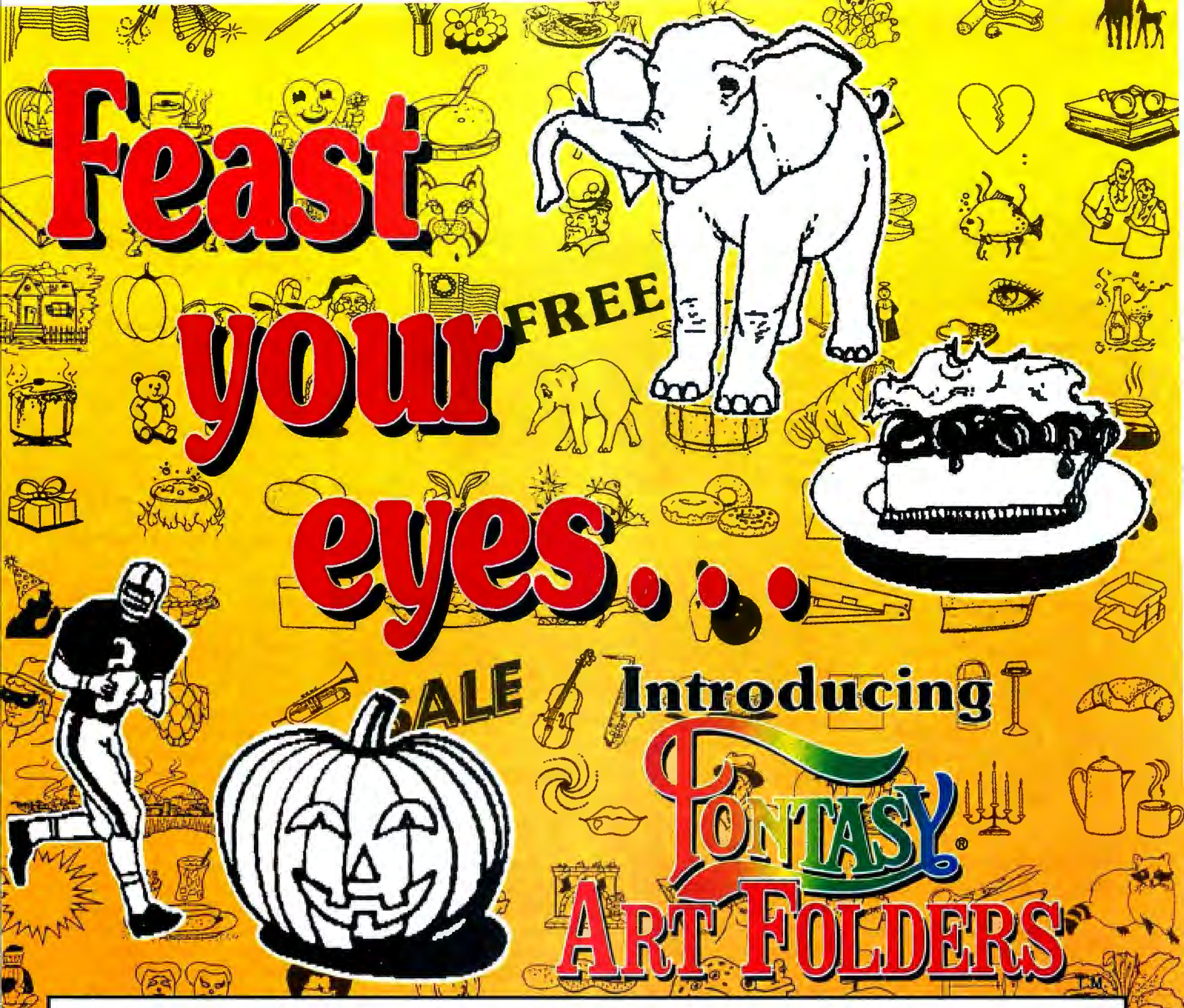

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QINT also sells a set of fifth-generation tools to work with QINT/SQL: QINT/TINA, a package that automates Nijssen's Information Analysis Methodology, a stepwise approach to data analysis based on semantic modeling concepts. TINA takes you through the necessary steps with a graphical interface and integrates and validates the components of the final Information Structure Diagram. TINA for micros is $5000.

Contact QINT Database Systems Corp., 125 Roberts Rd., Waltham, MA 02154, (617) 891-3377.
Inquiry 568.

Tandon Announces Line of PCs

After years of selling personal computers under other manufacturers' labels, Tandon has announced a line of computers that it will sell through retailers under its own label.

The XT-compatible models, called the PCX series, share the same capabilities and features as the IBM PC XT except that they include a parallel port as standard. A system with two floppy disk drives and 256K bytes of memory costs $1295. A 14-inch amber monochrome monitor lists for $190, and a display adapter card, which can display either text but no graphics on a monochrome display or color graphics on an RGB monitor, lists for $90. A serial port costs about $100.

The AT-compatible models, called the PCA series, are identical to the IBM PC AT except that they feature a dual-speed 80286 processor that runs at 6 or 8 MHz with one wait state. In addition, the operating system for these models can access disk drives that are larger than 32 megabytes, the limit for most MS-DOS-based systems. The PCA with a 1.2-megabyte floppy and 512K bytes of memory costs $2195, without a monitor. The PCA is also available with 20- and 40-megabyte hard disk drives for $2695 and $3595, respectively. Total system cost for a 20-megabyte unit with monitor and serial port is $3075. For more information, contact Tandon Corp., 20320 Prairie St., Chatsworth, CA 91311, (818) 993-6644.
Inquiry 569.

The Transpac portable hard disk drive for IBM PCs.

Portable Hard Disk

The Transpac from Microcomputer Memories is a portable 3½-inch hard disk drive that connects via cable to IBM and compatible computers. The unit has its own controller and uses the computer's power supply. Its average access time is 65 milliseconds.

The drive weighs less than 3½ pounds and measures about 2½ by 4 by 6 inches. Prices are $595 for a 10-megabyte model and $895 for a 20-megabyte model. For more information, contact Microcomputer Memories Inc., 6855 Vineland Ave., Chatsworth, CA 91605, (818) 700-8000.
Inquiry 570.

WHERE DO NEW PRODUCT ITEMS COME FROM?
The new products listed in this section of BYTE *are chosen from the thousands of press releases, letters, and telephone calls we receive each month from manufacturers, distributors, designers, and readers. The basic criteria for selection for publication are: (a) does a product match our readers' interests? and (b) is it new or is it simply a reintroduction of an old item? Because of the volume of submissions we must sort through every month, the items we publish are based on vendors' statements and are not individually verified. If you want your product to be considered for publication (at no charge), send full information about it, including its price and an address and telephone number where a reader can get further information, to* New Products Editor, BYTE, *One Phoenix Mill Lane, Peterborough,* NH 03458.

Fiber-Optic Ethernet Connections

Codenoll Technology introduced two fiber-optic Ethernet connections for the IBM PC, XT, AT, and compatibles that operate at a rate of 10 megabits per second. According to the company, the use of fiber optics permits throughput five times greater than that of broadband systems and two and a half times greater than that of twisted-pair systems. The connections, each of which comes on a plug-in board, contain a 2000-meter fiber-optic Ethernet Transceiver.

The Codenet-3051 Fiber Optic Ethernet PC Connection is compatible with 3Com products and costs $995. The Codenet-3061 Fiber Optic PC Network Adapter Card, which sells for $1195, is compatible with Sytek products and IBM's NETBIOS. For more information, contact Codenoll Technology Corp., 1086 North Broadway, Yonkers, NY 10701, (914) 965-6300.
Inquiry 571.

PC-based Protocol Analyzer

FELINE (Frederick Engineering's Dataline Monitor/Protocol Analyzer) is a general-purpose data communications protocol analyzer on a board that plugs into an IBM PC or compatible computer. Priced at $1595, the board features multiple protocols, bit error rate testing, full-screen graphics presentation, and data analysis. FELINE comes with software, an RS-232C interface pod, and a carrying case. Contact Frederick Engineering Inc., 54 Cessna Court, Gaithersburg, MD 20879, (301) 926-6772.
Inquiry 572.

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Inquiry 301

A screen from Profit Technology's Breakthrough! package.

Two Megabytes of Memory for $398

The Breakthru/PC, a plug-in board for IBM PCs and compatibles, provides 2 megabytes of memory and conforms to the Lotus/Intel/Microsoft Expanded Memory Specification. The board sells for $398 with 2 megabytes of RAM or $150 without RAM.

Bundled with the board are RAM disk and print spooler utilities, as well as diagnostic software and a setup program for changing the configuration of expanded memory. The company claims that the board performs bank switching 15 percent faster than Intel's Above Board and 25 percent faster than AST's RAMpage. Contact Vericomp, 8825 Aero Dr., Suite 210, San Diego, CA 92123, (619) 277-0400.

Inquiry 564.

Productivity Tool

Profit Technology announced Breakthrough!, a productivity package that has knowledge databases and idea stimulants.

The program is divided into three sections: Interface and Work, Thought Triggering and Amplification, and Tools and Utilities. In the Interface and Work section, the user can use eight different text-editing environments. The section includes a 220,000-word thesaurus. In the Thought Triggering and Amplification section, you can access a preprogrammed database, which includes menu selection, word triggers, and five flashing windows. The Tools and Utilities section includes a biorhythm generator, a program customizer, and a report generator.

ProView, the windowing/applications manager, is a clone of IBM's TopView and enables you to run 250 programs simultaneously through its multitasking capability.

Breakthrough! costs $822 and requires an IBM PC, XT, AT, or compatible with 512K bytes of RAM, two floppy disk drives, a monochrome monitor, and PC-DOS or MS-DOS 2.0 or higher. Profit Technology recommends using an IBM EGA, a color monitor, and a hard disk. For more information, contact Profit Technology Inc., 39 Broadway, New York, NY 10006, (212) 809-3500.

Inquiry 565.

Hewlett-Packard's DraftPro Plotter

The DraftPro from Hewlett-Packard is an eight-pen plotter designed for PC-based computer-aided design. The plotter, which sells for $5400, produces color output on architectural and engineering C- and D-size and metric A1- and A2-size paper, vellum, or film.

Compatible with most computers, the DraftPro is supported by CAD packages such as AutoCAD and VersaCAD. It features a pen speed of 15 inches per second, a 0.001-inch addressable resolution, and 0.2 percent linear accuracy. The plotter's pen-sorting capability enables the device to draw a full buffer of vectors for one color before proceeding to another color, which reduces plot time.

An RS-232C interface and HP-GL support are standard; an HP-IB interface and Japanese kanji character set are available as options. For more information, contact Inquiries Manager, Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303, (800) 367-4772.

Inquiry 566.

Pop-up Outliner, Pop-up Calculator

Popular Programs has two new RAM-resident packages for IBM PCs and work-alikes: an outline processor and an equivalent of Hewlett-Packard's 12C calculator.

Pop-Up Partner, an idea/outline processor, is designed to help you organize information as lists. It uses pull-down menus and comes with outlines that serve as desktop tools (e.g., a phone book, calendar, and expense tracker). The "paragraph" feature lets you write while in the middle of an outline; anything you've written in Partner can be copied in a word-processor or spreadsheet document with a couple of keystrokes.

Partner takes up 99K bytes. It sells for $99.97.

Pop-Up PC-12C Calculator emulates HP's hand-held financial calculator and has the same programming features. It costs $69.95.

Both Pop-Ups run on the IBM PC line under any version of DOS. For more information, contact Popular Programs Inc., 135 Lake St., Suite 180, Kirkland, WA 98033, (206) 822-7065.

Inquiry 567.

Relational Database Compatible with SQL

QINT/SQL, a relational database system compatible with IBM's Structured Query Language/Data System and Database 2, is designed primarily for users of PCs in an environment where SQL/DS or DB2 is installed on IBM mainframes. The package enables you to access and manipulate mainframe data from a PC and to prototype systems on the micro and then migrate them to the bigger machine.

With the QINT/Application Development Tool, you can build customized end-user applications that utilize a database. ADT can work on several sets of rows of a table simultaneously. Calculations and system values can be shown on the same screen as data retrieved

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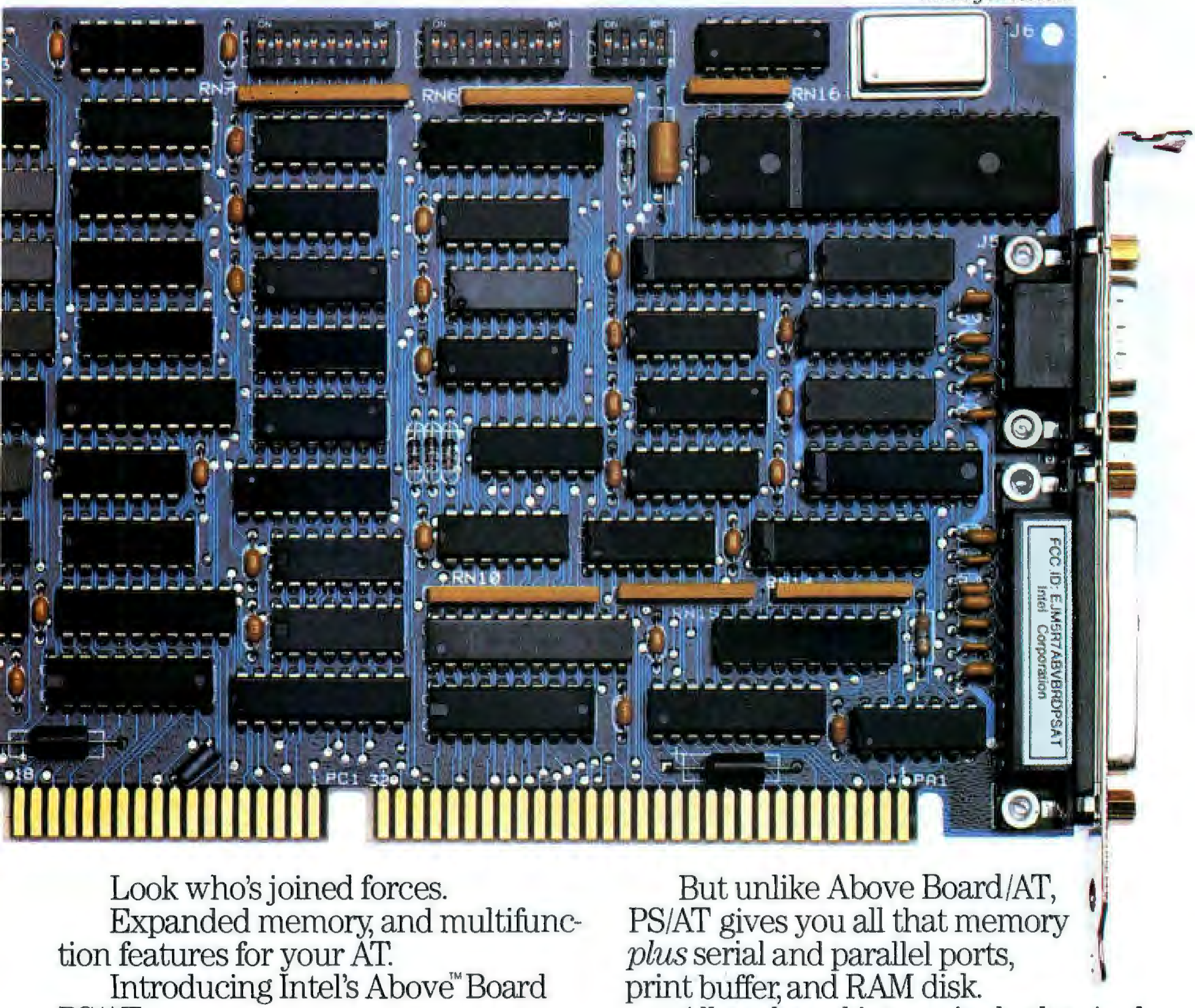
Intel announ

Multifunction



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Inquiry 78

ADVANCED MS-DOS
Ray Duncan
Microsoft Press
Redmond, WA: 1986
468 pages, $22.95

TECHNICAL TOPICS FOR THE IBM PC FAMILY OF MICROCOMPUTERS: An Annotated Bibliography of Recent Books

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ADVANCED MS-DOS
Reviewed by John D. Unger

If you are a programmer who needs to interface software and hardware with MS-DOS, *Advanced MS-DOS* by Ray Duncan will guide you. You can learn how to use MS-DOS interrupts and their associated functions so your application programs can do file I/O and write to the screen, or you can figure out how to access peripherals quickly and efficiently.

Given the title and subject matter of the book and its author's expertise, you might expect *Advanced MS-DOS* to be difficult to read, but that's not so. Duncan's informal style is carried over from his regular columns in *Dr. Dobb's Journal of Software Tools*. The opening chapter on the history of MS-DOS, for instance, reads like a good biography. *Advanced MS-DOS* exemplifies how a highly technical book can be both informative and readable.

READER REQUIREMENTS

To benefit from this book, you should be able to understand the 8086 assembly language programs that are liberally sprinkled throughout the text as examples. If you have already worked through a good introductory book on 8086 assembly language programming—such as *Assembly Language Primer for the IBM PC & XT* by Robert Lafore (New American Library, 1984)—you will be able to launch yourself into a higher level of assembly language programming with *Advanced MS-DOS*.

Duncan uses C-language programs as examples to explain how to interface high-level programs with MS-DOS functions. But because he is basically an assembly language programmer, he emphasizes writing efficient assembly language code either as stand-alone programs or as functions or procedures to be linked to other high-level language programs. Many of the programs are useful not only as examples but also as the basis of a library of valuable MS-DOS utility and programming tools.

Unless you enjoy typing in endless lines of source code and then searching for syntax errors and other self-induced bugs, you may want to take advantage of the companion disk to *Advanced MS-DOS*. This disk contains the assembly and C-language source code for all the example programs described in the book. Also included are ready-to-run, executable versions of these same examples. Although Duncan recommends using the latest versions of the Microsoft Macro Assembler, MASM version 4.0, and Linker, LINK version 3.05, to assemble and link the source code, I had no problems using MASM version 1.25 and LINK version 2.01 on an AT&T 6300. The .EXE and .COM programs ran perfectly.

The disk also includes utility and example programs that do not have source code listings in the book but that illustrate topics the author discusses. This disk is a great timesaver for those who will actually use the example programs; an order blank for the disk is included in the book.

APPEARANCE AND ORGANIZATION

The layout of *Advanced MS-DOS* is both handsome and helpful. The example programs and fragments of source code are printed in a reverse-video effect with black characters on a light brown background. This makes the code listings stand apart from the text without interfering with their readability.

The material is divided into four sections. The first and largest describes the MS-DOS system services on a category-by-category basis. Section 2, a complete reference guide to all the MS-DOS interrupts, is more than you would expect from a typical programmer's reference manual. Included with the description of how to load the proper registers to call a specific function are notes about the "nonstandard" behavior of the function and how it behaves under different versions of MS-DOS. This is clearly an added bonus of the author's expertise. Every function's description includes a short assembly language example program that can serve as invaluable code fragments when you're writing your own programs to call functions. Two final, shorter sections are reference guides to the special interrupts in the IBM PC ROM BIOS and to the Lotus/Intel/Microsoft expanded memory specifications.

HIGHLIGHTS

One factor that distinguishes *Advanced MS-DOS* from a technical reference manual is the way in which the author treats nonstandard methods of accessing system services. Duncan explains the "correct" and most portable method for accessing an operating system service. He also demonstrates how to use less portable, hardware-dependent methods when speed (rather than portability or compatibility with future versions of the operating system) is the driving force. This approach makes the book more valuable than a mere transliteration of a manual. The author's effectiveness as a programmer adds real merit to these explanations, providing insights into how to accomplish your programming tasks most efficiently.

A chapter on accessing MS-DOS's file- and record-manipulation functions is one of the book's highlights. Because of the historical ties between CP/M and MS-DOS, two methods of controlling files exist in MS-DOS. Duncan provides an in-depth discussion of file management first by comparing the file control block (FCB) and file han-

(continued)

dle methods of file access and then by explaining why he recommends the latter method.

The author devotes an entire chapter to programming for the character I/O devices, such as the video display, keyboard, printer, and serial port. He discusses the pros and cons of using three distinct methods of video display control on MS-DOS and PC-DOS microcomputers.

One example, from the chapter that discusses the MS-DOS EXEC function, presents a program for a simple, table-driven command interpreter shell that overlies COMMAND.COM. This program is designed as a model that can be expanded to provide a customized user interface for special applications. Two parallel listings of the program are presented, one written in C and the other in assembly language. The functions and procedures in the two listings are similar enough to enable the reader to compare and contrast the two versions of the program.

A Worthy Reference

Advanced MS-DOS is a good example of what a technical reference manual should be. Because my interest is in graphics programming, however, I wish that the author had addressed efficient use of the Enhanced Graphics Adapter functions. But because that is mainly a hardware-dependent problem, its lack of coverage does not detract from the book or its intention.

Clearly, Duncan's strengths include a style that is at once easily read, a thorough coverage of the subject matter heretofore unknown, and the frequent use of examples in the form of assembly language programs and code fragments. *Advanced MS-DOS* contains a great deal of valuable information that I know I will frequently refer to.

John D. Unger (P. O. Box 95, Hamilton, VA 22068) *is a geophysicist for the U.S. Government who also writes graphics programs in assembly language and C for microcomputers.*

TECHNICAL TOPICS FOR THE IBM PC FAMILY:
An Annotated Bibliography
Compiled by Donald Evan Crabb

This collection of book annotations, intended as a follow-up to those that appeared in BYTE's last IBM Special Issue (Fall 1985), covers several recently published books on technical topics addressing the IBM PC, XT, PCjr, AT, and compatible computers. The books, all softcover, are divided into three sections: hardware issues, PC-/MS-DOS and related operating systems issues, and programming. This bibliography reflects availability and bias and cannot be considered inclusive.

Hardware Issues

This topic is a catchall for books that cover the hardware design and architecture of the PC, including such issues

(continued)

as connecting your PC to a variety of external devices, how to design the hardware and software interfaces that are necessary, how to network PCs, and discussions of the hardware and software that make up the PC.

Berry, Paul. *Operating the IBM PC Networks*. Berkeley, CA: Sybex, 1986. $19.95. 363 pages.

As local area networks become more important to PC users, the plethora of conflicting network topologies, protocols, and systems becomes more and more mind-boggling. Paul Berry's *Operating the* IBM PC *Networks* helps to sort out some of this information for both the newly released IBM Token Ring network (a baseband configuration) and the older broadband PC Network.

This handbook should prove very useful to LAN users of either network, as well as to potential network customers. It covers information for network administrators, end users, and network consultants. The introduction to LANs is helpful, and the 14 chapters that follow cover most of the important aspects of the two networks in detail. Topics include how to set up and run the equipment, how to automate network usage for end users, how to start and restart the networks, how to use electronic mail over the LAN, how to manage shared resources and disks, and how to optimize the network performance.

The book's only drawback is that it limits coverage to PC Network and IBM Token Ring. I'd like to see similar handbooks for some of the other network systems crowding the market.

Byers, TJ. *Inside the IBM PC AT*. New York: McGraw-Hill, 1985. $19.95. 309 pages.

If you can ignore its enthusiastic narrative style, TJ Byers's *Inside the IBM PC AT* will reward you with comprehensive technical information about the AT. The author covers all the important hardware and software aspects of the AT in detail for experienced PC users and programmers.

Byers provides descriptions and illustrations to help novice AT users get their machines up and running, but the heart of the book lies in the technical discussions of PC-DOS, custom programming, and AT hardware.

Eggebrecht, Lewis C. *Interfacing to the* IBM *Personal Computer*. Indianapolis, IN: Howard W. Sams & Co., 1985. $16.95. 246 pages.

If you're about to attempt to interface a variety of devices to your PC and want to find out just what general issues are entailed, *Interfacing to the* IBM *Personal Computer* is a good place to start. Unfortunately, this reference handbook doesn't present specific interface designs, so much of its practical utility is lost. However, it does provide general information about interfacing the PC, details about the PC

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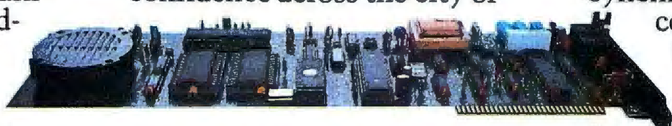

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bus, system interrupts, the 8088 microprocessor, memory, and interface signal conditioning. The book would have been much more useful had it discussed some sample interfaces in detail.

Foster, Dennis L. *The Practical Guide to the IBM Personal Computer AT*. Reading, MA: Addison-Wesley, 1985. $19.95. 455 pages.

Of the two handbooks annotated here that discuss the IBM PC AT (the other being Byers's book, above), this one is by far the better book for the novice. The architecture, design, and operation of the AT are covered in prose that users new to the AT will find easy to digest. Dennis Foster covers a number of software issues, including TopView, XENIX, PC-DOS (3.0 and 3.1), and the basics of networking. Hard disks and the new quad-density floppy disk drives are also examined.

Despite its 455 pages, *The Practical Guide to the* IBM *Personal Computer AT* seems a little thin, especially since its design leaves much of each page blank. The illustrations are also overly simplistic. For technical information about the AT, I preferred the Byers book.

Morse, Stephen P., and Douglas J. Alpert. *The 80286 Architecture*. New York: John Wiley and Sons Inc., 1986. $24.95. 279 pages.

Stephen Morse, the principal architect of the Intel 8086, has previously written about the 8086 and 8087. Douglas Alpert was formerly a staff engineer at Intel Corporation and along with Morse was instrumental in the development of the Intel 86 family of microprocessors. These men share impressive credentials for writing about the 80286 architecture, and they know what they're talking about. In a nutshell, their book is authoritative yet accessible to programmers who don't have a lot of assembly language background.

Morse and Alpert provide more than a detailed analysis and description of the Intel 80286 and 80287 chips. They discuss the chips' instruction sets; how their multitasking, virtual memory, and system security features work; and how you can build a computer around them. Further, the authors show how to program the 80286 and 80287 for scientific, business, and industrial purposes.

Morse and Alpert also offer us a brief history of the development of the modern microprocessor from the point of view of Intel Corporation. If you want the inside information about the 286/287, this is the book to read.

PC-/MS-DOS

More capabilities have been added to DOS as the PC has matured from an 8088-based machine to one using the

(continued)

80286 chip (DOS versions 1.1, 2.0, 2.1, 3.0, 3.1, 3.2, etc.). The books in this section are user's guides for DOS, written from the point of view of the serious PC user who wants more technical and practical information about the operating system and a DOS reference that's easy to use.

DeVoney, Chris. *Using PC-DOS*. Indianapolis, IN: Que Corporation, 1986. $21.95. 519 pages.

Chris DeVoney's *Using PC-DOS* is an interesting combination of a PC-DOS tutorial, a PC-DOS advanced guide, and a PC-DOS reference handbook. The material is familiar, of course, but the structure and explanations of this book help set it a step above the ordinary. The book could also serve as a textbook for a course on using DOS.

It's easy to read, and it covers all the DOS commands and usage that it should. The command reference section is particularly handy. Along with Wolverton's book (below), it's my favorite DOS handbook, primarily for its clarity and writing style.

Kamin, Jonathan. *MS-DOS Power User's Guide*. Berkeley, CA: Sybex, 1986. $19.95. 397 pages.

If you use your PC for more than a few hours a day, this is a useful book. Jonathan Kamin lists batch programs, BASIC programs, display screens, macro files, and assembly language programs, all of which are carefully designed to help you get more out of your PC. For example, you can configure your system using a chapter on writing CONFIG.SYS and AUTOEXEC.BAT files. If you want to customize the screen colors on your display, just refer to the chapter on customizing your screen and keyboard.

MS-DOS Power User's Guide contains valuable information about the PC and DOS. Undocumented commands and hard-to-find technical details abound. Much of what Kamin presents is available elsewhere, especially in the Peter Norton books (see last year's IBM bibliography), but the organization here is half the reason for buying the book. Kamin has made it easy to find the technical trickery you need to make your PC jump through hoops.

King, Richard Allen. *The MS-DOS Handbook*, 2nd edition. Berkeley, CA: Sybex, 1986. $19.95. 339 pages.

The MS-DOS Handbook is really two reference books in one. Richard King divides his text into a programmer's handbook and a user's handbook. The programmer's handbook discusses the detailed specifications of disk and file operations, keyboard control, monitor and port control, and memory management of MS-DOS. King also includes full descriptions of all operating system functions needed to write MS-DOS programs, including good programming examples.

The user's handbook includes information on EDLIN,

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DOS files, how to configure the system, batch processing, monitors, serial ports, and more.

The MS-DOS Handbook contains a good discussion on the issues of software compatibility, offers a guide to the different versions of MS-DOS. This is a useful book, especially for its programmer's handbook discussions. The novice material is neither as useful nor as detailed.

Siechert, Carl, and Chris Wood. ***The Power of Running PC/DOS***. Portland, OR: Management Information Source, 1986. $22.95. 386 pages.

The Power of Running PC/DOS is really a handbook for the latest versions of DOS (3.0, 3.1, and 3.2). It can be used equally well by novices and experienced PC users. Siechert and Wood cover familiar ground in their PC setup instructions, DOS command references, directory structures, and DOS utility programs. The book also includes a number of useful BASIC programs that you can type in and run.

It's clearly designed, easy to read, and contains useful examples. Overall, though, it's a bit thin; other books mentioned cover the same material in greater detail.

Wolverton, Van. ***Running MS-DOS***, 2nd edition. Redmond, WA: Microsoft Press, 1985. $21.95. 423 pages.

This book is simply the definitive handbook of PC-/MS-DOS. It has been expanded and improved to cover the newer releases of MS-DOS. *Running MS-DOS* is written for both novices and experienced users. Carefully structured, it contains copious examples and is a model of expository clarity. Van Wolverton's new edition fixes some mistakes of the first edition, adds new material, and explains all the commands and techniques users need to know about managing files and disks, creating custom commands, automating the execution of frequently used commands, managing a hard disk, and manipulating the screen display, printer, and telecommunication devices.

PROGRAMMING

The IBM PC and its compatibles work with a variety of high-level programming languages (through PC-/MS-DOS and CP/M-86): BASIC (interpreted and compiled), Pascal, FORTRAN, COBOL, LISP, and C. Also, the PC can be programmed effectively with 80xxx assembly language. The books listed here teach some technical aspects of high-level or assembly language programming on the PC.

Busch, David D. ***Program Your IBM PC to Program Itself!*** Blue Ridge Summit, PA: Tab Books, 1986. $12.95. 145 pages.

Though the title sounds strange, *Program Your IBM PC to Program Itself!* delivers on its promise. David Busch has

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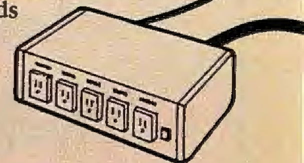

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assembled a collection of 19 BASIC programs that will save you a lot of time and effort. Included are programs that display graphics screens for presentations, create the skeleton for database programs, check programs for spelling mistakes or incorrect punctuation, provide screen editing, count the words in your document or program, redefine function keys, and design custom screens.

Each program is listed in full (a disk containing the programs is available for $24.95), and a useful description is also provided. The book assumes that you are a PC BASIC programmer and are familiar with PC-DOS.

Campbell, Joe. *Crafting C Tools for the IBM PCs*. Englewood Cliffs, NJ: Prentice-Hall, 1986. $21.95. 434 pages.

Just like Stevens's book discussed below, *Crafting C Tools for the IBM PCs* provides examples and tips for making programming tools. This book is also a C-language reference handbook, as well as a handbook for Intel 8088 assembly language and for PC-DOS. The emphasis here is more on using a combination of C and assembly language to perform such tasks as calling DOS and ROM BIOS routines, handling interrupts and screen cursor management, processing the PC's function keys, reading and setting the default drive and directory path, changing a file's time and date stamp and reading the system clock, and creating screen windows and pop-up menus. Although Joe Campbell's book has a wider reach and is easier for less experienced programmers to read than Al Stevens's *C Development Tools for the* IBM PC, novices should probably stay away. The book has a solid structure, with good use of examples. If you know C programming well and are going to use it frequently, put this book on your shelf, along with Stevens's.

Miller, Alan R. *Assembly Language Techniques for the IBM PC*. Berkeley, CA: Sybex, 1986. $22.95. 358 pages.

Assembly Language Techniques for the IBM PC helps you use and adapt assembly language utility programs for your PC. It is structured around a powerful library of assembly language macros that are discussed, explained, and dissected. Alan Miller has developed programs utilizing these macros and he teaches readers how to use them. Miller's book is written in a manner designed to teach you how to use the material presented—and it does a good job.

Miller's treatment of the subject is fairly comprehensive: He covers the ROM BIOS (both versions 2 and 3); PC-DOS (versions 2 and 3); and the system debugging program, DEBUG. The primary focus, however, is on the collection of macros and programs he has assembled that should run on PCs and ATs. These programs handle screen, port, and keyboard control, as well as memory management and disk I/O. A particularly useful program example shows

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you how to expand the PC's usable memory beyond 640K (to 704K) by using the 64K-byte block of memory normally left unaddressed by DOS.

To use the material presented by Miller, you should have experience as a high-level and assembly language programmer. You'll also need a PC with at least two disk drives, 256K bytes of RAM, the Microsoft or IBM assembler, a linker program, and a debugger. If you have the requisite hardware, software, and programming experience, *Assembly Language Techniques for the IBM PC* will reward you with a straightforward discussion of the technical problems and solutions involved in assembly language macro programming on the PC.

Scanlon, Leo J. *80286 Assembly Language on MS-DOS Computers*. New York: Prentice-Hall Press, 1986. $21.95. 316 pages.

Leo Scanlon's *80286 Assembly Language on MS-DOS Computers* can be used by both novice and experienced high-level language programmers who want to learn the Intel 80286 instruction set and assembly language programming on computers using it. The book starts with a brief introduction to binary and hexadecimal arithmetic, moves quickly to the fundamentals of assembly language programming, and then covers macro assemblers and how to build macro libraries.

The author uses plain English. His discussion includes useful programs and segments as illustrative tools. He also covers the SYMDEB debugger, the EDLIN line editor, and all the LINK utilities. He even throws in a discussion of how to program the Intel 80287 math coprocessor chip.

The program examples are so useful that you may well use them after you've finished the book. They include high-precision arithmetic programs, sorting programs, and code conversions.

Stevens, Al. *C Development Tools for the IBM PC*. New York: Prentice Hall Press, 1986. $22.95. 240 pages.

Not designed for the novice C programmer, *C Development Tools for the IBM PC* provides the experienced C programmer with a group of important development tools designed to assist in creating real applications. C language tools that support the development of on-line, interactive software systems on the PC are the province of Stevens's book. The book is really a tutorial workshop for tools such as file management, sorting, indexed data management (using B-trees), screen forms management, and menu management.

The author supplies the examples themselves, with thorough discussions of their purpose and use and the history of their development. It is full of technical details that will help you design and code programs of sound structure and proper syntax. If you are going to be doing

(continued)

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serious (e.g., production) programming on the PC, XT, or AT in C, keep this handbook nearby.

Troy, Douglas A. ***Complete C Language Programming for the IBM PC***. Boston, MA: Little, Brown and Company, 1986. $24.95. 505 pages.

When you start to read *Complete C Language Programming for the IBM PC*, you may forget that you are reading a book about programming a PC. Not because there aren't copious references to the PC—there are. Not because there aren't examples of specific PC implementations—there are. Not because there aren't discussions of C language compilers for the PC—they are here also. It's the tone and orientation of the book that might throw you. There's no doubt that this book is written by a systems analyst who's had a lot of experience designing and coding C programs on larger computers. Discussions of program development, design, and coding are written in a way that bespeaks a large systems analysis orientation.

Is this approach effective? Surprisingly, yes. In fact, the book does an excellent job of teaching C programming on the PC. I would have liked to see specific discussions of C compilers incorporated into examples in the text (rather than relegated to an all-too-brief appendix), since the differences in performance and implementation are much greater among compilers than Troy admits. But that's a small complaint. This book will teach you the C language with the proper emphasis on good programming style, including top-down design and structured development methods. Troy uses two application programs, a calculator and a stock-portfolio system, to teach C. They are developed and refined with each chapter as more of the C language is revealed. *Complete C Language Programming for the IBM PC* assumes that you have solid programming experience on the PC with another language—Pascal would be helpful.

OTHER SOURCES

Several sources exist for readers to research for further information relating to specific topics on IBM PCs. Although the sources that follow are general and include other aspects and machine-specifics, they can be very instructive.

Bowker, R. R., and Company. ***Bowker's 1985 Complete Sourcebook of Personal Computing***. New York: R. R. Bowker Company, 1985. $19.95. 1050 pages..

Brand, Stewart, ed. ***The Whole Earth Software Catalog for 1986.*** Garden City, NY: Quantum Press/Doubleday, 1985. $17.50. 224 pages.

Char, Carlene, ed. ***Computer Book Review.*** Honolulu, HI: Maeventec, 1986. $20 for 12 issues.

Couger, J. Daniel. ***Computing Newsletter for Schools of Business: Bibliography***. Colorado Springs, CO: University of Colorado, 1986. $4 annual issue.

Sammett, Jean E., ed. ***ACM Guide to Computing Literature.*** New York: Association for Computing Machinery, 1986. $60 annual issue.

Sammett, Jean E., ed. ***Computing Reviews.*** New York: Association for Computing Machinery, 1986. $60 for 12 issues. ■

Donald Evan Crabb is the Director of Instructional Laboratories and a lecturer (The University of Chicago, Department of Computer Science, Ryerson Hall 260, 1100 East 58th St., Chicago, IL 60637). His articles and reviews have appeared in several magazines.

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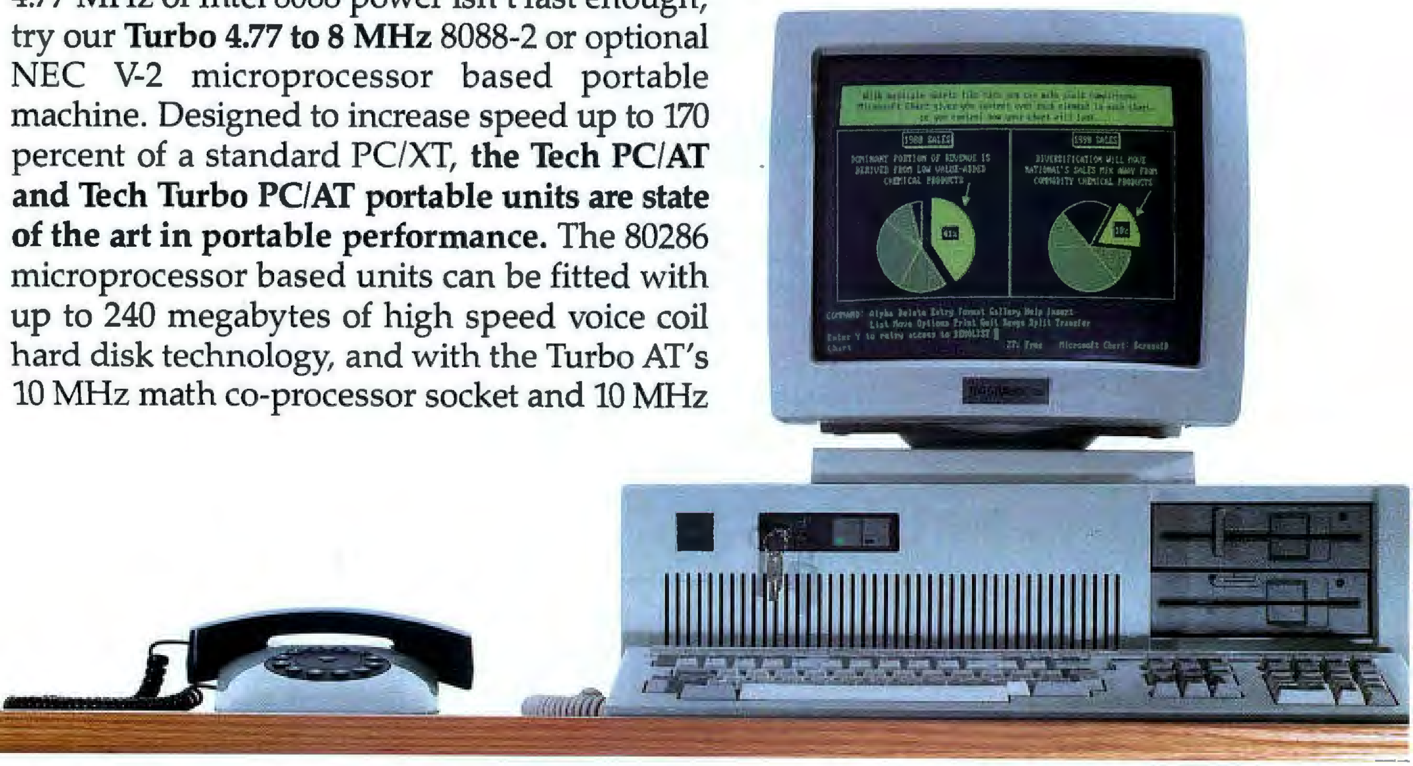

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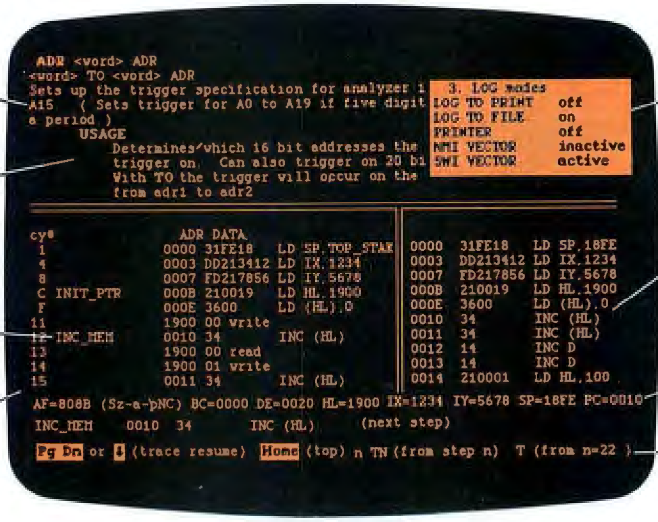

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The IBM RT Personal Computer

Inside IBM's RISC *processor and memory management unit*

BY RICHARD O. SIMPSON

BACK IN 1975 the IBM Research Division began a project to investigate the utility of simple but very high speed computer hardware in a practical computer system. This system became known as the 801 Minicomputer—"801" because the project was located in Building 801 of the IBM T. J. Watson Research Center in Yorktown Heights, New York, and "minicomputer" because the machine was envisioned as being less expensive and physically much smaller than the mainframes of the time.

People who observed noticed that programs running on complex high-performance machines spent most of their time performing only very simple instructions, such as Load, Store, Branch On Condition, and Add. A good deal of the control logic of a complex machine exists for the instructions that require multiple cycles and for the complexities of memory operands that cross page boundaries and therefore could cause a page fault partway through an instruction's execution.

A stripped-down machine, one that is simpler than the IBM System/370, for example, could be made faster if it didn't have to deal with complex but statistically seldom-used operations. The goal of the 801 computer project was to produce a machine that executed programs at a sustained rate of one instruction per machine cycle. To achieve this rate, the instructions could not be very complex. All arithmetic and logical instructions were defined to operate on the contents of registers; there were no instructions like Add To Memory or Move Memory To Memory. Only simple addressing modes such as base plus displacement and base plus index were provided so that effective address calculation could be executed in a single cycle.

Operations that would inherently take multiple cycles—such as Multiply—were not provided. Instead, a single-cycle Multiply Step instruction was provided. In addition, provisions were made for very efficient linkage to a subroutine that would build the complex Multiply function out of the primitive Multiply Step instructions.

Optimizing the Compiler

The level of the instruction set of the 801 was comparable to the microcode level of more traditional machines. As a result, more 801 instructions were needed to perform a given function than, for example, IBM System/370 instructions. The size of the programs was not a problem. Memory costs were decreasing, and any product based on the 801 would more than likely be a virtual memory system. However, if an 801 program were a great deal longer than the equivalent program for a traditional machine, it would take longer to execute even at only one cycle per instruction.

The solution was a highly optimizing compiler to shorten an 801 program by eliminating redundant calculations, moving calculations out of

(continued)

Richard O. Simpson holds B.S. and M.E.E. degrees from Rice University and is a member of IBM's Advanced Engineering/Scientific Development organization in Austin, Texas. Since 1981 he has been involved in the architectural definition of ROMP and its memory management unit and more recently in the definition of the IBM RT Personal Computer. He can be contacted at IBM Corporation, Advanced Engineering/Scientific Development, 11400 Burnet Rd., Austin, TX 78758.

loops, performing calculations at compile time, and eliminating unnecessary loads and stores. The compiler and the language it compiled were named PL.8; the language is a system-programming dialect of PL/I, and the ".8" refers both to 801 and to the fact that the language was originally PL/I with those features not useful for system programming (about 20 percent) removed.

The design of the 801 went through several iterations. An early version had sixteen 24-bit registers and a mixture of 2-byte and 4-byte instructions. (The registers were 24 bits wide to simplify construction of a prototype from discrete logic.) The final design had thirty-two 32-bit registers and only 4-byte instructions. Restricting the instruction format to only one size simplified instruction decoding enough so that the machine's cycle time could be reduced.

The instruction set of 801 was specified in conjunction with the design of the PL.8 compiler. Instructions were included based on the needs of the compiler rather than the perceived needs of an assembly language hand-coder. The high-level language was to be the programming interface, through the PL.8 compiler or other compilers.

The designers provided many general-purpose registers because it is easy for a compiler to manage such a large set and it makes for more efficient code by eliminating most "spill" code requirements. The shift in design from 16 to 32 registers was based on compiler studies, which showed that the extra registers were worth the extra hardware cost.

MEMORY BANDWIDTH

Each 801 instruction was one word (32 bits) long, aligned on a word boundary in memory. The width of the data path to and from memory was also 32 bits. Since about 30 percent of the dynamic instruction mix was Load and Store instructions, the memory interface had to supply an average of 1.3 words per machine cycle. To maintain this rate the 801 had separate caches for instructions and data, each of which could handle one word per cycle.

A load from the cache took two cycles altogether. In a form of delayed branch called Branch With Execute, the instruction physically following the branch was always executed regardless of the branch condition. This gave the instruction cache an additional cycle in which to supply the branch target.

These efforts to keep throughput high were successful. Executing instructions on the 801 was somewhat like drinking from a fire hose. The sustained execution rate was around 15.1 million instructions per second at a

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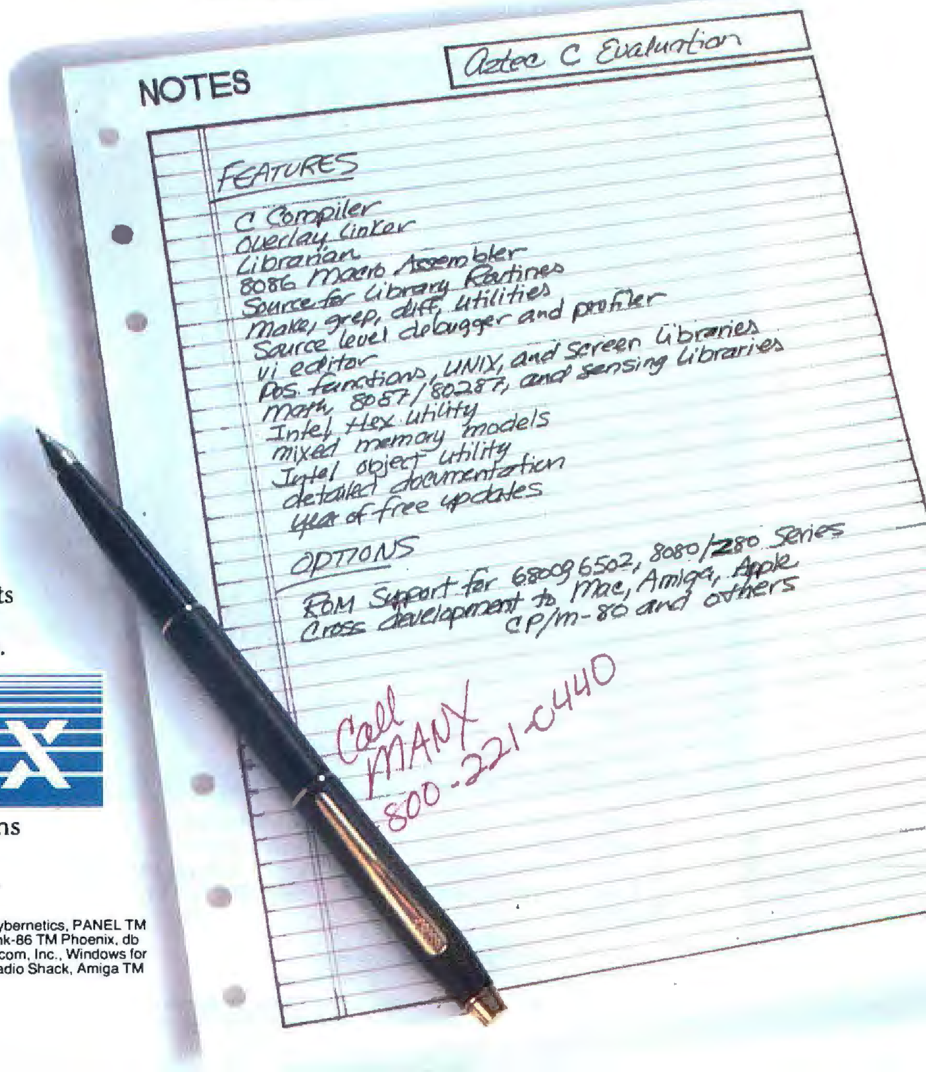

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cycle time of 63 nanoseconds, or about 1.1 cycles per instruction.

Other research groups outside IBM reached the same conclusions regarding rapid execution of simple instructions. The term RISC (reduced instruction set computer) was coined by a group at Berkeley that built a machine with a very simple instruction set. Another group at Stanford devised a machine (MIPS) in which simple operations were executed in parallel in a pipeline, with the compiler responsible for keeping conflicting operations from being scheduled simultaneously.

EVOLUTION OF ROMP FROM THE 801

After the definition of the 801, a project began in the IBM Office Products Division. Its goal was to apply what had been learned on the 801 project to a new microprocessor for use in IBM products. This processor became ROMP, an acronym for Research/OPD Micro Processor.

Most project code names in IBM are changed each year or two, but ROMP was appealing enough that it stuck with the project through the announcement and release of the IBM RT Personal Computer in early 1986. [*Editor's note: In the interest of consistency, the term* RT *processor is used throughout this article to describe the* RISC *chip. The acronym* ROMP *is used only where reference is made to the forerunner of the* RT *processor, the* Research OPD/Micro Processor.] As a microprocessor for a product rather than a minicomputer in a research project, from the start ROMP had different goals from the 801. The 801 strove to maintain the maximum execution speed consistent with its single-cycle-per-instruction design philosophy regardless of hardware cost. Thus the 801 had simpler hardware than, for example, the IBM System/370, but it still had two high-speed caches and multiple internal buses. These were not appropriate for the RT processor, which was to be a single-chip microprocessor.

The cost/performance ratio was important for the RT processor, and two caches were out of the question for a single-chip computer under design in the late 1970s. The lack of cache could not be made up by simply providing very fast memory, again for cost reasons. The RT processor design evolved from a complex set of tradeoffs involving hardware cost, machine cycle time, overall throughput, and the amount of logic that could be fitted onto one VLSI chip.

COMMON PHILOSOPHY

The RT processor and the 801 have the same architectural foundation. Both are true general-register ma-

(continued)

chines in which all computation is done on quantities in registers, and no distinction is made between computation on data and addressing arithmetic. Any register can hold a data quantity or a base address. In both machines the movement of data to and from memory is separated from computation by the use of explicit Load and Store instructions. Most instructions execute in a single cycle. The memory addressing model for each is a simple, linear, byte-space addressed by a 32-bit quantity.

DESIGN DIFFERENCES

The two machines could not be the same, however, because of the tradeoffs discussed above. The most pervasive change was the removal of the two caches. The lack of cache affected everything from the instruction set to the number of registers to page-fault handling.

All 801 instructions were one word long, which made for simple instruction decoding. The 32-bit format allowed room for multiple fields used to hold register numbers (each 5 bits long). The typical instruction specified two source registers and a destination register.

These three-address instructions made for efficient code because it was not necessary to copy one register to another to avoid destruction of one of the operands. The use of all 4-byte instructions means that the CPU's memory bandwidth requirements are greater than one word per cycle. Thus if the RT processor, without caches and with a memory bus width limited to 4 bytes, had implemented the 801 instruction set directly, it could never have achieved a rate of one instruction per cycle.

To reduce the RT processor's memory bandwidth requirements, a 2-byte instruction format was introduced. The instruction set was a mixture of 2-byte and 4-byte instructions with the short format predominating in the dynamic mix. The average instruction length is about 2.5 bytes (versus exactly 4 for the 801). Because about 30 percent of instructions are for loading or storing, the overall bandwidth requirement is about 3.7 bytes per instruction. A memory subsystem that could supply 4 bytes per cycle could keep up with the RT processor's bandwidth requirement.

The 2-byte format couldn't accommodate three 5-bit register fields plus a reasonable size op code, so the instructions were made two-address and the register field size was cut from 5 bits to 4. Consequently, the RT processor uses only 16 general registers (the 801 uses 32).

PRACTICAL COMPLEXITY

To make subroutine linkage as efficient as possible for the RT processor,

(continued)

instructions that load and store a series of registers were introduced. These were not needed on the 801, where a string of individual Load or Store instructions would execute at maximum speed, but they are handy on the RT processor because they allow the entire memory bandwidth to be used for transferring data.

These instructions are complex in comparison to the other single-cycle instructions. They require multiple cycles and must have the ability to handle cases in which a page fault occurs in the middle of the sequence of loads or stores. To provide for this type of instruction and allow other instructions to take multiple cycles (such as the infrequently used Divide Step), the RT processor was designed as a microcoded engine. (By contrast, the 801 was hard-wired.)

A microprogram is executed for each RT processor instruction, but for most of the instructions the microprogram is exactly one step long (most instructions take only one cycle). The microprograms for the more complex instructions take as many cycles as necessary. Microcode is also used for such housekeeping tasks as CPU checkout and register initialization after power-on reset.

RT Processor Programming Model

The RT processor registers visible to the programmer are shown in figure 1. There are sixteen 32-bit general-purpose registers, numbered 0 through 15. Bits are numbered left to right (high-order to low-order), 0 to 31. This left-to-right numbering scheme is used consistently throughout the RT processor architecture, including memory addressing.

All the general registers are equivalent and can be used for any purpose, addressing or data, with the exception of register 0. When register 0 is specified as a base register, the value 0 is used as the base address rather than the contents of register 0. This provides a means of addressing absolute locations in low memory without requiring that a base register be loaded or that some special direct-addressing mode be provided. This use of register 0 is exactly like that of the IBM System/370.

Each register holds a 32-bit word. Arithmetic is performed using two's-complement notation on the full 32-bit register contents. There are provisions for dealing with short integers (halfwords) and single bytes, both in memory and in the general registers. Some instructions treat the upper half (bits 0 through 15) or lower half (bits 16 through 31) of a register individually, and some deal with the individual bytes within a register (bits 0 through 7, 8 through 15, 16 through 23, and 24 through 31).

In addition to the general registers, the RT processor architecture provides for 16 system control registers (SCRs). As the name implies, most of these are used for controlling the state of the RT processor, but some are directly useful to the programmer. SCRs 6 through 8 are used to control the on-chip interval timer. SCR 10 is the Multiplier/Quotient (MQ) register and is the implied third operand of the Multiply Step and Divide Step instructions. SCR 11 holds Machine Check Status, which reports hardware malfunctions, and Program Check Status, which reports exceptions such as traps, page faults, and illegal operations.

The Interrupt Request Buffer, SCR 12, controls interrupts generated directly by software. SCR 13 is the Instruction Address register (IAR), or program counter. Machine state information, such as virtual address translation on/off, privileged versus unprivileged state, and interrupts enabled/disabled, is kept in SCR 14, the Interrupt Control Status register.

The Condition Status (CS) register (SCR 15) reflects the results of arithmetic operations, comparisons, and other tests. Not all of the 16 SCRs in the architectural scheme are implemented, and of those that are, only SCRs 10 (the MQ) and 15 (the Condition Status bits) are of interest to the

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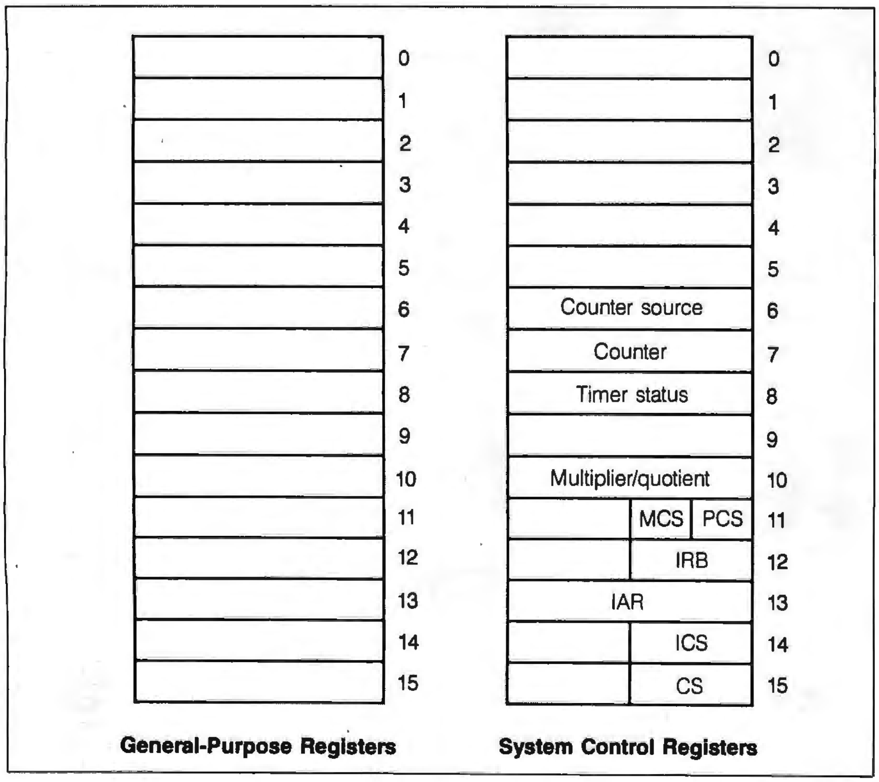

Figure 1: *A model of the RT processor registers. All figures in this article are © copyright International Business Machines Corporation, 1986.*

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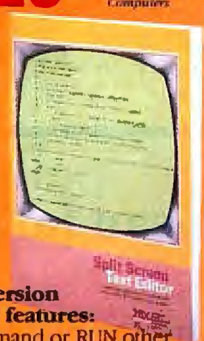

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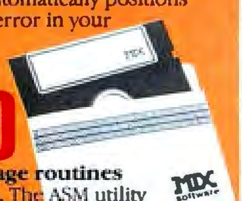

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application programmer. The value in the program counter (IAR) is not normally needed directly. Most branches are implicit relative to the IAR, and the value in the IAR is supplied in a general register automatically by the Branch And Link instructions.

MACHINE STATES

The RT processor has both a privileged state and an unprivileged state. All instructions are valid in privileged state. Instructions that deal with protected SCRs or that can directly modify the machine state or the state of the virtual addressing or memory protection hardware are not allowed in unprivileged state. In either privileged or unprivileged state, the virtual addressing and memory protection mechanism can be enabled (virtual mode) or disabled (real addressing mode).

Normally, the operating system runs all application code in unprivileged state with virtual addressing and protection turned on, while parts of the operating system itself run in real addressing mode.

When an interrupt occurs, the current state of the processor (the contents of SCRs 13, 14, and 15) is saved at a specified address in low memory. The saved data is referred to as PS, for processor status. The address at

(continued)

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Table 1: *The RT processor's complete instruction set.*

LOADS, STORES

Mnemonic	Bytes	Cycles	Instruction
L	4	1–6	Load
LS	2	1–6	Load Short
LH	4	1–6	Load Half
LHS	2	1–6	Load Half Short
LHA	4	1–6	Load Half Algebraic
LHAS	2	1–6	Load Half Algebraic Short
LC	4	1–6	Load Character
LCS	2	1–6	Load Character Short
LM	4		Load Multiple
ST	4	2–6	Store
STS	2	2–6	Store Short
STH	4	2–6	Store Half
STHS	2	2–6	Store Half Short
STC	4	2–6	Store Character
STCS	2	2–6	Store Character Short
STM	4		Store Multiple
TSH	4	1–6	Test And Set Half

COMPUTATION, REGISTER TRANSFER

Mnemonic	Bytes	Cycles	Instruction
ABS	2*	2	Absolute
A	2	1	Add
AI	4	1	Add Immediate
AIS	2	1	Add Immediate Short
AE	2	1	Add Extended
AEI	4	1	Add Extended Immediate
CAL	4	1	Compute Address Lower
CAL16	4	1	Compute Address Lower, 16-bit
CAS	2	1	Compute Address Short
CAU	4	1	Compute Address Upper
CA16	2	1	Compute Address, 16-bit
C	2	1	Compare
CI	4	1	Compare Immediate
CIS	2	1	Compare Immediate Short
CL	2	1	Compare Logical
CLI	4	1	Compare Logical Immediate
CLRBL	2	1	Clear Bit Lower
CLRBU	2	1	Clear Bit Upper
CLZ	2	1	Count Leading Zeros
D	2	3	Divide Step
DEC	2	1	Decrement
EXTS	2	1	Extend Sign
INC	2	1	Increment
LIS	2	1	Load Immediate Short
M	2	4	Multiply Step
MC03	2	1	Move Character Zero From Three
MC13	2	1	Move Character One From Three
MC23	2	1	Move Character Two From Three
MC33	2	1	Move Character Three From Three
MC30	2	1	Move Character Three From Zero
MC31	2	1	Move Character Three From One
MC32	2	1	Move Character Three From Two

(continued)

which the PS is stored depends on the type (machine check, program check), or I/O level number, of the interrupt. A new PS is then automatically loaded from a location specific to the type or level of interrupt, and processing continues. This new PS specifies (presumably) privileged state, real addressing mode, interrupts disabled, and the address of the interrupt handling routine.

At the conclusion of an interrupt handler, the interrupted program is resumed via a Load Program Status instruction that reloads the saved PS and thus restores the original state. General registers and SCRs other than 13 through 15 are not saved automatically; such saving and restoring must be done by the interrupt handler.

INSTRUCTION SET

The term RISC applies to the RT processor more in the concept of simple one-cycle instructions than in the actual size of the instruction set. The RT processor has 118 instructions (the Berkeley RISC-I had 31). The concept is that if a machine has a certain data flow and an ALU that can perform certain functions, then all the operations those resources can perform that are useful to the compiler are exposed as instructions. This results in some instructions that might not be the first choice in a machine designed for assembly language programming (example: shift left paired immediate plus 16), but the functions they perform are called for by the compiler often enough to warrant their inclusion.

The RT processor's 118 instructions can be divided into six major categories. There are 17 load/store variations, 73 computation and register transfer instructions, 16 branching instructions, 3 traps, 7 system control instructions, and 2 I/O instructions. The complete instruction set is listed in table 1.

There are load instructions for fullwords (32 bits), halfwords (16 bits, padded on the left with 0s to 32 bits when loaded), algebraic halfwords (16 bits, sign-extended to 32 bits when

(continued)

Mnemonic	Bytes	Cycles	Instruction
MFTB	2	1	Move From Test Bit
MFTBIL	2	1	Move From Test Bit Immediate Lower
MFTBIU	2	1	Move From Test Bit Immediate Upper
MTTB	2	1	Move To Test Bit
MTTBIL	2	1	Move To Test Bit Immediate Lower
MTTBIU	2	1	Move To Test Bit Immediate Upper
N	2	1	AND
NILO	4	1	AND Immediate Lower Extended Ones
NILZ	4	1	AND Immediate Lower Extended Zeros
NIUO	4	1	AND Immediate Upper Extended Ones
NIUZ	4	1	AND Immediate Upper Extended Zeros
O	2	1	OR
OIL	4	1	OR Immediate Lower
OIU	4	1	OR Immediate Upper
ONEC	2	1	One's Complement
S	2	1	Subtract
SIS	2	1	Subtract Immediate Short
SE	2	1	Subtract Extended
SF	2	1	Subtract From
SFI	4	1	Subtract From Immediate
SETBL	2	1	Set Bit Lower
SETBU	2	1	Set Bit Upper
SL	2	1	Shift Left
SLI	2	1	Shift Left Immediate
SLI16	2	1	Shift Left Immediate Plus 16
SLP	2	1	Shift Left Paired
SLPI	2	1	Shift Left Paired Immediate
SLPI16	2	1	Shift Left Paired Immediate Plus 16
SR	2	1	Shift Right
SRI	2	1	Shift Right Immediate
SRI16	2	1	Shift Right Immediate Plus 16
SRP	2	1	Shift Right Paired
SRPI	2	1	Shift Right Paired Immediate
SRPI16	2	1	Shift Right Paired Immediate Plus 16
SAR	2	1	Shift Algebraic Right
SARI	2	1	Shift Algebraic Right Immediate
SARI16	2	1	Shift Algebraic Right Immediate Plus 16
TWOC	2	1	Two's Complement
X	2	1	Exclusive-OR
XIL	4	1	Exclusive-OR Immediate Lower
XIU	4	1	Exclusive-OR Immediate Upper

BRANCHING

Mnemonic	Bytes	Cycles	Instruction
BALA	4	5–7	Branch And Link Absolute
BALAX	4	5–7	Branch And Link Absolute With Execute
BALI	4	5–7	Branch And Link Immediate
BALIX	4	5–7	Branch And Link Immediate With Execute
BALR	2	5–7	Branch And Link Register
BALRX	2	5–7	Branch And Link Register With Execute
BB	4	*	Branch On Condition Bit Immediate
BBX	4	*	Branch On Condition Bit Immediate With Execute
BNB	4	*	Branch On Not Condition Bit Immediate
BNBX	4	*	Branch On Not Condition Bit Immediate With Execute
BBR	2	*	Branch On Condition Bit Register
BBRX	2	*	Branch On Condition Bit Register With Execute

(continued)

loaded), and bytes (8 bits, padded on the left with 0s to 32 bits when loaded). A Load Multiple instruction loads from 1 to 16 registers from consecutive words in memory. For each of these there is a corresponding store instruction.

Simple base-register plus constant-displacement addressing modes are provided. More complex modes (base plus index register, for example) are constructed by the compiler from the primitive instructions. The 73 computational instructions include all of the ordinary integer arithmetic, logical, and shift instructions, plus a group of address computation and register transfer instructions.

In general, the arithmetic instructions set the Condition Status bits according to their result, while the address computation instructions do not. In some cases the only difference between an arithmetic instruction (Add, Add Immediate) and an address computation instruction (Compute Address, Increment) is whether the Condition Status is affected. This gives the compiler more freedom to rearrange and optimize computations.

There are two classes of conditional branches: jumps, which are 2-byte branches, relative to the contents of the IAR; and branches, which are generally 4 bytes and can be either branch absolute, branch relative (to the IAR), or branch register (via an address in a register). The branches have a traditional form and a delayed-branch form, which is referred to as Branch With Execute. Conditional branches, or jumps, test the value of one of the bits in the Condition Status register. Unconditional branches are done by testing a particular bit in the CS register that is permanently zero. Subroutines are called using Branch And Link instructions that place the address of the instruction following the branch in a general register. Subroutine returns are via a Branch Register instruction that branches to the address saved by the call.

The trap instructions provide an efficient way to test array indexes, case-statement values, and the like, against

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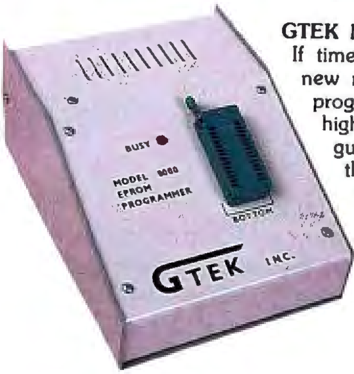

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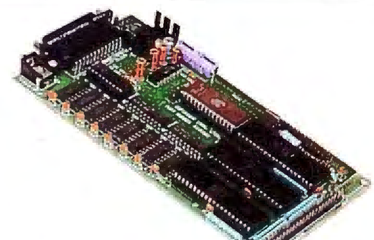

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Mnemonic	Bytes	Cycles	Instruction
BNBR	2	*	Branch On Not Condition Bit Register
BNBRX	2	*	Branch On Not Condition Bit Register With Execute
JB	2	*	Jump On Condition Bit
JNB	2	*	Jump On Not Condition Bit

* Conditional branches and jumps take
1 cycle if unsuccessful (fall through)
5–7 cycles if successful

TRAPS

Mnemonic	Bytes	Cycles	Instruction
TGTE	2	2	Trap If Register Greater Than Or Equal
TLT	2	2	Trap If Register Less Than
TI	4	2	Trap On Condition Immediate

SYSTEM CONTROL

Mnemonic	Bytes	Cycles	Instruction
LPS	4	12–16	Load Program Status
CLRSB	2	4	Clear SCR Bit
MFS	2	2	Move From SCR
MTS	2	3	Move To SCR
SETSB	2	4	Set SCR Bit
SVC	2	16–20	Supervisor Call
WAIT	2		Wait

INPUT/OUTPUT

Mnemonic	Bytes	Cycles	Instruction
IOR	4	1	Input/Output Read
IOW	4	2	Input/Output Write

upper and lower bounds. Such instructions perform a logical (unsigned) comparison of a register against an immediate value, or against another register, and cause an interrupt if the specified trap condition "springs."

For arrays with a lower bound of zero, a single trap instruction will catch positive indexes greater than the upper bound and all negative indexes (negative values appear to be large positive values in unsigned comparisons). For nonzero lower bounds an additional add or subtract instruction must precede the trap. The compiler subjects such trap code to the same optimizations as all the rest of a program's computations. As a result, bounds checking for a language like Pascal can be done very efficiently.

The system control instructions perform low-level hardware operations, such as resetting interrupt requests, manipulating the contents of the privileged SCRs, and loading new program status. One system control instruction, Supervisor Call (SVC), is provided for use by unprivileged state code, to switch to privileged state in a controlled manner. SVC causes an interrupt and passes a 16-bit code to the Supervisor Call Interrupt Handler; the operating system then interprets the code as a request for some specified service, performs the requested action, and resumes the program via Load PS.

There are two I/O instructions that transfer 32-bit values between general registers and the I/O bus, but most I/O is memory-mapped and is done using the normal Load and Store instructions. Control of the address translation hardware in the MMU is done by privileged state programs using the I/O instructions directly.

Basic Data Types

The fundamental unit of memory is the 32-bit word, and all memory operations involve 32-bit words. The words are further subdivided into halfwords and bytes. Memory is addressed by byte address, and words and halfwords are required to be on appropriate boundaries. That is, a word address must be a multiple of four, and a halfword address must be a multiple of two. Such alignment requirements make for faster execution and simplify the handling of page faults.

Loading a 4-byte word that crosses a word boundary would require two memory operations rather than one, while the corresponding Store would require two read-modify-write cycles rather than one simple write. If such a misaligned word also crosses a page boundary, then it's possible that a page fault or protection exception could occur partway through a memory operation. Such complexities are handled for Load Multiple and Store Multiple, but they are not warranted for the very heavily used Load and Store instructions.

Signed two's-complement integers can occupy words or halfwords. These halfwords will be sign-extended to fullword quantities when loaded into a general register. Individual bytes can also be loaded and stored but when loaded are extended on the left with 24 zero bits. Thus bytes can naturally hold small unsigned integers as well as characters.

Individual bits cannot be addressed in memory directly but can be manipulated in the general registers once a byte, halfword, or fullword has been loaded. In addition to the normal complement of logical and shift in-

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structions, there are two instructions (Move To Test Bit, Move From Test Bit) that allow individual bits to be moved between registers or into the Condition Status register and thus affect a conditional branch directly.

Quantities larger than fullwords, such as character strings, are not operated on directly by the RT processor hardware but are treated as sequences of words or bytes. Character strings do not normally have any boundary alignment requirements.

Floating-point quantities handled by the IBM RT Personal Computer's floating-point unit have alignment restrictions as required by the floating-point hardware. Floating-point values are not processed directly by the RT processor.

MEMORY MODEL

The RT processor's memory model is extremely simple, and intentionally so. Memory is addressed at the byte level, with bytes numbered from left to right. Any quantity (byte, halfword, fullword) loaded from memory into a register appears in the register exactly as it did in memory; bytes are never reversed. The memory address of any instruction, primitive data item, or data structure is always the address of its leftmost (high-order) byte, without exception.

In real memory mode, addresses are treated as byte numbers in the range of 0 to $2^{24}-1$. The maximum real memory size is 16 megabytes. The RT processor begins execution in real memory mode after power-on reset, and this mode is used by some of the low-level operating system code, such as interrupt handlers.

Almost all programs are executed in virtual memory mode, including all application code and most of the operating system. In this mode addresses are again simply byte numbers, but with an extended range: 0 to $2^{32}-1$, thus spanning 4 gigabytes.

A program sees virtual memory as a large, linear byte-space with no arbitrary boundaries or overlapping segments. This is an important simplification and contributes to the ease of generating code for the RT processor. The compiler doesn't have to worry about whether a data structure, a stack frame, or even a program will fit within some restricted addressing range covered by a segment register.

Of course, there are not really 4 gigabytes of main memory behind the 32-bit addresses generated by a program. Address translation hardware in the MMU maps virtual addresses to real addresses, signaling a page fault on references for which a mapping does not currently exist. The fault is resolved by reading in the relevant

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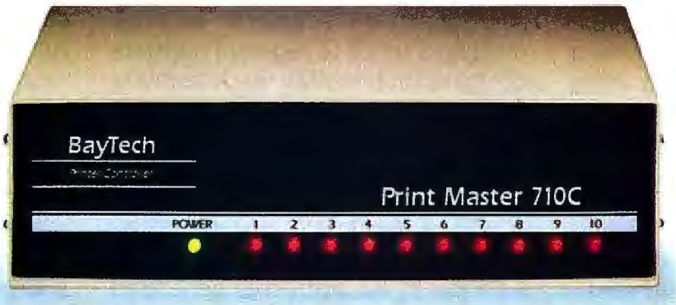

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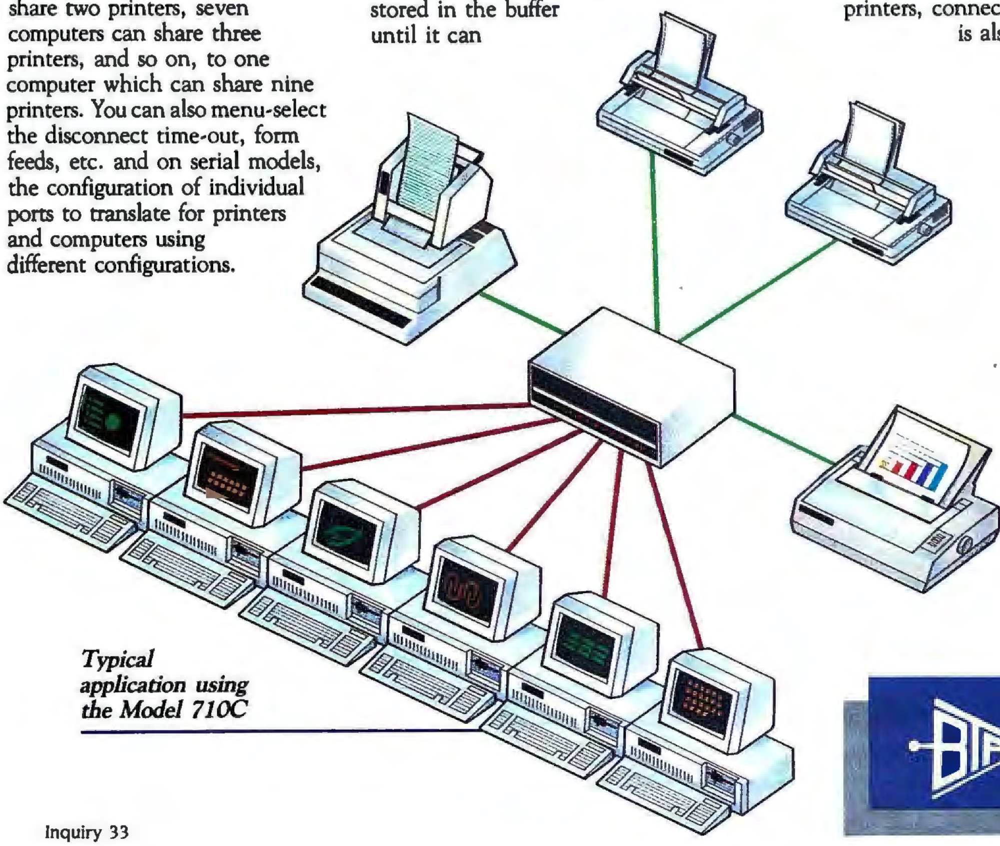

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page from disk or creating an empty page on first reference (perhaps first writing out some other page to make room in memory), updating the virtual address mapping information, and restarting the faulting program. Mapping is done on a per-page basis, with page sizes of either 2K bytes or 4K bytes. Page size is fixed at system initialization (the operating system for the IBM RT PC uses 2K-byte pages).

Virtual memory is organized into large segments, and each segment is composed of a collection of pages (see figure 2). Segment sizes can range up to 2^{28} bytes, or 256 megabytes. The pages of a segment are related in some way. A segment may make up a file in the file system, it may be all the computational (local) memory of a running program, or it may be all the executable code loaded for a particular task.

Each segment in active use is assigned a 12-bit number called a segment ID, or SID. A program can access up to 16 segments at once through a set of 16 segment registers contained in the MMU. Each segment register contains an SID, and the contents of the segment registers (i.e., the collection of names of segments to which a task has been given access) is part of the "state," maintained by the operating system, for each task.

Of the 32-bit addresses generated by a program, bits 0 through 3 (the high-order 4 bits) select one of the segment registers (0 through 15), and bits 4 through 31 specify an offset within the segment. Address translation is performed on the combination of the 12-bit SID from the selected segment register and the 28-bit offset. A 40-bit virtual address is formed by concatenating the SID and the offset. The virtual addressing range is therefore 2^{40} bytes, or 1 terabyte (one terabyte = 1024 gigabytes; tera- is the standard prefix denoting a factor of 10^{12}, from the Greek *teras*, which means "monster").

The loading of the segment registers is restricted to privileged state programs, but via an SVC an application can cause any segment, to which it has been granted access, to be mapped using any segment register. A task may access many more than 16 segments by reloading the segment registers. Segments can be shared among tasks merely by loading the same SID value into a segment register for each task. Since the translation is done on the 40-bit address rather than the 32-bit address, it does not matter that a shared segment is mapped using, say, segment

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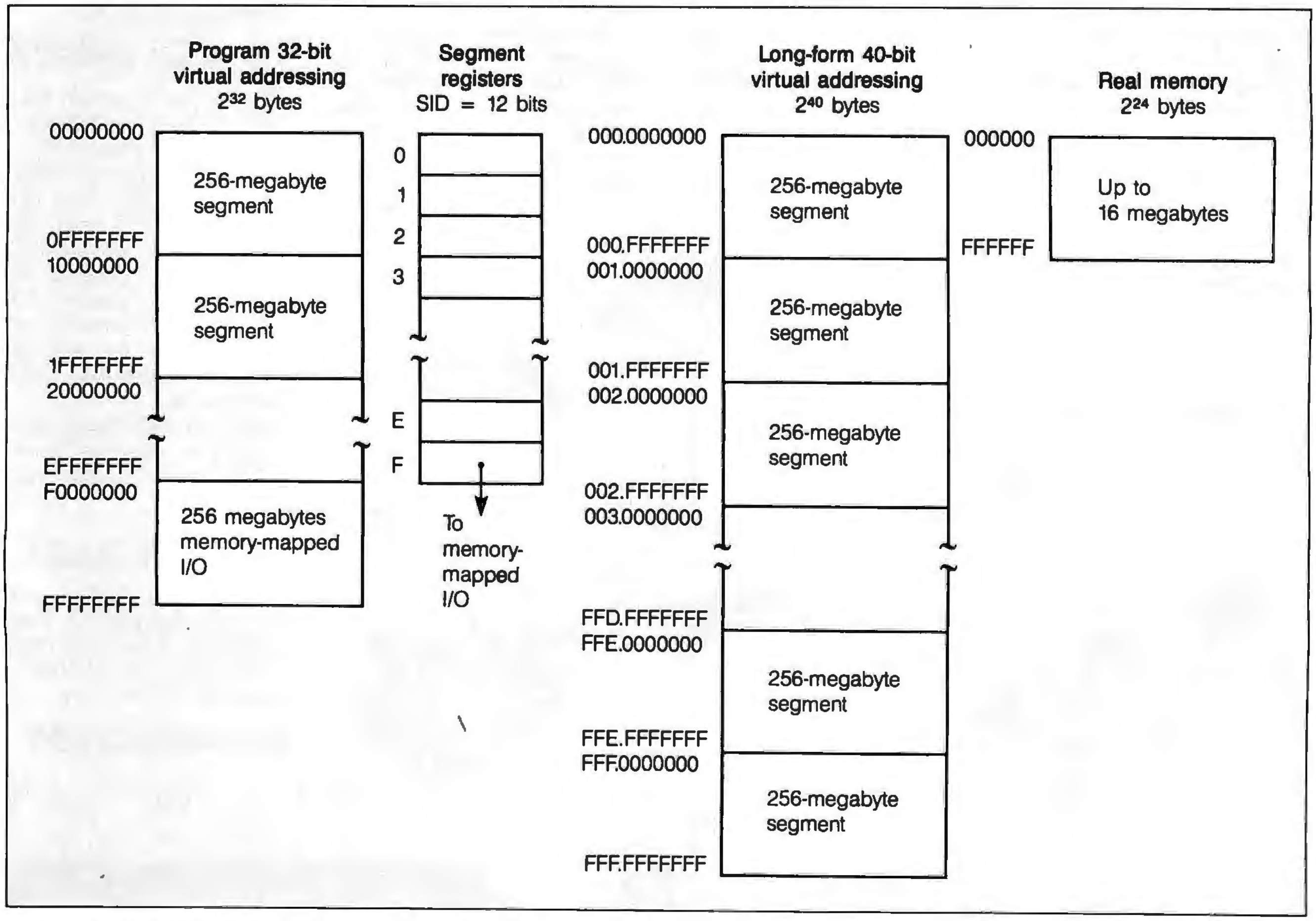

Figure 2: A *model of* RT *processor memory addressing.*

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Table 2: *Protection conditions associated with a virtual page.*

Page Key	Type of Page	SR Key	Load	Store
00	Key 0 fetch-protected	0	Yes	Yes
		1	No	No
01	Key 0 read/write	0	Yes	Yes
		1	Yes	No
10	Public read/write	0	Yes	Yes
		1	Yes	Yes
11	Public read-only	0	Yes	No
		1	Yes	No

register 12 in one task and segment register 7 in another, as long as both tasks use the same SID.

For each segment, one of two types of memory protection can be specified. A bit in each segment register tells whether the associated segment is normal or special. For normal segments, protection is at the page level. Access rights to each page can be specified as read/write, read-only, or no-access, depending on a segment-key bit in the segment register and two page-key bits in the page table entry. Operating system programs normally run with the segment-key bit = 0, while applications run with the segment-key bit = 1. (Table 2 shows the various protection conditions associated with a virtual page.)

A finer-grained type of protection is available for special segments. Pages of special segments are divided into 16 "lines" of 128 bytes each (for 2K-byte pages) or 256 bytes each (for 4K-byte pages). Read-only or read/write access can be granted on an individual "line" basis, per task.

This type of protection is intended for use by sets of tasks that share a data segment and that need hardware assistance in controlling access to shared data items smaller than a page. Special segments require more effort on the part of the operating system because more manipulation of the page table is involved.

The Memory Management Unit

The MMU performs the address translation and memory protection operations described above. It is the "physical memory" controller for the RT processor as well. All requests for memory read or write go through the MMU, including requests from the RT processor proper and from direct memory access I/O devices. Each request is distinguished (by a control line during the bus transfer) as real, which requires no translation, or virtual, which requires translation and memory protection checking.

Segment Registers

The 16 segment registers described in the memory model reside in the MMU. Address and data transfers to and from the MMU are 32 bits wide. The 32-bit virtual addresses are expanded to 40 bits in the MMU by stripping off bits 0 through 3 and using them to select one of the segment registers. The resulting 40-bit address is then translated to real, and the real address is used to drive the memory arrays. The contents of the segment registers can be read and written by the operating system using the RT processor's I/O instructions.

Inverted Page Table

Conceptually, address translation is performed by looking up the virtual page number (the high-order bits of the 40-bit virtual address) in a table, finding the associated real page number; and substituting the real value for the virtual one. Since the pages are fixed in size (all 2K bytes or all 4K bytes) and must reside in memory on a boundary that is a

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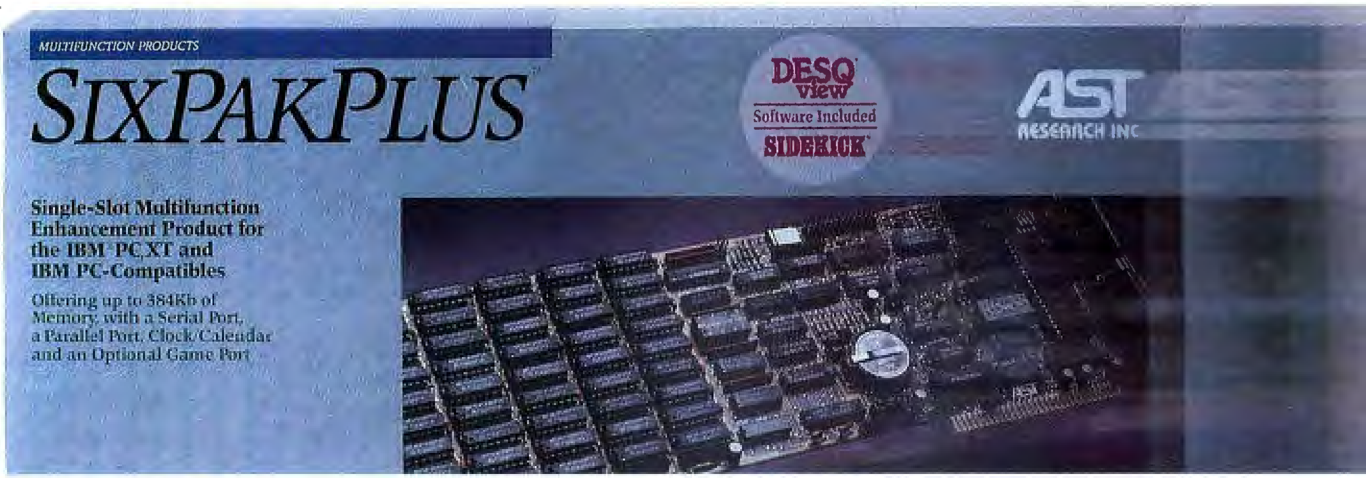

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multiple of that size, the low-order bits of the virtual address reflect an offset within the page and are not used in the translation. The virtual page number is the high-order 28 or 29 bits of the 40-bit address, depending on page size.

In traditional translation schemes such as that of the IBM System/370, the page table is organized by virtual address. That is, the virtual page number is used directly as an index into a one- or two-level table to obtain the real page number. As virtual storage becomes very large and as the number of independent tasks supported increases, such tables can become unwieldy because the overall table size is proportional to the amount of virtual storage supported by the operating system.

The RT processor uses an inverted page table instead, an approach first used on the IBM System/38. The table is organized by real address with the contents of each entry being the corresponding virtual address. The table's maximum size is therefore one entry per real page rather than one entry per virtual page. Only a fixed percentage of the machine's real memory is required for the inverted page table regardless of the amount of virtual storage in use.

If the page table entries are in order by real address, how can a virtual-to-real translation be done quickly? It would seem that a sequential scan of the page table would be required, comparing the virtual address with each table entry until a match is found. On the average, half the table entries would have to be checked.

The RT processor avoids this sequential search by using a hashing technique to quickly find an entry for a given virtual address (see figure 3). The 28- or 29-bit virtual page number is "hashed" into a number in the range of 0 to $n-1$, where n is the number of pages of real memory. Thus the range of 2^{28} or 2^{29} virtual page numbers is quickly reduced to one-of-n congruence classes. For each congruence class there is a chain of entries threaded through the inverted page table. Each entry on a given chain is for a real page whose virtual page number hashes to the same congruence class (i.e., a "hash collision").

Translating from virtual to real, then, requires only a simple hash operation (just an exclusive-OR) followed by a sequential search of the entries on the hash chain. This technique works well if the hash chains are very short compared to half the total number of entries in the table. In fact, the average chain length is between one and two entries, so that only a few memory accesses are required to find the real entry for a virtual page. The worst case, of course, would occur if all the virtual pages in the system wound up on the same hash chain, but the chances of that happening are exceedingly remote.

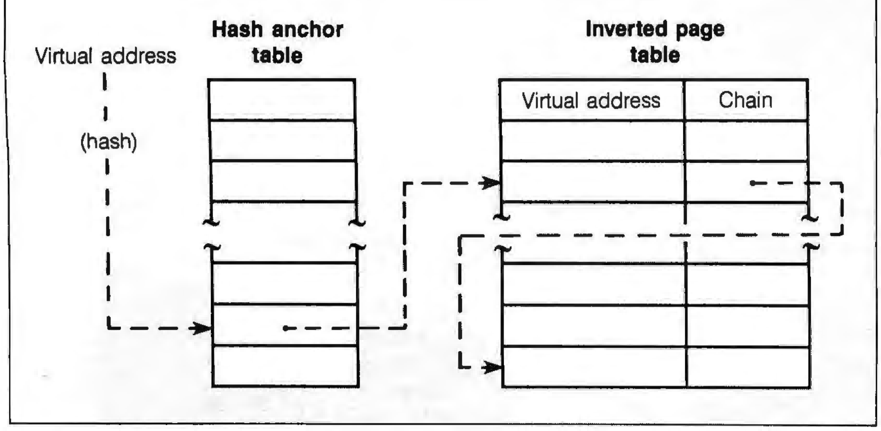

Figure 3: RT *processor hash anchor table and inverted page table.*

TRANSLATION LOOK-ASIDE BUFFER

Regardless of page table organization, no system in which performance is a goal can afford to go to the page table in main memory for each and every translation. In the MMU, a cache of recently used translations is kept in a translation look-aside buffer, or TLB. This is a two-way, set-associative table with 32 total entries. Each entry contains a virtual page number, its corresponding real page number, and memory protection information for the page.

One of 16 congruence classes is selected by using the low-order 4 bits of the virtual page number. For that class, two comparisons are made, in parallel, against the remainder of the virtual page number. If a match is found, the translation can be completed immediately. If no match is found in the TLB, the page table must be searched and the TLB updated.

Hit ratios of address translation caches are typically very high, much higher than those of data caches, for example. The hit ratio for the TLB is about 99.5 percent. As a result, address translation is normally completed within a single cycle. When the TLB does miss, translation is usually extended by only 8 to 11 cycles while the TLB is reloaded.

HARDWARE IMPLEMENTATION

The RT processor and its MMU are each implemented as single VLSI chips. With a cycle time of 170 nanoseconds, the sustained execution rate of the RT processor on a typical mix of instructions in the IBM RT PC is ap-

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PIPELINES

There are two levels of pipelining in the implementation of the RT processor (see figure 4). First, the execution of instructions is done by a four-stage pipeline that overlaps instruction fetch, instruction decode and operand fetch, execution, and result storeback. At a higher level, memory operations (Load, Store, Instruction-Fetch) are pipelined so that several memory operations can be in progress at once and so that the processor need not wait for the completion of a memory operation before executing subsequent instructions. In the current version of the RT processor, instruction fetching is pipelined, but loads and stores are not (in virtual memory mode) so that precise page-fault interrupts can be presented.

In the low-level pipeline, the first stage is unique in that it proceeds asynchronously with the rest of the stages. That is, the instruction fetch mechanism is usually fetching a word that is several instructions beyond the one currently entering decode.

The instruction fetch unit in the RT processor tries to keep its 4-word buffer full by fetching the word at the next sequential address, incrementing its pointer by 4, and repeating this until all 4 words are full. If a branch occurs, the execution unit resets the instruction fetch unit's pointer to the branch target address and marks the four buffer entries "empty." The instruction fetch unit then starts fetching the new instruction stream.

The other three stages of the pipeline run in lockstep. In the first stage, a prefetched instruction is decoded and the contents of registers that it uses as source operands are fetched from the register file. Two registers can be read from the file and two written simultaneously. The first (usually the only) microcode word for the instruc-

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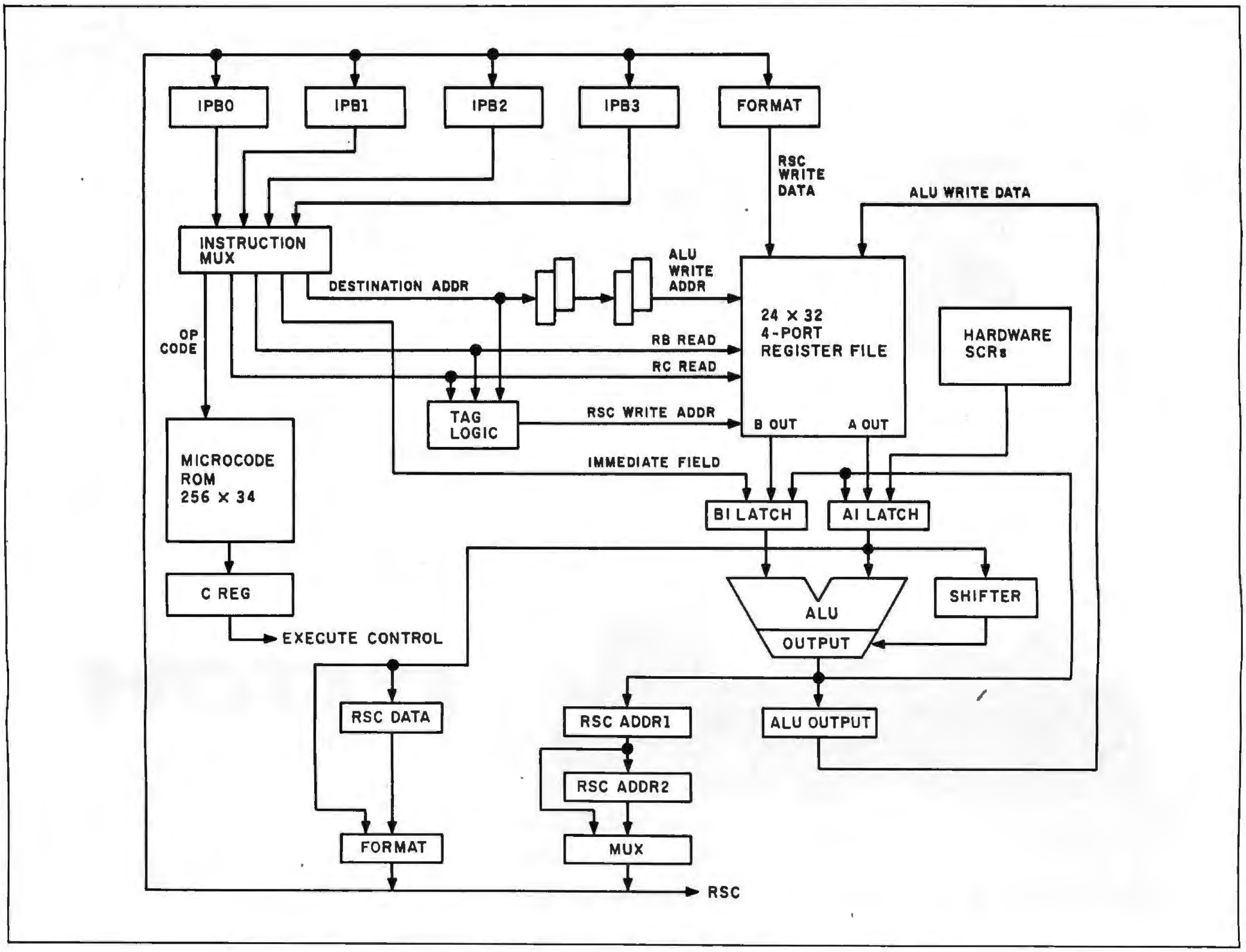

Figure 4: A *data flow block diagram of the* RT *processor.*

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tion is fetched simultaneously with the operand registers. The microcoded design of the RT processor does not slow down execution because the microword fetch is overlapped with the fetching of the operands.

In the next stage the decoded instruction is executed using the previously fetched register contents. In the last stage the results of the execution are stored back into the register file or are sent out to memory if this is a Store instruction. In addition, the register file is bypassed when an instruction uses the results of the preceding instruction. The output of the ALU is fed back around to be the input on the next cycle. In the normal course of events the instruction fetch unit will have fetched instructions far enough ahead so that the decoder does not have to wait. There will then be three instructions in process: one in decode, one in execution, and another in storeback so that the throughput is one instruction per cycle (see figure 5).

Multicycle instructions such as Divide Step spend several cycles in execution, thus delaying the instructions that follow them. In addition, it may not be possible to start execution of an instruction if one of the registers it uses is the target of a previous Load instruction that is not yet complete.

PACKET-SWITCHED MEMORY BUS

A Load instruction may not have been completed due to the pipelining of the memory interface. Since the RT

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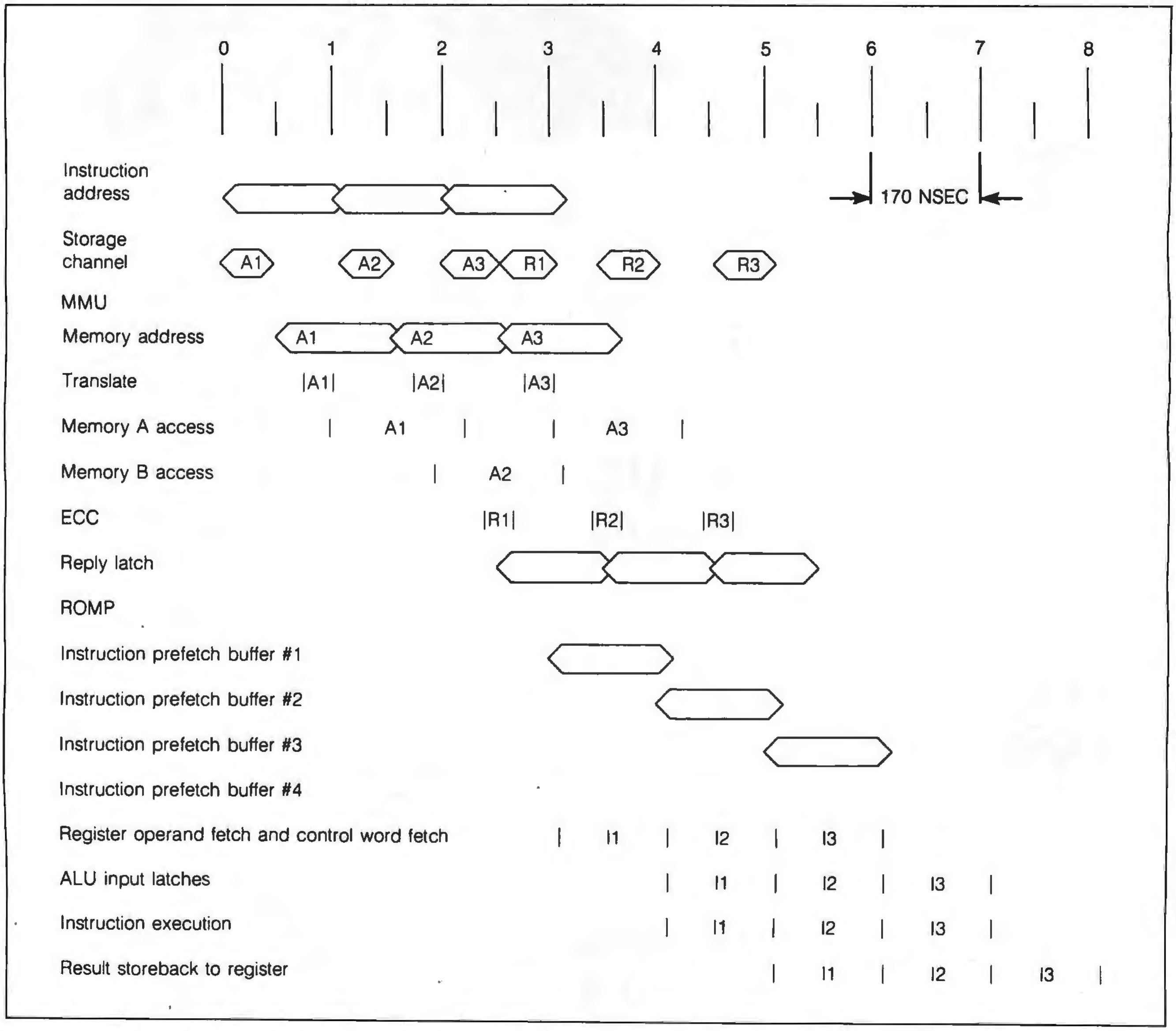
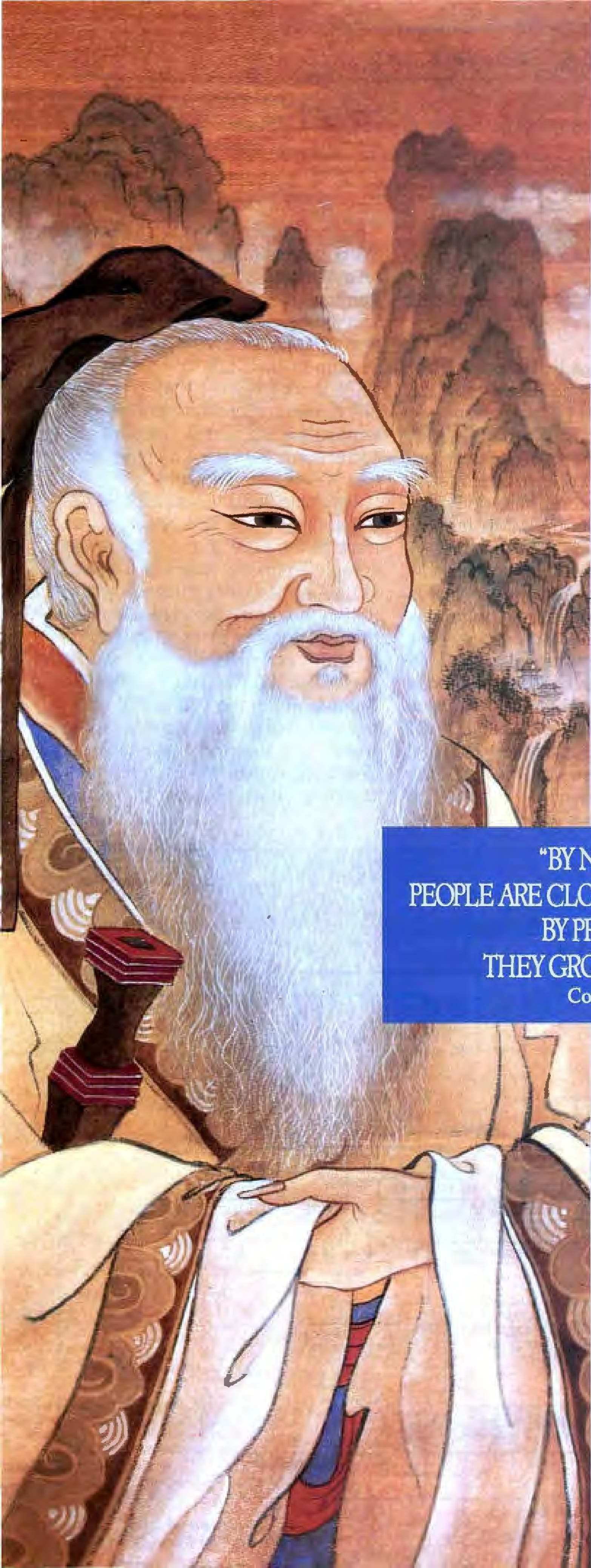


Figure 5: *Three 32-bit instructions. Note the timing overlap in memory access, instruction prefetch, operand fetch, and storeback to registers.*



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processor's main memory does not run as fast as a cache, it would be time-consuming to wait for each Load or Store operation to end before beginning the next operation. To allow multiple memory operations to be in progress at once and to gain maximum use of interleaved (multibanked) memory, a packet-switched bus was defined between the RT processor, the MMU, and the I/O controller.

This bus is known as the ROMP storage channel, or RSC (unfortunately, a nested acronym). The RSC runs synchronously with the RT processor cycle, with two RSC cycles per processor cycle. The standard RT processor cycle time in the IBM RT PC is 170 nanoseconds (the RSC runs at 85 ns/cycle). Even-numbered RSC cycles are used to transmit addresses from the RT processor or from DMA I/O to the MMU, while odd-numbered cycles are used to transmit data.

Each transfer is 32 bits wide. In each processor cycle, therefore, both a memory request (address) and a unit of data (a word loaded or stored) can be transferred, for a net throughput of

$$\frac{4 \text{ bytes}}{1.7 \times 10^{-7} \text{ sec.}} = 23.5 \text{ megabytes/sec.}$$

The address and data portions of the cycle are not necessarily related. In the first half of a processor cycle (i.e., in the even-numbered RSC cycle), the processor may send out an address for a load or instruction fetch, while in the second half (odd-numbered RSC cycle) the MMU may respond with the data for an earlier request. Requests are not necessarily responded to in order, depending on whether the required memory bank is busy when the MMU processes the request. To keep the outstanding requests straight, each request (address) has an associated tag, a 5-bit value that tells who owns the request (RT processor or I/O controller) and what should be done with the response when received (sent to the instruction fetch unit or to a general register).

Further pipelining occurs within the MMU (see figure 6). We have seen that several memory requests can be outstanding at once. The MMU overlaps operations for the various requests—performing address translation (lookup in the TLB) for one request while driving the memory arrays for one or two earlier requests while performing an ECC (error checking and correction) check for a memory read that has been completed.

Assuming that a virtual address has a mapping in the TLB, which is true most of the time, translation can be completed in one cycle. For a typical virtual mode Load instruction in the RT PC, the total time from execution of the instruction in the RT processor to return of the data by the MMU is five cycles. If the required translation is not found in the TLB (a TLB miss), the MMU takes additional cycles to search the inverted page table as described earlier. The hash chain for the congruence class for the virtual

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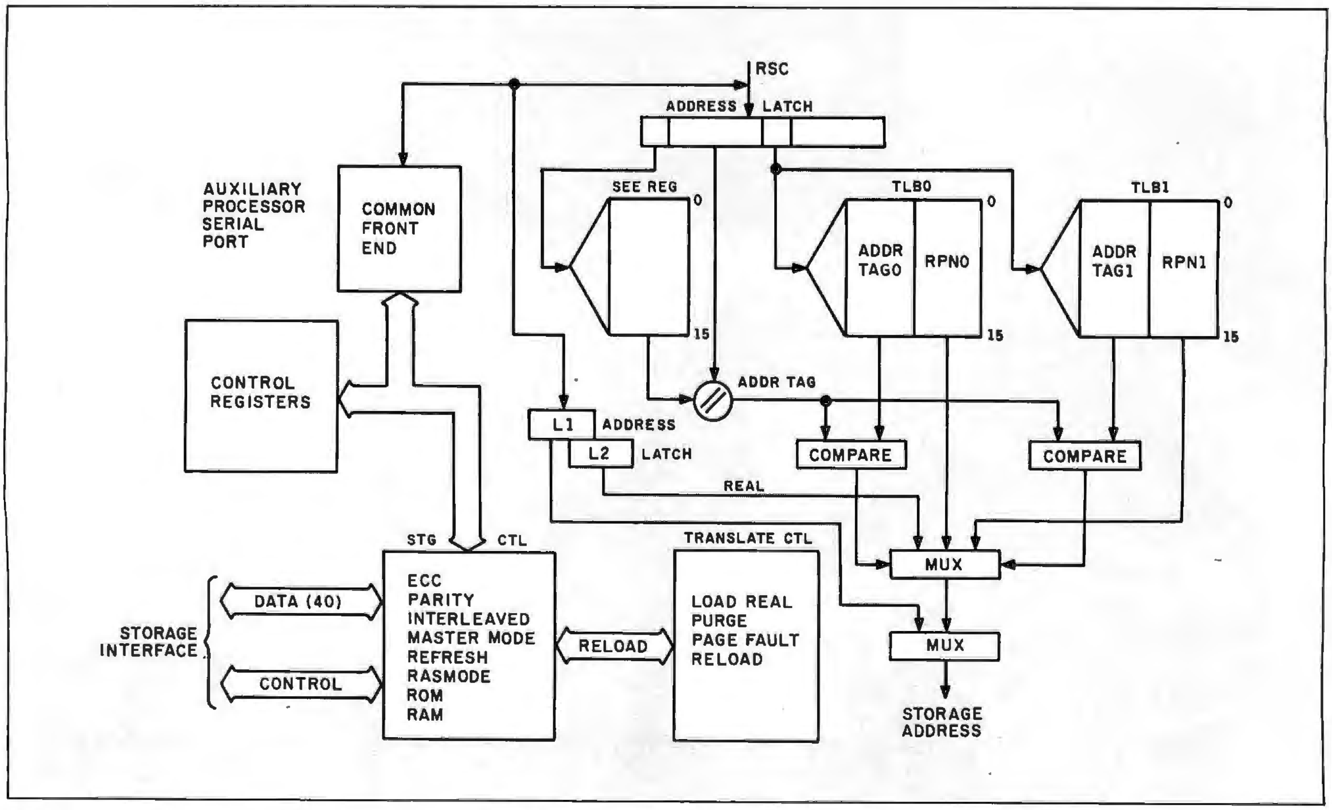

Figure 6: RT *processor memory management unit data flow.*


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page number is searched, and if a matching page table entry is found, it is automatically loaded into the TLB in place of the least recently used TLB entry for its TLB congruence class, and the translation is completed.

Given that the hash chains are short, this typically adds 8 to 11 cycles to the translation operation. With a hit ratio in the 99.5 percent range, this automatic page table search only degrades the overall RT processor performance by a few percent. By contrast, if the TLB miss resulted in an interrupt to the processor and a table search by software, the overall performance could be degraded by 30 percent or more.

When both the TLB and page table searches fail, the result is a page fault. In this case the MMU does not complete the memory request and causes a page-fault processor interrupt. The operating system then resolves the fault by reading in or creating a page and restarting the faulting program (or by terminating the task, if this access is really an error).

Instruction fetch requests, which are interleaved with Load/Store requests from the instruction stream, can also cause page faults. The MMU translates these requests in the same way and reports page faults to the processor, but the processor does not generate an interrupt unless the faulting word is actually needed by the instruction stream. The RT processor therefore does not process spurious page faults caused by the eager instruction fetch unit fetching ahead beyond the end of a page, when the instruction stream will actually branch before crossing the page boundary.

If the translation is successful but the memory protection bits for the page don't match the type of request, then an interrupt similar to a page fault is generated. The operating system can change the protection status of the page and restart the program, or it can terminate the task in the case of an addressing error.

To assist the operating system in selecting pages for replacement, the MMU maintains a table of reference and change bits for each real page. This table is stored in a small static RAM connected to the MMU and is updated in parallel with the actual memory operations. The operating system can read these "flags" for each page to determine which pages are "dirty" and must be written to disk before being reused and which pages have not been referenced at all and are therefore good candidates for reuse.

As the physical memory controller in an RT processor–based system, the MMU is also in charge of such mundane matters as hidden refresh for dynamic RAMs and performing ECC or parity checks on data read from memory. Either ECC (40 bits wide, on a 32-bit word) or parity (1 parity bit per byte) can be used with the RT processor. (The IBM RT PC uses the ECC mode.)

Timing values that control access to the dynamic RAM arrays are set by components external to the MMU, so that a wide variety of RAMs can be used with an RT processor–based system. The IBM RT PC uses 150-ns access time memory chips interleaved in two banks. The MMU also supports the use of read-only memory in addition to RAM. On the IBM RT PC the initial RT processor checkout program begins executing from ROM. This program initializes the RAM, reads in a larger initialization program from disk, branches to the program in RAM, and then switches the ROM out of the addressing space, causing all further execution to be from RAM.

THE FUTURE

Improvements to the RT processor system and RT processor's MMU could come from two sources: technological advances over time and architectural enhancements. RISC architectures like that of the RT processor scale well as technology improves. With smaller dimensions of VLSI geometry come both increased density and faster clock times. Since most RT processor instructions require only one cycle, a reduction in the cycle time translates directly into increased execution speed.

(continued)

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The greater density available in future technologies will permit the addition of architectural features that had to be omitted from the current RT processor and MMU. Probably the most obvious enhancement would be the restoration of one or both of the caches from the original 801 design. Additional silicon space would also permit the inclusion of functions that do not fit the RISC paradigm of one cycle per instruction but that have proven (by measurement of significant running code) to be very useful for enhanced performance.

The MMU's virtual memory mapping functions permit the operating system to create a one-level store in which objects traditionally considered to be disk files become simply arrays of data structures in virtual memory. I/O operations on such a file, instead of being explicit reads and writes, are implicit and are handled by the Paging Supervisor. This can be much more efficient as well as being far easier to program than the traditional access methods. Increases in memory size and cache size will mean that programs traditionally thought of as I/O-bound may become processor-bound. These programs will benefit even more from a faster processor.

For both areas, pure technological speedup and additional functions, the architecture of the RT processor provides an extensible base for the future.

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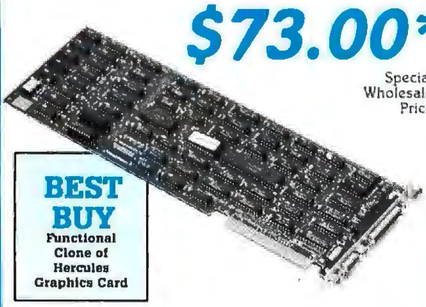

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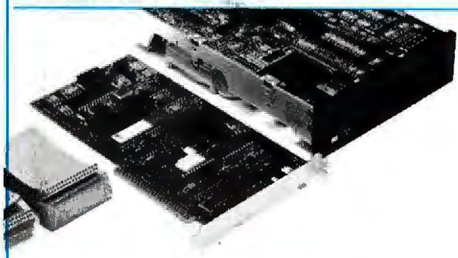

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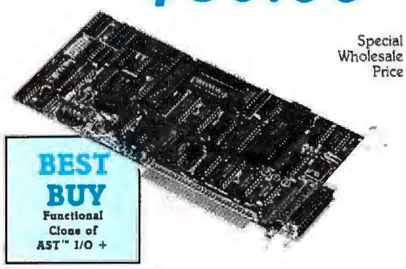

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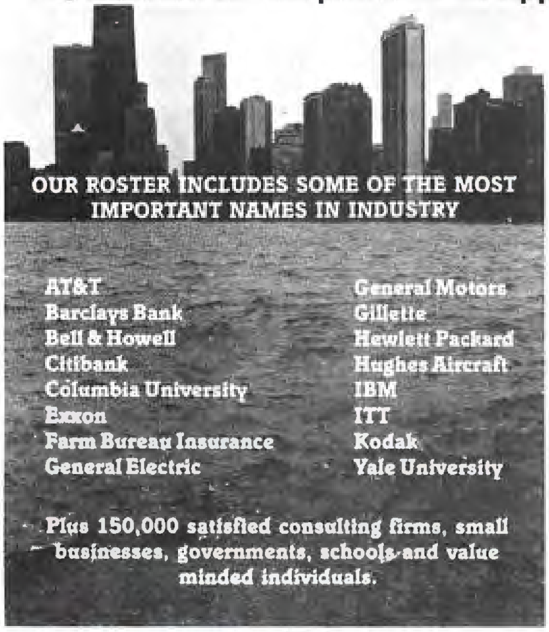

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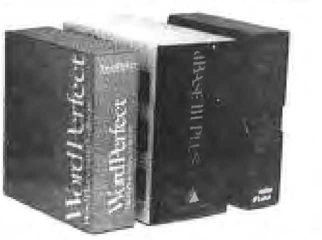

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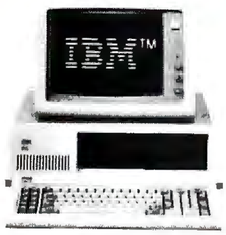

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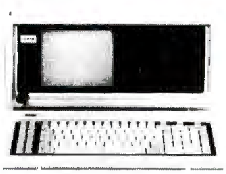

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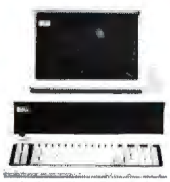

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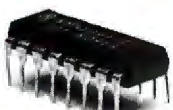

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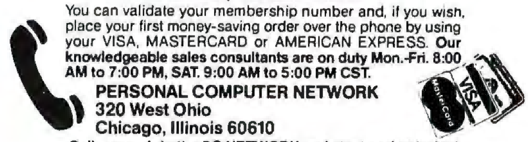

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LEADING EDGE

THE IBM PC CONVERTIBLE

A portable that offers many different options and up to 512K bytes of memory

BY G. MICHAEL VOSE

Editor's note: The following is a BYTE product description. It is not a review. We provide an advance look at this product because we feel that it is significant. We plan to provide a complete review in a subsequent issue.

IBM'S PC Convertible looks like a portable computer complete with a movable handle but feels more like a transportable computer, such as the Compaq. Packed in its optional carrying case, the PC Convertible and battery pack weigh over 15 pounds, a little over one-half the weight of a Compaq. The machine offers up to 512K bytes of memory, 1.4 megabytes of on-line disk storage, and a readable 80-column by 25-line liquid-crystal display, as well as IBM PC compatibility.

The Convertible's many options include a parallel/serial adapter, a portable printer, a monochrome and color display adapter, a 9-inch monochrome or 13-inch color monitor on its own pedestal, 128K-byte memory upgrades, and an internal 110/300/1200-baud modem. These options can increase the Convertible's base price from $1995 to as much as $3000.

IBM supplies some bundled software with the Convertible, including several notebook-like applications for note-taking, phone-number files, and the like. However, the Convertible uses 3½-inch disks, so obtaining other software for the machine presents a problem.

MACHINE INTERNALS

A CMOS version of Intel's 8088 microprocessor powers the PC Convertible. Driven by a 33 percent duty-cycle crystal similar to the IBM PC's, this 14.31818-MHz oscillator's frequency is divided by three to drive the 80C88 at 4.77 MHz. The 80C88's internal circuitry is static, eliminating the need for refresh clock cycles for its on-chip registers, counters, and latches. The 80C88's clock-cycle time is 210 nanoseconds and the Convertible's main-memory cycle is 840 ns, while the I/O cycle is 1.05 microseconds.

The Convertible uses a system timer compatible with the Intel 8253 Programmable Interval Timer, and it provides two programmable channels. The base timing resolution for a timer channel is 840 ns. The interrupt controller on the Convertible duplicates the functions of the Intel 8259 Programmable Interrupt Controller. This interrupt controller provides nine interrupt levels, one of which is nonmaskable. The system clock, interrupt controller, and other devices (keyboard controller, audio controller, and I/O controller) reside on the motherboard in a VLSI gate-array chip. Another gate array houses the disk and printer interface circuitry, time-of-day clock, and system timer. All the Convertible's circuitry, including a total of five gate arrays, resides in just 19 surface-mounted chips on the machine's motherboard (see photo 1).

The Convertible's standard 256K bytes of nonparity-checked RAM resides on two small removable circuit boards located just under the machine's keyboard. To add an additional 256K bytes of RAM to the machine, you plug two similar 128K-byte boards alongside the existing ones for a total of four boards. The Convertible's static RAM features 256K by 1-bit chips. [*Editor's note: Peripheral manufacturer* STB *Systems has already announced a* 384K-*byte*

(continued)

G. Michael Vose is a senior technical editor for BYTE *(One Phoenix Mill Lane, Peterborough,* NH 03458).

PHOTOGRAPHED BY PAUL AVIS

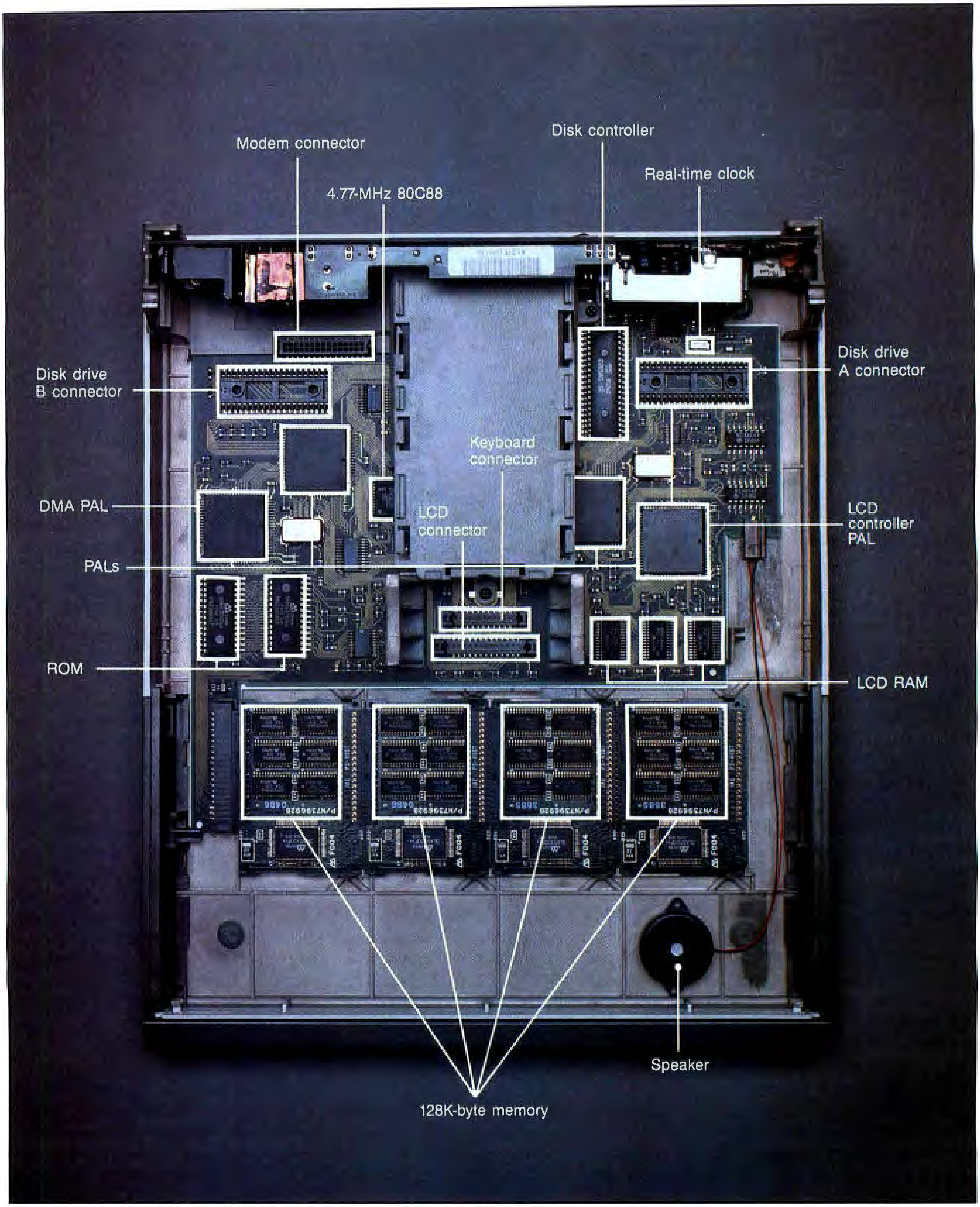


Photo 1: *The sparsely populated PC Convertible main circuit board and 128K-byte memory boards.*

expansion board that lets the Convertible use a full 640K *bytes of* RAM; *see the* What's *New item on page* 14.]

Two 32K-byte ROMs contain the PC Convertible's on-board system software. The machine's resident BASIC uses 32K bytes and the POST (power-on self-test) and BIOS routines occupy the other 32K bytes in separate 24K and 8K segments.

The two 3½-inch disk drives in the PC Convertible offer formatted storage of 720K bytes per disk. The disks used by these drives store data at 135 tracks per inch (80 tracks per side) and can be accessed by the drives at 6 milliseconds track to track. The maximum data-transfer rate is 250K bytes per second. The NEC μPD765 floppy-disk controller manages the I/O control of the disk drives.

The Convertible's DMA (direct memory access) controller is compatible with the Intel 8237 programmable DMA controller and regulates the movement of data from memory to I/O devices without involving the microprocessor. Since the Convertible's static RAM requires no refreshing, the DMA controller does not support refresh; therefore, it supports three DMA channels instead of four (as in the IBM PC) and uses five clock cycles (1.05 μs per byte) for every DMA data transfer. The 16-bit control registers in the DMA controller require the use of a page register to develop the 20-bit addresses possible within the Convertible's 1-megabyte addressable memory. The DMA controller does not support memory-to-memory data transfer, cascading, or automatic initialization.

To beep error messages or to play music, the Convertible uses a small speaker on the motherboard controlled by an audio controller that receives its signals from the system timer and the I/O controller.

The LCD measures 3¾ inches high by 10¾ inches wide (see photo 2). It displays 25 lines of 80 characters at a resolution of 640 by 200 pixels. The LCD disconnects from the Convertible's system unit via a 20-pin male/female edge connector for the convenience of users who elect to use an optional monochrome or color display. The LCD is not backlit but is adjustable for accommodating ambient room light. The aspect ratio of the LCD differs from standard CRT devices by about 20 percent.

The LCD controller uses an interface similar to that of the Motorola 6845 CRT controller, and thus allows the operation of programs written to use the IBM monochrome display adapter or the IBM color/graphics display adapter. The LCD controller has its own 16K bytes of video RAM and uses either the main font (the IBM PC character set) or an alternate font to display up to 256 characters per font.

The keyboard on the Convertible is similar at first glance to the PCjr keyboard—function keys in a row across the top, a small function key on the bottom left, and a cluster of cursor keys on the bottom right. However, the similarity to the PCjr ends here. The Convertible has 78 keys on a keyboard with a surprisingly solid feel for such a small device (see photo 3). The Convertible keyboard generates all the scan codes recognized by the IBM PC BIOS and includes an Alternate key and a Control key.

Supplying Power

There are four ways that a PC Convertible can get electricity: an AC adapter, a battery pack, a battery charger, or an automobile adapter that plugs into an automobile cigarette lighter. You can use the battery charger only to charge the batteries, not to run the computer. The AC adapter and the automobile adapter will run the Convertible and charge the battery pack at the same time. The AC adapter uses 90- to 265-volt, 50/60-Hz electrical-source power.

The battery pack supplied with the PC Convertible has eight nickel-cadmium cells and, when fully charged, can power the machine for 6 to 10 hours depending on the installed memory and the use of disk drives and attached peripherals. If the battery-pack power gets low, an icon that looks like a flashlight battery blinks in the upper right corner of the screen to warn you to correct the problem. Recharging the Convertible's battery is a 12- to 14-hour process after you see a low-power warning.

To preserve power, the Convertible will power down if there is no disk or keyboard activity for two minutes. During its power-down operation, it saves a variety of information about the state of the machine at the time of shutdown.

Optional Hardware

Since the PC Convertible has no external connectors for serial or parallel printers, the serial/parallel adapter is an important option. IBM gets away with making these ordinarily indispensable outputs optional by offering

(continued)

Photo 2: *The* PC *Convertible's* LCD *screen.*

a low-power, thermal-transfer, serial dot-matrix printer that attaches to the Convertible's system bus. However, many users will elect to use their own printers rather than buy another one, and those users must buy the adapter. The serial/parallel adapter attaches to the back of the Convertible, connecting to the 72-pin system bus. The system bus is brought out on the other side of the adapter so that you can still attach other peripherals to the computer.

The serial/parallel adapter differs slightly from the IBM PC's in the way that it implements the functions of the PC's asynchronous communications adapter. The Convertible's BIOS contains routines that allow control of local power on the serial adapter. Additionally, the maximum data-transfer rate of the serial/parallel adapter's serial port is 9600 baud.

Another important Convertible option is the internal modem. This modem was not available for my use, so I have to take IBM's word that it actually exists. According to IBM, this modem is an auto-answer, auto-dial device that supports tone or pulse dialing. It supports full-duplex operation at 110, 300, or 1200 baud, conforming to the frequency specifications of the Bell 103A or 212A standards. The modem is not Hayes-compatible.

The PC Convertible printer runs off either the computer's battery pack or separate AC power. Weighing in at 3½ pounds, it prints unidirectionally at 40 characters per second in one pitch (10). The printer uses a 24-pin, thermal-transfer, nonimpact, dot-matrix print head that requires either thermal paper, a thermal-transfer ribbon and thermal-transfer paper, or high-quality (20-pound or less) plain paper. Supporting condensed, double-wide, and emphasized print modes, the printer will underline text and can print sub- and superscripts.

Photo 3: *The PC Convertible case and keyboard.*

OTHER OPTIONS

For LCD haters, IBM offers several display options including monochrome, color, and TV (RF modulator) adapters. IBM also sells a 9-inch monochrome or 13-inch color monitor attached to its own tiltable pedestal for use with the Convertible. The distance between the bottom of the pedestal and the CRT is sufficient to slide the Convertible neatly between the two. The monochrome and color monitors run only on AC power, so you'll be stuck with the LCD at the beach unless you have a long extension cord.

The CRT display adapter supports these direct-drive or composite monitors: the PC Convertible monochrome and color displays, the IBM PCjr color display, the IBM PC color display, or a standard TV set (using the IBM PCjr connector for TV). You can also use any IBM-compatible monitor with the Convertible. Since you'll have to be close to an AC outlet to use a monitor, IBM specifies that you must use the AC adapter to operate the Convertible when the CRT display adapter is connected to the computer. I used the machine without the AC adapter with no apparent ill effects, but I'm sure IBM advises against this practice to avoid quickly draining the battery.

My favorite option for the PC Convertible is the carrying case. It is made of canvas with lots of foam padding, and its design reminds me of a military flak jacket (its color is a conservative gray.) This carrying case will lend an air of strategic importance to your portable computing.

PC CONVERTIBLE SOFTWARE

The PC Convertible uses PC-DOS 3.2 to manage its hardware resources. Since it is a fully IBM PC–compatible computer (assuming, as IBM insists, that applications software makes BIOS and DOS calls only), the Convertible will run any IBM PC software.

However, the availability of your favorite software on 3½-inch disks could be a problem. At BYTE we use the Manzana MDP3A disk drive with accessory package software ($495 from Manzana, 935 Camino del Sur, Isla Vista, CA 93117, (805) 968-1387) to transfer software to the 3½-inch format for test purposes. I copied my favorite word-processing program onto a formatted 3½-inch PC Convertible disk and used it to write this article. I reformatted the disk after I copied the article back to a 5¼-inch disk.

Concurrent with the Convertible's debut, IBM announced two versions of a 3½-inch stand-alone disk drive for use with all the computers in the PC family. The availability of this drive (which requires PC-DOS 3.2) makes porting non-copy-protected software to the 3½-inch format less of a problem.

If you cannot acquire software on 3½-inch disks, you can still use a PC Convertible. The Convertible comes with an applications disk that contains a note writer, a scheduler, a phone list, a calculator, and some help files and utilities.

The note writer lets you create, save, and print notes up to six pages (12,000 characters) in length. You can adjust the left and right margins, do block moves or copies, and display a directory of existing notes. You cannot adjust line spacing or delete blocks.

The scheduler lets you set up a calendar of daily, weekly, or monthly appointments. You can set an audible alarm and mark appointments with an asterisk to remind you of important dates. You can even print out your weekly or daily schedule. You can set up the schedule profile with any start and end time and specify the time increment from 5 to 60 minutes.

The phone list lets you create and store name, address, and phone-number files. The program will even auto-dial numbers in the file if you have an internal or external modem attached to your Convertible.

The calculator adds, subtracts, multiplies, divides, figures percentages, and prints a log of your calculator operations.

The utilities supplied with the Convertible, called tools, mostly assign standard DOS functions such as FORMAT, ERASE, and DISKCOPY to the function keys for single-keystroke invocation.

CONCLUSIONS

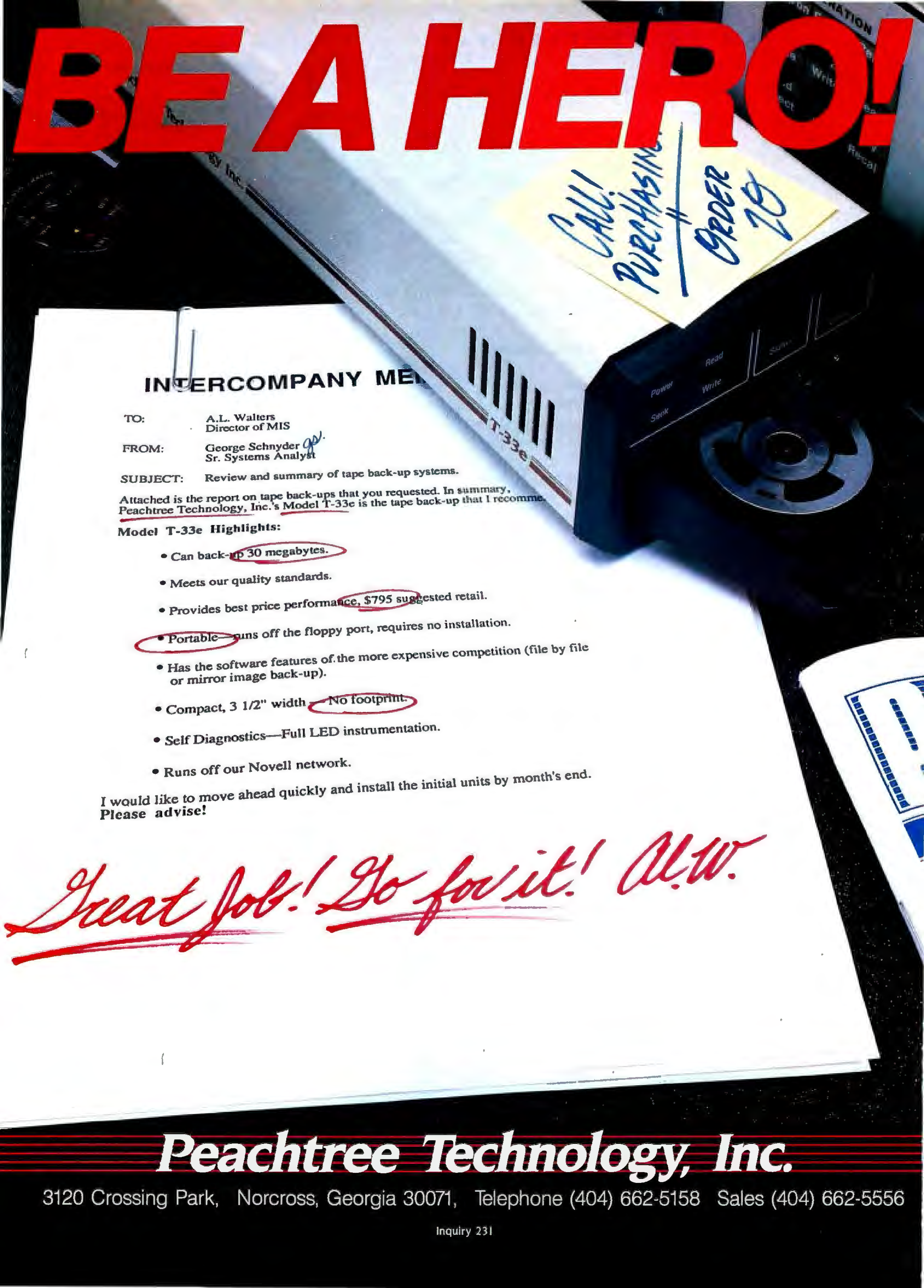
In BYTE, product descriptions give readers a first look at hardware or software prior to an in-depth product review. Therefore, I will make no judgments about the PC Convertible other than to say that it was easy to set up, add optional equipment to, and use to write this article. The machine worked without any failures during the few days I used it. I found the LCD to be readable for short stretches; however, I used the monochrome display for my longer text-composition stints. I like the keyboard as well as that of any portable computer I've tried. The layout of the Convertible's disk drives is attractive and useful.

How compatible is the PC Convertible? IBM makes no secret of the fact that the BIOS microcode is not identical to that of other IBM PC models. Programs that bypass the BIOS and directly access the hardware of IBM PCs might not run correctly on the Convertible as a result.

Many of the Convertible's incompatibilities are subtle. For example, the LCD can display reverse video but not high-intensity text. Another subtle incompatibility is the machine's static RAM; since the RAM needs no refresh, there are more microprocessor cycles available for any set period of time, making the processor appear to run faster. This apparent speed increase can affect programs that use timing loops for delays.

If you plan to write software for the PC family and want to have your program check to see if it is running on a Convertible, you can read the value in memory location FFFFE—a hexadecimal value of F9 means the machine is a Convertible.

Editor's note: See the editorial on page 6 for a discussion of some other IBM PC*–family compatibility issues.* ■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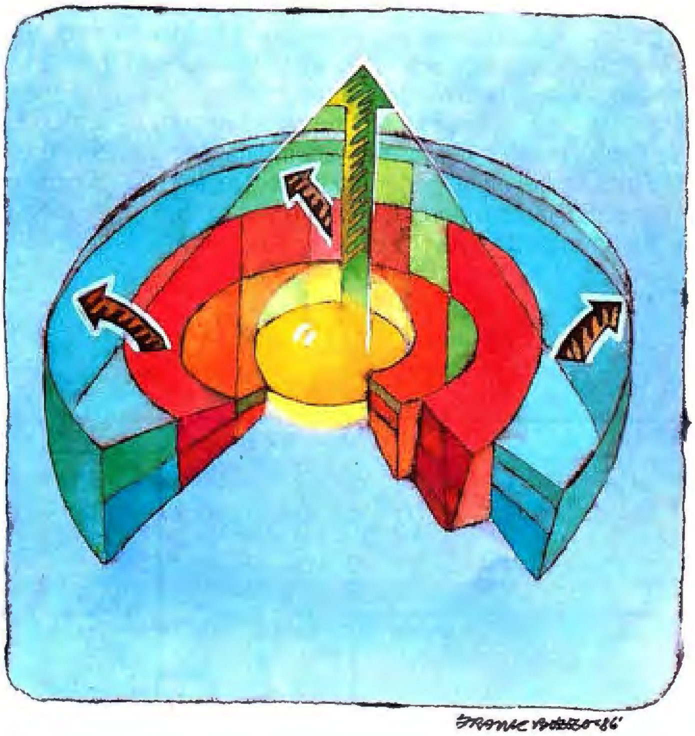
INTEL'S 80386 ARCHITECTURE

The 80386 combines pipelined architecture, segmentation, and paging in a multitasking environment

BY PAUL WELLS



WITH A SUSTAINED performance of 3 to 4 million instructions per second, the 80386 CPU surpasses the speed of many current superminicomputers and matches the mainframes of only 10 years ago. The chip's full 32-bit architecture furnishes a high degree of parallelism and an extremely fast local bus. Hardware-supported multitasking and protection mechanisms push system performance and integrity further into the mainframe range.

The 80386 is designed to handle mainframe-size applications with typically large integers, data structures, and large numbers of programs. The 80386 can address 4 gigabytes of physical memory and supports virtual memory, a capability pioneered on mainframes.

MEMORY CAPACITY

Virtual memory allows the use of programs and data structures larger than the actual physical memory, and the 80386's 64-terabyte (2^{46} bytes) virtual memory capacity lets the processor accommodate even the largest programs and data structures.

The 80386 gives designers a wide choice of memory models from which to choose: flat physical addressing, flat demand-paged, or a fully segmented protected model. This versatility and combination of both segmentation and paging traces its origins to mainframe systems like the Control Data Cyber 180 and the IBM 360/67.

The 80386 provides object code compatibility with programs created for Intel's iAPX processor family: 8088, 8086, 80186, 80188, and 80286. Moreover, the 80386's virtual 8086 facilities let MS-DOS–based 8086 programs run concurrently with programs written for 32-bit operating systems, with each program operating as a separate task in a protected multitasking framework.

HARDWARE IMPLEMENTATION

The 80386 is manufactured using Intel's CHMOS III process, combining the high performance of HMOS with the low power dissipation of CMOS. Double metal layers and 1.5-micron lithography allow a chip density of more than 275,000 transistors. The chip is available in 12- and 16-megahertz versions and is housed in a 132-lead ceramic pin-grid array (PGA), a package designed for compactness and high reliability (see figure 1).

32-BIT ARCHITECTURE

The 80386 includes a full complement of 32-bit registers and 32-bit-wide internal data paths. You can use eight general registers interchangeably as accumulators, for arithmetic and logical operations, or as addressing registers or data registers. Each register can be used for 32- or 16-bit values, and four of them can be split into pairs of 8-bit registers. A 32-bit flags register contains processor-control flags and records the results of logical and arithmetic instructions. A 32-bit instruction pointer controls instruction fetching.

Six 16-bit segment registers implement memory segmentation. When you add the 80387 numeric coprocessor, eight 80-bit floating-point registers are available for numeric computations. The operating system uses a number of system registers, which are invisible to the application pro-

(continued)

Paul Wells is the technical marketing manager for Intel and can be contacted at Intel Corporation, 3065 Bowers Ave., Santa Clara, CA 95015, (408) 987-8080.

ILLUSTRATED BY FRANK BOZZO

The 80386 is partitioned into a six-stage pipelined architecture.

grammer, for initialization, system management, exception handling, and multitasking. Six debug registers allow the setting of code or data breakpoints for previously unavailable debug capabilities. An additional register supports the 80386 self-test capability, which lets the chip test more than half its transistors. (Figures 2a, 2b, 2c, and 2d illustrate the 80386 CPU registers in detail.)

The principal data types are 8-, 16-, and 32-bit integers and ordinals; packed and unpacked decimals; near and far pointers; and strings of bits, bytes, words, and dwords.

A complete set of instructions, including bit-manipulation instructions, implements the processing of these data types. The 80386 instruction set is a superset of 8086 and 80286 instructions. Instructions average 3.1 bytes in length and require 4.4 clock cycles for execution when measured in a typical application mix.

The 80386's symmetric addressing modes can use any combination of the eight general-purpose registers and support efficient access to standard data structures like arrays, records, arrays of records, and records containing arrays.

OPTIMIZING FOR SPEED

The 80386 is partitioned into a six-stage pipelined architecture (see figure 3). Each processor's six functional units can work independently and in parallel with the others, enabling the chip to overlap execution of multiple instructions. The bus unit carries out bus transactions for other units, while the prefetch unit reads the next 4 bytes of the instruction stream into the prefetch queue when idle bus cycles are available. The decode unit converts each instruction to its component microinstructions, and the execution unit executes these microinstructions.

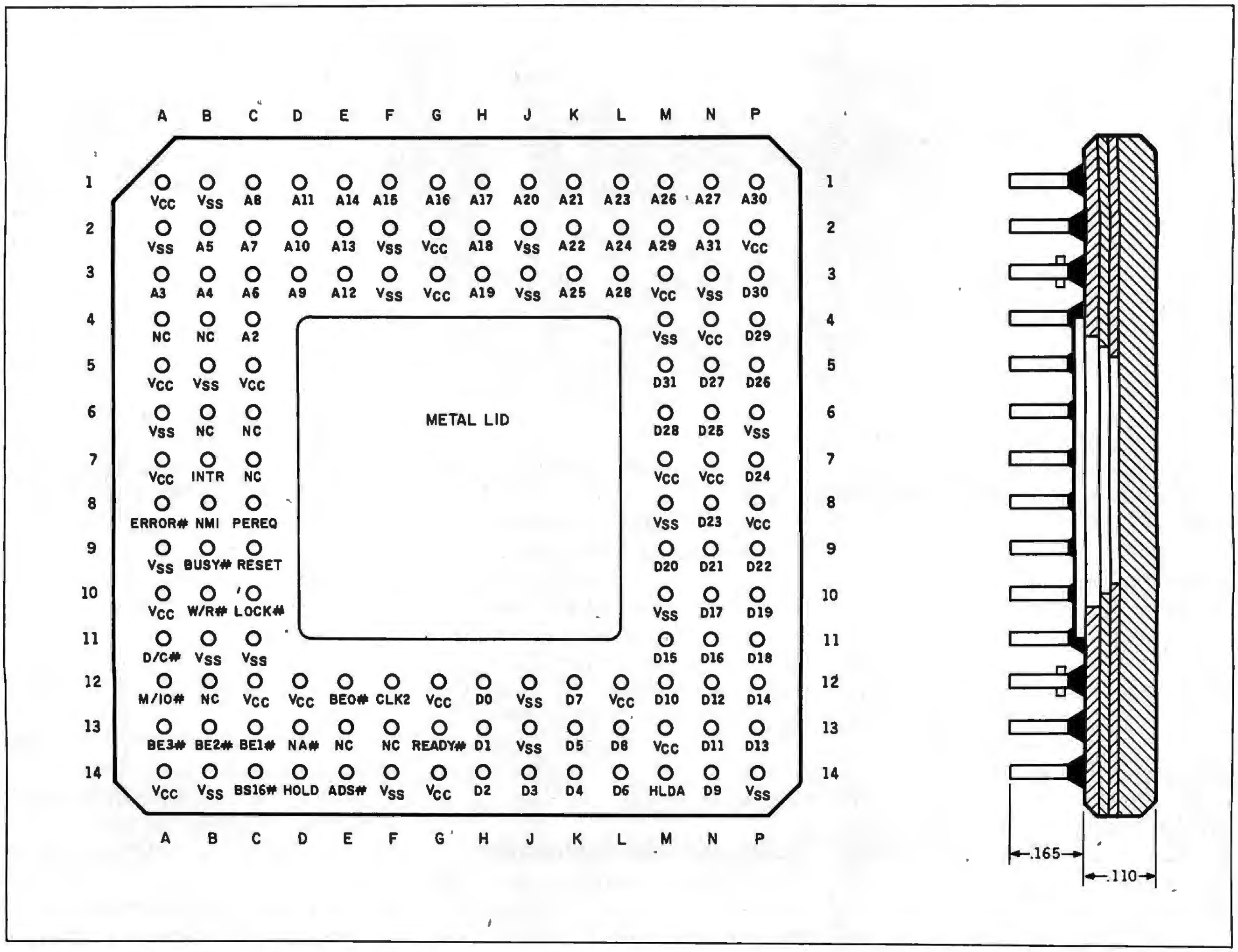


Figure 1: PGA *package and pin-out of the* 80386 *processor.*

The paging and segmentation units are also part of the pipeline. Together, these constitute the processor's memory management unit, which speeds up the address-translation process. By operating in parallel with other CPU activities, the on-chip MMU avoids the wait states associated with off-chip memory management and allows virtual-to-physical address translation with little effective delay.

The 80386 execution unit can sum two 32-bit registers in 2 clock cycles, while the multiply/divide hardware uses an advanced early-out algorithm to perform 32-bit multiplications in from 9 to 42 clocks (the exact number of clocks depends on the number of significant digits). A 64-bit barrel shifter can perform shifts of 1 to 64 bits in a single clock cycle.

The 80386 local bus achieves an overall throughput of 32 megabytes per second at 16 MHz, employing separate 32-bit data and address lines. The bus can complete an address-to-data-bus cycle in only two clocks, enabling very fast access to cache memory. Alternatively, a control feature can be used to pipeline the address from one cycle with data from the previous cycle, giving a three-clock latency appropriate to inexpensive dynamic RAMs. While the address-to-data-bus cycle increases to three clocks, address outputs and data inputs continue at a frequency of two clocks, avoiding any degradation of the processor's high bandwidth.

CACHE STRATEGY

Although a number of microprocessors feature on-chip code and data caches, their average size is about 256 bytes (too small to provide significant performance benefits). The 80386 is optimized for off-chip caching, providing a two-clock access to arbitrarily large caches. Such caches can be designed for hit rates in the 90 to 99 percent range, whereas on-chip code and data caches typically reach hit rates of only 20 to 30 percent, thus providing minimal performance benefits.

Dynamic bus sizing allows transfers of 16- or 32-bit data. This allows arbitrary combinations of 16- and 32-bit memory subsystems, connection to 16-bit buses like Intel's Multibus I, and compatibility with 16-bit peripheral devices. The processor can change the bus size during any bus cycle, and the mechanism is completely transparent to the application programmer.

PERFORMANCE

Pipelining, the on-chip MMU, a fast local bus, and the processor's compact code contribute to a fast

(continued)

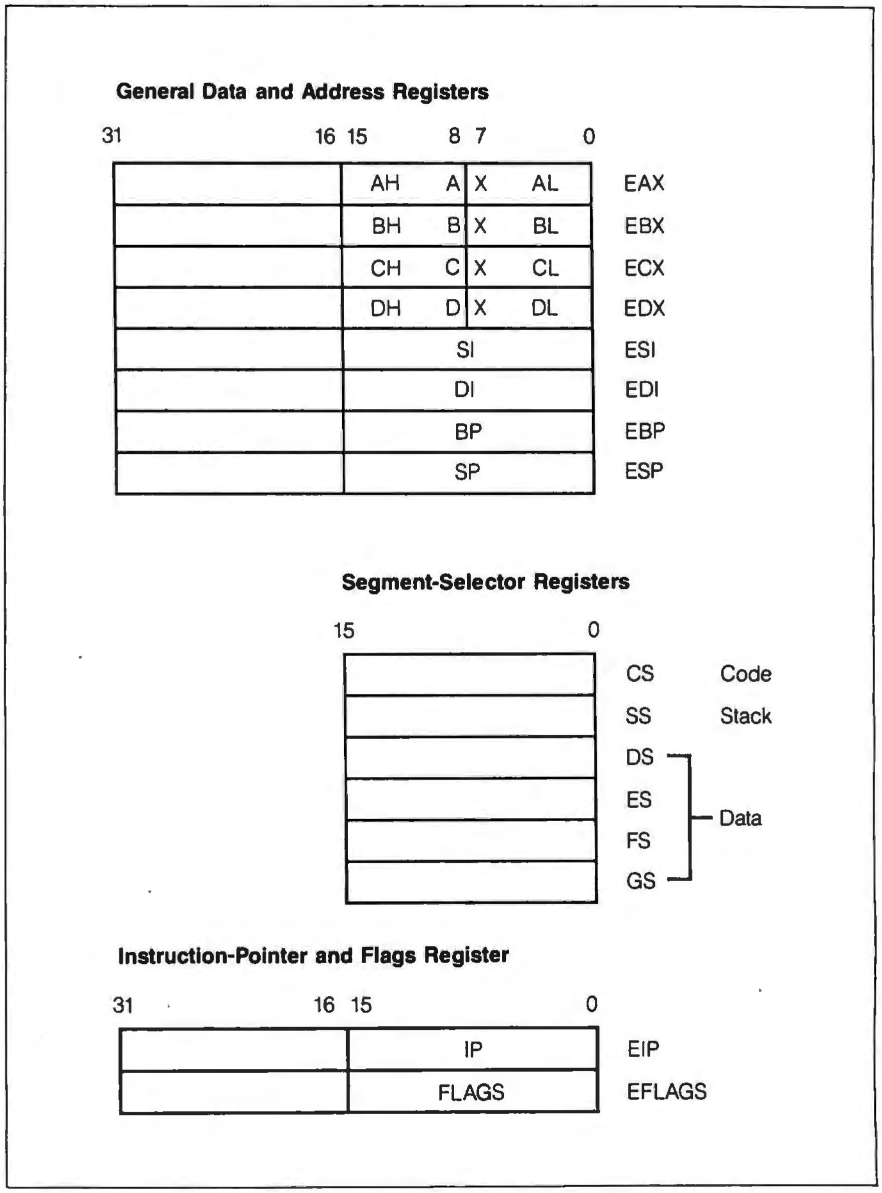


Figure 2a: *The* 80386 CPU *general data and address registers. The least significant* 16 *bits of the registers can be accessed separately using the two-letter register names* (AX, BX, *etc.*). *The* 8-*bit operations can access the individual bytes of the* 16-*bit registers using the byte names* (AL, AH, BL, BH, *etc.*). *The lower* 16 *bits of the instruction-pointer register and flags register* (EIP *and* EFLAGS) *are named* IP *and* FLAGS *and are used for* 8086 *and* 80286 *emulation.*

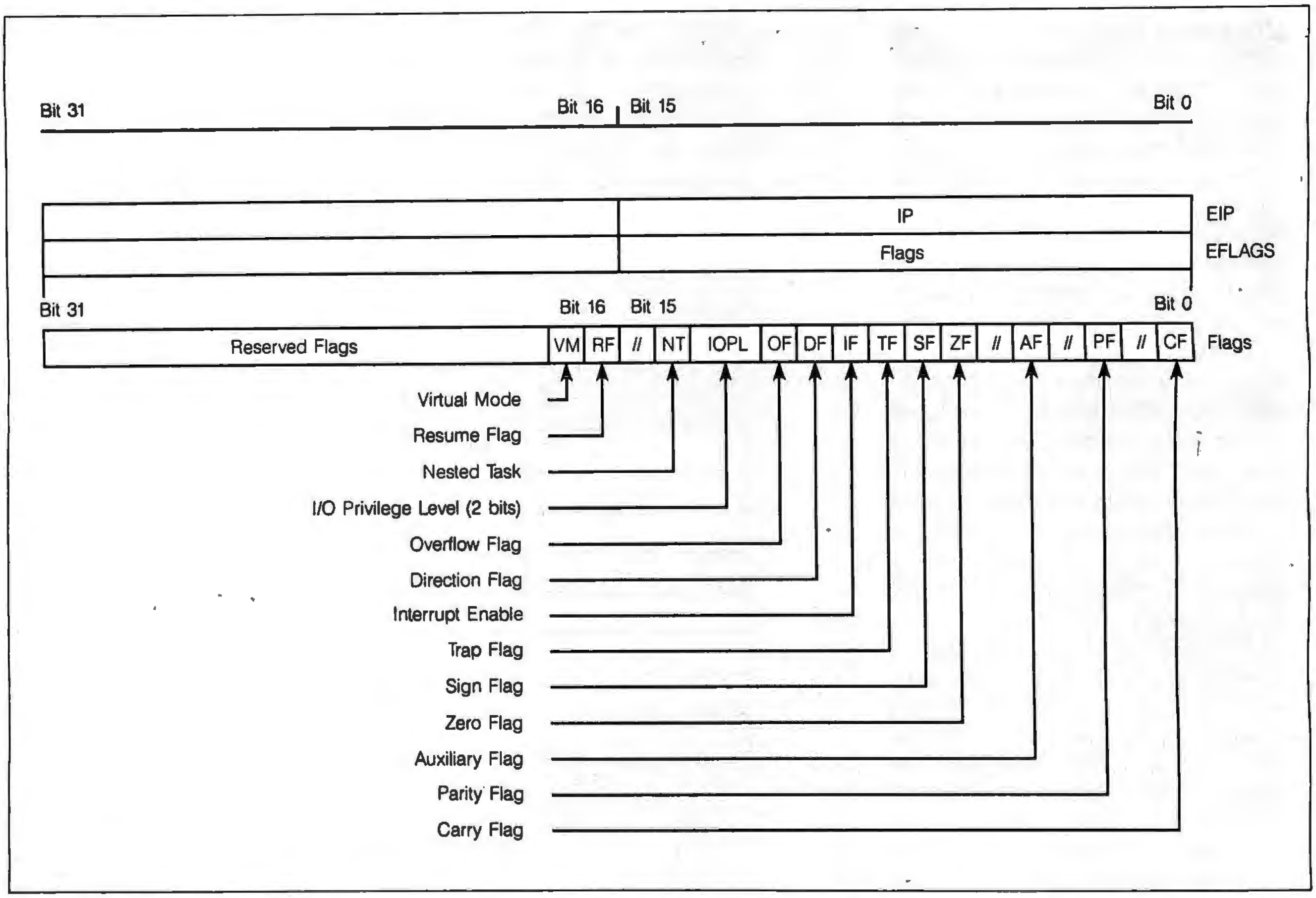


Figure 2b: *The 80386 instruction-pointer and EFLAGS registers. The 32-bit instruction-pointer register holds the offset (to be added to the base address of the current segment) for the next instruction to be executed. EFLAGS-register bit VM enables 8086 emulation when the CPU is in protected mode. The RF (resume flag) bit is used in conjunction with debug-register breakpoints. It causes the bug fault to be ignored on the next instruction. The other 16 flags are common to 8086 and 80286 modes.*

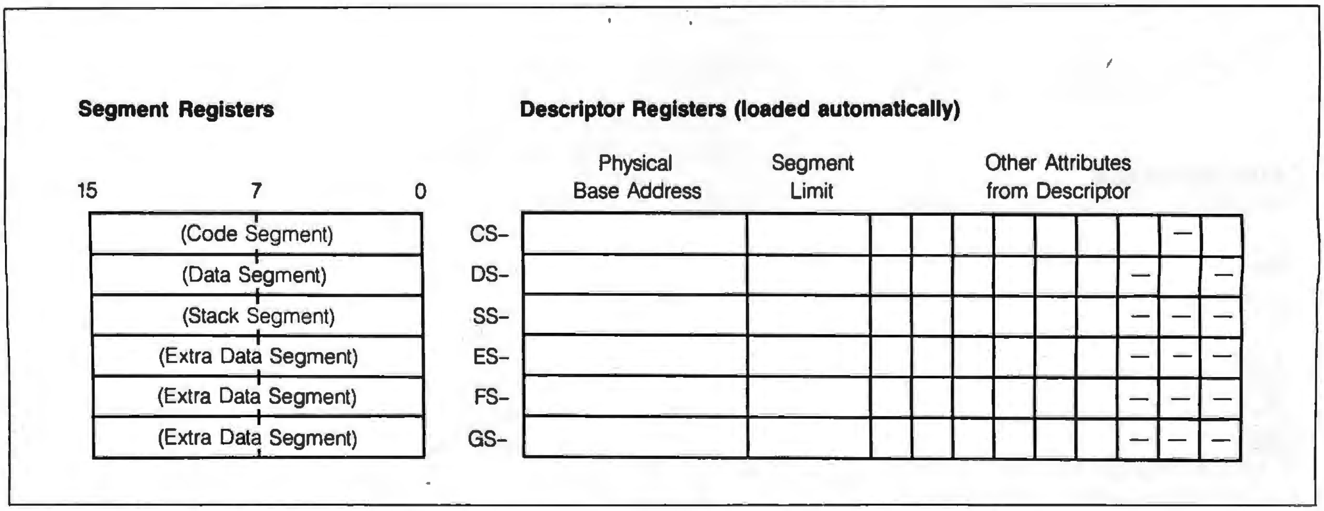


Figure 2c: *The 80386 segment registers. The 16-bit segment registers hold the selector values to the currently addressable memory locations. Real address mode segments can be 1 byte to 2^{16}, or 64K bytes in size. Protected-mode addressing allows segments of 1 byte to 2^{32} bytes, or 4 gigabytes, in size.*

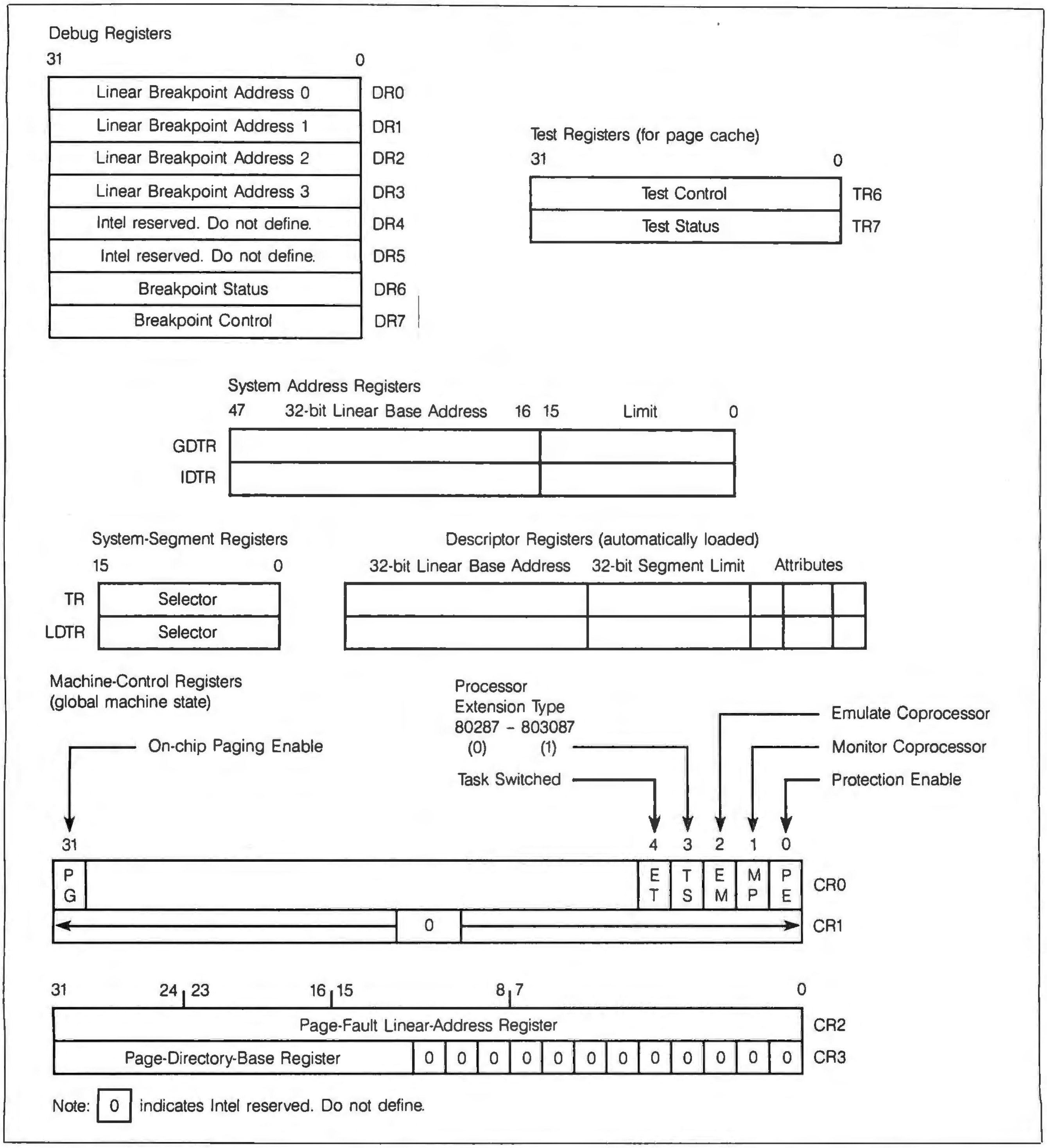


Figure 2d: *Ancillary 80386 registers. Debug-control register DR7 is used to set the breakpoints. Debug-status register DR6 holds the current state of the breakpoints. The four special system-address registers are used to reference tables or segments required by the 80286/80386 protected mode. They are named GDTR (global-descriptor-table register), IDT (interrupt descriptor table), LDT (local descriptor table), and TSS (task-state segment). Control register 0 (CR0) holds the machine-status word. Control register 2 (CR2), the page-fault linear-address register, holds the 32-bit linear address that caused the last page fault. Control register 3 (CR3), the page-directory base-address register, holds the physical base address of the page-directory table.*

Logical addresses pass through translation hardware to yield the physical address.

throughput. Recent benchmark tests set the 80386's performance at 3.64 MIPS, averaged over 14 applications and 31 million instructions.

The chip's interrupt response has been clocked at 3.7 microseconds from event to first handler instruction. Other benchmarks show the 80386 executing at 6133 Dhrystones per second. This compares favorably with the VAX-11/780's rate of 1662 Dhrystones per second and the VAX 8600 at 7000. The 80386's performance can be further boosted with an 80387 coprocessor (attaining 1.8 million Whetstones per second) or a Weitek 1167 floating-point coprocessor (4.0 million Whetstones per second).

All Intel results were obtained using a 16-MHz 80386 CPU and zero-wait-state memory. Whetstone and Dhrystone measurements used Intel's revision X.02 C compiler.

MEMORY MANAGEMENT

Virtual memory defines a logical address space that can exceed the size of the actual physical address space, letting you use mass storage devices in place of a large RAM array.

Logical addresses pass through translation hardware to yield the physical address (see figure 4). The large logical address space is subdivided into units of allocation, segments or pages, that can be swapped into and out of main memory from secondary storage devices to provide a task with necessary code or data. Swapping is performed under the management of the operating system and is transparent to the application.

Both paging and segmentation schemes have particular advantages. The 80386 provides a choice of these

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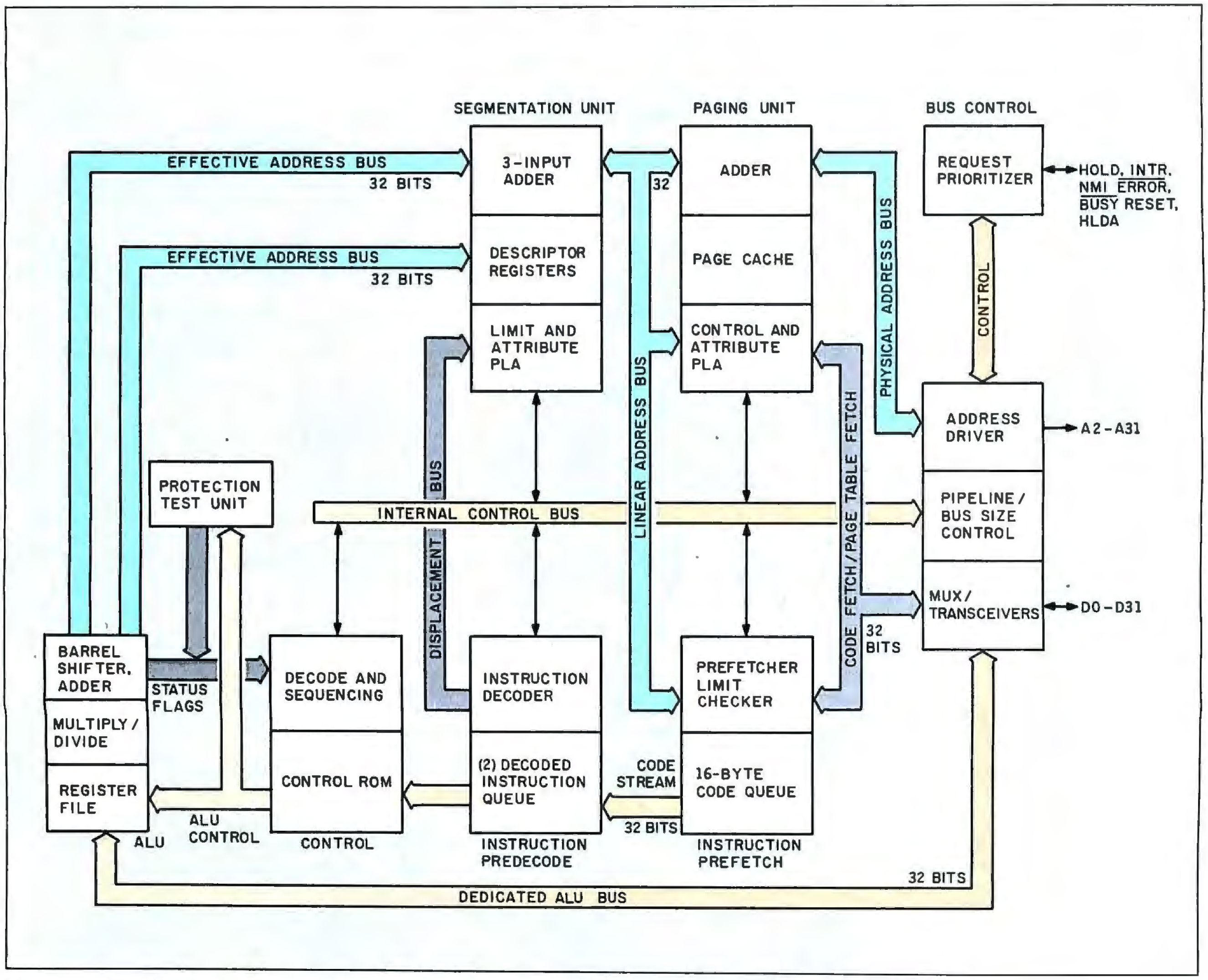

Figure 3: *The* 80386 CPU *pipeline architecture.*

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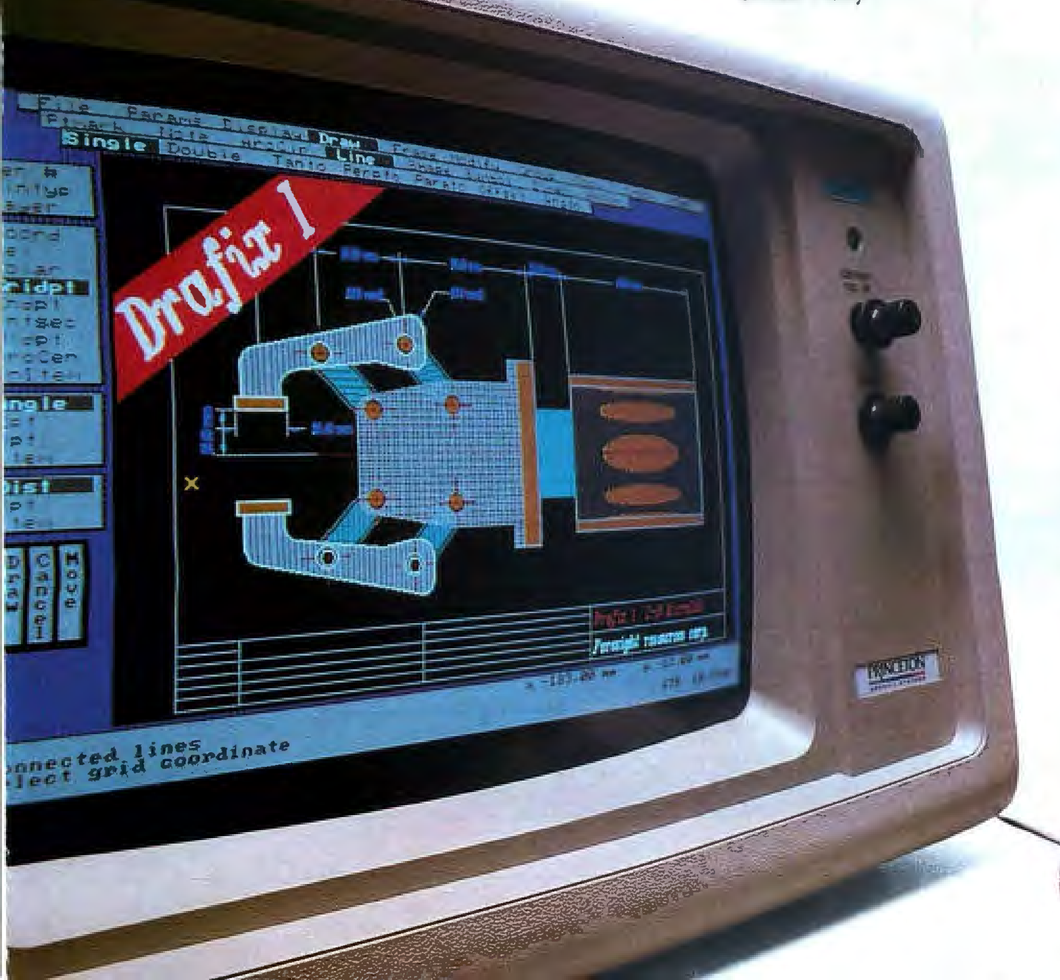

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two major memory models, to be used alone or in combination. System designers can choose the model best suited to their specific application.

In the simplest case, designers can elect not to employ virtual memory. They can group all addresses in a single segment, equivalent in size to the entire physical memory (up to 4 gigabytes). Addresses are organized in a linear, unstructured array. No MMU translation is required, and the logical address is precisely equivalent to the physical address. Such flat memory organizations are often preferred in embedded real-time systems like industrial controllers and private branch exchanges.

SEGMENTATION

In segmented models, logical memory is subdivided into segments of variable length (see figure 4). Each code

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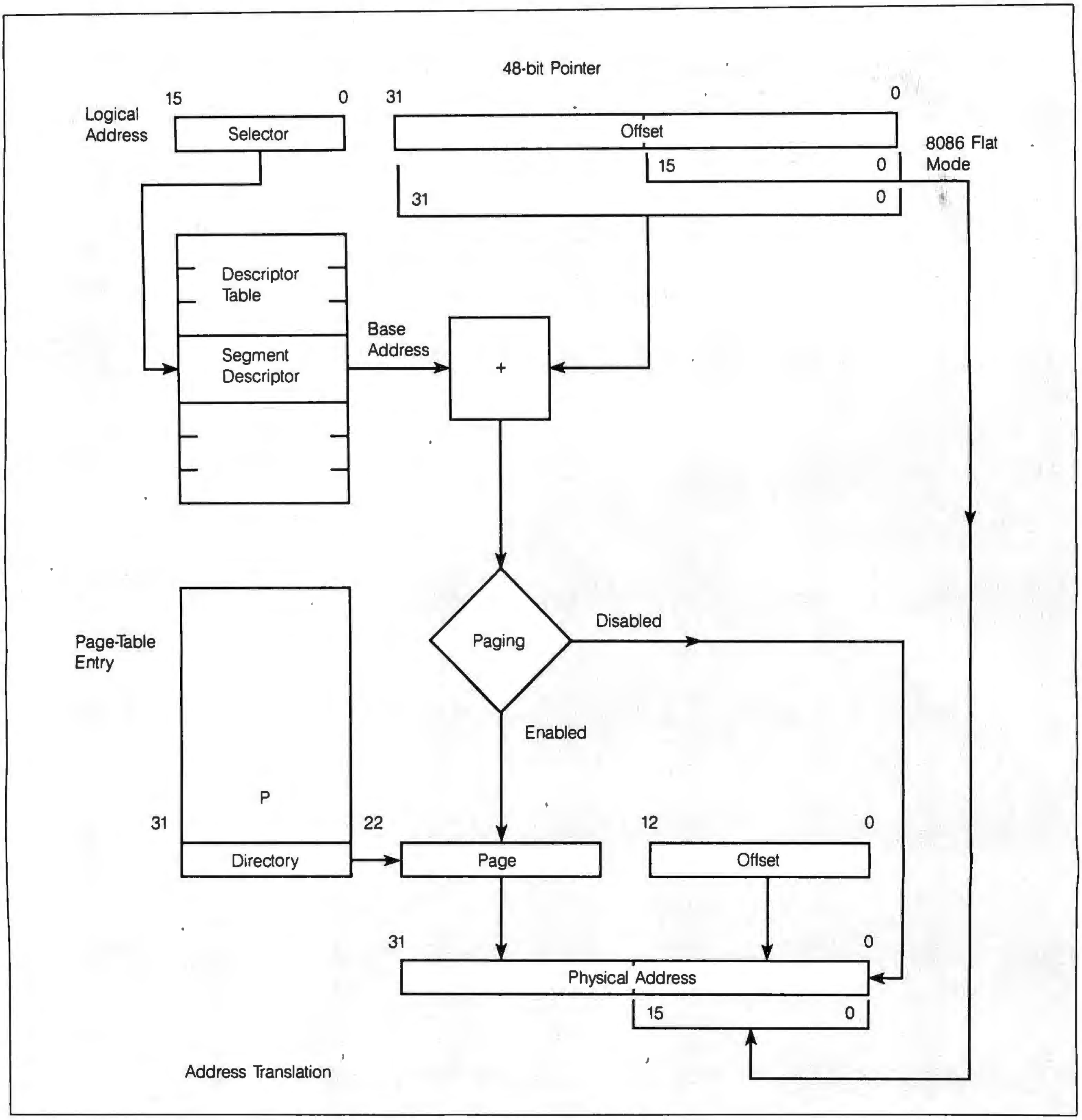

Figure 4: 80386 *address translation.*

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SYSTEMS IMPLICATIONS OF THE INTEL 80386

BY BILL NICHOLLS

What is a "systems" point of view? Briefly stated, it is the evaluation of a component's performance while it is part of a functioning system. This is a real-world view of performance, since no component operates without some interface to other equipment. Evaluation of a new processor must therefore be done in light of current and future demands on the whole computer system.

CLASSIFYING THE 80386

Classification of a processor is not one-dimensional. The primary dimensions are speed, architecture, and technology. In these broad terms, the 80386 is fast in operation (12- to 16-megahertz processor timing), complex in architecture (large instruction set, levels of protection, and virtual memory support), and current in technology (CHMOS).

How does the 80386 compare to other processors, small and large? Clearly, the 80386 is a microprocessor because of its implementation on a single chip. But do its characteristics qualify it as a mainframe? Certainly its speed is more than adequate for that classification. But while the architecture is as complex as some mainframes, it is incomplete in the area of I/O paths.

The 80386 can perform a number of direct I/O functions of various types and sizes. However, each element transferred requires the execution of one or more instructions to perform the transfer. Low-speed I/O can be done this way using interrupts, but high-speed I/O requires interrupts to be locked out and the chip dedicated to one peripheral device. This is acceptable only in some dedicated systems, not in general-purpose systems.

The inability to perform I/O while continuing to compute separates the 80386 from a full mainframe classification. Clearly, other chips can perform that function, and the combination of those chips and an 80386 is functionally equivalent to a mainframe.

Given a proper I/O design and adequate memory size and speed, the 80386 would compare closely in performance to an IBM Model 4341-1 or 4341-2, depending on a number of factors. The higher instruction-execution rate of the 80386 would be offset by the more powerful instructions of the 4341. Memory and I/O bandwidth would also have to be evaluated for specific designs. In capability, however, the 80386 could perform at the level of an IBM 4341. The major differences in performance would depend on how the 80386's I/O subsystem compared to the 4341's I/O subsystem and the use of special 4341 instructions.

HIGH-PERFORMANCE HARDWARE

In this context, high performance means maximizing system performance relative to the design objective without excessive cost. For systems with the same processor, different design objectives will lead to different performance levels due to the economic choices made.

The primary requirement for a high-performance 80386 system is adequate memory bandwidth. Bandwidth as measured in megabytes per second is an important number. However, bandwidth that is not carefully matched to the processor cycle is usually wasted.

Some additional bandwidth is required for I/O. For example, an 80386 with a 12.5-MHz clock tick (25-MHz crystal) requires an 80-nanosecond memory access for zero wait states and 160 ns for one wait state. With a zero-wait-state memory, the processor is internally (CPU) limited; with a one-wait-state memory, it is bus-limited. If a processor is bus-limited, I/O cycles on the bus will interfere with processor execution, causing some reduction in processing capacity. For designs like single-user computers, this is probably acceptable. For large multiuser systems, it means trading off memory cost against performance gains that are important but hard to justify.

Until recently, there was no easy way to match a fast processor to slower memory speeds without loss of performance. The typical solution was to use a small but fast cache memory and a larger but slower main memory. The added complexity and cost removed this technique from the personal computer market. The 80386 offers a method for adding this performance boost.

Using an external pin called *next address*, the designer can have the processor output the next address before the current memory cycle is finished. This enables the address to be decoded for the next memory access to happen concurrently with the current memory data cycle. This is called pipelined mode access.

Table A shows the trade-off between processor clock speed, wait states, and required memory-access time. The Bus Cycles Available column shows the percentage of the bus that can be used

Table A: *The differences in processor clock speed, wait states, and memory-access times for the Intel* 80386.

Processor Clock	Access Mode	Memory 0 ws	Access 1 ws	Bus Cycles Available 0 ws	Bus Cycles Available 1 ws
12.5 MHz	2-cycle	80 ns	160 ns	27%	14%
	2-pipe	160 ns	240 ns	21%	11%
16 MHz	2-cycle	45 ns	107 ns	27%	14%
	2-pipe	108 ns	170 ns	21%	11%

Note: 2-cycle is the standard memory access; 2-pipe is the 2-cycle pipelined mode of access.

by I/O before interference with the processor is certain. Below that level, I/O interference is small.

Another way to enhance large-system performance is with banked memory, a technique used in large mainframes. The basic system can be delivered with a single bank of memory. As the system grows in the field, a second bank of memory could be added so that sequential addresses would then alternate banks. This bank alternation works for both I/O and processor access. Large mainframes may use up to 16-way bank interleave, but multiprocessor microcomputers will probably need no more than 4-way banked memory for higher performance.

FAST I/O

Fast I/O is not well supported in the 80386. An external direct memory access is required. With the complexity of addressing in the 80386, even simple DMA can be awkward. A single I/O command can refer to data that spans over page boundaries and is relocated in noncontiguous real memory addresses. Thus, the operating system must first test for this condition and split one logical I/O operation into more than one physical I/O operation, then schedule and coordinate the physical I/O operations, and finally notify the calling program when done. In addition to adding significant overhead, it also complicates error recovery.

A second type of DMA, "smart" DMA, is now available. It can perform multiple operations as a single logical I/O operation and relieve the processor of substantial overhead. Large-scale systems have had this feature, *scatter read/gather write*, for some time. This means the DMA chip can read a physical record from scattered locations and gather scattered data to write as a single record. These features are incorporated in the Intel 82258 DMA chip.

In addition to a powerful DMA capability, the hardware must support higher transfer rates than the current 5 megabits per second. Multiple transfers on different channels at the same time must also be supported. Both of these requirements can be met with the 82258, which can support four high-speed channels with a maximum throughput of 16 megabytes per second. The 82258 can also operate as three high-speed channels and one multiplexed channel supporting 32 subchannels at up to 30k bits per second each.

Few programs will be able to fully utilize an 80386, even with fast I/O. One way to use the available time is to run multiple programs or tasks. Multitasking divides the processor's time in slices and allocates one slice to each task, switching rapidly between tasks to give the illusion of continuous operation. Some tasks may slow down compared to running alone, but overall throughput increases up to a point.

That point is determined primarily by the operating system overhead in performing its primary services: I/O control and task switching. More tasks, more I/O, or shorter time slices increase the overhead. When the increase in overhead exceeds the improvement in throughput, system performance begins to degrade. If the processor provides fast methods for I/O processing and task switching, a system with a well-designed operating system will reach a higher level of throughput before system performance degrades.

The Intel 80386 processor has fast task switching in its instruction set. A single instruction will totally switch tasks including registers and environments in 17 to 20 microseconds. This is an order of magnitude faster than processors without this instruction and significantly reduces overhead in support of multitasking. Interrupts can use task switches or, for fastest response, calls that execute in 3 microseconds but do not switch task environments.

Bill Nicholls is president of, and a software engineer at, BGW Systems Inc. (16714 Meridian S, Suite 200, Puyallup, WA 98373).

and data module (such as file buffers, program variables, and so on) can be assigned a different segment. Since each module has its own logical memory address space, it is easy to implement schemes that protect individual modules, share them selectively between tasks, and manipulate them separately or together. Segments in the 80386 can be any size up to 4 gigabytes (enough for the largest code and data modules), with a maximum of 16,000 segments per task.

This is how the 80386 implements segmentation. The logical address used by the application consists of a 16-bit segment selector and a 32-bit offset into the selected segment. The selector references a segment descriptor held in a table that the operating system maintains. The 64-bit descriptor contains the segment's 32-bit base address and limit (length), together with swapping information and protection parameters like privilege level, access rights, and segment type. In addition, the descriptor's present bit tells the processor whether the desired segment is present in memory or needs to be swapped in from disk.

The segment's base address, obtained from the descriptor, is added to the offset to give a linear address. The linear address is then passed through the paging unit to yield the physical address unless paging is disabled, in which case the linear address is the physical address.

The processor automatically maintains descriptors for the current segment in an on-chip cache, minimizing the need to index memory-based descriptor tables. The cache-resident segment descriptor is replaced automatically with a new one whenever a new segment selector is loaded into a segment register. Programs can address up to six segments at a time: a code segment, a stack segment, and up to four data segments.

PAGING

While segments vary in size and map well to programming constructs, pages are small blocks of fixed size

(continued)

The page-table entry includes attributes like present, rights, accessed, and dirty.

(4K bytes in the 80386). Paging simplifies swapping algorithms by providing uniform units of allocation and relocation. Thus, while segmentation can be used to structure the logical address space, paging can be used to manage the physical memory.

The paging system uses a 32-bit linear address. The upper 10 bits of the address index a 1024-entry page-table directory to obtain a page-table address (see figure 5). The middle 10 bits of the linear address are added to the page-table address to get a page-table entry that describes the target page. The final 12 bits of the linear address are added to the page address to generate a 32-bit physical address.

Just as the processor's segmentation mechanism caches segment descriptors, the paging unit supplies an on-chip associative cache containing mapping information for the 32 most recently used pages. The cache, called a translation lookaside buffer (TLB), has a hit rate of 98 to 99 percent, minimizing the performance impact of enabling the paging system.

The page-table entry includes attributes like present, rights, privilege level, accessed, and dirty. The accessed bit is set automatically whenever a page is read or written. The dirty bit is set whenever a page is written. By monitoring accessed and dirty bits, the operating system can implement a variety of page-replacement algorithms, like least recently used (LRU) approximation algorithms. No other microprocessor provides both dirty and accessed bits.

COMBINING PAGING AND SEGMENTATION

Although it is possible to use paging or segmentation alone, the 80386 also lets designers combine the advantages of both models, providing a powerful capability.

The application programmer employs segmentation to implement data sharing, software protection, and multitasking, while paging provides the underlying physical memory management. The segmentation/paging combination was first used by Control Data and IBM mainframes and is also employed by UNIX System V, which allots each task a segment for code and a segment for data and the stack.

When the two memory management organizations are used together in the 80386, linear addresses pro-

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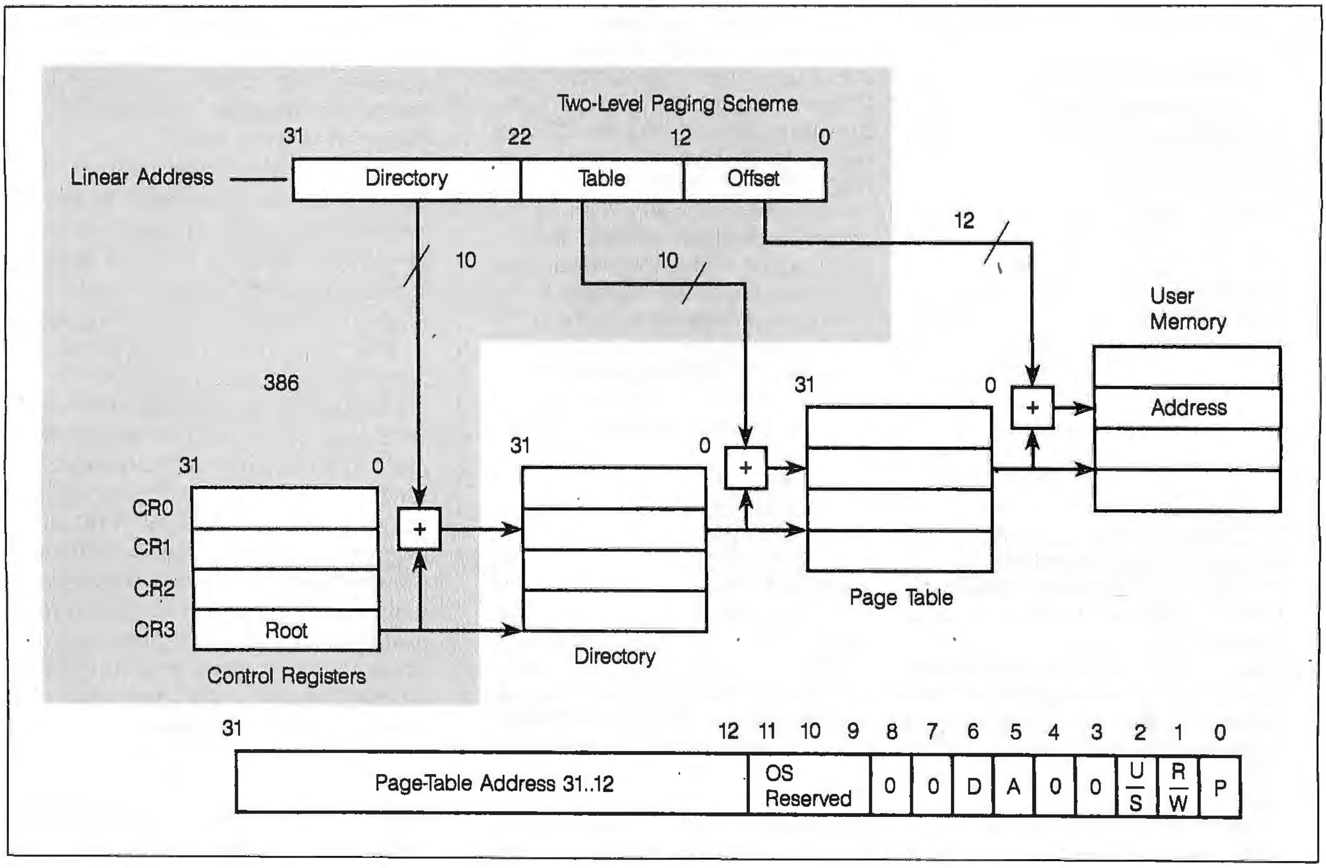

Figure 5: 80386 *paging system.*

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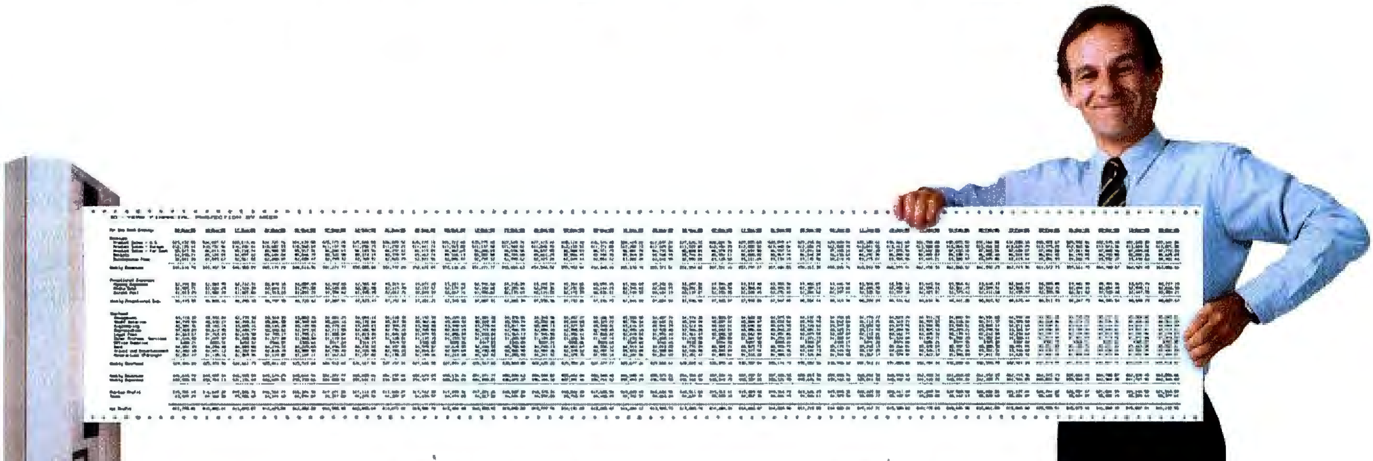

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duced by the segmentation unit are passed through the paging mechanism to generate the final physical address. Overall, this multistage address-translation facility is fast, due to the on-chip translation caches and the pipelining of memory management functions. Translation from logical to physical address typically requires only one and a half clocks. From the user's perspective, the effective delay is zero clocks since translation is performed on-chip, overlapped with other processor activities.

PROTECTION HARDWARE AND SOFTWARE

An additional benefit of the 80386's on-chip MMU is an array of protection mechanisms that operating systems can selectively employ, including separation of task address spaces, typed segments, access rights for segments and pages, and segment-limit checking.

A frequent and insidious problem occurs when an erroneous task violates the address space of another task and overwrites code or data. In this way, bugs can propagate through a system and be nearly impossible to track. The 80386 protects task address spaces by assigning them to different segments and/or separate page directories and page tables. Segment-descriptor tables prevent unwarranted access by other tasks.

In addition to isolating tasks from one another, the processor provides a ring-protection mechanism that can guard low-level software both from bugs in overlying layers and from intentional tampering at the application level. Each segment descriptor and page-table entry has a field that defines the segment's and page's privilege level, ranked from 0, the most privileged level, to 3, the least trusted. Programs at a given level can access data and code only at the same or a numerically higher level (see figure 6).

Segment descriptors hold not only privilege information but also the segment limit (references to the segment must fall within the limit, preventing

(continued)

31	24	16	8	5	0	
Selector		Offset 15...0				0

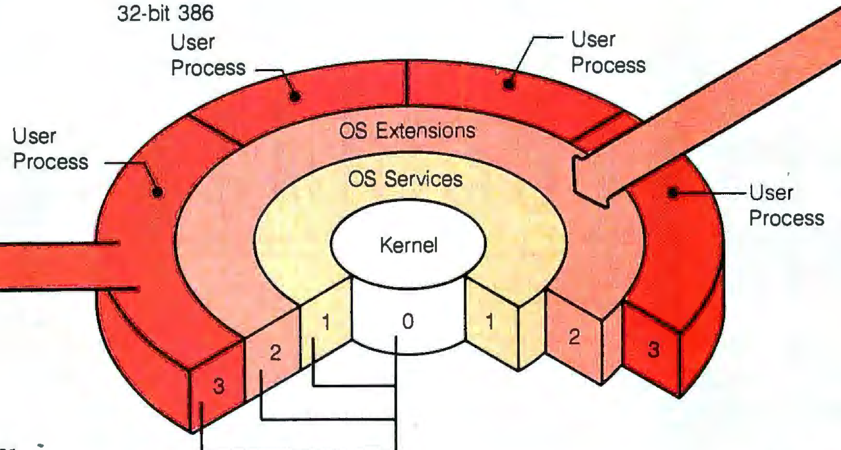
Offset 31...16	P	DPL	0	Type	0	0	0	Word Count 4...0	+4

Gate Descriptor Field

Name	Value	Description
Type	4	286 call gate
	5	Task gate (for 286 or 386 task)
	6	286 interrupt gate
	7	286 trap gate
	C	386 call gate
	E	386 interrupt gate
	F	386 trap gate
P	0	Descriptor contents are not valid
	1	Descriptor contents are valid

DPL—least privileged level at which a task may access the gate. WORD COUNT 0-31—the number of parameters to copy from caller's stack to the called procedure's stack. The parameters are 32-bit quantities for 386 gates and 16-bit quantities for 286 gates.

Destination Selector	16-bit selector	Selector to the target code segment or Selector to the target task-state segment for task gate
Destination Offset	offset 16-bit 286 32-bit 386	Entry point within the target code segment



Segment Descriptor

31											0	Byte Address
Segment Base 15...0						Segment Limit 15...0						0
Base 31...24	G	D	0	0	Limit 19...16	P	DPL	S	Type	A	Base 23...16	+4

Base	Base address of the segment
Limit	The length of the segment
P	Present Bit 1=Present 0=Not Present
DPL	Descriptor Privilege Level 0-3
S	Segment Descriptor 0=System Descriptor 1=Code or Data Segment Descriptor
Type	Type of Segment
A	Accessed Bit
G	Granularity Bit 1=Segment length is page granular 0=Segment length is byte granular
D	Default Operation Size (recognized in code segment descriptors only) 1=32-bit segment 0=16-bit segment
0	Bit must be zero (0) for compatibility with future processors

Figure 6: *Four levels of protection.*

Segment Descriptor-Cache Register Contents

	32-bit Base (Updated during Selector Load into Segment Register)	32-bit Limit (Fixed)	Other Attributes (Fixed)									
	Base	Limit	Present	Privilege Level	Accessed	Granularity	Expansion Direction	Readable	Writable	Executable	Stack Size	Conforming Privilege

Real Address Mode (Segment Limit and Attributes are Fixed)

	Base	Limit	Present	Privilege Level	Accessed	Granularity	Expansion Direction	Readable	Writable	Executable	Stack Size	Conforming Privilege
CS	16X Current CS Selector*	0000FFFFH	Y	0	Y	B	U	Y	Y	Y	–	N
SS	16X Current SS Selector	0000FFFFH	Y	0	Y	B	U	Y	Y	N	W	–
DS	16X Current DS Selector	0000FFFFH	Y	0	Y	B	U	Y	Y	N	–	–
ES	16X Current ES Selector	0000FFFFH	Y	0	Y	B	U	Y	Y	N	–	–
FS	16X Current FS Selector	0000FFFFH	Y	0	Y	B	U	Y	Y	N	–	–
GS	16X Current GS Selector	0000FFFFH	Y	0	Y	B	U	Y	Y	N	–	–

Key:
- Y = yes
- N = no
- 0 = privilege level 0
- 1 = privilege level 1
- 2 = privilege level 2
- 3 = privilege level 3
- U = expand up
- D = expand down
- B = byte granularity
- P = page granularity
- W = push/pop 16-bit words
- F = push/pop 32-bit dwords
- – = does not apply to that segment-cache register

*Except the 32-bit CS base is initialized to FFFFF000H after reset intersegment CALL or intersegment JMP, or INT).

Protected Mode (Loaded per Descriptor)

	Base	Limit	Present	Privilege Level	Accessed	Granularity	Expansion Direction	Readable	Writable	Executable	Stack Size	Conforming Privilege
CS	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	d	N	Y	–	d
SS	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	r	w	N	d	–
DS	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	d	d	N	–	–
ES	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	d	d	N	–	–
FS	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	d	d	N	–	–
GS	Base per Seg Descr	Limit per Seg Descr	p	d	d	d	d	d	d	N	–	–

Key:
- Y = fixed yes
- N = fixed no
- d = per segment descriptor
- p = per segment descriptor; descriptor must indicate "present" to avoid exception 11 (exception 12 in case of SS)
- r = per segment descriptor, but descriptor must indicate "readable" to avoid exception 13 (special case for SS)
- w = per segment descriptor, but descriptor must indicate "writable" to avoid exception 13 (special case for SS)
- – = does not apply to that segment-cache register

Virtual 8086 Mode within Protected Mode (Segment Limit and Attributes are Fixed)

	Base	Limit	Present	Privilege Level	Accessed	Granularity	Expansion Direction	Readable	Writable	Executable	Stack Size	Conforming Privilege
CS	16X Current CS Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	Y	–	N
SS	16X Current SS Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	N	W	–
DS	16X Current DS Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	N	–	–
ES	16X Current ES Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	N	–	–
FS	16X Current FS Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	N	–	–
GS	16X Current GS Selector	0000FFFFH	Y	3	Y	B	U	Y	Y	N	–	–

Key:
- Y = yes
- N = no
- 0 = privilege level 0
- 1 = privilege level 1
- 2 = privilege level 2
- 3 = privilege level 3
- U = expand up
- D = expand down
- B = byte granularity
- P = page granularity
- W = push/pop 16-bit words
- F = push/pop 32-bit dwords
- – = does not apply to that segment-cache register

Figure 7: *Segment-descriptor registers.*

such common errors as stack overflow and array subscript errors); segment type, such as code or data (thus catching an attempt to overwrite code, for example); and access rights, such as read-only.

Thus, a spectrum of protection schemes is possible, ranging from no protection to a four-level hierarchy that separates the operating system kernel, residing at level 0, from the operating system services at level 1, custom operating system extensions at level 2, and applications at level 3. (Figure 7 shows segment-descriptor-register contents for real address, protected, and virtual 8086 modes of operation.)

Of course, it is necessary to let applications at low privilege levels make occasional calls, like disk I/O requests, to more protected levels. To handle cases such as this, the operating system can define entry points called gates. Gates contain the logical addresses of entry points and a set of attributes.

MULTITASKING

The 80386 was designed for high-throughput multitasking, in which each task sees only its own execution context and is unaware of other tasks running concurrently. The operating system switches the processor from one context to another, interleaving tasks in accordance with a scheduling policy.

Several data structures, transparent to applications, are defined to support the operating system, principally the task-state segment (TSS). The TSS holds the state of tasks, including processor-register values and data such as scheduling priority, address-space definitions, descriptors, and page-table-directory base. Values held in the 80386 task register point to the running task's TSS.

Because task switching can be frequent, the 80386 provides special high-speed hardware to support this operation. In response to a jump instruction with a special address, the processor automatically stores the state of one task and loads the state of another (at a speed roughly 10 times as fast as software-controlled multitasking).

SOFTWARE COMPATIBILITY

The 80386 supplies binary code compatibility with all previous 8086-family software applications. You can port operating systems and programming tools directly to the new processor without recompilation or assembly.

For 8086 programs, the processor provides virtual 8086 mode, which establishes a task-selectable protected 8086 environment within the multitasking framework. In this environment, 8086 tasks can take advantage of the 80386's protection and paging

(continued)

The I/O privilege level is used to control interrupt enabling, disabling, and system calls.

mechanisms, while running nonprivileged 8086 instructions directly at roughly 16 times the speed of an 8086. If the 80386 operating system you are using supports virtual memory, you can swap 8086 tasks just like any other tasks.

VIRTUAL 8086 MODE

In virtual 8086 mode (activated by the VM86 flag in the flags register), the 80386 presents 8086 operating systems and applications with a virtual machine (the 80386 looks and acts just like an 8086 to the application program). Segment-register semantics are the same as in the 8086.

The total address space of the 8086 is 1 megabyte. Addresses generated by virtual 8086 tasks will all fall within the first megabyte of the 80386 linear address space. In order to assign each task a separate address space, paging is used to relocate the linear address spaces to different areas of the physical address space.

Many 8086 programs were designed. for single-tasking environments, and many use I/O and interrupt control in a manner inappropriate for multitasking systems. The 80386 therefore provides mechanisms to selectively trap and manage this I/O and interrupt activity.

I/O PRIVILEGE LEVEL

The I/O privilege level (IOPL) is used to control interrupt enabling, disabling, and system calls. The I/O-port permission map selectively controls access to I/O ports. Memory-mapped devices can be managed using page-level protection attributes. The software module that manages these operations is called a virtual machine monitor.

With the exception of interrupts and system calls, all 8086 application instructions execute directly on the 80386 at full CPU speed. And since the 80386 is a proper superset of the 80286 architecture, the 80386 runs 80286 applications unchanged. Because the virtual 8086 mode is selectable on a per-task basis and the execution of 16-bit 80286 code is selectable on a per-segment basis, the 80386 can run 8086 applications, 80286 applications, and 32-bit 80386 applications concurrently in a protected multitasking environment.

MULTIPLE EXECUTION ENVIRONMENTS

Taken together, the 80386's flexible memory management architecture, multitasking, protection, and virtual 8086 mode open a vast range of design options. Most striking is the ability to host multiple concurrent-execution environments. Numerous applications, written for different operating systems and different memory management schemes, can run under a 32-bit operating system. An 80386-based system using a UNIX System V kernel could simultaneously support 16-bit 8086 MS-DOS applications running in virtual 8086 mode; XENIX-based 16-bit 80286 applications using segmentation and paging; code ported from linear UNIX environments, like Berkeley 4.2, running in a paged linear model; and UNIX System V applications using segmentation and paging. Despite their diversity, such tasks could coexist, each in its own protected address space. The operating system could switch between environments in the space of a single instruction.

Future 80386 applications might include multiuser microcomputers running mainframe-size programs at mainframe speeds, engineering workstations executing sophisticated UNIX CAE programs concurrently with popular MS-DOS office-automation packages, and 80386-based superminicomputers for on-line transaction processing. ■

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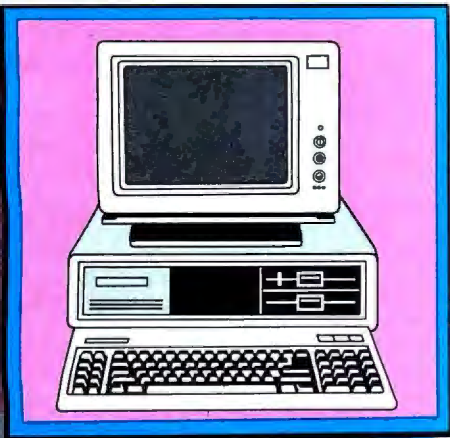

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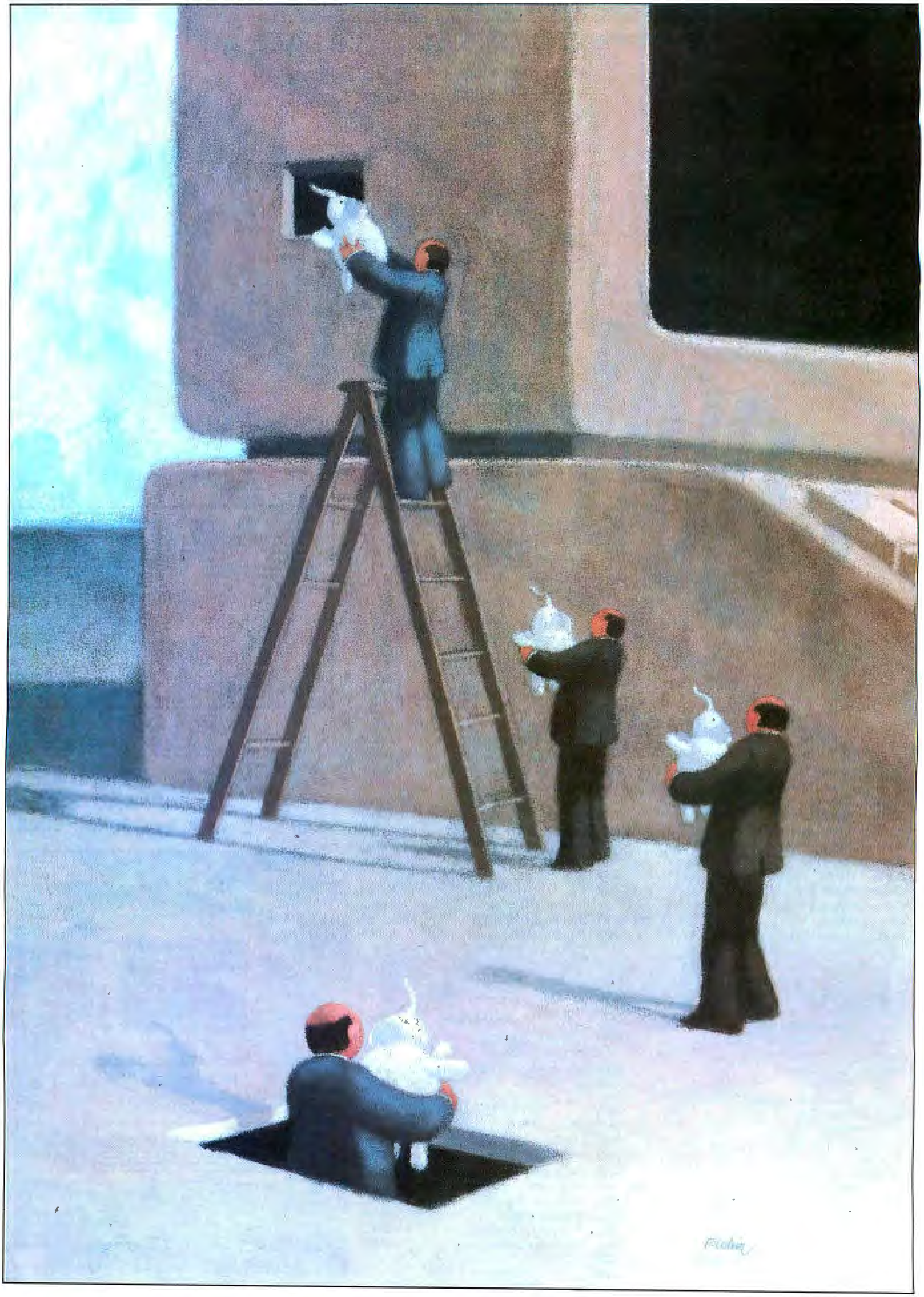

ILLUSTRATED BY ROB COLVIN

VIRTUAL MEMORY, VIRTUAL MACHINES

The 80386 offers virtual memory capabilities with memory protection

BY JON SHIELL

VIRTUAL MEMORY is a method for making the amount of memory that a program uses independent of the actual amount of RAM in the machine. In virtual memory systems, the disk memory effectively becomes the main memory, and the RAM becomes a temporary holding area for code and data that the processor is currently using. With virtual memory, the programmer doesn't care how much RAM (hereafter called *real memory*) the machine has. In fact, the program has no way of knowing how much real memory the system has. Instead, the program cares only about how big the virtual address space is.

The 8086 (which does not support virtual memory), the 80286, and the 80386 in real mode have a real address space of only 1 megabyte. The 80286 in protected mode has a virtual address space of 1 gigabyte and a real address space of 16 megabytes. The 80386 in protected mode has a virtual address space of 64 terabytes and a 4-gigabyte real address space. For comparison, IBM's latest mainframe architecture, 370/XA, can have virtual address spaces that add up to 128 terabytes and a real address space of 2 gigabytes. The 80286's 1-gigabyte virtual address space is composed of 16,000 segments of 64K bytes each. The 80386's 64-terabyte virtual address space is composed of 16,000 segments of 4 gigabytes each. [*Editor's note: The latest version of the* 80386 *is* B1.]

Virtual memory systems must provide hardware support for the translation of the virtual (or logical) addresses into real (or physical) addresses. During the translation, the hardware must be able to recognize those portions of code and data that are not resident in real memory. Such recognition is commonly called a *fault*. An interrupt must notify the operating system that such portions are needed and must be brought into real memory from the disk (see figure 1).

A virtual memory system must also be able to handle the situation where either the next instruction that is to execute or data that the current instruction needs is not resident. In such cases, the hardware has to fault to the operating system, which then brings in the required code or data. Then the operating system must be able to resume execution of the program at the instruction where the fault occurred without the fault being visible to the program. In other words, the instructions must be *restartable*.

A couple of ways exist to make an instruction restartable. For those instructions that write a single result, you can have the instruction issue all its accesses before it attempts to write the result. For more complex instructions that store multiple results, you have two options. The instruction has to either test all result locations to make sure they are resident before it actually stores to any of them or it must be interruptible: It must save enough state information to be able to resume execution at the point at which it was stopped.

VIRTUAL MEMORY SCHEMES

There are three kinds of virtual memory (VM) schemes. Segmenting schemes break memory into variable-length units called *segments*. Paging schemes divide memory into fixed-length units called *pages*. Finally, the hybrid scheme (like that in the 80386) uses variable-length segments that are divided into pages.

In virtual memory schemes, you have a trade-off between the amount of real memory in the system and the amount of virtual memory that it can support with reasonable performance. Typically, what you need is enough real memory to hold the working sets of a significant fraction of the programs that you want to run. Having less than this amount of real memory causes a tremendous increase in disk I/O due to paging or segment swapping. (Swapping of pages is called *paging*. Bringing something from a disk to real memory is a page-in operation; moving something from real memory to a disk is a page-out operation.) When the system reaches the point where a large amount of its time is spent paging in and paging out instead of executing programs, it is said to be *thrashing*.

The 8086/8088 microprocessors cannot implement virtual memory because they don't have the required address-translation hardware on-chip and they don't support an off-chip memory management unit. The only memory management that they can perform is overlays, which require that the program explicitly manage its own swapping of resident and disk code and data. Almost all big MS-DOS programs use overlays: Lotus 1-2-3 and WordStar are two examples. DOS provides explicit support for overlays via a DOS function call. Overlays have certain disadvantages. First, an individual section of an overlay can be

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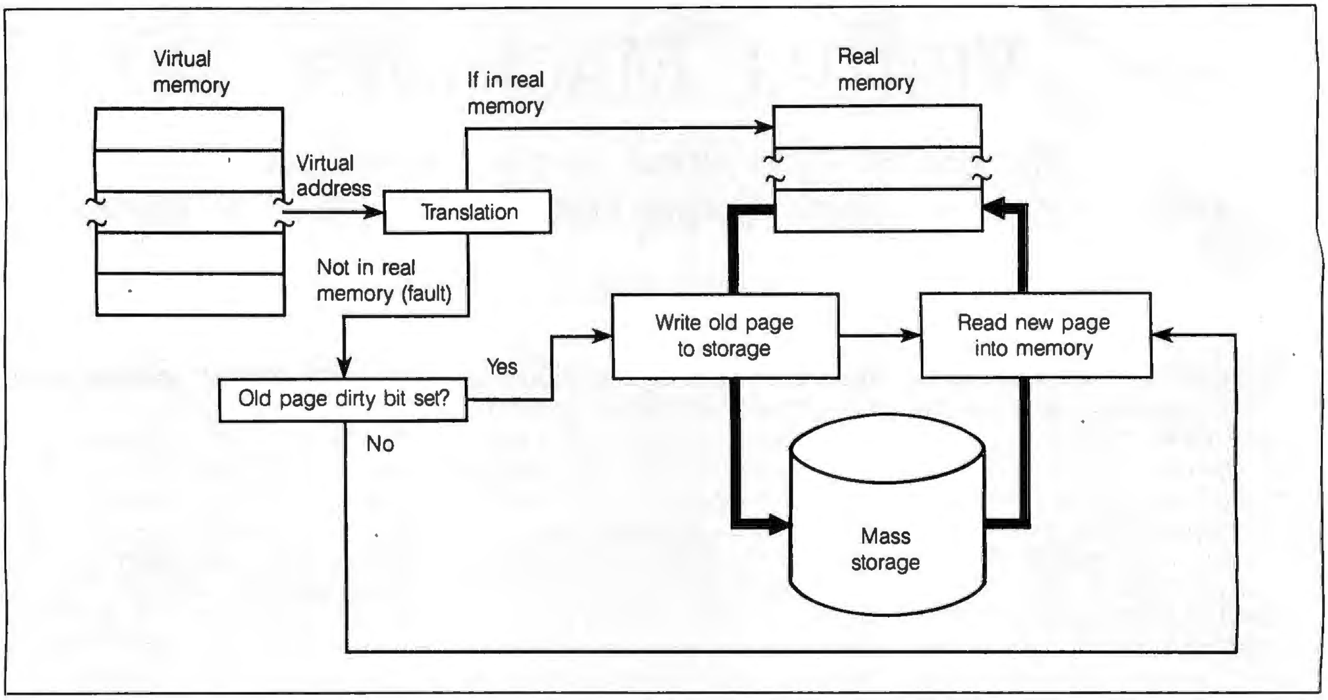


Figure 1: A *virtual memory system.*

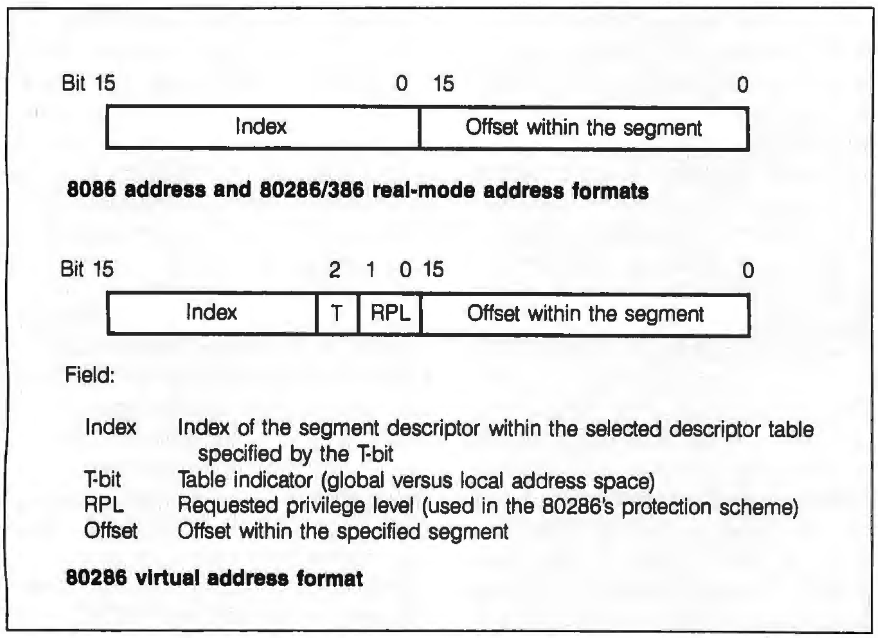


Figure 2: *Addressing formats for* iAPX *microprocessors.*

no larger than some fraction of the available real memory. Second, the programmer is responsible for managing the overlays.

The IBM PC multitasking environments (like TopView, CCP/M, and DESQview) do not fully implement virtual memory in that each program can use only what real memory is available to it. But by using time-slicing and swapping, such systems make memory appear large enough to hold multiple programs. Because the 8086/8088 doesn't provide any memory protection, it is possible for a program to corrupt the operating system or anything else in memory.

The 80286 VM Scheme

One of Intel's major enhancements in defining the 80286 was a protected mode that includes the logic required to implement VM. (From now on, references to the 80286 or the 80386 are to their protected modes.) The virtual addresses in the 80286 are split into two 16-bit segments. The first half is a segment selector that specifies the segment to be used. The other half is the offset within the segment, thus permitting access to any byte within a 64K-byte address space. The format of these two halves is shown in figure 2, along with the 8086/8088 addressing scheme.

Note that the format of an 80286 segment selector differs from that of the 8086. This is the major reason that many programs written for MS-DOS or other 8086 operating systems won't run in 80286 protected mode. The problem is that addresses in protected mode cannot be treated as 32-bit integers because of the T and RPL fields in the segment selector.

The presence of these fields means that the 8086 method of doing simple 32-bit arithmetic for addressing structures bigger than 64K bytes doesn't work in protected mode. A couple of methods that will work are detailed in listing 1. Also note that the 80286's segments—like the 8086's—can be from 1K to 64K bytes long. However, the 8086 segments start on a 16-byte boundary; thus, the segment number can overlap the apparent offset (see figure 3). The 80286's segment numbers do not overlap the offset values, so they appear on 64K-byte boundaries in the virtual address space.

Intel has solved this 8086 addressing compatibility problem in the 80386 by providing an 8086 virtual machine mode that I will discuss in more detail later. In this mode, even though the machine is running in protected mode, the 80386 uses 8086-type selector and addressing.

The 80286 (used in the IBM PC AT and its clones) implements virtual memory at the segment level, that is, by swapping whole segments. Thus, address translation in the 80286 consists of remapping segments from one spot within the virtual address space into another within the real memory (see figure 4). This is done by providing a P-bit (present bit) in the segment descriptor that indicates whether or not the segment is present in real memory. When software attempts to load a segment register with a descriptor whose P-bit is 0, the hardware takes an interrupt of type 11 or, for stacks, interrupt type 12 (see table 1).

This interrupt lets the operating system fault handler load this segment into real memory, possibly overwriting a current segment. If the segment to be overwritten has been modified since being brought in from disk, the operating system will write the modified segment out to disk before overwriting it. Once the required segment has been brought in, the fault handler can return to the interrupted program, letting the program continue operation without knowing anything happened. The instruction pointer that is saved on the stack points to the first byte of the faulted instruction. This facilitates restarting the interrupted program from the fault handler via the IRET (interrupt return) instruction.

THE 80386 VM SCHEME

The 80386 overcomes the addressing compatibility problems between the 80286 and 8086 by implementing both of their addressing modes as well as its own 32-bit native addressing mode. There is no specific 80286 compatibility mode. Instead, each time the 80386 switches between tasks, it specifies the mode of its target program (see figure 5) via the TYPE and D bit fields of the code-segment descriptor. Unlike the method used for 80286 compatibility, 8086 mode is explicitly specified by the VM bit in the processor's FLAGS register.

In addition to the segment-level protection provided by the 80286, the 80386 provides page-level protection when paging is used. Since the 80386 first performs segment translation, followed by page translation, it is possible to have two or more small segments share a single page. In this

(continued)

Listing 1: *Pseudocode example of address arithmetic in 80286 protected mode.*

```
Adding a displacement of 16 bits or less:  (offset in DX, displacement in AX)
    Add new displacement to DX.
    If carry-out then
       Move DS into BX.
       Add '0008'x to BX.     (add 1 to index field)
       Move BX back into DS.

Adding a displacement of more than 16 bits: (offset in DX, displacement in BX:AX)
    Add new displacement to DX.  (DX <- DX + AX)
    Add carry-out to BX.
    Left-shift BX by 3.  (align with index field)
    Move DS into CX.
    Add CX to BX.     (add displacement high to index field)
    Move CX back into DS.

80386 handling of displacements of up to 32 bits
    in native mode: (offset in EDX, displacement in EAX)

    Add EDX, EAX
```

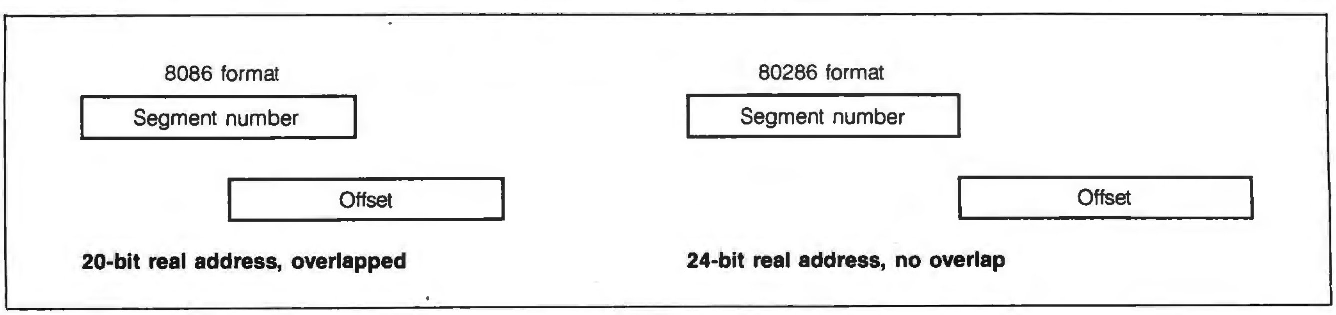


Figure 3: *Differences in address translation between the 8086 and 80286.*

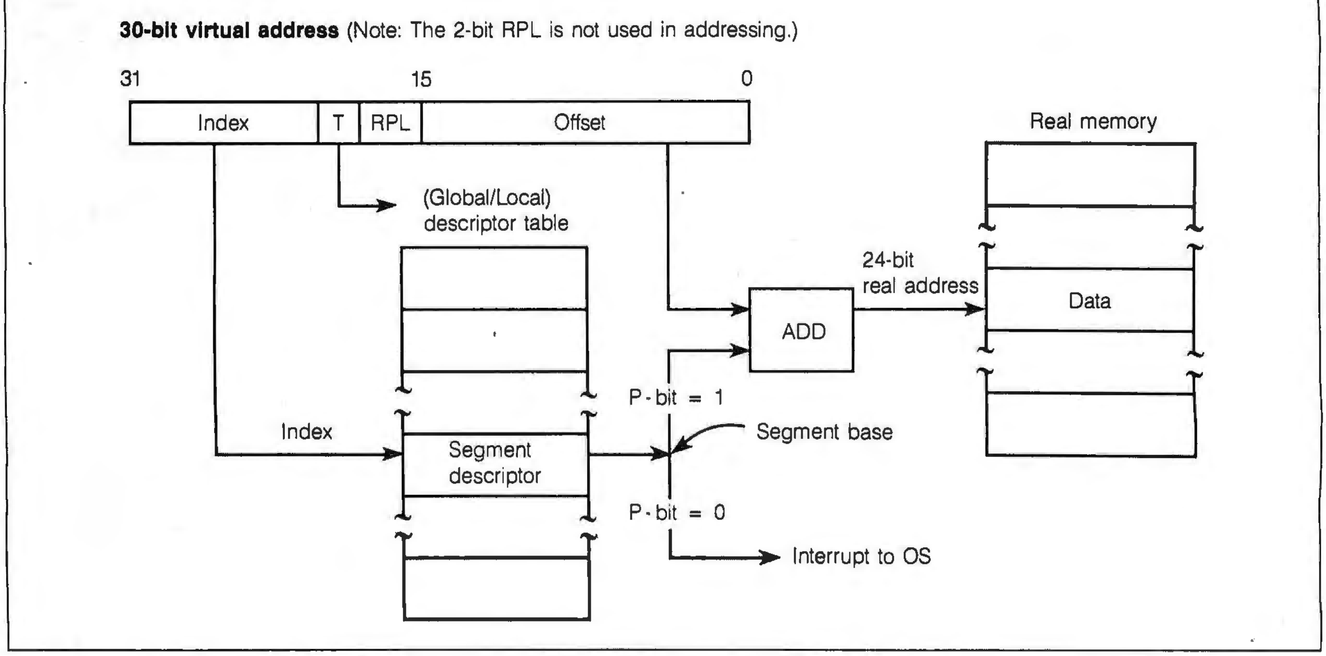


Figure 4: *80286 virtual address translation.*

Table 1: *80386 interrupt vectors.*

Function	Interrupt Number	Instruction That Can Cause Exception	Return Address Points to Faulting Instruction
Divide error	0	DIV, IDIV	Yes
Debug exception	1	Any instruction	Yes
NMI interrupt	2	INT 2 or NMI	No
1-byte interrupt	3	INT	No
Interrupt on overflow	4	INTO	No
Array bounds check	5	BOUND	Yes
Invalid op code	6	Any illegal instruction	Yes
Device not available	7	ESC, WAIT	Yes
Double fault	8	Any instruction that can generate an exception	
Invalid TSS	10	JMP, CALL, IRET, INT	Yes
Segment not present	11	Segment-register instructions	Yes
Stack fault	12	Stack references	Yes
General protection fault	13	Any memory reference	Yes
Page fault	14	Any memory access or code fetch	Yes
Coprocessor error	16	ESC, WAIT	Yes
Intel reserved	17–32		
2-byte interrupt	0–255	INT n	No

case, the page-level protection would not be used. Note that the operating system can still use the paging scheme for memory management; however, care must be taken to ensure that the page is swapped out only when all the segments in the page are not in use.

The 80386 VM scheme implements virtual memory via mainframe-style paging schemes using two-level translation tables. The first level, pointed to by CR3 (control register 3), is the page-directory table containing from 1 to 1024 page-directory entries of 4 bytes each. Each of these PDEs points to a page containing page-table entries of 4 bytes each, for up to 1024 pages. Each PTE contains the address of a 4K-byte block in real memory called a *page frame.* Thus, a PDE points to PTEs describing up to 4 megabytes of real memory. Both the PDT and each page table will not exceed one page (4K bytes) in length and are aligned on page (4K-byte) boundaries. Also, the pointer in CR3 and the pointers within the PDEs and PTEs are real addresses, not virtual addresses. If they were not real addresses, you would run the risk of your page tables being paged out, effectively hanging the system.

Figure 6 shows the format and contents of a PTE. The accessed and dirty bits of a PTE are used for memory management. The OS will use the accessed bit to keep track of how often a program uses a page and the dirty bit to tell whether the page must be copied out to the disk before the new page overwrites it. The standard method of tracking a program's page use is to have the operating system periodically clear the accessed bit of all pages a program has in real memory and then check, after a certain period, which pages have their accessed bits set. This information, collected over a period of time, tells which pages a program is currently using. This set of pages is called the program's *current working set.* Also, a P-bit indicates to the processor whether this page is present in real memory. If the bit is off, the processor takes a page fault to the operating system so

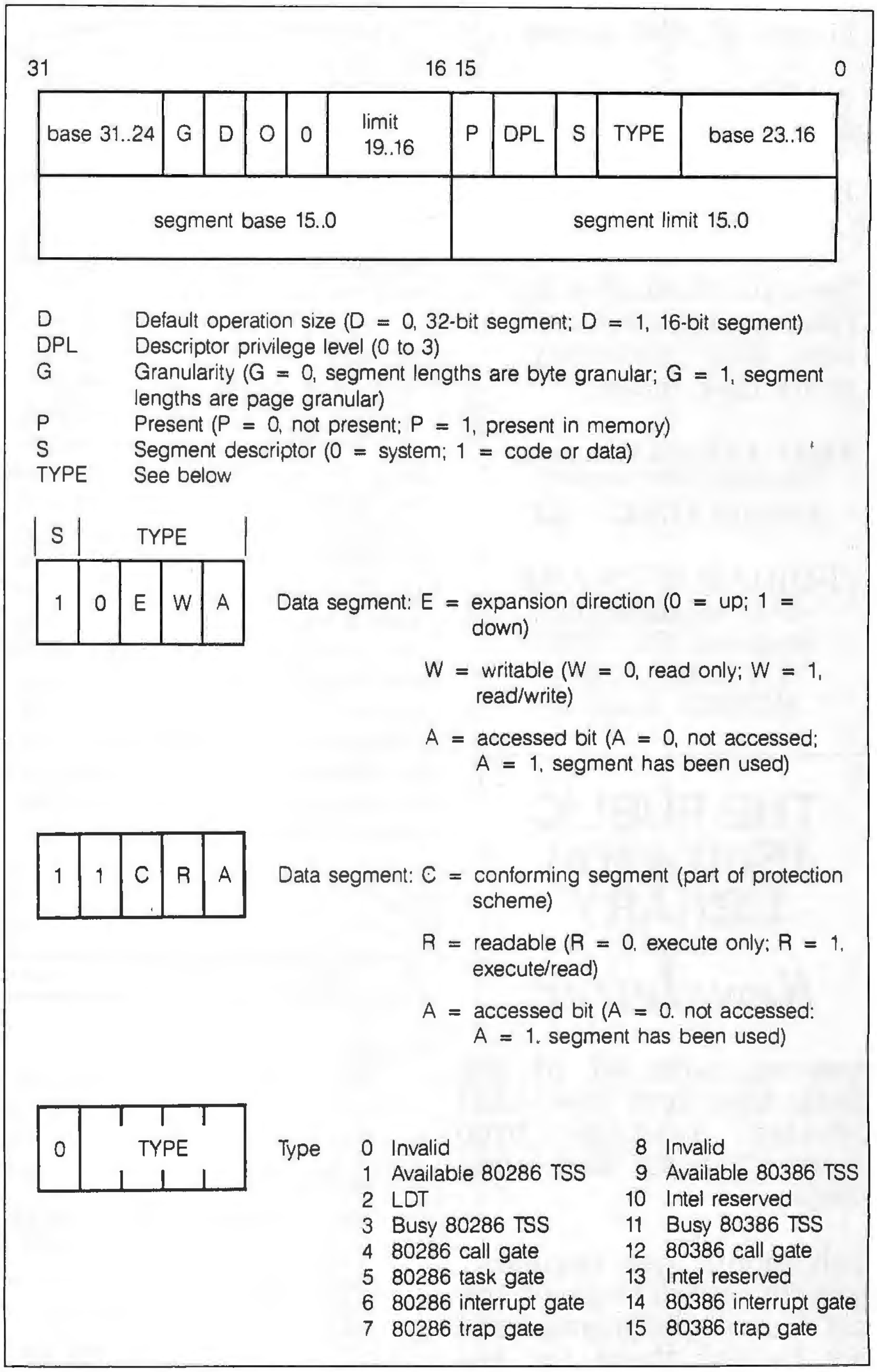


Figure 5: 80286/80386 *segment-descriptor format.*

it can bring in the page from disk. The process of bringing in a page when a program faults on it is called *demand paging.*

The translation of virtual addresses requires two accesses—the first to get the PDE and the second to get the PTE—for each access done by the program. Rather than run at less than one-third of its potential speed, the 80386 uses an on-chip address cache called a translation-lookaside buffer. This cache, unlike a "normal" cache, returns a PTE—instead of a data word—when given an address. The

(continued)

80386 has a 32-entry, four-way set (that is, four sets of eight PTEs each) associative TLB, which should give a hit rate of about 98 percent (see figure 7). In other words, 98 percent of the time the TLB will contain the PTE that you need. The other 2 percent of the time, the processor must actually do the translation and then load the new PTE into the TLB.

The dirty bit indicates that the page has been altered by the processor since being brought into real memory. When a program does a write to memory, the processor sets the dirty bit in the PTE. What actually occurs is that the 80386 sets the real dirty bit on the first write, because a copy of this bit is kept in the TLB. Note that the 80286 segment descriptor doesn't have a hardware dirty bit. The way that an 80286 operating system tells that a segment is dirty is to initially make all the program's segment descriptors write-protected when they are brought in from disk. When the program attempts to write (first time only) to the segment, an exception occurs and the operating system takes control. The operating system sets a software dirty bit, removes the write-protection from the segment, and restarts the task.

Effects of Virtual Memory

For a system based on segment swapping (the 80286), the only requirement is that I/O can't cross a segment boundary. The OS must load the starting real address into the direct-memory-access unit instead of the starting virtual address, unless the DMA unit is capable of handling the translation and knows where the tables are. In either case, the OS must not swap out the segment until I/O finishes. Thus, the operating system must "lock" a segment into memory. A software-only bit in the descriptor is normally used for this purpose.

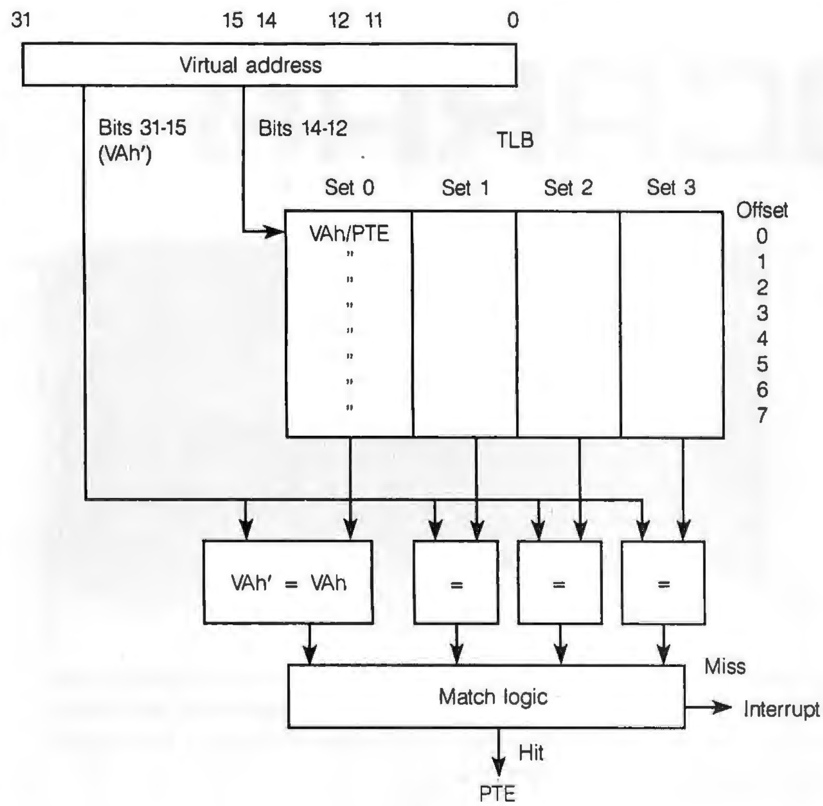
For a paged system, things are further complicated by the fact that a segment can span more than one page. This leads to three possible ways to handle DMA. In the first and simplest (this is the case for PCs so

Bit 31–12	11–9	8	7	6	5	4	3	2	1	0
Page-frame address (PFA)	OS Res	0	0	D	A	0	0	U	R	P

Field:

PFA	Real address bits 31-12. If it's a directory entry, this is the real address of a page frame containing the page table. If it's a page-table entry, this is the address of a page frame for program use.
OS Res	Reserved for operating system use.
D-bit	Dirty page bit. If a 1, the page has been modified; it's set when a write to an address in the page occurs.
A-bit	Accessed bit is set to 1 when any kind of access (read/write/execute) occurs to an address in the page.
U-bit	User access permitted. If a 1, access is permitted by level-3 programs. If a level-3 program attempts to access a page with a U-bit of 0, an exception occurs.
R-bit	Level-3 access control (assuming U-bit is 1). If a 0, only read/execute accesses are allowed; if the R-bit is a 1, writes are also permitted.
P-bit	Present bit. If P=1, page is present in real memory; if P=0, page is swapped out. An interrupt is generated when a program attempts to use this page. If P=0, the rest of the word is undefined from hardware's point of view.

Figure 6: 80386 *page-directory/table-entry format.*



How a TLB works:

Use a portion of the VA, bits 14-12 in this case, as the index into the TLB arrays. Read out one entry per set in the TLB, four entries in this case. The entries that were read out consist of three parts: VA entry, PTE, and control information. Compare the VA in each entry with the VA you are looking up. If any matches, you have your translation (unless control indicates this entry is invalid). Otherwise, signal a TLB miss to the processor so it can get the correct translation.

Figure 7: *Sample diagram for a 32-entry translation-lookaside buffer.*

far), the DMA unit doesn't know about paging and the processor must set up each page transfer separately. In the second way, the DMA unit knows how to handle a string of real addresses and counts that point to each page that I/O is to address and specify the number of bytes to be moved. Finally, the DMA unit itself can use virtual addressing, in which case it must be given a translation table address in addition to a starting address and count. Of course, the pages that I/O will be addressing should be locked.

An 80386 running in 8086 virtual machine mode treats segment descriptors as the 8086 does: They are simple 16-bit integers that are multiplied by 16, then added to the 16-bit offset to get a 20-bit virtual address. Unlike the 8086, the 80386 then performs page translation on the address. Thus, the 1-megabyte address space of an 8086 program is split into 256 4K-byte pages. Using paging to remap the address space permits the sharing of pages that are not written to. This reduces the real memory required to support multiple 8086 virtual machines. Also, the host operating system can use the remapping function to provide page-level protection for the guest operating system.

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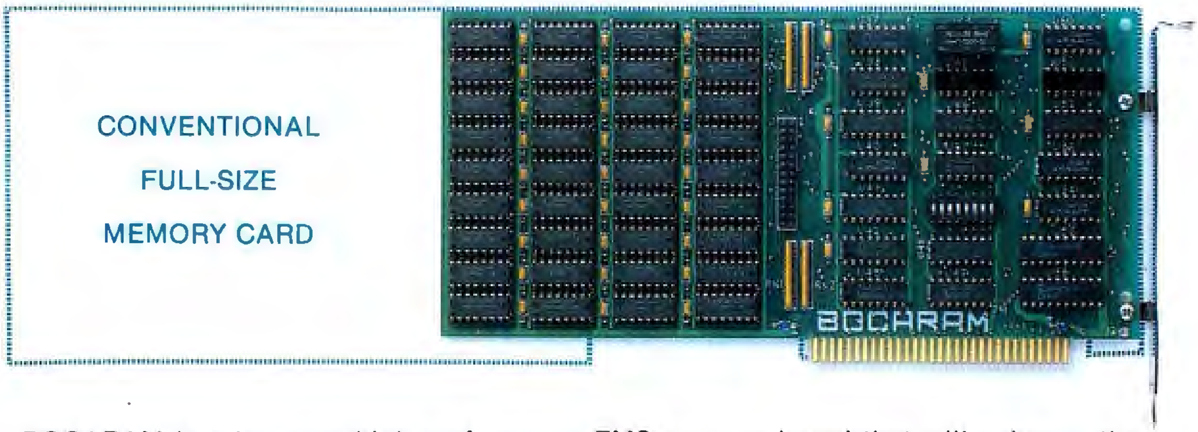

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WHY NO 80386 VIRTUAL MACHINE?

One reason the 80386 cannot "virtualize" itself is the asymmetric behavior in its instruction pairs, such as PUSHF and POPF. PUSHF saves the REAL flag values in protected mode. POPF will not cause a general-protection exception in protected mode. Even if an attempt is made to alter the I/O privilege level or interrupt flag bits without sufficient privilege level, no interrupt will occur for an unauthorized alteration attempt; it is simply ignored.

Consider the attempt to virtualize XENIX-286 under the current 386 architecture. The XENIX kernel may use the POPF instruction to alter the current IF bit. This works in native 286 mode (no VM). Under VM, the hardware will not allow the change, and no notification will occur (via a general-protection exception) that an attempt to alter the IF bit was made. As far as the host CP is concerned, the guest XENIX OS is still able to receive interrupts from the outside. If XENIX is in the middle of altering a critical area where interrupts can't be tolerated (such as stack changes or modifying the global-descriptor table) and the host CP has no way of knowing its guest's state, the interrupt is passed to XENIX at the wrong time, causing the guest to crash.

A similar problem exists with the task-register load and store instructions (LTR/STR). Again, consider the attempt to virtualize XENIX-286. It's normal for XENIX to store its current task register during preparation for a task switch (many operating systems do this). In the current 386 architecture, if XENIX attempted to load the task register, this would cause a GP exception and appropriate simulation by the CP could be done. However, when XENIX stores its task register (which has been virtualized), no GP exception occurs, and the real (CP) task register is stored. If XENIX had stored the TR with a value, say, of 21F (a XENIX task-register value), the LOAD might return a value of 1C (the real CP value). Any internal bookkeeping XENIX was doing that depended on LTR/STR being a matched set is destroyed, and bugs will result.

The final problem with virtualizing the 80386 relates to addressing problems. Part of the difficulty is that the CP must share the same address space with the guest. The other part of this problem deals with interrupts: For a virtual machine interrupt, the address that you transfer to is a virtual address. This causes the following problem when attempting to run an 80386 virtual machine. Say that a guest OS is using linear address 8000000 for some control information. Suppose that the host CP also uses that address for some purpose. Due to the nature of the 80386, the host CP cannot set up the page tables to prevent this, and data is overwritten.

It is even possible to support virtual expanded memory.

VIRTUAL MACHINES

A virtual machine is the extension of the concept of virtual memory to an entire machine, including I/O devices and privilege levels, so that a program can't tell that it doesn't have a real machine—in this case an 8086—to itself. A virtual machine lets multiple operating systems (which may be incompatible) run concurrently with no modification or conflict. A program running in a virtual machine sees whatever memory and I/O the host operating system desires, not the amount of memory in or the I/O devices of the real machine. It is important to note that a virtual machine is not an emulator, nor is a virtual machine as efficient as a real machine.

Why use virtual machines in the first place? Because this permits an 80386 system to run multiple PC-DOS programs unmodified in what appears to be their native environment. Thus, the

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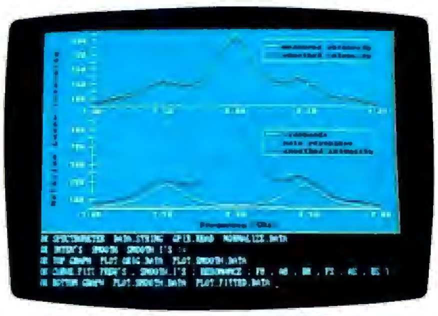

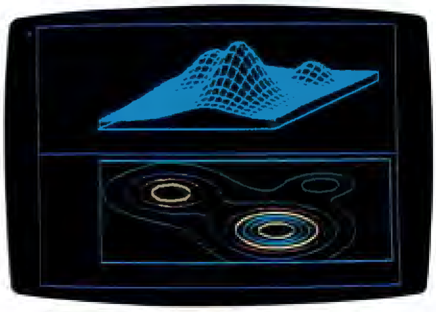

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ASYST is a trademark of Macmillan Software Co. ASYST was developed by Adaptable Laboratories Software, P.O. Box 18448, Rochester, NY 14618 need to modify existing programs so that they run in protected mode is avoided. This ability to run multiple operating systems lets the 80386 run an 8086-type UNIX or CP/M-86 at the same time, in addition to the native-mode user interface.

To support multiple virtual machines, a control program (CP) actually manages the real machine's resources (real memory, I/O, privilege levels). The CP creates and handles multiple virtual machines, distributing the real machine resources in an orderly fashion. The CP is not an operating system: It is a layer of software that mediates requests from the operating system to the hardware.

For a processor to support virtual machines, all instructions that would let a program be able to tell that it is running in user mode must be privileged. Access to some facilities, such as I/O and timers, must be restricted. There must be no possibility of a conflict between a guest address space and the host operating system's address space. This becomes especially evident when you attempt to run a copy of the CP in a virtual machine.

While the current 80386 supports virtual 8086 machines, it does not support virtual 80286 and 80386 machines. This is due to problems in handling the PUSHF and POPF instructions and the store-system-register instructions (STR, SGDT, SLDT, SMSW) and to the fact that the address to which an interrupt transfers control is a virtual address using the local-descriptor tables and global-descriptor tables at the time the interrupt occurred. (For additional information, see the text box "Why No 80386 Virtual Machine?" on page 119.) While the lack of ability to run a virtual machine other than an 8086 is a real limitation, it doesn't seem to be a fatal flaw. Intel might fix this in a later release of the chip.

The 80386 CP invokes an 8086 virtual machine by performing a task switch where a program's task-state segment has the 8086 virtual mode bit (bit 17) set in its copy of the EFLAGS register. Virtual 8086 programs run at the lowest privilege level, so to utilize specific privileged instructions, the I/O permission-level field in the EFLAGS register and the I/O permission bit map (located in the task-state segment) must also be set up. Now any interrupt or exception causes the 80386 to switch back into protected mode (native 80386 mode) before invoking the handler pointed to by the interrupt-descriptor table. Thus, the routines that are invoked must be 80386 native-mode routines. In most cases, these routines will emulate the operation requested by the virtual machine—for example, an OUT instruction—then return to 8086 virtual mode via an IRET instruction.

When the 80386 runs in virtual 8086 mode, it does address generation like an 8086 but the 20-bit address that is produced is a virtual address. The page-translation hardware then translates the virtual address into a page number and a starting offset within that page. This lets the 80386 CP use a page-level protection "below" the guest operating system, so that elements such as ROM can be emulated (just mark the page "read-only"). This same method lets the host share portions of memory between multiple virtual machines. So while the 8086 virtual machine can't use the segment-level protection that is available to both 80286 and 80386 mode programs, the 80386 CP can use protection at the page level to enhance real memory utilization of the guest machines.

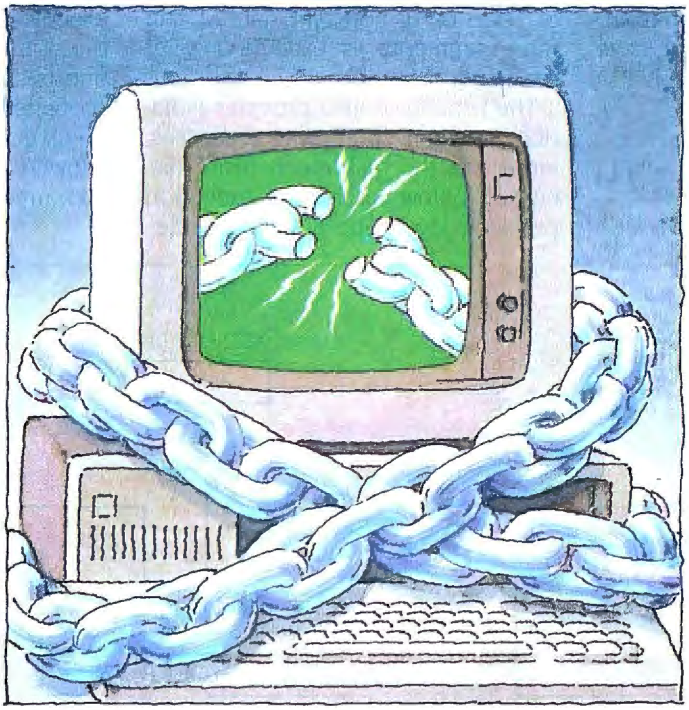
THE WRAP-UP

Virtual memory lets you run a program even if your system doesn't have enough real memory. It also makes multitasking much safer by providing the ability to isolate tasks from one another. The virtual machine mode will protect your investment in 8086 software while providing a relatively painless method of entrance to virtual memory, multitasking, and the 80386 itself. If Intel corrects the inability of the 80386 to "virtualize" itself and the 80286, the same path provided for 8086 software will be available for 80286 software such as XENIX and protected-mode DOS. ■

A PROTECTED-MODE PROGRAM FOR THE PC AT

A program that lets you tap the 80286's power by using its native mode

BY ROSS P. NELSON



THE COMPUTER industry usually ties new-generation hardware to the older hardware by making it compatible with existing software. To take advantage of the machine's newer features, you must write software for its native mode. Such is the case with the IBM PC AT's central processor, the Intel 80286, which runs software written for the 8086/8088 processors.

Due to lack of operating system support, very little software has appeared for the 80286's native mode, called the protected virtual address mode, leaving the processor's power largely untapped in current microcomputer systems. Ironically, applications programs that adhere to a few simple rules will run unmodified in the native mode, but only if you dramatically modify the operating system. I've written a program, PM_AT.EXE, that places an IBM PC AT in its protected mode and provides a base for future expansion and experimentation with the protected mode in the 80286. [*Editor's note*: PM_AT.EXE, PM_AT.ASM (*the source code for* PM_AT.EXE), *and* PROTECT.INC, *a module for the program, are available on disk, in print, and on* BIX. *See the insert card following page* 176 *for details. Listings are also available on* BYTE*net*. *See page* 4.]

PROCESSOR OVERVIEW

In the 8086 emulation mode (which is equivalent to the standard operating modes of the 8088, 8086, 80188, and 80186), the 80286 has one type of system object, the segment. The processor grants access to a segment when a value is loaded into a segment register. The processor then allows direct access to the 64K-byte block of memory beginning at location <value> × 16.

In protected mode, the processor views the system much the same as an operating system would. The processor "knows" about objects other than memory segments. Each object is referenced by a descriptor, which contains information about the object. When the system is in protected mode, the value loaded into the segment register does not point to the object itself, but to a table of descriptors where the object is described. From that table, the physical address and size of the object (assuming it is a memory segment) are extracted. Memory segments can range from 1K to 64K bytes in size, and the processor verifies that every memory access is within the bounds of the segment size (see figure 1).

In addition to segments, the 80286 works with descriptor tables, task segments, and gates. A particular type of descriptor is used to reference each object (see figure 2). The processor uses descriptors to ensure that system security is not violated. To prevent a valuable program from being disassembled, the processor would use an execute-only descriptor for the code segment; any program that tried to read that segment as data would fail.

The 80286 requires two tables of descriptors whenever the system is running in protected mode: the global descriptor table (GDT) and the interrupt descriptor table (IDT). A number of local descriptor tables (LDTs) can also exist. LDTs are associated with the 80286 task implementation. The GDT and LDTs contain descriptors for code and data segments. The IDT is analogous to the 8086 interrupt vector table and contains special code descriptors known as gates.

(continued)

Ross P. Nelson (1821 Ashmeade Ct., San Jose, CA 95125) is a systems programmer.

ILLUSTRATED BY BENJAMIN PEREZ

In 80286 parlance, the 16-bit value loaded into the segment register is called a selector. A selector accesses a system object by selecting the descriptor for the object. A selector has three components: the table indicator (TI), which selects either the GDT or the currently active LDT; the desired descriptor within the table (Index); and a requested privilege level (RPL). Normally, the RPL is the same as the operating privilege of the currently executing code. The 16 bits that are loaded into the segment register have the following format:

```
15 3                2    1 0
-----------------------------
|  INDEX            |TI| RPL|
-----------------------------
TI = 0 / GDT,  TI = 1 / LDT
```

For example, the processor interprets the value 13A1 hexadecimal in a segment register as a request to access descriptor 274 hexadecimal in the GDT with a privilege of 1.

PROTECTION

In protected mode, as the name implies, the 80286 is concerned with system integrity. It makes every effort to ensure that the flow of execution is well behaved. To prevent corruption of code or of constant data, it can mark segments as execute-only or read-only.

The processor also provides isolation between coresident processes, either via the task mechanism (discussed below) or by the execution privilege level. The 80286 provides four levels of security, numbered from 0 (most secure) to 3 (least secure). A program may access any descriptor with a descriptor privilege level that is numerically equal to or higher (less secure) than its own execution level. Typically, operating system code executes at the most privileged levels, and the applications execute at less privileged levels.

This arrangement presents a problem when an application attempts to execute subroutines that are part of the operating system, such as I/O requests. The code segments should be protected from corruption, but less privileged applications should still be allowed access. The 80286 provides two mechanisms to deal with this

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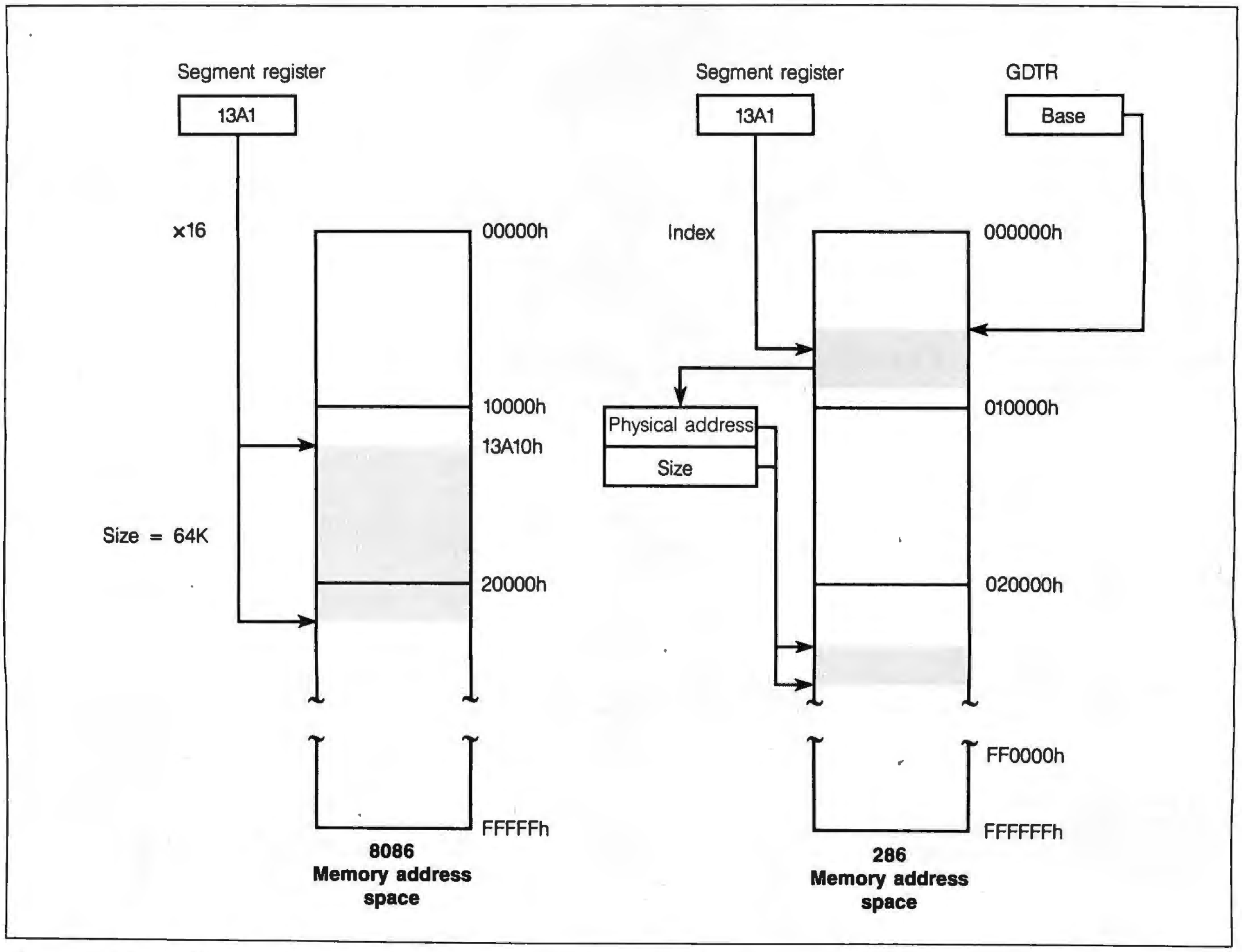

Figure 1: *Direct addressing of real-address mode versus the indirect addressing of protected mode.*

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problem. The first is the conforming code segment, used when the shared code does not need to access restricted elements of the system, such as hardware I/O ports. Libraries of routines that perform data conversion between ASCII and binary or floating-point, for example, could take advantage of conforming segments.

The other mechanism is a descriptor called the gate, which provides a

(continued)

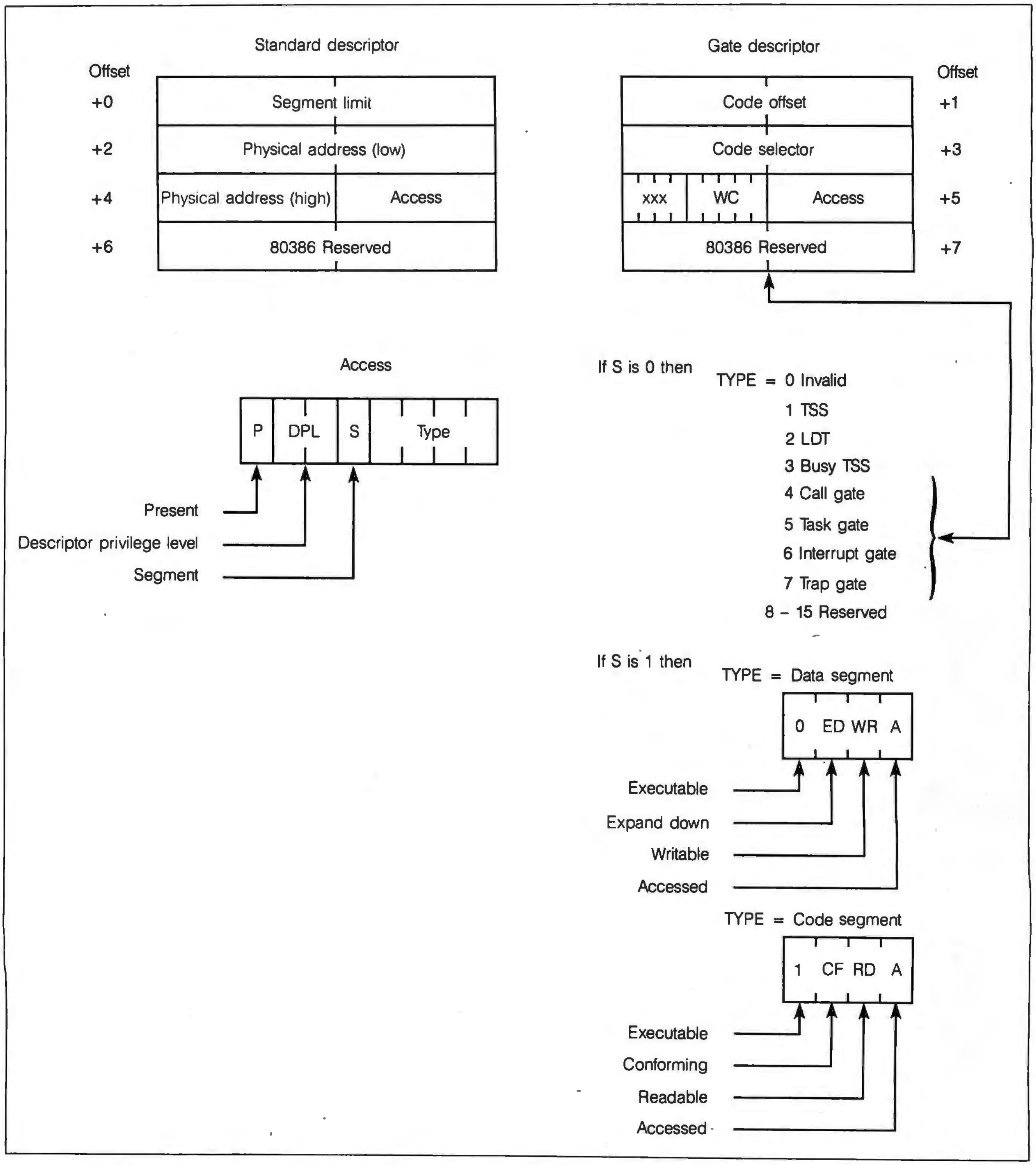

Figure 2: *The format of a descriptor.*

DD: Two *Ctrl* and *Alt* keys for ambidextrous access.
IBM: Same

DD: Positive-tactile, firm-feel keys.
IBM: Same.

DD: 12 *Function* keys for increased automatic operation.
IBM: Same.

DD: Extra-wide, easy-to-find *Return* key.
IBM: Changed sizes again by shrinking their Return key.

DD: Dedicated *Function Control* keys.
IBM: Same.

DD: *Caps, Num* and *Scroll* Lock indicator lights.
IBM: No lights on their XT.

DD: Isolated *Escape* key.
IBM: Same.

DD: Enlarged *Backspace* and *Shift* keys
IBM: Same

DD: Separate dedicated *Numeric Pad* with enlarged *Enter key,* four *Arithmetic Function* keys.
IBM: Same.

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DD: Separate *Cursor* and *Screen Control* keys.
IBM: Same.

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passageway to a more privileged execution level. It does this with an additional level of indirection. A gate has a privilege level that is separate from the privilege level of the code segment to which it points (see figure 3). For example, a call gate that has a descriptor privilege level of 3 could point to a code segment with a descriptor privilege level of 0. This means that any executing code segment could issue a call through the gate because 3 is the least privileged level. Since the gate points to a level-0 segment, the 80286 would change the privilege of the currently executing task to level 0 to match the new segment. Thus, the application runs at a higher privilege level, but only while executing the operating system's secure code. It then returns to its original level after the return instruction.

The 80286 architecture also provides interrupt and trap gates for handling hardware and software interrupts.

The notion of a task is built into the 80286 architecture. Loosely defined, a task is a set of segments required to perform a particular series of operations. The 80286 creates this union of segments with the help of two descriptors, the task-state segment and the LDT.

It is often helpful to think of tasks as separate programs executing on their own individual microprocessors. The task-state segment provides a good simulation of this notion, since each task-state segment holds a copy of all the machine registers used by the task. Because in most cases a single processor handles all the tasks in a system, the operating system switches between the tasks, executing one for a period of time, then another. In this way, a multitasking system appears to be running many programs concurrently. When a task-switch operation is performed on the 80286, the current values of all the registers are stored in the task-state segment of the executing segment; the registers are then loaded from the task-state segment of a new task, which begins execution based on the new value of the instruction pointer.

The segment descriptors in the task's LDT are available only to that task; another task cannot access them. This isolation provides an excellent form of protection.

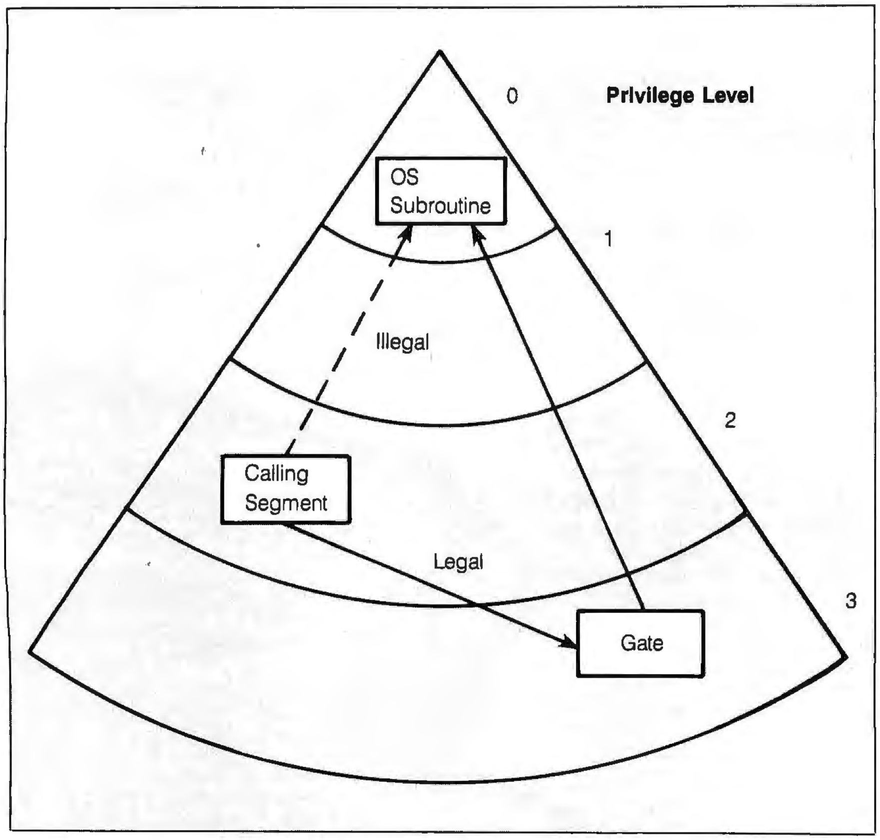

Figure 3: *A call gate that has a descriptor privilege level of 3 but points to a code segment with a descriptor privilege level of 0.*

THE PROTECTED-MODE PROGRAM

My program, PM_AT, places the IBM PC AT into protected mode and provides support scaffolding for further experimentation with protected mode. The program illustrates various features of the 80286's native mode and includes examples of fault handlers, conforming code segments, gates, and task switching.

I wrote the program using the IBM Macro Assembler version 2.0. Since this product was designed for the 8086 family of processors, it does not support some features of protected mode. In some cases, I have resorted to programming tricks to provide a reasonable approximation of the missing features.

The PROTECT.INC listing contains a set of macros that let the user assemble 80286 protected-mode instructions. The 80286's instruction set contains two kinds of enhancements over the 8086 family: the addition of new instructions such as PUSH <data> and ENTER, and the protected-mode instruction set. The IBM Macro Assembler version 2.0 supports the first group of new instructions but not the second. When you include PROTECT.INC, macros simulate the unsupported op codes such as LGDT and ARPL.

TABLES

Three macros help build the descriptor tables. Each segment in the program is defined with either a memory-segment (MSEG) or a system-segment (SSEG) macro. These two macros

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create assembler variables that contain information necessary for building a descriptor. A third macro, the descriptor (DSCRP) macro, builds a descriptor from the variables when given the name of a segment. The DSCRP macro also accepts an optional export name that is used as a selector for the descriptor. This trick works because the format of a level-0 GDT selector is equivalent to the index multiplied by eight. Since each descriptor takes up 8 bytes, the byte offset of the descriptor equals the index times eight.

The GDT begins with the line

```
DESCRIP <0, 0, 0, 0>
```

which builds the first GDT entry via the DESCRIP data structure. The system can never access descriptor 0 in the GDT; therefore, it is null. Descriptors 1 through 7 are set up to meet the requirements of the INT 15h function call. Descriptor 8 provides a task-state segment for the initialization code. The INT 15h protocol does not require the creation of a task, but a task fault will occur at the first task switch if the task register has not been loaded.

The next four descriptors are for the portion of code that I call the MiniBIOS. The MiniBIOS handles the hardware interrupts and provides screen-handling routines similar to those normally found in the standard ROM BIOS; however, the ROM functions will not execute correctly when the processor is in protected mode. When you invoke the MiniBIOS functions (via a trap gate at INT 30h), the privilege of the executing task is set to 0 for the duration of the function.

The next nine descriptors point to the fault handlers I have implemented. As you add new code to the system, it is inevitable that at some point a routine will fail. The handlers that are a part of PM__AT will indicate the type of fault and the location in the program where the fault occurred. The descriptors provide code, data, and task segments for the fault-handling code. The last of these descriptors is initially unused but available for the fault-handling routines to modify as needed.

The next two descriptors provide access to a library of ASCII/binary-conversion routines. The first descriptor, shlib__code, is a level-0 conforming code segment. Programs with a lower privilege can gain access to this code via the CALL__ GATE descriptor, which has a privilege level of 3. Since the code segment is conforming, the privilege of the calling task does not change when executing the code in shlib__ code.

The next descriptors provide the system-level descriptors for a second task to illustrate the 80286's task-switching capabilities.

(continued)

The final four descriptors are null and are available for future expansion. Normally, an operating system will provide functions such as CREATE_TASK, ALLOC_SEGMENT, and FREE_SEGMENT, which create new descriptors or free up entries in the GDT for later use. The operating system would have access to the GDT as if it were a standard data segment (via descriptor 1). Obviously, this sort of access to the GDT must be limited to only the most secure portions of the operating system.

The GDT requires the physical starting address of the segment as a part of segment descriptors. The assembler places the 16-bit (real address mode) segment address in the prototype GDT. A subroutine in the program's initialization portion adjusts all the addresses, multiplying them by 16. It assumes all data resides in the first 1 megabyte of memory.

The IDT contains a set of gates that point to the routines that handle interrupts and faults. It contains only trap, interrupt, or task gates. Trap gates handle software-interrupt requests, and interrupt gates handle hardware interrupts. You can invoke a task gate by hardware or software; it causes an immediate task switch.

As defined under DOS, the interrupt structure of the PC AT resembles that of the standard PC or XT. Unfortunately, IBM chose to use some of the interrupts that Intel designated as reserved. In the AT, this causes a conflict between the way DOS wants to use the interrupts and the way the processor wants to use them. In my program, I followed the Intel specification and allocated the first 32 interrupts for exceptions and fault handling, mapping the hardware interrupts to vectors 32 (20 hexadecimal) and above (see table 1).

Descriptors 0 through 31 handle processor faults. All these gates are interrupt gates except for 8, 10, and 12, which are task gates. Task gates are required because the failures that cause these interrupts are so serious that the processor must load an entirely new machine state to continue running.

Table 1: *The interrupt vector mapping used in* PM_AT *contrasted with* DOS.

Vector	Function	DOS Equivalent
00	Divide fault	0
01	Trap (single step)	1
02	NMI	2
03	BRKPT (INT 3)	3
04	Interrupt on overflow	4
05	Bound interrupt	
07	80287 not available	
08	Double fault	
09	80287 segment overrun	
10	Invalid TSS fault	
11	Not present fault	
12	Stack fault	
13	General protection fault	
16	80287 error	
17 . . . 31	Reserved	
32	Timer	08
33	Keyboard interrupt	09
35	Com port 1	11
36	Com port 2	12
37	Printer 2	13
38	Floppy disk	14
39	Printer 1	15
40	Real-time clock	
45	80287 request	
46	Hard disk	

The hardware interrupts are found at vectors 20 to 2F hexadecimal. The change from the DOS vector locations is accomplished by programming the 8259A interrupt controller. In the PC AT, the BIOS call INT 15h takes care of this detail.

Interrupt vectors 30 and 31 hexadecimal have been allocated to the MiniBIOS. Since INT 30h provides display services, its privilege level is set to 3 so that any task may request its services.

The last page of the program contains an LDT for the second task. The code and data segments for the second task are in the LDT rather than the GDT. When an LDT is used for each task, the GDT will contain only a task-state segment and an LDT descriptor for the task. The descriptors for the code and data segments need not appear in the GDT.

INITIALIZATION

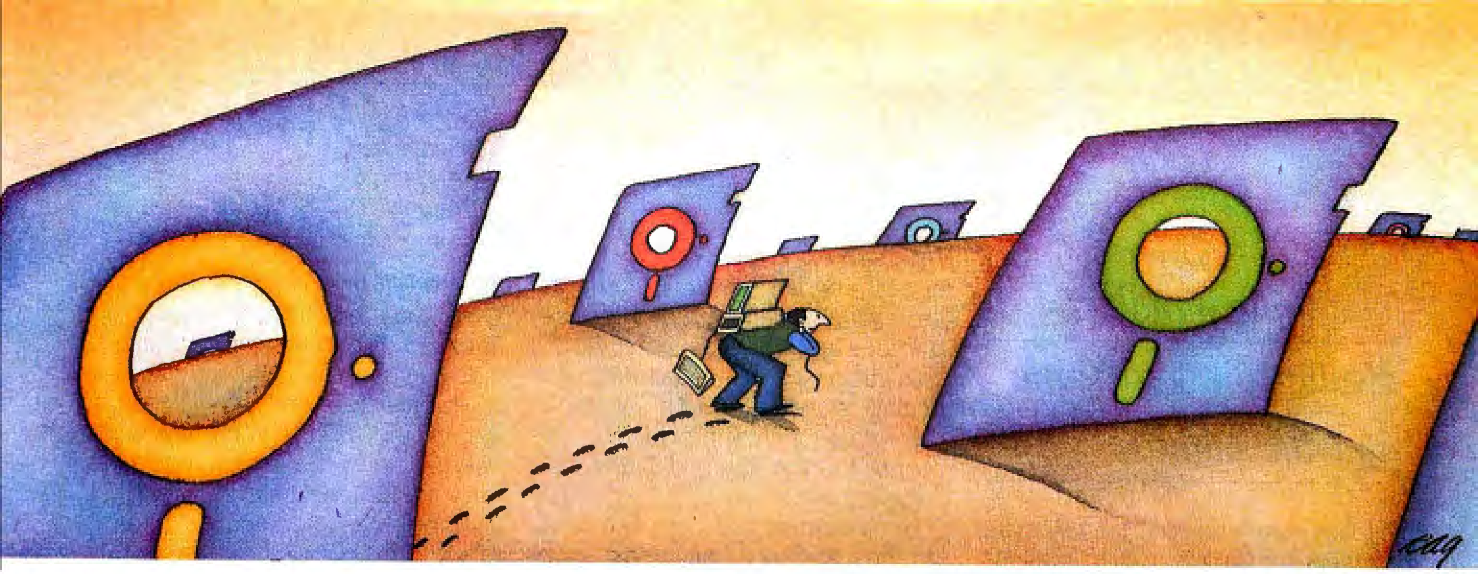
After MS-DOS loads PM_AT, execution begins at the label START. The program then calls the subroutine ADJUST_ADDR to fix up the physical addresses in the GDT and LDT, converting them from 16-bit real address mode segments to 24-bit physical addresses. It then calls the ROM BIOS to request protected mode.

The PC AT BIOS provides a function (code 89 hexadecimal of INT 15h) that places the processor into protected mode. To do this, it loads the GDT and IDT base registers, programs the 8259A interrupt controller with the hardware vector locations, and frees up the A20 address bit. (Due to a design oversight at Intel, the 80286 occasionally generates addresses beyond 1 megabyte. The PC AT includes hardware to force the A20 bit to 0 while running in emulation mode.) It then sets the protected-mode bit in the machine status word (MSW) register of the processor and returns to the calling program.

PROTECTED-MODE EXECUTION

The only setup required after the program returns from the INT 15h call is

(continued)



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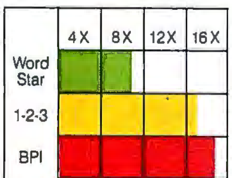

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The fault handlers display the fault type and the address.

to load the task register. The task-state segment for the initial task contains no data but must be present for a task switch to occur.

Program execution is very simple. The program beeps once to let you know all is well, clears the interrupt-register masks, enables interrupts, and goes into a loop. The main task prints the number of clock ticks that have occurred since interrupts were enabled. It then invokes a second task, which merely displays a message and returns. The program loops until you generate a keyboard interrupt; it will then halt and reset the system.

The second task runs at privilege level 3, the way most applications would in a standard operating system. Its execution privilege level is determined by the privilege of its code-segment descriptor found in the task's LDT. When it invokes the display services via INT 30h, however, its execution privilege is changed to level 0 for the duration of the call. To prevent an errant program from corrupting the local variables and return addresses of the level-0 code, the 80286 changes to a level-0 stack before it begins level-0 execution. A level-0 memory segment is provided for this purpose in the task's LDT and task-state segment.

The executing tasks use two small libraries of code. One is the set of routines that does ASCII/binary conversion. They are located in a conforming code segment, and any task can call them via the CALL_EX macro. This macro takes an export name and a privilege level and creates a FAR call to the object. It can be used with any export segment or gate. The other set of routines provides display services and is part of the Mini-BIOS. Since these routines require access to hardware, they will execute at privilege level 0 and are invoked via the gate at interrupt 30h.

The ASCII/binary-conversion library is located in the shlib_code segment. This library provides the following 16-bit conversion functions: ASCII hexadecimal to binary, binary to ASCII hexadecimal, ASCII signed integer to binary, binary to ASCII signed integer, ASCII unsigned integer to binary, and binary to ASCII unsigned integer. The actual calling sequences are documented in the code.

PM_AT provides a set of rudimentary display utilities for character and line output and cursor manipulation. These are invoked via the trap gate at INT 30h. The current implementation of the program supports only the IBM monochrome display. To support the color adapter, you replace the DEV_MONO literal with DEV_COLOR. To prevent snow on the display, a color implementation should also loop and wait for a retrace before writing any characters to the display.

Fault Handlers

If you use this program as a basis for your own experiments with protected mode, the fault handlers are important. Whenever the 80286 detects a violation of its protection rules, it issues an interrupt that will vector through the IDT to the appropriate fault-handling routine. My fault handlers display the fault type and the address of the instruction that caused the fault. They will also display the fault code for the "general protection" fault and other faults that provide an error code. The format of the address is <selector>:<offset>. You will have to extract the selector's index

(continued)

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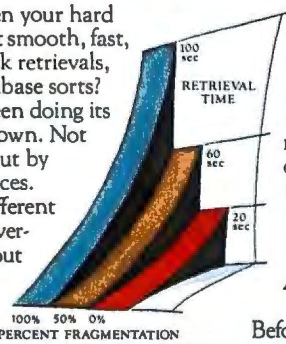

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portion to determine which code segment was executing when the fault occurred.

In a complete operating system, the different faults would be handled differently. For example, the "not present" fault (INT 11h) would probably cause the operating system to load the referenced segment from virtual memory and restart the instruction that caused the fault; the "general protection" fault (INT 13h) would normally cause termination of the offending task and the logging of a message to the appropriate terminal.

My program assumes that any fault is a programmer error. It will display the location and type of fault on the display, pause, and reboot the system. Should you attempt to make the fault handlers more sophisticated, you might run across two other conditions: double fault and shutdown. Double fault (INT 8) occurs when the system is attempting to process a fault but is prevented from doing so by another protection violation. The double-fault handler, therefore, should be an isolated task that makes as few assumptions as possible. Should the processor detect another violation while attempting to handle the double-fault condition, it will give up entirely and shut down. The PC AT includes hardware that detects the shutdown status on the bus and resets the processor.

SUGGESTIONS FOR EXPANSION

To understand all the complex interactions of the protected mode, you will almost certainly need Intel's *iAPX 286 Programmer's Reference Manual.* This manual includes a pseudocode description of the processor microcode for instructions such as INT or CALL FAR. Unfortunately, in the latest edition (1985), some of the steps are missing. However, after you've worked with the processor for a while, you should get a feel for the types of operations being carried out.

The next logical step in developing the code is adding a keyboard driver. After you get this working, you will have a small interactive system to build on and could add a debugger/monitor. This would let you recover more gracefully from certain errors rather than reset the system.

The complexity of the native-mode 80286 is an order of magnitude greater than that of the previous generation of microprocessors. But as powerful support for secure multitasking operating systems, it will be much appreciated by designers of the next generation of operating systems. ■

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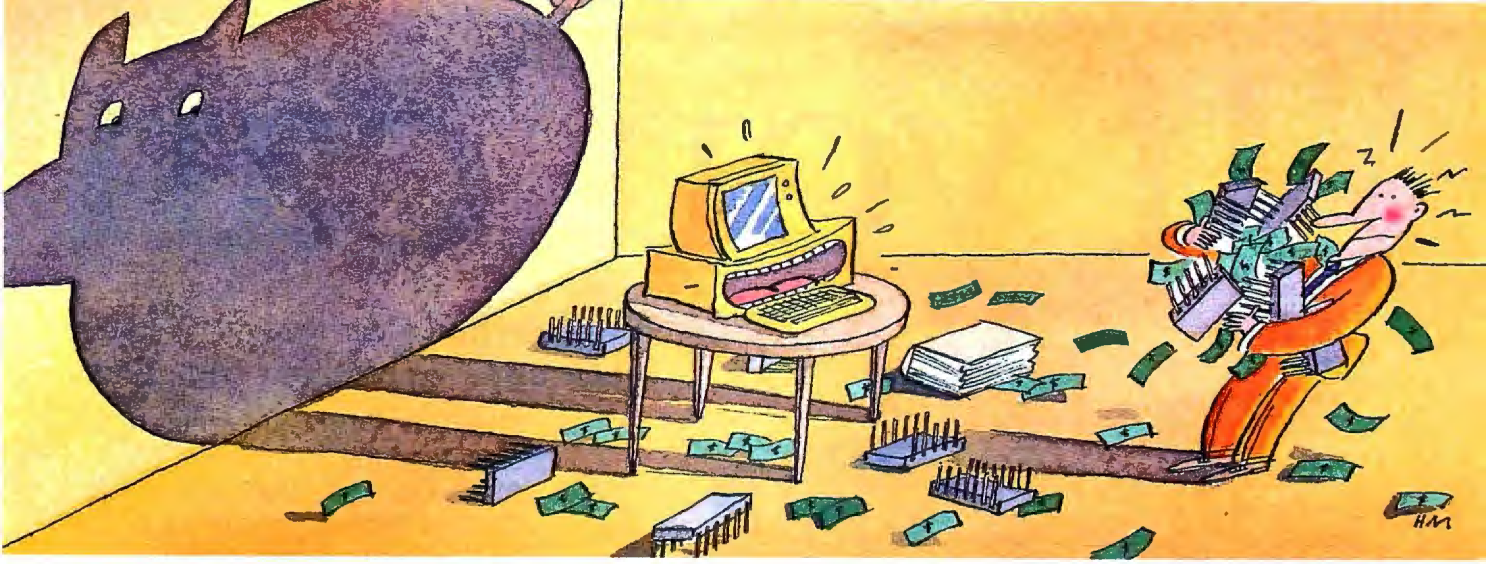

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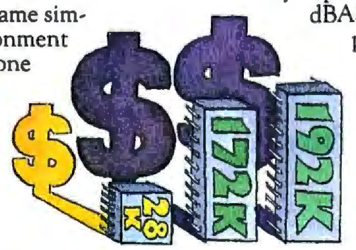

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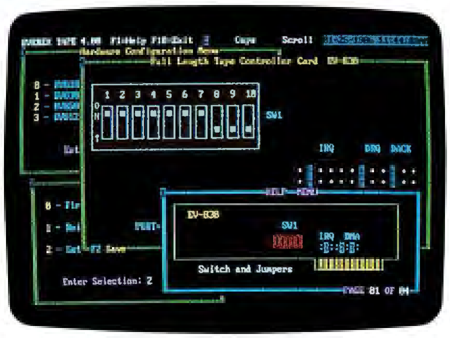

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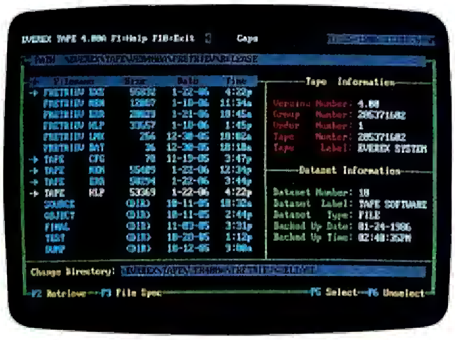

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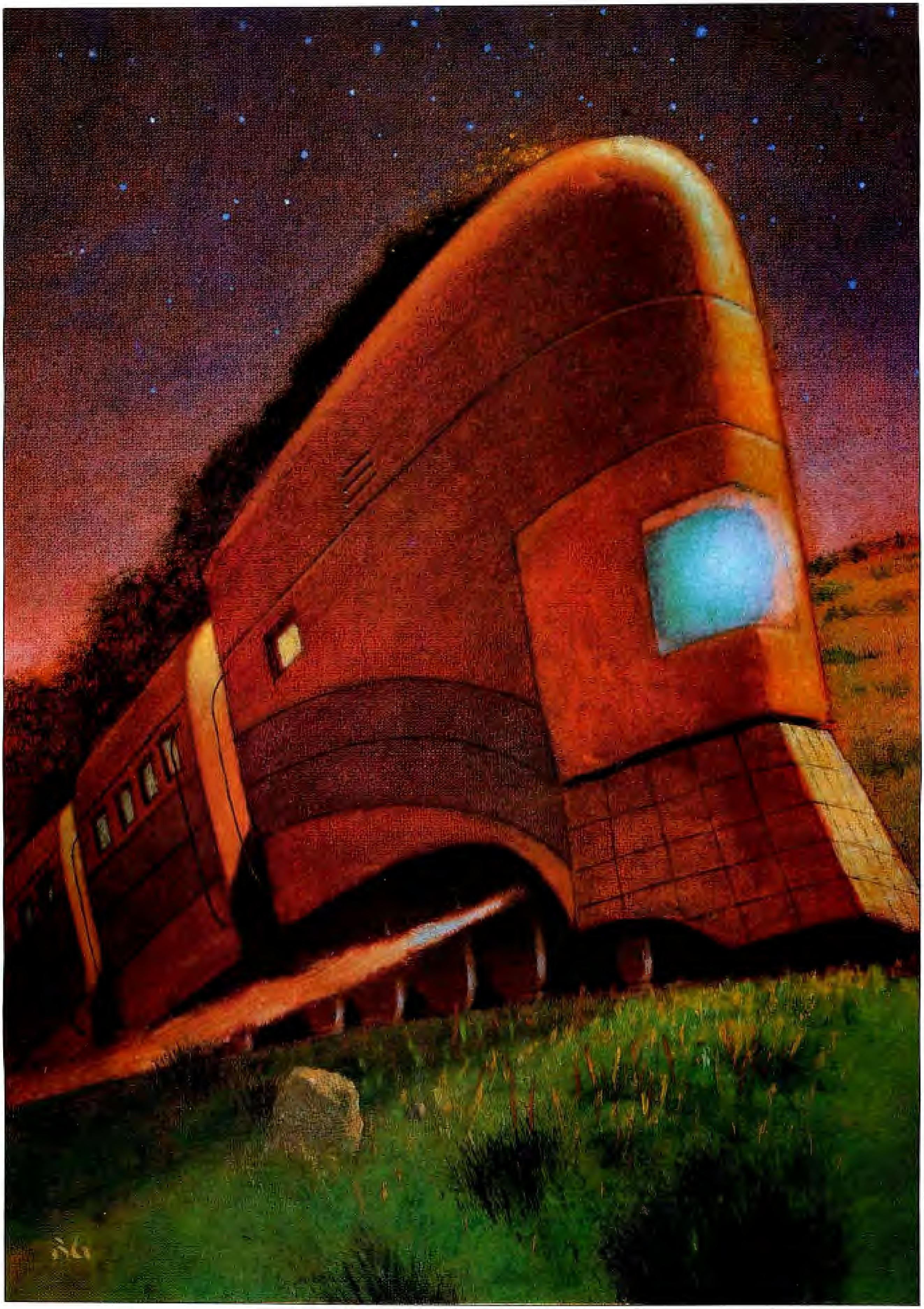

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IBM PC ACCELERATORS

The theory of operation of three kinds of speedup boards for PCs

BY STEPHEN S. FRIED

EXPANSION BOARDS are available that can speed up your IBM PC or XT. These accelerator boards cost from $149 to $2000 and can result in increased system throughput of 50 to 350 percent (i.e., system speedups of 1.5 to 4.5 times). Some accelerators claim to be better than this, but, for average programs, a speedup factor of 4.5 is the best that can be expected with the average IBM PC. Since a number of accelerators convert your machine into a device that performs as well as or better than the AT, I have included the AT in this article for comparison purposes. Also, the AT has the advantage of running at a number of different speeds. However, in many ways, accelerators are clearly superior to the AT. For example, many of them will be more compatible with your existing hardware and software than the AT, many have faster numerics than the AT, and most eliminate the need to upgrade to 16-bit expansion boards.

Unfortunately, deciding which accelerator to buy can be difficult. For the most part, you must make the decision on your own or with the advice of a friend who has already made such a purchase. Accelerator technology is over the heads of most retailers and does not help them sell new machines. Speeding up an existing machine can involve the use of motherboard boosters, coprocessor accelerators, or emulator accelerators with or without cached memory.

This article will clarify how accelerators work, help you understand how to compare accelerator speed and compatibility, and give you an idea about what type of accelerator does or does not suit your needs. I'll start off with an intuitive discussion of what an IBM PC–compatible accelerator is, followed by a description of the system constraints within which any accelerator must work and of the three classes of accelerators in today's market.

WHAT IS AN ACCELERATOR?

An IBM PC–compatible accelerator is a hardware product that runs at least MS-DOS applications faster than your original IBM PC. Some, but not all, accelerators will run other operating systems and applications that use the hardware directly. I have already suggested that at least two classes of accelerators exist: those that run MS-DOS only and those that run all PC applications. I will show that there are actually three classes and that the division is dictated by the hardware interface between the CPU on the accelerator and the PC's motherboard.

To perform in the total system environment, the accelerator must provide some mechanism for the CPU on the accelerator to communicate and manage its own devices and those on the system board. These devices include memory on the accelerator, motherboard, or in the I/O channel; the DMA controller on the motherboard; and cards in the I/O channel, such as hard disk controllers and graphics adapters.

The typical accelerator contains a clear dichotomy: Most accelerators speed up because they have internal 16-bit data buses instead of the 8-bit bus that is standard on the PC. This means that the accelerator must be able to operate in two modes: 16-bit and 8-bit. For the devices on the motherboard or in the I/O channel to function properly, the accelerator's CPU must access them in a manner that makes the motherboard think they are being controlled by an 8088 running at 4.77 MHz. Three approaches will placate the motherboard: leaving an 8088 behind to manage the motherboard, emulating the 8088 with a faster CPU on the accelerator, or ignoring the rules and speeding up the motherboard in the hope that your motherboard is much better than the one IBM designed in 1981. I will refer to these three approaches as coprocessing, emulating, and motherboard boosting.

COMPATIBILITY

Compatibility is a more important issue than speed, and I will treat it first. The accelerator that runs 99 percent of your software three times faster will always be a better buy than the accelerator that runs 85 percent of your software four times faster. This is because the cost of a system's software is often much greater than the cost of the hardware and often cannot be replaced at a reasonable price. Having made a large investment in software that works, people are normally reluctant to sacrifice an old machine for a newer one unless the newer one will run the installed software base.

An accelerator can attempt to achieve four levels of compatibility: source code level, operating system level, object code level, and PC hardware level. The first two levels, source

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and operating system, normally go together and do not require a particular hardware configuration to achieve. For example, it is easy to port UNIX applications written in C among different processors that run UNIX. As a result, many of the minicomputer vendors who have mature products that run under UNIX have chosen coprocessor boards that run UNIX (better than the 80286) for their ports to the PC market. This strategy is probably based as much on greed as speed, since the code that runs on these boards is worthless without the hardware and the vendors don't sell you their personalized accelerator without the software. As another example, in the early days of the PC, I easily ported applications written in Microsoft BASIC that ran on my TRS-80 over to my PC. While this definitely increased the speed of my applications, I could not move all of them because many of the best were written in assembly language.

To run programs written in assembly language, an accelerator has to use a CPU that is object-level-compatible with the original used in the PC. It turns out that it is possible to translate 8080 (Z80 is a superset of the 8080) assembly code to run on the 8088, but it is not possible to run 8080 object code on an 8088 (the machine-level encoding of the instructions is different). The object-level differences between the 8088 and the 8080, 6502, and 68000 have spawned a market for coprocessor boards that run your old programs on your new machine. For an accelerator to run 8088 code, it must contain an object-level-compatible (or machine-level-compatible) processor. Examples of processors that are object-level upward-compatible with the 8088 include the Intel 80186, 8086, 80286, and 80386, and the NEC V20 and V30.

The NEC V20 and V30 can switch back into modes that can also run Z80 object code. Had they appeared in 1981, they could have changed the course of microcomputer history and extended the economic life cycle of CP/M-80. The 80386 does some similar tricks within the Intel family. Like the 80286, the 80386 boots up in an 8086 object-compatible mode called real address mode. Unlike the 80286, it can switch over to a virtual 8086 mode in which it can run one or more 8088 or 8086 programs that have their own private virtual address space. However, in its pure 32-bit mode, the 80386 is not object-compatible with the 8088. This feature indicates recognition of the importance of object-level upward compatibility from the microprocessor vendors themselves. As VLSI designs get more dense, it becomes possible to guarantee the future suc-

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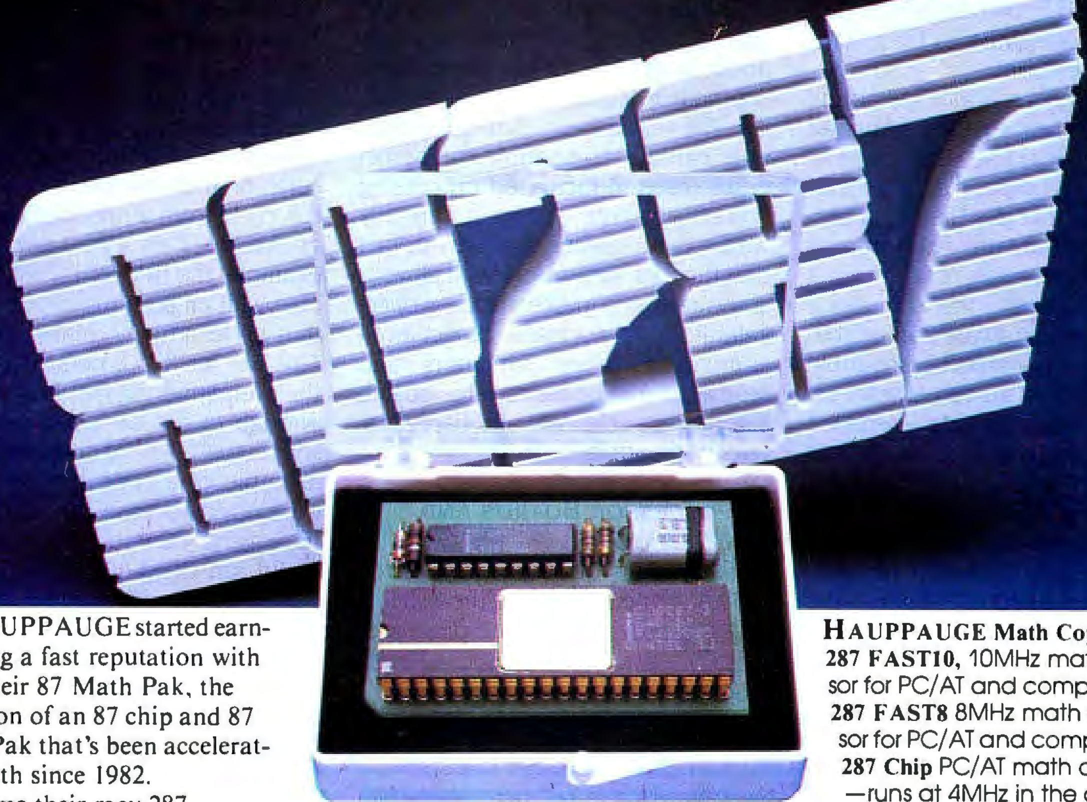

cess of new products by incorporating older designs as subsets. Thus, an activity that used to be relegated to the OEM is now relegated to the microprocessor merchant.

Object-level compatibility is not all that is needed to guarantee that all programs will work. Accelerators exist that are object-compatible but will not run programs that use the PC's hardware directly; they are not compatible at the PC-hardware level. From a practical viewpoint, the difference between a PC-hardware-compatible accelerator and an object-compatible accelerator is that an object-level accelerator will run any well-behaved MS-DOS application, while a PC-hardware-compatible accelerator will run any operating system or application that controls the hardware in the machine directly. Clearly, the PC-hardware level of compatibility is the ultimate and will run the broadest range of your existing applications.

Because there are special situations where object-level compatibility can have big payoffs, I must be cautious about simply blacklisting object-level-compatible accelerators as incompatible. The very aspects that make them only partially compatible can sometimes result in increased processing power. However, you must carefully weigh this increase against the fact that they will never work with all your software. The coprocessor class of accelerators is normally object-level-compatible, while emulators and motherboard boosters are object-level-compatible *and* PC-hardware-level-compatible.

Coprocessor Boards and Accelerators

The first class of accelerators is the oldest. Its members leave the 8088 intact and provide a second processor on an expansion card that fits into the I/O channel. Because those accelerators have two active processors, they occasionally exhibit some parallel execution or coprocessing, hence the name. "Co" can also imply that either processor can control the system bus.

Coprocessors don't necessarily accelerate; their most common job is to run code from a previous generation of machines on a new machine. For example, the IBM RT PC will be available with an 80286 coprocessor card that will let it run normal PC programs. This will let RT owners break out of their engineering applications long enough to run off a few worksheets with Lotus 1-2-3, for example. Another example of a coprocessor that was developed to ease the transition to the original PC is the Baby Blue, which could run CP/M-80 programs.

Today the most popular PC copro-

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cessor products are those that let alternate sophisticated operating systems and processors run in the AT. The operating system that drives most of these coprocessor boards is UNIX, and the processors of choice for this job include the IBM 370 on a board, the Motorola 68000/68020, and the National Semiconductor 32032. The key to three of these coprocessor boards is that they let minicomputer software developers move their UNIX applications to the AT. At a recent CAD/CAE show, I saw at least five $30,000 electronic-design packages, each of which ran on the AT and came with its own $6000 accelerator. While some argument can be made that the C implementations on some of the minis are more powerful than those available on a PC, I don't think the work involved in porting these applications to UNIX on the coprocessor boards was much more involved than a C port straight to an AT.

When a coprocessor board uses a processor that is object-level-compatible with the 8088, I call it a coprocessor accelerator. This type of accelerator offers two advantages over a conventional PC. First, the boards have two processors; the original 8088 stays in place to handle I/O tasks, while the on-board coprocessor is available for CPU-bound tasks. Because the 8088 is not removed, a coprocessor accelerator is slightly easier to install than an emulator. Second, since the I/O interface between the CPU on the accelerator and the 8088 is nonstandard, the cards will usually work only with MS-DOS–compatible software that does not use the hardware directly. Since your nonstandard architecture is going to force you to write an operating-system-interface layer, it pays to add other nonstandard features such as increased system memory. I am not familiar with all the benefits of all the boards on the market, but these nonstandard benefits appear to include increases in DOS memory and the ability to run several coprocessor cards in the same PC.

Faster I/O is not usually a result of installing a coprocessor accelerator. I/O ought to be faster in this type of accelerator and is when the bottleneck in an application is the time spent by the operating system handling I/O calls. However, this is rarely the case. Operating systems such as MS-DOS spend a small proportion of their time in the OS as opposed to the hardware driver. On the other hand, sophisticated multiuser and real-time operating systems often bog down in the layers of the OS. Unfortunately, these operating systems rarely run on coprocessor accelerators, so this

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benefit is not realized in practice. The usual reason that I/O is slow is slow I/O devices. I will show this in the benchmarks, where the range in I/O throughput varies over a factor of 60 to 1 in going from RAM disks to floppies.

When really fast I/O devices are used, coprocessors lose ground with respect to emulators. This is the result of the fact that they use the relatively slow 8088 for I/O, whereas the emulator uses its on-board 8086 or 80286 for I/O. A novel installation I was involved in recently used an emulator accelerator to speed up motherboard I/O by effectively replacing a PC's 8088 with an 8086. It also used an Orchid Turbo board with an 80186 that accelerates CPU-intensive activities. While this installation worked, I am not convinced that the combination is any better than a straight 8086 board running with a RAM BIOS that speeds up the ROM I/O routines by moving them to 16-bit RAM. A simple analysis of the situation reveals that, since MS-DOS is single-threaded, there would be no parallel processing of I/O with CPU-bound activities. Consequently, the two boards would alternate back and forth, and the total time to do a job would be the sum of the time taken by each board. Since the 9.54-MHz 8086 board has a higher throughput than the 8-MHz 80186 on the Orchid Turbo, my guess is that an 8086 board by itself would have run as fast or faster than the combined installation.

The main benefit of coprocessor accelerators, the possibility of achieving concurrent I/O, is also their biggest drawback. The key to leaving the 8088 behind on the system board is a software layer that translates calls that would normally go to the ROM BIOS into commands that now have to be shipped to the system board's 8088. As long as you are running MS-DOS applications that avoid direct manipulation of the hardware, all is fine. However, any time an application or new operating system attempts to directly control the hardware, a problem arises: The coprocessor board has a different architecture than the original machine and responds differently to hardware commands. Operating systems such as XENIX, RTOS, UCSD p-System, and Concurrent DOS, and operating environments such as Window, DESQview, DoubleDOS, and GEM are all examples of programs that have to directly control the hardware and will not work with a coprocessor unless the interface layer between the board and the 8088 is rewritten for each application. Reworking this interface turns out to be an incredibly expensive task and is the reason why popular coprocessor boards such as the Orchid Turbo, Pfaster-286, and

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PCelevator work only with MS-DOS and applications that avoid controlling the hardware.

EMULATOR ACCELERATORS

The second class of accelerators requires that you remove the 8088 on your motherboard using a simple tool and replace it with a 40-pin plug that is connected to the accelerator, which you then install in the I/O channel. This type of board normally includes a 16-bit CPU and the circuitry required to let the 16-bit CPU mimic the 8088 using the 40-lead ribbon cable that plugs into the 8088 socket. Since this process is usually called processor emulation, I refer to this class as emulator accelerators.

There are at least three types of emulators on the market. These can be distinguished by the type of memory that resides on the accelerator and include no memory, 16-bit cached memory, and 16-bit true memory. Cards are available that provide a combination of cache and pure memory. From the viewpoint of speed, the more pure memory a board has, the faster it will run. Whatever type of memory is used, the processor on an emulator has to be an 8088 object-compatible (8088, 8086, 80186, 80286, V20, or V30) device that is capable of running at a clock speed greater than 4.77 MHz.

The classic emulator accelerator gets most of its speed by the increase in data-bus bandwidth between the CPU and the memory resident on the accelerator. Simply stated, the 8086 is hooked directly to a 16-bit memory bank on the accelerator via a 16-bit data bus. This bus is twice as wide as the 8-bit data bus on the motherboard and is running at twice the clock speed. Multiplying the increase in width (two) by the increase in frequency (two) gives a data-bus bandwidth increase of four.

Unfortunately, the accelerator has to communicate occasionally with the motherboard through the 40-lead cable that plugs into the 8088 socket. All communication with the motherboard requires that the 8086's 16-bit

(continued)

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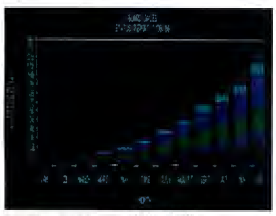

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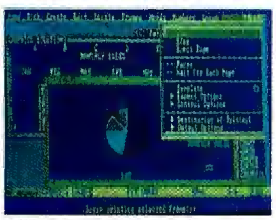

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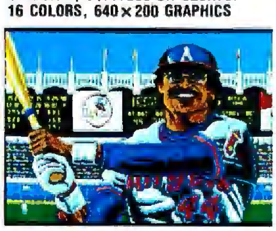

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Inquiry 25

requests be converted into two 8-bit requests to the motherboard. This is done by a combination of buffers and latches—controlled by the main accelerator logic—that idles the 8086 for sixteen 9.54-MHz clock cycles while it generates two 8-cycle I/O requests to the motherboard. These requests are synchronized with the PC 4.77-MHz clock, which interprets them as two normal 4-cycle requests. The control circuit must also generate 8088 status signals whose job is to keep the PC motherboard asleep during 9.54-MHz operation and turn it on during emulation cycles.

All normal I/O cycles need servicing and include memory reads and writes, I/O reads and writes (to ports), and DMA requests made by the DMA controller on the PC's motherboard. DMA requests can be complicated. You can't boot a PC unless it has memory on its motherboard, so you have to leave some memory in the PC's motherboard. Also, the DMA controller on the motherboard will see this memory in the normal course of events. This brings up an interesting situation.

What happens if the DMA controller does a read of memory in the case where that memory resides both on the motherboard and on the accelerator? The answer is that, unless both the 8- and 16-bit memories contain the same information, there will be a battle over the bus and the board that has the stronger drivers will win. Two techniques exist for eliminating this conflict. Whenever you write to an address that is populated on the motherboard and the accelerator, you do a simultaneous write to both. This will result in a small reduction in speed for programs that write frequently to low memory; you can almost eliminate it if you limit low memory to 64K bytes or fill it up with a utility such as a RAM disk.

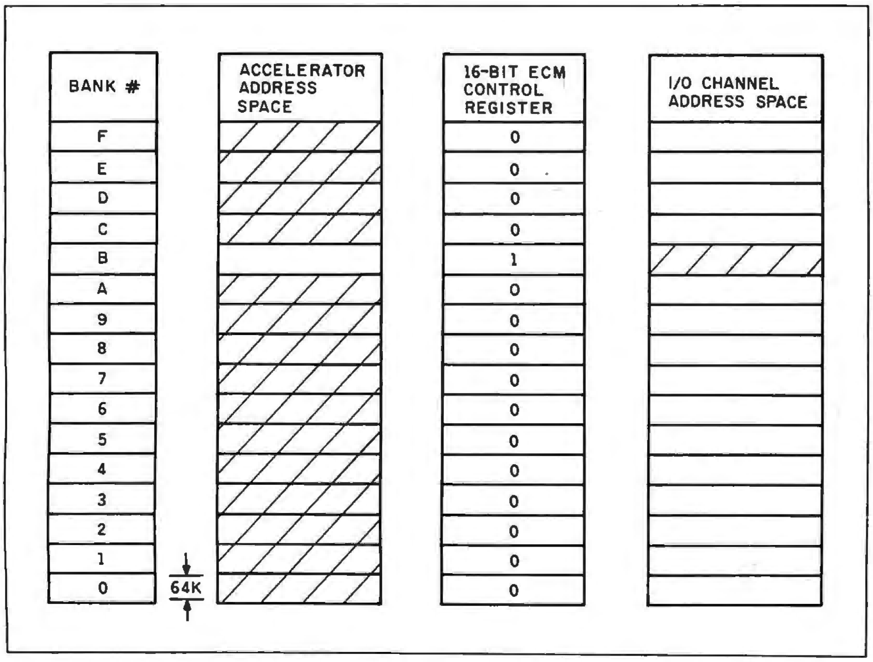

Figure 1: *Extended Conventional Memory uses a 16-bit register to partition the 8086's address space from that of the I/O channel. Each register bit controls whether a corresponding 64K-byte bank of the address space is on board the accelerator or in the I/O channel. The register in this figure shows the state of the machine when a 1-megabyte DOS partition has been interrupted to read or write to a graphics adapter that is addressed through bank B. If an Enhanced Graphics Adapter were being written to, the driver would have to switch both banks A and B. (The cross-hatched areas indicate currently active banks.)*

The other solution is to duplicate the four DMA high address bit registers that the PC has on its motherboard with a similar set of registers on the accelerator and then write a phony value into the registers on the motherboard that points to an address for which the motherboard has no RAM. Without proper DMA control, neither your floppies nor your hard disk will work. If the emulator accelerator you purchase does not have a DMA test program, you could be asking for trouble. Make sure you test system DMA if possible and, if you cannot, start off with floppies only or back up your hard disk.

Whenever the speedup board reads or writes to the motherboard or I/O channel, the data-bus bandwidth falls back to that of the PC's original 8088. However, in most programs the number of emulation cycles that have to be run is very small. To help reduce this count, many emulators have a feature that maps the highest 64K-byte bank of memory on the board into bank F of the 8086 address space. After this is done, a software routine moves the contents of the motherboard ROMs to RAM. This typically results in a factor of three speed increase in interpreted BASIC programs and some I/O, especially screen I/O. Of course, this technique also reduces the amount of 16-bit memory available for DOS from 640K to 576K bytes, but it is usually worth it. In cases where memory is dear, it is possible to place a bank on another board in the I/O channel or buy an emulator that can be populated over 640K bytes.

Figure 1 shows the memory-mapping scheme for a 1-megabyte accelerator that I designed. This board uses a 16-bit register to control how memory is mapped. When a bit in the register is on, the corresponding bank will reside on the 8-bit side of the machine. When a bit is off, the bank is on the accelerator. For example, if all the bits are off, all the memory in the system is on the accelerator.

This brings up an intriguing question: What prevents this system from

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running with a DOS that has 1 megabyte available to it? The answer is: not very much. The key is a little software routine that traps screen I/O requests to the ROM BIOS and swaps the graphics-adapter memory in and out as needed (i.e., turns on bank B by writing to the memory-control register with bit B set on). You also must change the value of the DOS memory size byte (in low memory) and then call for reboot with INT 19h. I make this sound a little easier than it is. You also have to worry about resizing DOS back to 640K or 704K bytes, moving hard disk drivers out of the way, overwriting BASIC, and so on. However, all these problems are surmountable and result in a DOS that has 1016K bytes available to it. In fact, the only memory not available is the 8K bytes taken up by the ROM BIOS in high memory.

I call this technique Extended Conventional Memory (ECM). (Figure 2 shows the block diagram of an accelerator incorporating ECM.) It works well with applications generated by existing FORTRAN, BASIC, and C compilers that do not address the screen directly (i.e., that use DOS or INT 10h). Since most applications compiled by end users fall into this category, this board is a useful partial solution to the memory squeeze play. However, ECM will work only with applications like Lotus 1-2-3 and large memories if the screen drivers are modified to swap bank B before and after every screen operation. In the case of Lotus 1-2-3 and most products that have separate screen drivers, this job is not a big one. Fortunately, if a product does not work with ECM and it does not pay to patch it, you can

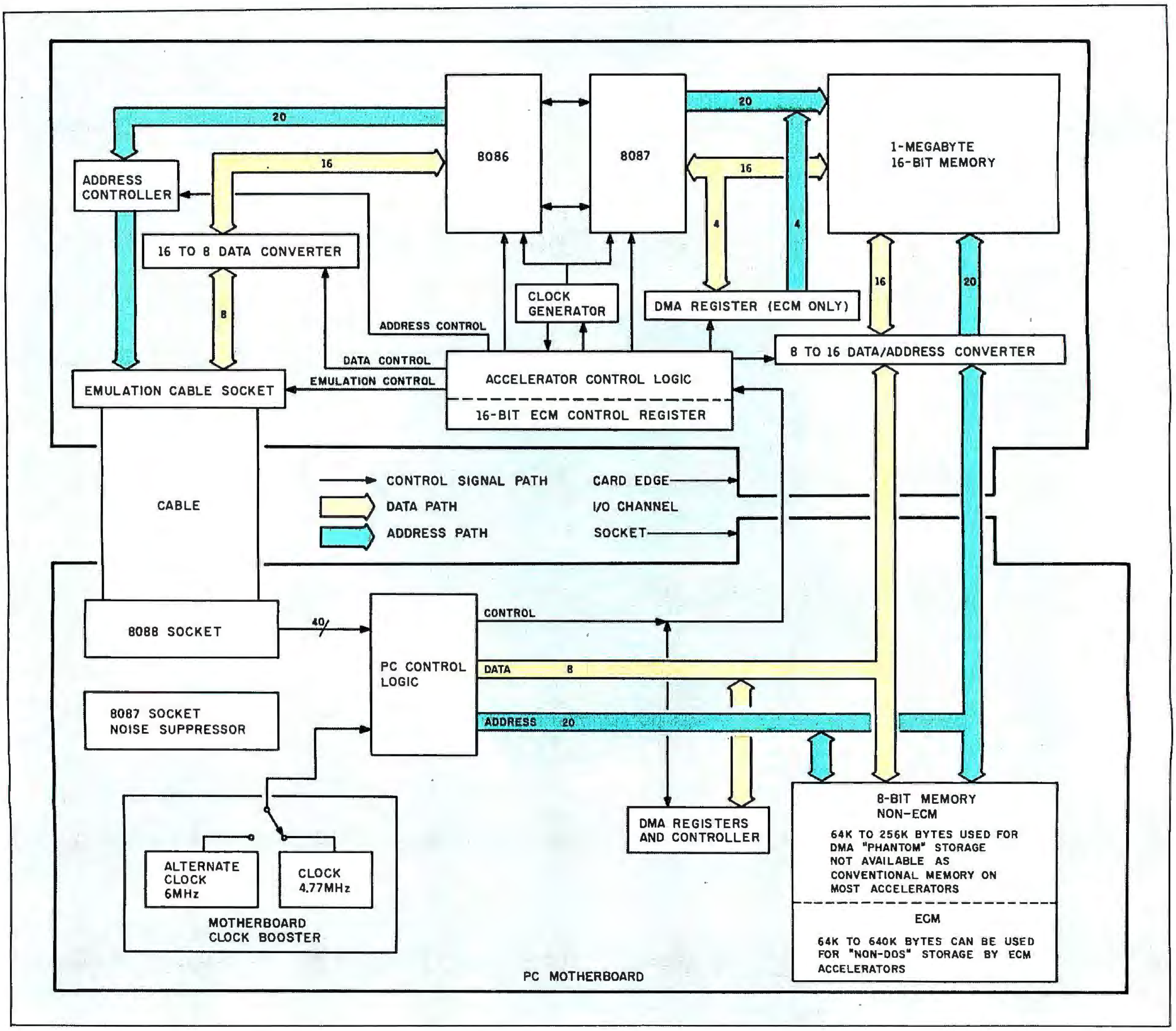

Figure 2: *The block diagram for an accelerator board design incorporating the Extended Conventional Memory scheme.*

always reboot the board to a 640K- or 704K-byte machine. The memory-control register also makes it possible to use the memory on your motherboard and in your I/O channel for I/O utilities such as RAM disks, print spoolers, and disk caches.

Another popular form of emulator uses cached memory instead of real memory. Cached memory is composed of fast static RAMs and is usually small. The theory behind cached memory is to save money on fast RAM by using a small, very high speed cache for tight program loops. In normal practice, this means placing a small cache inside the processor itself. For normal accelerators, there is no cost issue involved in buying faster RAM. The same 150-nanosecond devices that work on your motherboard at 4.77-MHz work fine on a 9.54-MHz 16-bit accelerator.

What is the issue then? First, duplicating existing RAM. Some people like to think that the 256K to 640K bytes that they paid dearly for two years ago is still worth something. The second issue is space. It is possible to build a half-size accelerator without going to semicustom chips if you use a cache instead of true RAM. As an advocate of true RAM, I believe that having all your memory set up as 16 bits instead of 8 guarantees that all CPU operations speed up at a reasonable incremental cost. The 36 chips that make up a megabyte these days cost about $80 as compared with six 55-ns static RAMs that cost $42. The other benefit of a megabyte of RAM on an accelerator is that you can do other things with it, like ECM.

I will now examine how cache is used in an emulator. The theory is simple: Well-written programs spend 90 percent of their time in 10 percent of the code. If this code is mostly in a small fast memory that has to be updated only when you pass out of the hot code (the 10 percent that runs the most), you have a cost-effective way of building a system that minimizes the use of expensive fast RAM. The 90 percent/10 percent principle for programs reads a little differently at the machine level. What typically happens is that a small number of routines that are several hundred bytes long become the hot areas. The key to designing a cache is to figure out where these areas are, keep them in the cache, and go to slower system memory only when other information needs to enter the processor.

This is easier said than done. In practice, you don't examine a program to decide what to cache and what not, but you build a machine that automatically brings information into the cache whenever it is needed but is not already in the cache. In this way, the sections of a program that are hot will end up in the cache because they repeat (i.e., if the cache is long enough, they will still be in the cache from the previous access).

Caching is accomplished via elegant schemes, one of which is called a write-through cache. An 8K-byte write-through cache is composed of three parts: a linear array of static RAM that is organized as 4096 sixteen-bit words, 4096 tag bytes, and logic that is capable of comparing the tag bytes with the address bus to determine whether the cache contains the data of interest. The entire 1-megabyte address space of the processor is mapped onto this 8K-byte area using a simple technique.

When the 16-bit processor on the accelerator accesses a word, the lowest 12 bits are used to index into the tag array, and the 8-bit value of the tag is then compared against the highest 8 bits on the address bus. A match means that the 16 bits of data in the cache at the index location are valid and the processor is passed these bytes. This is called a cache hit. If the tag does not agree with the address bus, the value in the cache is incorrect and that causes an 8088-emulation cycle that reads 16 bits of data from the motherboard. When this information comes up, it is simultaneously read into the processor and the cache, and the tag for the address in question is changed. Any write from the processor to memory automatically writes to both the cache and the motherboard; this is the write-through. In this scheme, the data-bus bandwidth between the processor and cache memory is 100 percent for repeat reads of the cache. Memory reads that miss the cache and writes run at the speed of the 8088.

For the 7.2-MHz 80286 cache board used in the benchmarks, the data-bus bandwidth between the processor and the cache was 6 times that of the 8088 in a PC. Assuming that the cache were to be hit 5/6 of the time (82 percent), this would result in an overall bandwidth that was three times that of a PC. Simply stated, the misses that happen 1/6 of the time take as long to execute as the hits, since the misses run 6 times slower. This doubles the execution time, which effectively halves the data-bus bandwidth. As I will show below, the cache's no-wait-state memory is so fast that it is mostly wasted. Only about 5 percent of the instructions in a no-wait 80286 system are limited by the data bus, while nearly 66 percent are limited in a one-wait-state 80286 or 8086 system. What this means is that the high-speed data-bus bandwidth is less than 6.0, which implies that programs that hit only 82 percent of the time speed up less than 3 to 1.

The final emulator-type accelerator has no memory on it at all. The idea is simple: Increase the speed of register instructions only. This type of device is best described as an 8087 accelerator, as the 8087 is the only component that spends many more cycles on the average executing than it does reading the bus. These devices involve little logic and a small increase in speed; they plug directly into the 8088 only.

Most emulators are PC-hardware-compatible. The main compatibility problems are the result of hardware that is being driven with software that contains timing loops. For these devices, it is necessary to either slow the board up or patch the drivers. The other problem is software that knows it is on a PC and can't find an 8087 (because the system has an 80287) but knows the 8087 toggle is set to on. The best example of this problem was an early version of the Intel

(continued)

Above Board that did not take kindly to 80287s on accelerators in PCs. Another incompatible accelerator is the ECM. As long as it is running in the ECM mode, it works with all software that obeys the rules IBM set down with PC-DOS. When an application disobeys those rules, the board must be reset with software to the 640K bytes that most software expects. Clearly, it helps to have a firm grounding in the operation of both PCs and DOS to overcome the challenges that running at high speed produces.

MOTHERBOARD ACCELERATORS

The third class of accelerators is the simplest. Its members provide an alternate clock frequency for the 8088 on your motherboard (or your AT), upgrade the 8088 to an 8088-2 or NEC V20, or do both. Lately, this group of products has become more sophisticated. One product lets you control the processor's speed by a switch and software, while another inserts wait states during I/O cycles, thus discriminating between I/O cycles and internal CPU cycles. Without wait states, it is possible to run some motherboards up to 8 MHz.

The motherboard boosters come in a number of forms. The key to their use is the PC's 8284 clock chip that is socketed in about 60 percent of the machines that IBM built. The principle is simple: Remove the chip and plug in a board that pipes new clock signals down onto your motherboard. Of course, you might not have a socket. The solution is to have a reputable repair person replace your chip with a socket. The latter is easy to do yourself, if you know what you are doing. The risk is that you might have to replace your motherboard, a $200 expense. If you want to get the best performance from your motherboard, buy one that is guaranteed to work at 8 MHz and is socketed. This eliminates having to remove 200-ns RAM chips from your old PC motherboard, and motherboard accelerators run faster with clones than they do with IBM motherboards.

The main problem with the inexpensive clock-upgrade approach is that it can extend the system components out of their rated timing specifications. While it is possible for the system to run at speeds above specification, it will probably be more prone to intermittent failures and crashes. In addition, it is often a hit-or-miss business figuring out exactly how far above specification a particular PC is capable of running. The uncertainty results from the fact that a PC is a real-time system, and it is possible to have rare combinations of events occur that overextend the system. On the positive side, a PC performs 200,000 to 500,000 operations per second and, except for unusual events, it should not take it long to explore its operating-phase space.

The motherboard accelerator route, if you pursue it with care, can be the most cost-effective form of acceleration. It is important to buy an accelerator that you can slow down with software or that comes with its own device drivers for the floppy and hard disks. My experience shows that, up to 6.7 MHz, your machine will either run or crash. If it crashes, you have an early PC or one built with marginal components. Above 6.7 MHz, the speed of RAMs and the *quality* of your floppy and hard disk controllers starts to become critical. Above 7.4 MHz, you will definitely have to slow up when you do I/O to your storage systems. This is most easily accomplished with a resident driver that traps requests to INT 13h, slows the accelerator to 4.77 MHz, waits for the I/O to complete, and then speeds back up. With such a driver, it is possible to run some motherboards up to 8 MHz. My experience shows that

Table 1: *Results from runs of the Performance Index benchmark on several different accelerator boards.*

Components of the PI Benchmark

Machine	Numeric Data Processor		Data Bus		Register			Disk	
	1	2	3	4	5	6	7	8	9
PC 4.77	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
PC V20/8	1.71	1.71	1.71	1.70	3.59	5.51	1.77	1.0	1.0
PC2	2.06	2.08	4.05	4.02	2.00	2.03	2.74	.72	.76
PC2 V30	2.11	2.26	4.09	4.06	4.25	6.70	2.79	.77	.77
PC2 12	2.65	2.80	5.17	5.17	2.56	2.54	3.53	.74	.74
AT 6/4	.72	.94	3.27	3.34	3.46	7.74	2.53	3.03	1.1
AT 6/8	1.06	1.54	3.27	3.34	3.46	7.75	2.54	3.03	1.1
AT 6/10	1.15	1.77	3.27	3.34	3.46	7.75	2.54	3.03	1.1
AT 8/8	1.23	1.68	4.50	4.54	4.73	10.9	3.41	3.14	1.1
AT 8/10	1.37	1.98	4.50	4.46	4.78	10.9	3.44	3.90	1.1
PC 7/8	1.2	1.61	4.58	.99	3.19	9.1	2.18	3.0	1.0
					6.00(b)		1.92(b)		
PC 7/10	1.47	2.00	4.57	.98	3.24	9.6	2.15	3.2	3.9
					6.00(b)		1.92(b)		

Legend:

Machine	Processor	MHz	NDP	MHz
PC 4.77	8088	4.77	8087	4.77
PC V20/8	V20	8.0	8087	8.00
PC2	8086	9.54	8087	9.54
PC2 V30	V30	9.54	8087	9.54
PC2 12	8086	12.00	8087	12.00
AT 6/4	80286	6.00	80287	4.00
AT 6/8	80286	6.00	80287	8.00
AT 6/10	80286	6.00	80287	10.00
AT 8/8	80286	8.00	80287	8.00
AT 8/10	80286	8.00	80287	10.00
PC 7/8	80286	7.20	80287	8.00
PC 7/10	80286	7.20	80287	10.00

IBM motherboards top out at 7.4 MHz and good-quality clones run up to 8 MHz.

The motherboard-acceleration technique has one advantage over the coprocessor and emulator techniques: It speeds up motherboard operations, including DMA, which is not affected by the other two classes of accelerator. No matter what technique you use for accelerating, you will have some motherboard operations that detract from overall speed, so picking up the motherboard speed is a good way to bring up the system's slowest activities. When combined with an emulator or coprocessor, the motherboard accelerator forms a hybrid system that improves the performance of all the components, including the accelerator.

Using this technique, I have boosted a motherboard to 6 MHz and run a 9.54-MHz 8086 accelerator at 12 MHz. At this speed, the 8086 outperforms an 8-MHz 80286 in all but two benchmarks (see table 1). The 12-MHz 8087 on this board beats an 8-MHz 80287 by over a factor of two for the most common operations. Not all accelerators can be boosted with this technique. The two that I have successfully boosted required design changes to run at the higher speed.

For speeding up word processors or running 8087-bound applications, the motherboard accelerator is an exceptional buy. An 8-MHz V20 system does numerics faster than an 8-MHz AT and generally increases throughput by 70 percent for only $149 ($298 if you need to replace your old 8087).

Benchmarking Accelerators

People buy accelerators because they want to spend less time waiting for results. Unfortunately, most are not in a position to try a number of accelerators running with their specific applications before they buy. At this point, you might be wondering if there is a simple universal benchmark comparing all accelerators and predicting the relative speed of these boards running any application. Such a benchmark cannot exist because most PC applications fall into one of at least five different categories and, since it takes at least four measurements to gather even basic information, one benchmark could never do.

The five categories are number-bound, mass-storage-bound, data-bus-bandwidth-bound, integer-register-bound, and bound by two or more of the four processes. A sixth type of instruction, which grossly distorts many of the published benchmarks, is dominated by integer multiplies and divides; I have not included it as a category because it plays such a limited role in real programs. This is documented in my BYTE article "The 8087/80287 Performance Curve" (*Inside the IBM PCs*, Fall 1985).

In that article, I showed that for a particular accelerator running an 8086, one-third of the instructions were bound by the internal processor throughput, which is proportional to clock speed (and which I therefore call clock-bound or register-bound), and two-thirds were bound by how fast the processor could fetch new instructions (data-bus-bandwidth-bound). In particular, I found that a 9.54-MHz 8086 runs three times faster than a 4.77-MHz 8088 and that this speed could be derived using a simple theory that can be summarized as follows: The average of the speedups (two for clock-bound instructions and four for data-bus-bandwith-bound instructions) equals the average speedup, three. In this article, a similarly interesting principle applies when there are more than two processes determining the speedup of an application: The overall increase in speed is equal to the average of the slowest and fastest processes that comprise 10 percent or more of the total instructions. This principle could be thought of as taking the average of significant extremes and throwing out processes that rarely occur.

Before I present my benchmark and findings, I want to examine a famous benchmark that reviewers and manufacturers everywhere use but which often yields anomalous results: SI by Peter Norton. This benchmark, which is part of Norton's SysInfo utility, can over- or underestimate the average speed of a board by as much as 100 percent. The best example is the 9.54-MHz 8086 accelerator. SI usually yields a value of 2 for this processor, which, to take the benchmark literally, would imply that a 9.54-MHz 8086 is only twice as fast as a 4.77-MHz 8088. Since that is exactly equal to the increase in clock speed, an innocent application of SI generates the false conclusion that there is no benefit in going from an 8-bit to a 16-bit data bus. I know for a fact that a 9.54-MHz 8086 runs three times faster than a 4.77-MHz 8088 when executing typical applications and that all this fuss over 16- and 32-bit data buses is for real. This also tells me that SI is composed of 100 percent clock-bound operations, which is why it scales with clock speed when run on an 8086.

The NEC V20 and V30 speed up a number of clock-bound operations, such as integer multiplies, divides, and string operations. For typical applications, it is reasonable to expect a 5 to 15 percent increase in speed from the NEC V-series processors over their Intel counterparts; you can occasionally get up to a 40 percent increase when performing floating-point arithmetic without an 8087.

So what happens when I replace the 9.54-MHz 8086 with a 9.54-MHz V30? I get a jump in SI results from 2.0 to 4.0. Where SI underestimated the 8086's performance, it now overestimates the V30's performance. If SI were a true index of system speed, it would read about 3.1, not 4.0, for a V30 running at 9.54 MHz. The interesting fact that I have uncovered in SI is that it is bimodal: On the 8086 it is clock-bound, while on the V30 it becomes data-bus-bandwidth-bound. I came to this conclusion without the aid of a debugger, but I suspect from an examination of the pure benchmarks that make up PI benchmarks that SI is partially made up of block moves and integer arithmetic, two rarely used operations in compiler-generated code.

Finally, SI acts strangely on some compatibles, and it is possible to get

(continued)

speedups like 101 or different values every time you run the benchmark. In general, I would divide any advertised SI claim for an 80286 machine in half, as the benchmark was inflated by a factor of two in the first place by its sole use of operations that are rarely used and are among the slowest in the 8088 repertoire. If the manufacturer of an 80286 board claims it is 6.6 times faster than a PC, the estimate is probably based on SI, and 2.7 to 3.3 is a much better estimate. This rule does not hold for 8086 boards, which actually run faster than SI by 50 percent. In conclusion, for a benchmark to be meaningful, it must sample the mainstream of processor activities in the user's applications and it must be documented.

THE ACCELEROMETER PI

By now, I hope that you are convinced of at least three things. First, a number of underlying processes come into play in a system. Also, an understanding of what those processes are is fundamental to using benchmarks for making system measurements. Finally, benchmarks that measure pure processes can be useful in predicting what happens in complex real-world situations. Toward that end, I designed a suite of benchmarks to measure the pure processes that go on in object-compatible Intel accelerators.

My accelerometer is called PI (see listing 1), which stands for Performance Index. It was my intention to create a program that would let users design their own complex benchmarks from a number of pure ingredients that I built into PI. The results of running PI on a number of different machines are in table 1. [*Editor's note: The Performance Index benchmark,* PI.BAS, *and several associated files are available on disk, in print, and on* BIX. *See the insert card following page* 176 *for details. Listings are available on* BYTEnet; *see page* 4.]

PI is composed of nine standard benchmarks and two alternates that measure interesting properties of cache cards or 80286 cards with no wait states. There are four groups of benchmarks: numeric, data-bus-bandwidth-limited, register- or clock-bound, and disk-bound.

INTERPRETING THE RESULTS

Benchmarking accelerators using the PI benchmarks resulted in two points of interest: the data-bus bandwidth of the PC and that of the AT. At 4.77 MHz, an average PC clock cycle takes 210 ns, and it takes four cycles to perform a memory read or write; that is, it takes 840 ns to move a byte over the 8-bit-wide bus that results in a data-bus bandwidth of 1.19 megabytes per second. This pure band-

(continued)

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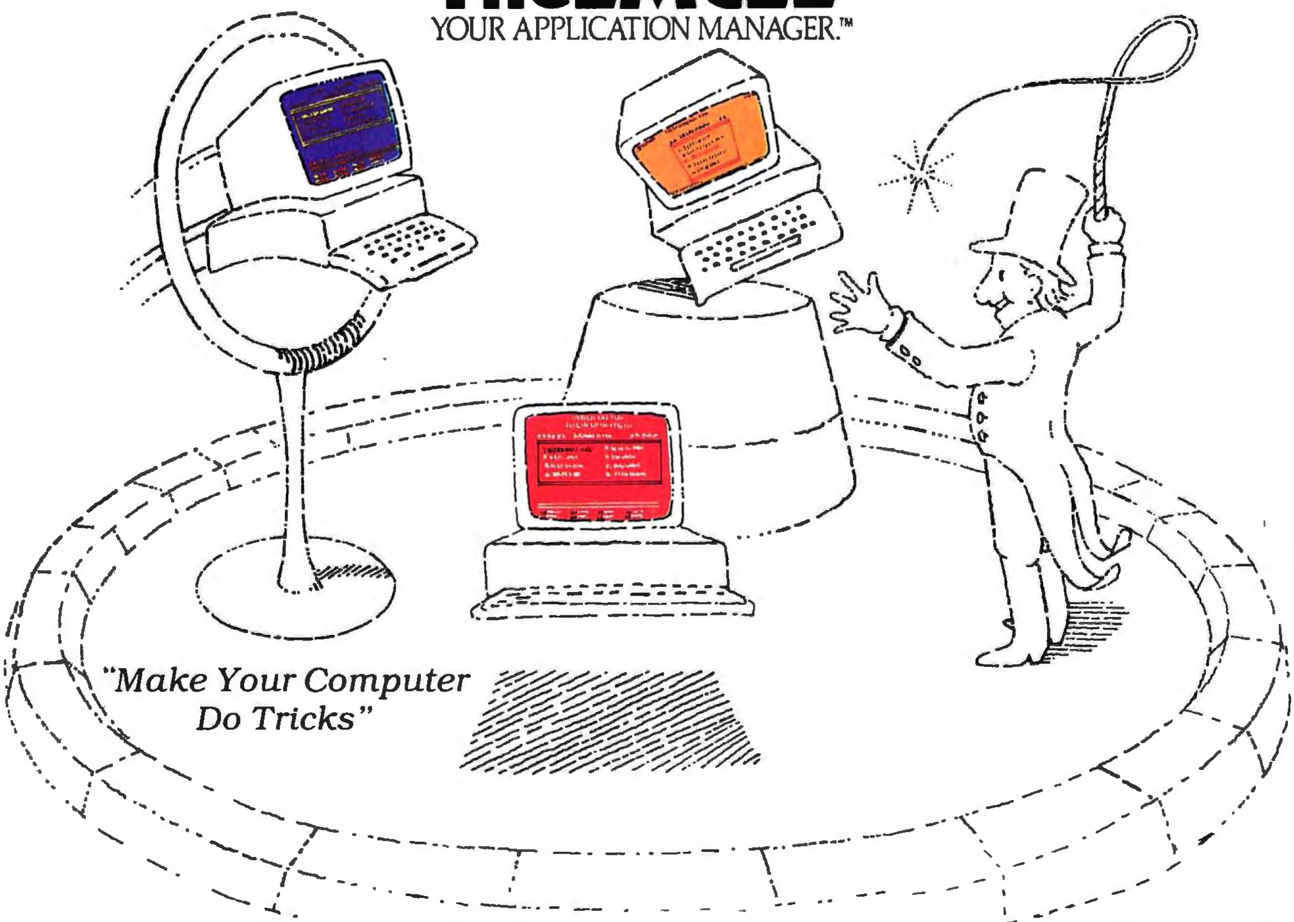

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Listing 1: The Performance Index benchmark main program. This IBM BASIC Compiler (version 2.00) program calls several assembly language routines to perform the actual benchmarks. The program uses the object module TIME100 to perform the timing function.

```
10 REM  PI.BAS -- Performance Index Benchmark Program
20 REM Copyright (C) MicroWay, Inc., 1986
30 REM MicroWay, Inc.    PO Box 79    Kingston MA 02364    (617) 746-7341
40 REM
50 REM Does not use Numeric Coprocessor (8087 or 80287).  See PI87.BAS for
60 REM a similar program which does use the Numeric Coprocessor.
70 REM Compiled with IBM BASIC Compiler V2.00 (/O switch).  Linked with
80 REM assembly language subroutines:
90 REM DBB4 DBBCACHE DBB16 CB4 CB16 IA XFER TIME100
100 REM
110 DEFINT A-Y
120 DIM NAME$ (11), SECTION$ (11), ZF (11), ZP (11)
130 DIM DSRC (10249), DDEST (10249)
140 COMMON DSRC (), DDEST (), SPC1!, SPC2!, SPC3!, SVA!, SVB!
150 DEF FNS# (X$) = 60# * (60# * VAL (MID$ (X$, 1, 2)) + VAL (MID$ (X$, 4,
2))) + VAL (MID$ (X$, 7, 2)) + .01# * VAL (MID$ (X$, 10, 2))
160 LINES$ = "" : FOR I = 1 TO 69 : LINES$ = LINES$ + CHR$ (205) : NEXT I
170 PRINT CHR$ (201); LINES$; CHR$ (187)
180 PRINT CHR$ (186); " M i c r o W a y   P e r f o r m a n c e   I n d e x
P r o g r a m "; CHR$ (186)
190 PRINT CHR$ (200); LINES$; CHR$ (188)
200 PRINT "                          Copyright (C) MicroWay, Inc., 1986."
210 PRINT "                  (This version does not use the Numeric Coprocessor)"
220 PRINT
230 DATA 0.6013,0.5607,0.6,0.6,0.595,0.589,0.62,0.6,0.6,0.6064,0.6064
240 DATA " 1"," 2"," 3"," 4"," 5"," 6"," 7"," 8"," 9","10","11"
250 DATA "Floating point -- arithmetic                       "
260 DATA "Floating point -- Savage (transcendentals)         "
270 DATA "Data bus bound -- 4K bytes of instructions         "
280 DATA "Data bus bound -- 4K bytes of register moves       "
290 DATA "Data bus bound -- 16K bytes of instructions        "
300 DATA "Clock bound -- 4K byte block moves                 "
310 DATA "Clock bound -- 16K byte block moves                "
320 DATA "Integer multiply and divide                        "
330 DATA "Subroutine calls and stack operations              "
340 DATA "Disk I/O -- sequential read from random file       "
350 DATA "Disk I/O -- sequential write to random file        "
360 DATA 25,25,11.111111,11.111111,11.111111,8.333333,8.333333,0,0,0,0
370 CALL TIME100
380 FIRSTTIME = 1
390 FOR I = 1 TO 11 : READ ZF (I)        : NEXT I
400 FOR I = 1 TO 11 : READ SECTION$ (I) : NEXT I
410 FOR I = 1 TO 11 : READ NAME$ (I)     : NEXT I
420 FOR I = 1 TO 11 : READ ZP (I)        : NEXT I
430 MAXWRITES = 20 : MAXREADS = 20
440 GOTO 570
450 REM *** Create file so that reads will have something to work on
460 REM *** and so that writes will not have to create new records.
470 IF MAXWRITES > MAXREADS THEN MPUT = MAXWRITES : ELSE MPUT = MAXREADS
480 OPEN "TEMP.TMP" FOR RANDOM AS #1 LEN=2048
490 FIELD #1, 2048 AS S$
500 T$ = "" : FOR I=0 TO 1023 : T$ = T$ + MKI$ (256 * RND (I)) : NEXT I
510 LSET S$ = T$
520 FOR I = 1 TO MPUT : PUT #1, I : NEXT I : CLOSE #1
530 PRINT "Please enter percentage of benchmark devoted to each operation."
540 FOR I = 1 TO 11
550 PRINT "Section ";SECTION$ (I);"   ";NAME$ (I);": "; : INPUT "", ZP (I)
560 NEXT I
570 ZT = 0 : FOR I = 1 TO 11 : ZT = ZT + ZP (I) : NEXT I
580 IF ZT > 99.5 AND ZT < 100.5 THEN GOTO 640
590 PRINT : PRINT "Caution: percentages total "; ZT;
600 INPUT " Adjust to 100% ? ", ADJ$ : PRINT : ADJ$ = LEFT$ (ADJ$, 1)
```

(continued)


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```
610 IF ADJ$ = "Y" OR ADJ$ = "y" THEN GOTO 630
620 IF ADJ$ = "N" OR ADJ$ = "n" THEN GOTO 660 : ELSE GOTO 600
630 IF ZT = 0! THEN GOTO 840
640 Z100 = 1# / ZT : FOR I = 1 TO 11 : ZP (I) = ZP (I) * Z100 : NEXT I
650 ZT = 100# : GOTO 670
660 FOR I = 1 TO 11 : ZP (I) = .01 * ZP (I) : NEXT I
670 PRINT "Section                    Description                    Performance
Index"
680 PRINT "======= =============================================
================="
690 ZTET = 0# : FOR J = 1 TO 11
700 ZITER = 60# * ZP (J) / ZF (J)
710 ITER = INT (ZITER) : IF ZITER - ITER > .1 THEN ITER = ITER + 1
730 ON J GOSUB 930,970,1000,1010,1020,1030,1040,1050,1060,1070,1140
740 ZET = FNS# (B$) - FNS# (A$)
750 IF ITER <> 0 THEN ZET = ZET * ZITER / ITER : ELSE ZET = 0#
760 PRINT "  ";SECTION$ (J);"    ";NAME$ (J);"      ";
770 IF ZET = 0 THEN PRINT "  ----" : GOTO 790
780 PRINT USING "###.##"; ZF (J) * ZITER / ZET
790 ZTET = ZTET + ZET
800 NEXT J
810 PRINT : PRINT "Performance index for entire benchmark is ";
820 IF ZTET = 0 THEN PRINT "not meaningful." : GOTO 840
830 PRINT USING "###.##"; .6# * ZT / ZTET
840 PRINT
850 INPUT "Would you like to run again, specifying the section weights
yourself? ", MORE$ : MORE$ = LEFT$ (MORE$, 1)
860 IF MORE$ = "Y" OR MORE$ = "y" THEN GOTO 900
870 IF MORE$ = "N" OR MORE$ = "n" THEN GOTO 880 : ELSE GOTO 840
880 IF FIRSTTIME > 1 THEN KILL "TEMP.TMP"
890 END
900 PRINT : FIRSTTIME = FIRSTTIME + 1
910 IF FIRSTTIME = 2 THEN GOTO 450 : ELSE GOTO 530
930 A$ = TIME$ : FOR I = 1 TO ITER : ZA# = 0# : FOR K = 1 TO 114
940 ZB# = (ZA# + 1#) * (ZA# + 2#) / (ZA# + 3#) + (ZA# + 2#) * (ZA# + 3#) /
(ZA# + 1#) + (ZA# + 3#) * (ZA# + 1#) / (ZA# + 2#)
950 NEXT K : NEXT I : B$ = TIME$ : RETURN
970 A$ = TIME$ : FOR I = 1 TO ITER : ZA# = 1# : FOR K = 1 TO 9
980 ZA# = TAN (ATN (EXP (LOG (SQR (ZA# * ZA#))))) + 1#
990 NEXT K : NEXT I : B$ = TIME$ : RETURN
1000 A$ = TIME$ : FOR I = 1 TO ITER : CALL DBB4  : NEXT I : B$ = TIME$ :
RETURN
1010 A$ = TIME$ : FOR I = 1 TO ITER : CALL DBBCACHE:NEXT I: B$ = TIME$ :
RETURN
1020 A$ = TIME$ : FOR I = 1 TO ITER : CALL DBB16 : NEXT I : B$ = TIME$ :
RETURN
1030 A$ = TIME$ : FOR I = 1 TO ITER : CALL CB4   : NEXT I : B$ = TIME$ :
RETURN
1040 A$ = TIME$ : FOR I = 1 TO ITER : CALL CB16  : NEXT I : B$ = TIME$ :
RETURN
1050 A$ = TIME$ : FOR I = 1 TO ITER : CALL IA    : NEXT I : B$ = TIME$ :
RETURN
1060 A$ = TIME$ : FOR I = 1 TO ITER : CALL XFER  : NEXT I : B$ = TIME$ :
RETURN
1080 IF ITER = 0 THEN A$=TIME$ : B$=A$ : RETURN
1090 OPEN "TEMP.TMP" FOR RANDOM AS #1 LEN=2048
1100 FIELD #1, 2048 AS S$
1110 A$ = TIME$
1120 FOR K = 1 TO ITER : FOR I = 1 TO MAXREADS : GET #1, I : NEXT I : NEXT K
1130 B$ = TIME$ : CLOSE #1 : RETURN
1150 IF ITER = 0 THEN A$=TIME$ : B$=A$ : RETURN
1160 OPEN "TEMP.TMP" FOR RANDOM AS #1 LEN=2048
1170 FIELD #1, 2048 AS S$ : LSET S$ = T$
1180 A$ = TIME$
1190 FOR K = 1 TO ITER : FOR I = 1 TO MAXWRITES : PUT #1, I : NEXT I : NEXT K
1200 B$ = TIME$ : CLOSE #1 : RETURN
```


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width is degraded by the DMA controller, which runs 7 percent of the time refreshing memory, resulting in an actual bandwidth of 1.10 megabytes per second.

On the other hand, the AT has a 16-bit bus and a cycle time at 6 MHz of 167 ns. Its 80286 normally takes only two cycles to perform a memory operation, but in the AT it was set up with a single wait state, resulting in a total memory-fetch time of 500 ns. The rate of 2 bytes every 500 ns is the same as 4 bytes every microsecond or 4 megabytes per second. In the case of the AT, only 5.3 percent is lost to refresh, resulting in a net bandwidth of 3.78 megabytes per second. Dividing these rates yields a PI for the AT in this department of 3.44, which is close to the 3.27 actually observed for the AT running at 6 MHz in table 1. The experimental difference could be attributed to inaccurate information from IBM on the refresh overhead, loop overhead, or system-background operations, such as timer-interrupt routines. Using the same benchmark on the 9.54-MHz 8086 accelerator running on a PC, I got 4.02, which agrees well with the 4.0 I would expect upon doubling the data-bus width and frequency.

I obtained this benchmark using an assembly language subroutine that did a large number of fast-running 8086 operations. By definition, any operation whose binary machine code takes longer to fetch from memory into the processor than it does to run will end up producing a data-bus-bandwidth-limited situation (i.e., the speed of the sequence is controlled by how fast you can fetch in op codes). The criterion of which operations are data-bus-bandwidth-limited is an easy one, but it is also machine-dependent. The PC takes four cycles to fetch a byte; therefore, any operation whose instruction is a byte long must execute in less than four cycles. Two byte-long instructions must execute in less than eight cycles, etc. The AT takes three cycles to fetch a word, and the criterion for a 2-byte instruction is that it take three cycles to execute to remain under the fetch time. When I apply this reasoning to a cached board with no wait states, I come to the conclusion that very few of the instructions are bus-limited, for I must be able to execute byte-long instructions in one cycle (there are none) and word-long instructions in two cycles. As a result, I rewrote the data-bus-limited benchmark so it would work with no-wait-state 80286 boards. Listing 2 shows the code stream of the original benchmark.

Listing 2's sequence of instructions was repeated to build a 4000-byte-long sequence that was then called as a subroutine. These instructions are all bus-limited for an 8088, 8086, or

(continued)

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Listing 2: *The assembly language code for the data-bus-bandwidth benchmark.*

Op code		Number of bytes	Number of cycles
XOR	AX,AX	2	3
XOR	DX,DX	2	3
ADD	AX,DX	2	3
ADD	AX,DX	2	3
SUB	AX,DX	2	3
SUB	AX,DX	2	3
CLC		1	2
CLD		1	2
NOP		1	3
NOP		1	3

80286 with one wait state but are not bus-limited for a no-wait-state 80286. To reexamine the bus limit in this card, I replaced this 10-byte sequence with a 10-byte sequence of

MOV AX,BX

which obeys the criterion. Then I labeled this benchmark 3b. It takes a cached board at 7.2-MHz two cycles or 277 ns to read in a word. The same process in a PC takes eight cycles or 1680 ns. The ratio of these times is 6.06, which agrees very well with the value of 6.0 for the cache board. In the process of creating this benchmark, I have also learned that only one kind of instruction, interregister moves, is bus-limited in the cached board.

The data-bus-bandwidth benchmark teaches us a lot about 80286 machines. As the data bus goes from one wait state to no wait states, the data-bus activity starts to dry up. Watched on a scope in a six-line loop, the processor performs a flurry of fetches and then goes into an idle state for quite a while as the program works its way back to the bottom of the loop. From a designer's point of view, this means that a no-wait-state board does not exhibit the optimal distribution of data-bus speed to register speed. If memory fetches are done consistently faster than register-bound operations and fast memories cost a lot of money, you would do just as well with slower-speed memories that provide the needed instructions just as the register-bound operations complete. Put in other terms, I think the IBM one-wait-state approach might be near optimal for 80286 machines that are not bogged down with DMA cycles, and the hoopla about no-wait-state memories could very well be a lot of nonsense.

This idea is also highlighted in the *iAPX 286 Hardware Design Manual*, which points out that with no wait states the bus is idle 75 percent of the time, versus 90 percent with one wait state. This document also states that the main beneficiary of no-wait-state memories is block moves. Block moves get used primarily in I/O-intensive applications such as RAM disks and disk caches. It is unlikely that the added speed they represent would make much of an impact on typical single-user applications, although they might make a difference in multiuser operating systems. Unfortunately, when run in protected mode on an 80286, these operating systems will become more register-speed-dependent (a feature of protected mode); that would again argue against ultra-fast memories to improve overall throughput.

CONCLUSION

Accelerators have been available for the IBM PC for three years. They are a cost-effective method to either speed up or extend the architecture of the computer. Extended architectures range from adding new CPUs to increasing the memory available for MS-DOS 3.0. Three types of accelerators were discussed in this article. Of these, the emulator approach is the most compatible and reliable and the route that provides the largest benefit-to-cost ratio for the average user. Speedup factors of two to three can be obtained using emulators for as little as $500, depending on the amount of 16-bit memory that the board contains. For most users, a $500 accelerator that triples the speed of everything from word processing to FORTRAN applications is more than a good deal, it's addicting; users get mad if they have to put the original 8088 back in.

Accelerators that give more than a 3 to 1 increase in speed also suffer from increased incompatibility and installation problems. I found that going from 9.54 MHz to 12 MHz quadrupled the number of problems I had with emulator installations. If you are contemplating an 8086 emulator that runs faster than 9.54 MHz or an 80286 cached emulator that runs faster than 7.2 MHz, it's a good idea to make sure that the product in question has a provision for running at slower speeds as well. Software-controlled speed is a real benefit at the highest speeds: It is easy to trap the hardware interrupts that control specific devices in the PC and thereby tailor the accelerator to the slow I/O boards or a poor DMA controller on an older motherboard.

The users of accelerators have a tendency to cluster around certain type of products. Individuals running intensive, floating-point-bound problems end up with 8086/8087-based emulators, and these have a tendency to get a reputation for being math-only accelerators, which they are not. Individuals who are doing word processing or program development have recently been heading toward the 80286 cache boards. For I/O-bound applications such as code development, the I/O software utilities that come with an emulator often contribute as much to the speed as the increase in CPU throughput. The factor of two to four that a disk cache adds to hard disk access speed drowns out any difference between the 8086 and the 80286. Finally, there is the support issue. Good support direct from the manufacturer is more critical with accelerators than with any other type of add-in card. ■

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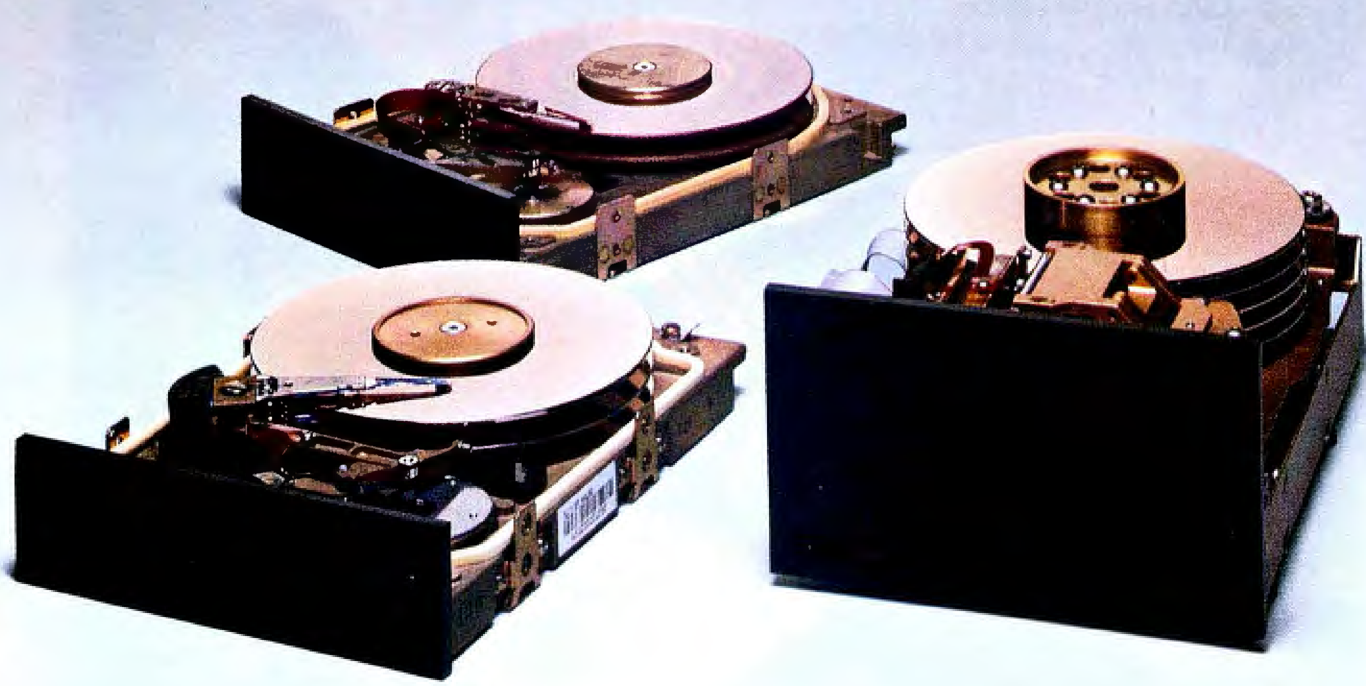

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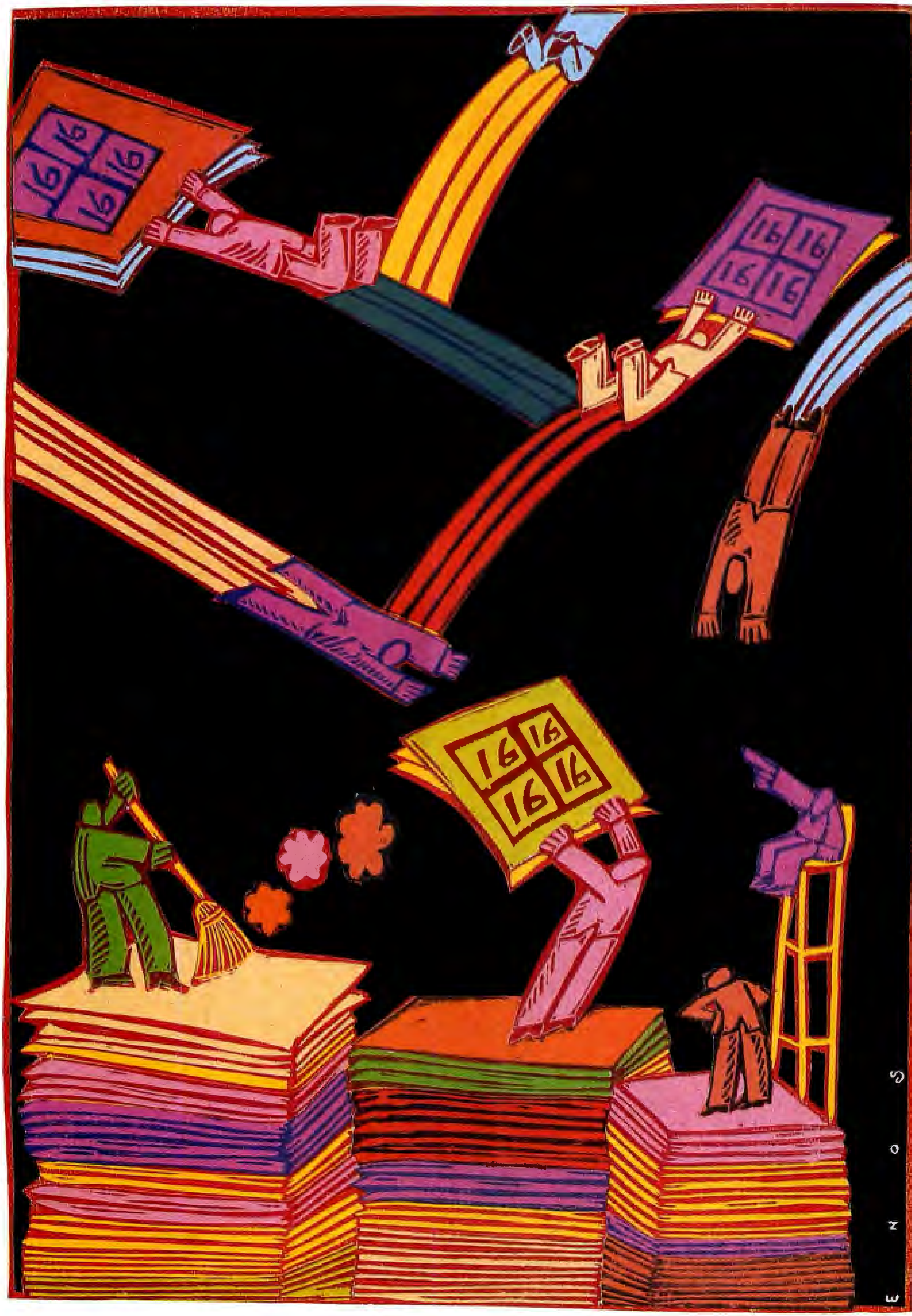

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LOTUS/INTEL/MICROSOFT EXPANDED MEMORY

This version of bank-switched memory provides a uniform software interface to all applications regardless of hardware differences

BY RAY DUNCAN

THE LOTUS/INTEL/MICROSOFT Expanded Memory Specification (EMS) 3.2 is a functional definition of a bank-switched memory-expansion subsystem made up of hardware expansion modules and a user-installable, resident driver program specific for those modules.

Bank switching is a technique whereby the central processor can make one of many *logical* memory pages available for access in a window at a predetermined physical address. It's somewhat like bringing one card to the top of the deck where you can read it.

Bank-switched memory is hardly a new idea. It has been used on Apple and 8080/Z80 S-100 bus computers since the early days of microcomputing to overcome the addressing limitations of the 8-bit processor. For the IBM PC, Tall Tree Systems has been selling a bank-switched memory board called JRAM with electronic disk and print spooler software for several years. But the LIM EMS version of bank-switched memory is a step ahead: It provides a uniform software interface to all applications, regardless of the differences in the underlying hardware. LIM EMS is not, however, the only memory-expansion subsystem available. See the text box "The AST Enhanced EMS" on page 170.

From a hardware standpoint, EMS allows you to install as much as 8 megabytes of expanded memory in a system. This expanded memory is available to application software in 16K-byte logical pages, which are mapped for access onto one of four 16K-byte physical pages. These physical pages exist in a contiguous 64K-byte area called the *page frame*. You can configure the location of the page frame to avoid conflict with other hardware options, but it always resides above the MS-DOS/PC-DOS main memory area (0K to 640K bytes).

Expanded memory should not be confused with *extended* memory. Extended memory is IBM's term for the memory at physical addresses above 1 megabyte that an 80286 microprocessor can access in protected mode. Current versions of MS-DOS run the 80286 in real mode (8086-emulation mode), where extended memory is not directly accessible.

The EMS installable driver, called the Expanded Memory Manager (EMM), provides the hardware-independent interface between application software and expanded-memory hardware. The EMM comes as an installable character device driver that links into the operating system by adding a DEVICE line to the CONFIG.SYS file.

Internally, the EMM is divided into two major sections: the driver and the manager. The driver mimics some of the actions of a real device driver; it includes initialization and output-status functions and a valid device header. The manager is the true interface between application software and the expanded-memory hardware. The EMM provides several classes of services:

- Status of hardware and software modules
- Allocation of expanded-memory pages
- Mapping logical pages into the physical page frame
- Deallocation of expanded-memory pages
- Support for multitasking operating systems
- Diagnostic routines

Application programs communicate with the EMM directly via software interrupt 67h. MS-DOS is not involved. However, Microsoft Windows (which runs on top of MS-DOS) makes heavy use of expanded memory, if it is present, for program swapping. It seems reasonable to expect that future multitasking versions of MS-DOS and other operating systems for the 8086/88 family may do the same.

USING EXPANDED MEMORY

Expanded memory is a system resource and must be treated like one. Application programs must acquire, use, and release expanded memory in a manner that doesn't cause problems for other programs that are trying to use it.

Before you use expanded memory, you must determine that the EMM is present in the system. There are two approved methods of testing for the existence of the EMM.

The first method is to issue an open request (interrupt 21h, function 3Dh) using the device name of the EMM driver: EMMXXXX0. If the open succeeds, either the drive is present or there is a file on the default drive by that name. To rule out a duplicate file-

(continued)

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THE AST ENHANCED EMS

AST Research has also formulated and announced a bank-switched memory subsystem specification. The Enhanced Expanded Memory Specification (EEMS) is upward-compatible with LIM EMS version 3.2 but technically more complex.

EEMS differs from EMS in two important ways:

- In EMS, the 64K-byte page frame is located *above* the 640K-byte MS-DOS area and is used to map four different 16K-byte logical pages into physical memory simultaneously. In EEMS, as many as 64 logical pages can theoretically be mapped into physical memory at once. Practically speaking, on a typical IBM PC under MS-DOS, about 15 logical pages simultaneously mapped into memory is probably the upper limit. (This is the memory above the 640K-byte MS-DOS area minus the addresses occupied by system ROMs and video buffers.)
- In EMS, logical pages cannot be bank-swapped into the 640K-byte memory area controlled by MS-DOS, making it difficult to use expanded memory for paging executable code. In EEMS, logical pages can be mapped into physical memory anywhere in the microprocessor's address space, making it possible for specially designed multitasking operating systems to use expanded memory for very fast switching between processes.

AST's EEMS redefines the software interfaces between the EMM and the application program (see table 2) only slightly. It extends function 5 (Map Memory) to allow physical page numbers larger than 3 and adds function 33 to allow applications to obtain a list of all the physical page addresses. For upward compatibility with EMS, EEMS requires that the first four physical 16K-byte pages be contiguous.

Although EEMS is more sophisticated than EMS and has considerably more potential if properly used by an operating system designed to exploit all its features, to date it has received little support from other PC software and hardware developers. Currently, the only commonly available programs that use EEMS are Quarterdeck Systems' DESQview and Digital Research's Concurrent DOS XM. The only other manufacturer of EEMS hardware, Quadram, has reported delays in designing a board that is simultaneously EMS- and EEMS-compatible.

name on another drive, you issue a get-output-status request via the IOCTL (input/output control) function (interrupt 21h, function 44h); the status returned in register AL will be 0FFh if the driver is present and 0h if not. Either way, you should then close (interrupt 21h, function 3Eh) the handle obtained from the open so the system can reuse it. (See listing 1.)

The second method is to use the address found in the vector for interrupt 67h to inspect the device header of the presumed EMM. If the EMM is present, the name field at offset 0Ah of the device header will contain the string EMMXXXX0. This approach is nearly foolproof and avoids the relatively high overhead of an open. However, it is somewhat less "well behaved" since it involves inspecting memory that does not belong to the application. (See listing 2.)

After establishing that the EMM is present, a typical application follows this general sequence to use expanded-memory resources:

1. Check the operational status of the EMM (EMS function 1).
2. Check the version number of the EMM (EMS function 7) to make sure that all the services that the application needs are available.
3. Obtain the segment of the page frame that the EMM uses (EMS function 2).
4. Allocate the desired number of expanded-memory pages (EMS function 4). If the allocation is successful, the EMM returns a *handle* that the application then uses to refer to the expanded-memory pages that it "owns." This is analogous to opening a file and using a handle for any

(continued)

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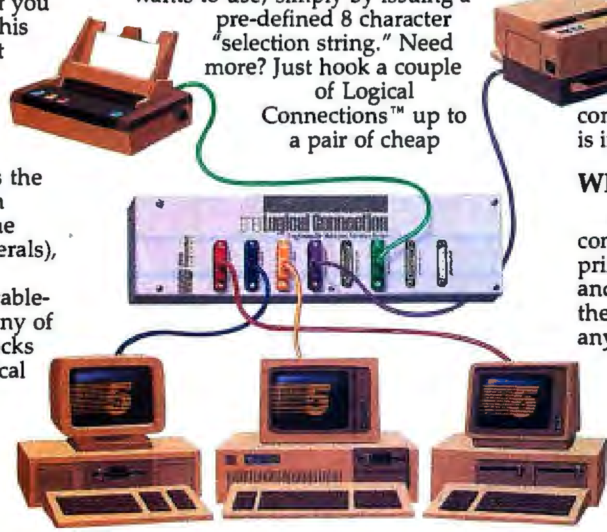

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Listing 1: *Testing for the* EMM *via the* MS-DOS open *and* IOCTL *functions.*

```
              mov   ah,3dh              ;function 3Dh = open.
              mov   al,0                ;mode = read-only.
              mov   dx,seg emm_name     ;DS:DX = addr of name
              mov   ds,dx               ;of Expanded Memory Manager.
              mov   dx,offset emm_name
              int   21h                 ;transfer to MS-DOS.
              jc    emm_absent          ;open failed, driver absent
                                        ;or no more handles.

                                        ;open succeeded, make sure
                                        ;it was not a file.
              mov   bx,ax               ;BX = handle for EMM.
              mov   ah,44h              ;function 44h = IOCTL.
              mov   al,7                ;subfxn 7 = get outp. stat.
              mov   cx,0                ;CX = bytes to read.
              mov   dx,offset emm_buff  ;DS:DX = dummy buffer addr.
              int   21h                 ;transfer to MS-DOS.
              push  ax                  ;save code from IOCTL.
                                        ;close file or device
                                        ;to reclaim handle.
              mov   ah,3eh              ;function 3Eh = close.
              int   21h                 ;BX still contains handle.
              jc    close_failed        ;jump if error on close.
              pop   ax                  ;now look at status code
              or    al,al               ;returned from IOCTL.
              jz    emm_absent          ;if status = "not ready"
                                        ;then it was a file, not
                                        ;the expected EMM driver.
              .
emm_present:  .                         ;driver is present.
              .
emm_absent:   .                         ;driver absent, or no
              .                         ;more handles available.
              .
close_failed: .                         ;error on close.
              .

emm_name      db    'EMMXXXX0',0        ;device name for Expanded
                                        ;Memory Manager

emm_buff      dw    0                   ;dummy buffer for IOCTL call
```

Listing 2: *Testing for the* EMM *by inspecting the name field in the driver's device header.*

```
emm_int       equ   67h                 ;Expanded Memory Manager
                                        ;interrupt vector.
              .
              .
              .
              mov   ah,35h              ;DOS function 35h =
              mov   al,emm_int          ;get interrupt vector
              int   21h                 ;into ES:BX.
                                        ;assume ES:0000 points
                                        ;to the base of the EMM.
              mov   di,10               ;ES:DI = addr of name
                                        ;field in Device Header.
              mov   si,seg emm_name     ;let DS:SI = addr of
              mov   ds,si               ;guaranteed driver name
              mov   si,offset emm_name  ;for EMM.
              mov   cx,8                ;length of name field.
```

```
                cld
                repz cmpsb              ;compare strings.
                jnz  emm_absent         ;strings didn't match.
                .
                .
emm_present:    .                       ;driver present.
                .
emm_absent:     .                       ;driver absent.
                .

emm_name        db    'EMMXXXX0',0      ;device name for Expanded
                                        ;Memory Manager.
```

Listing 3: *The sector mapping routine from the* EMSDISK.ASM *program. This is an example of a program mapping its internal records onto the* EMS 16K-*byte logical pages.*

```
;
; Map into memory a logical "disk" sector from the EMS
; pages allocated to the EMSDISK.
;
; Called with:  AX    = logical sector number
;
; Returns:      CY    = clear if no error
;               AX    = offset within EMS page frame
;               AX,CX,DX destroyed
;
;               CY    = set if EMM mapping error
;               AX,CX,DX destroyed
;
map_sec proc    near

        mov     dx,0            ; divide sector no. by sectors
        mov     cx,sec_per_page ; per page, to get EMS page number
        div     cx              ; now AX=EMS page,DX=rel. sector
        push    dx              ; save remainder
        mov     bx,ax           ; BX <- EMS page number
        mov     ax,4400h        ; map function, phys. page=0
        mov     dx,emm_handle   ; process ID for EMSDISK
        int     67h

        or      ah,ah           ; if EMM error, jump to return flag
        jnz     map_sec1

        pop     ax              ; get remainder (relative sector)
        mov     cx,sec_size     ; remainder*sec_size to get offset
        mul     cx              ; into EMS logical page
        clc                     ; return CY=clear for no error
        ret                     ; back to caller

map_sec1:                       ; come here if EMM mapping error
        add     sp,2            ; clear stack
        stc                     ; return CY=set for error
        ret

map_sec endp
;
```

subsequent read or write operations on it.

5. If the requested number of pages is not available, the application can query the EMM to find out how many pages are available (EMS function 3). Then the application can determine if it can continue processing in a degraded fashion.

6. Perform mapping requests (EMS function 5) as needed to gain access through the page frame to the expanded-memory logical pages that the application owns. Any further

(continued)

blocking, deblocking, or imposing a record structure on the expanded memory must be done at the application level. (The routine map__sec, which is extracted from EMSDISK.ASM, is an example of such mapping. See listing 3.)

7. Deallocate the expanded-memory pages and release the EMM handle obtained earlier (EMS function 6) when it has finished using them. If the application doesn't perform this housekeeping, those pages will be unavailable to other programs until the system is rebooted.

Application programs communicate with the EMM directly via interrupt 67h. The basic calling sequence for the EMM is shown in listing 4. In general, registers ES:DI are used to pass the address of a buffer or an array, and register DX is used to hold an EMM handle. Upon return from an EMM function call, register AH will contain zeros if the function was successful or an error code with the most significant bit set if the function failed (see table 1). Other values are typically returned in registers AL and BX or in a user-specified buffer. Table 2 contains a summary of the services available from the EMM.

An interrupt handler or a resident driver that uses EMS follows the same general procedure that an application does, with a few minor variations. It may need to acquire an EMM handle and allocate pages before the operating system is fully functional. Thus, since it may or may not have MS-DOS file open, close, and IOCTL functions available, it must use a modified version of the get-interrupt-vector technique to test for the existence of the EMM.

A resident driver or an interrupt handler typically owns its expanded-memory pages on a permanent basis (until the system is rebooted) and never deallocates them. It must also save and restore the EMM's page mapping context (EMS functions 8 and 9, respectively), so it won't disturb a foreground program's use of EMS.

The EMM relies heavily on the good behavior of other software to avoid the corruption of expanded memory. If several applications that use expanded memory run under a multitasking manager, such as Windows or TopView, and one of them does not abide strictly by the EMM's conventions, the data of some or all of those applications may be destroyed.

Listing 4: *The calling sequence for the* EMM.

```
mov   ah,function          ;AH always determines service type
.
.                          ;load other registers with values
.                          ;specific to the EMS function
.
int   67h
```

Table 1: EMM *error codes. After a call to the* EMM, *register* AH *will contain a zero if the function was successful or an error code in the range* 80h–8Fh.

Error Code	Significance
00	Function was successful.
80h	Internal error in the EMM software.
81h	Malfunction in the expanded-memory hardware.
82h	Memory manager is busy.
83h	Invalid handle.
84h	Function requested by the application is not defined.
85h	No more EMM handles available.
86h	Error in save or restore of mapping context.
87h	An allocation request specified more logical pages than are physically available in the system; no pages were allocated.
88h	An allocation request specified more logical pages than are currently available in the system (the request does not exceed the physical pages that exist, but some are already allocated to other handles); no pages were allocated.
89h	You cannot allocate zero pages.
8Ah	The logical page that was requested is outside the range of logical pages allocated to the handle.
8Bh	Illegal physical page number in mapping request (not in the range 0 to 3).
8Ch	The save area for mapping contexts is full.
8Dh	Save of mapping context failed because save area already contains a context associated with the requested handle.
8Eh	Restore of mapping context failed because save area does not contain a context for the requested handle.
8Fh	Subfunction parameter not defined.

THE EMSDISK PROGRAM

EMSDISK is an installable RAM disk driver for MS-DOS 2.0 or higher that uses expanded memory and the EMM services. Written in assembly language, it can emulate a fixed disk as large as 8 megabytes and store the files in expanded-memory pages for extremely fast access. It was tested on a Compaq running PC-DOS 3.1, using the Intel Above Board and its EMM version 3.3. [*Editor's note:* EMSDISK.ASM *is available on disk, in print, and on* BIX. *See the insert card following page* 176 *for details. Listings are also available on* BYTE*net. See page* 4.]

Don't confuse the EMSDISK driver with the EMM driver that is provided with the expanded-memory board. The EMM is a proprietary software product of the board manufacturer. EMSDISK requires the EMM in order to operate, but the only resemblance between the two programs is that they are both user-installable device drivers. (To implement EMSDISK on your system, see the text box "Putting EMSDISK to Work" below.)

EMSDISK follows the structure required of an installable block device driver under MS-DOS. For more information about the structure or programming of installable drivers, see the bibliography at the end of this article.

The EMSDISK driver contains two critical data structures: the device header and the BIOS parameter block (BPB). The device header contains linkages to the driver's routines, a device-attribute word that describes its nature and capabilities, and a link to the next installed driver in the chain. The BPB is supplied by block device drivers for use by MS-DOS and describes the size and location of a disk's control and data areas.

EMSDISK breaks down logically into two major modules: the initialization module and the driver proper. MS-DOS calls the initialization module when it first loads EMSDISK. This module is responsible for determining whether the EMM is present, checking its version, getting the segment address of the EMM's page frame, allocating memory pages for EMSDISK, setting up the BPB, printing the program's identification message, and notifying the operating system of the amount of memory the program occupies and the number of logical disk units it supports. The initialization routine is used only once, and the

(continued)

PUTTING EMSDISK TO WORK

To assemble the source code into a usable EMSDISK driver module, you need the Microsoft Macro Assembler (MASM.EXE), the Microsoft Linker (LINK.EXE), and the EXE-to-BIN conversion utility (EXE2BIN.EXE). Put these three programs and the source file, EMSDISK.ASM, on a working disk, then enter the following sequence of instructions:

```
MASM EMSDISK;
LINK EMSDISK;
EXE2BIN EMSDISK.EXE
  EMSDISK.BIN
DEL EMSDISK.EXE
```

Now copy the resulting EMSDISK.BIN file to the root directory of your system boot disk. Finally, to link the EMSDISK driver into the operating system, you need to add the line DEVICE= EMSDISK.BIN to the CONFIG.SYS file on your system boot disk. This line must occur after the line that loads the EMM (DEVICE=EMM.SYS in the case of the Intel Above Board).

If you enter the DEVICE line as given, all the available expanded-memory pages will be allocated to the EMSDISK. If you want a smaller size EMSDISK, enter the line DEVICE= EMSDISK.BIN *nnn*K. For example, to create an EMSDISK of 512K bytes, you would enter DEVICE= EMSDISK.BIN 512K in your CONFIG.SYS file. If you omit the *nnn*K parameter, or specify more expanded memory than actually exists or is available, the EMSDISK driver will simply allocate all of the available expanded-memory pages.

When the system is booting, EMSDISK will display a message on the screen to let you know that it has installed successfully, what drive letter is assigned to it, and how much memory is allocated to it. The drive letter that is assigned to the EMSDISK depends on the number of other block devices in your system and the position of the DEVICE=EMSDISK.BIN line in the CONFIG.SYS file. Under DOS 3.x, the drive letter is made available to the EMSDISK driver in the initialization process and is printed out in the driver identification message; under DOS 2.x, you have to figure out which drive letter it is.

Finally, you can create multiple EMSDISK drives by placing multiple DEVICE=EMSDISK.BIN *nnn*K lines in your CONFIG.SYS file, allocating a portion of the available expanded memory on each line. Realize, however, that if you omit the *nnn*K parameter, the first DEVICE=EMSDISK.BIN line will allocate all the available expanded memory, and none will be left for the others.

Table 2: A *summary of software interfaces to application programs provided by the* EMM.

Function Name	Action	Called With	Returns	Comments
Function 1: Get Manager Status	Tests whether the expanded-memory software and hardware are functional.	AH = 40h	AH = status	This call is used after the program has established that the EMM is present, using one of the techniques presented in listings 1 and 2.
Function 2: Get Page Frame Segment	Obtains the segment address of the EMM page frame.	AH = 41h	AH = status BX = segment of page frame, if AH = 0	The page frame is divided into four 16K-byte pages, which are used to map logical expanded-memory pages into the physical memory space of the 8086/88.
Function 3: Get Number of Pages	Obtains the total number of logical expanded-memory pages present in the system and the number not already allocated.	AH = 42h	AH = status BX = unallocated EMS pages, if AH = 0 DX = total EMS pages in system	The application need not have already acquired an EMM handle to use this function.
Function 4: Get Handle and Allocate Memory	Obtains an EMM handle and allocates logical EMS pages to be controlled by that handle.	AH = 43h BX = logical pages to allocate	AH = status DX = handle, if AH = 0	Equivalent of a file open function for the EMM. The handle that is returned is analogous to a file handle and "owns" a certain number of EMM pages. The handle must be used with every subsequent request to map memory and must be released by a close operation when the application is finished. The function may fail because available EMM handles or EMS pages have been exhausted.
Function 5: Map Memory	Maps one of the logical pages of expanded memory assigned to a handle onto one of the four physical pages within the EMM's page frame.	AH = 44h AL = physical page (0 to 3) BX = logical page (0. . .[*n*−1]) DX = handle	AH = status	The logical page number must be in the range (0. . .[*n*−1]), where *n* is the number of logical pages previously allocated to the EMM handle with function 4. To access the memory once it has been mapped to a physical page, the application also needs the segment of the EMM's page frame, obtained with function 2.
Function 6: Release Handle and Memory	Deallocates the logical pages of expanded memory currently assigned to a handle and then releases the handle for reuse.	AH = 45h DX = EMM handle	AH = status	This is the equivalent of a close operation on a file. It notifies the EMM that the application will not be making further use of the data it may have stored within expanded-memory pages.
Function 7: Get EMM Version	Returns the version number of the EMM software.	AH = 46h	AH = status AL = EMM version, if AH = 0	The returned value is the version of the EMS that the EMM driver complies with. It is returned encoded as BCD, with the integer part in the upper 4 bits and the fractional part in the lower 4 bits.
Function 8: Save Mapping Context	Saves the contents of the expanded-memory page mapping registers on the expanded-memory boards, associating those contents with a specific EMM handle.	AH = 47h DX = handle	AH = status	This function is designed for use by interrupt handlers and resident drivers or utilities that must access expanded memory. The handle supplied to the function is the handle that was assigned to the interrupt handler during its initialization sequence, not the one assigned to the program that was interrupted.

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Function Name	Action	Called With	Returns	Comments
Function 9: Restore Mapping Context	Restores the contents of all expanded-memory hardware page mapping registers to the values associated with the given handle.	AH = 48h DX = EMM handle	AH = status	Use of this function must be balanced with a previous call to EMS function 8. It allows an interrupt handler or resident driver that used expanded memory to restore the mapping context to its state at the point of interrupt.
Function 10 (0Ah): Reserved				This function was defined in the EMS 3.0 specification, but it is no longer documented in EMS version 3.2.
Function 11 (0Bh): Reserved				This function was defined in the EMS 3.0 specification, but it is no longer documented in EMS version 3.2.
Function 12 (0Ch): Get Number of EMM Handles	Returns the number of active EMM handles.	AH = 4Bh	AH = status BX = number of EMM handles, if AH = 0	If the returned number of handles is zero, none of the expanded memory is in use. The number of active EMM handles will never exceed 255.
Function 13 (0Dh): Get Pages Owned by Handle	Returns the number of logical expanded-memory pages allocated to a specific handle.	AH = 4Ch DX = EMM handle	AH = status BX = logical pages, if AH = 0	A single program can make several allocation requests and therefore "own" several EMM handles. The number of pages returned will always be in the range of 1 to 512—never zero if the function is successful.
Function 14 (0Eh): Get Pages for All Handles	Returns an array that contains all the active handles and the number of logical expanded-memory pages associated with each handle.	AH = 4Dh DI = offset of array to receive information ES = array segment	AH = status BX = number of active EMM handles If AH = 0, array is filled in as described in the Comments column.	The array is filled in with 2-word entries. The first word of each entry contains a handle; the next word, the number of pages associated with that handle. The value returned in BX gives the number of valid 2-word entries in the array. Since the maximum number of active EMM handles is 255, the array need not be larger than 1024 bytes.
Function 15 (0Fh): Get/Set Page Map	Saves or sets the contents of the EMS page mapping registers on the expanded-memory boards.	AH = 4Eh AL = subfunction number DS:SI = array holding mapping information (subfunctions 1 and 2) ES:DI = array to receive information (subfunctions 0 and 2)	AH = status AL = bytes in page mapping array (subfunction 3) Array pointed to by ES:DI receives mapping information for subfunctions 0 and 2.	Subfunctions: 0 = get mapping registers into array 1 = set mapping registers from array 2 = get and set mapping registers in one operation 3 = return needed size of page mapping array This function was added in EMS version 3.2 and is designed to support multitasking operating systems. It should not ordinarily be used by application software. The array contains hardware- and EMM-software-dependent information. It may contain other information that is necessary to restore the expanded-memory subsystem to its previous state, as well as the contents of the mapping registers themselves.

Listing 5: *An extract from the initialization module of the* EMSDISK *program.*

```
init2:  xor     ax,ax               ; if EMM driver present,
        mov     es,ax               ; address in vector
        mov     bx,emm_int*4        ; points to EMM driver.
        mov     es,es:[bx+2]        ; ES:0000 points to EMM hdr,
        mov     di,10               ; ES:DI = addr of device
                                    ; name field, DS:SI = addr
                                    ; of EMM driver name
        mov     si,offset emm_name
        mov     cx,8                ; length of device name fld
        cld
        repz    cmpsb               ; if EMM name matches
        jz      init3               ; driver header, jump.
        mov     dx,offset msg1      ; if strings didn't match,
        jmp     init_err            ; driver is absent, exit.

init3:  mov     ah,40h              ; EMM driver is present,
        int     67h                 ; test EM Manager status.
        or      ah,ah
        jz      init4               ; jump, driver is OK
        mov     dx,offset msg2      ; EMM non-functional, print
        jmp     init_err            ; error message and exit

init4:  mov     ah,46h              ; check EM Manager version
        int     67h
        or      ah,ah
        jz      init5               ; jump, got version ok
init45: mov     dx,offset msg3      ; print EMM error message
        jmp     init_err            ; exit, discarding driver

init5:  cmp     al,030h             ; check at least ver. 3.0
        jae     init6               ; jump if EMM version OK
        mov     dx,offset msg6
        jmp     init_err            ; EMM version too low, exit

init6:  mov     ah,41h              ; get page frame segment
        int     67h
        or      ah,ah
        jnz     init45              ; jump if didn't get frame
        mov     page_frame,bx       ; save segment of page frame

        mov     ah,42h              ; get number of pages avail
        int     67h
        or      ah,ah
        jnz     init45              ; jump if error on get pages
        mov     total_pages,dx      ; save total EMM pages
        mov     avail_pages,bx      ; save available EMM pages
        or      bx,bx
        jnz     init7               ; proceed if some pages
                                    ; available
        mov     dx,offset msg4
        jmp     init_err            ; no EMS pages left, exit

init7:  call    get_kb              ; convert desired size
                                    ; of EMSDISK
        mov     ah,43h              ; try and allocate EMM pages
        mov     bx,owned_pages
        int     67h                 ; if allocation is
        or      ah,ah
        jz      init8               ; successful, jump
        mov     dx,offset msg5      ; if it failed, print
        jmp     init_err            ; error message and exit

init8:  mov     emm_handle,dx       ; save EMM handle
                                    ; for this driver
```

(continued)

```
         call    setup              ; set up BPB

         call    format             ; format the EMSDISK
         jnc     init9              ; jump if no format error
         mov     dx,offset msg7     ; formatting error, exit
         jmp     init_err

init9:   call    signon             ; format and display driver
         .                          ; identification
         .
         .
```

memory it occupies is discarded afterward. If it can't find the EMM or no pages are available, it aborts the installation of the entire program so that no system memory is wasted. (See listing 5.)

The driver proper is composed mainly of the read and write subroutines that transfer logical sectors to and from expanded-memory pages. Two other minor subroutines, media_chk and build_bpb, provide MS-DOS with information about the RAM disk's logical structure.

EMSDISK contains a fair amount of code that is not strictly necessary for its operation but is provided as an example of good behavior. This includes checking the DOS and EMM versions, testing the maximum command code passed to the driver in the request header, discarding the EMSDISK driver if the EMM cannot be found or if inadequate expanded memory is available, and using a local stack (to avoid overflowing the DOS stack) in the interrupt routine. On the other hand, I have omitted many optimizations from EMSDISK that could increase performance, such as conserving page mappings when multisector transfers are requested by DOS.

There are three values in the EMSDISK program that you may wish to fine-tune to change its behavior. Two of these are equates at the beginning of the program: sec_size, which sets the logical sector size (I have used 512 bytes for symmetry with other IBM media), and dir_size, which specifies the maximum number of entries in EMSDISK's root directory. The sector size should be an even multiple of 512 bytes (512, 1024, 2048, . . . , 16384). If you modify sec_size, you will need to set the non-IBM-format bit in the device-attribute word of the device header.

The third value that you can alter is the number of sectors per cluster. This value is calculated in the setup subroutine according to the number of logical sectors that will fit into the allocated expanded-memory pages. Raising the number of sectors per cluster trades wasted disk space for a faster access speed. On average, one-half cluster per file is wasted space on the disk.

A Lasting Effect

The RAM disk program EMSDISK is only one way in which you can use expanded memory. Several of the most popular spreadsheet and integrated data management programs have been released in new versions to take advantage of the additional fast storage that is provided by expanded memory. ■

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Inquiry 16

Performance Programming

Developing a single program for a variety of IBM PC compatibles

BY JOEL ROSENBLUM AND DAN JACOBS

IF YOU CREATE programs for the IBM PC, you often need to sell separate versions of your software for particular "compatible" machines. The wide variety of so-called PC compatibles creates problems for you as a software engineer trying to write one version of your program that operates on as many machines as possible.

As many buyers have already discovered, some IBM PC clones are not true clones at all. These machines either are enhanced with features that give them a marketing edge over the original IBM machine or are so restricted that they have trouble using common existing software such as Lotus 1-2-3 and dBASE III. All this hardware incompatibility makes it more difficult to design and sell your programs to everyone who can use them. Your customers send you back to the salt mines to develop 16 different versions of the same software product.

Defining Performance Programming

We have developed a methodology that lets you design "generic" software; it will operate with most IBM-compatible machines that use MS-DOS.

Best of all, our procedures will let your programs automatically take advantage of PC hardware features. Your programs will know when they can write directly to video memory or access the IBM BIOS low-memory variables. If your program encounters a machine it doesn't know, it can decide whether certain features exist for it to use or whether it should treat the new machine as generic until you can incorporate that machine's features into the next release of your software. We will also describe some methods that allow user-selectable compatibility so your customers won't have to wait for your next software release. Now you can sell only one version of your program. However, that version is special because you create it using a method we call performance programming.

We will explain how to program for performance while maintaining compatibility. Our approach is twofold. First, we define a generic PC as a model on which to base your program. Then we define and use a features table that automatically determines IBM PC compatibility by reading the manufacturer's copyright notice contained in the machine's BIOS ROMs. We next look at how you can use the presence of other equipment within your machine to set "performance bits" and how you can incorporate that information into your overall program design. Finally, we will give some examples relating to processor detection and speed determination, video capability, extended character set presence, ANSI cursor addressing, and use of other set bits in your program.

Defining the Generic PC

We define a generic PC as a computer that is only minimally compatible with the IBM PC. The requirements of our theoretical generic PC design are the presence of an Intel 8088 or equivalent processor, the ability to read/write either IBM PC 5¼-inch or 3½-inch disks, MS-DOS, the ability to

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ILLUSTRATED BY ALEXANDRA BOIES

display 25 lines of either 40- or 80-column text, and an ASCII keyboard without cursor and function keys.

Our generic PC does not include the following features present in a true IBM PC: an IBM extended character set, direct cursor-key positioning, bit-mapped screen graphics, the ability to use BIOS calls and corresponding access to low-memory variables, and the ability to access hardware directly.

We assume that a generic PC has a text-only screen display that supports only the standard ASCII character set and has a keyboard without cursor-positioning or function keys. You might note that the Zenith Z-100 is close to qualifying as our theoretical generic PC. Also, the generic system does not have an IBM- compatible BIOS even though it supports MS-DOS. This implies that all operating system function calls for a generic PC must occur at the highest level, which in this case is by using DOS system interrupt calls 20h through 27h. More information about these OS interrupt calls appears in IBM's *Disk Operating System Technical Reference*, available through IBM dealers or directly from IBM (write IBM Technical Directory, P.O. Box 2009, Racine, WI 53404-3336 or call (800) 426-7282).

The advantages of generic PC software are threefold. From your standpoint as a programmer, your software will work on most IBM PCs and compatibles. As a software publisher and dealer, you have to stock and sell only one version of a program. Finally, as a user, you do not need to be concerned about program compatibility or special steps to install the software on your IBM PC–compatible hardware.

On the other hand, generic software cannot take advantage of the advanced features present in the original IBM PC and some compatibles. Software with only scrolling generic screens and no graphics capability is not acceptable for some users. Here the second part of our methodology, the features table, comes into play.

DEFINING A FEATURES TABLE

A features table lets your programs take advantage of a particular compatible's features by determining the equipment your program is operating on. Your software automatically enhances itself for certain compatibles, so your program runs faster and more efficiently and has an improved user interface.

If your program is to operate with this type of intelligence, it must reliably determine the equipment. Your software can't read the label on the outside of your compatible, so we rely primarily on the copyright notice contained inside the machine's BIOS ROMs.

When an engineer designs a PC compatible, he or she incorporates into that machine's ROMs a set of routines that directly control the hardware. Those routines are the BIOS. A manufacturer of PC compatibles can write his or her own BIOS or purchase a BIOS from another manufacturer such as Phoenix Software Associates or Faraday Electronics.

The manufacturer can also market a machine that is made by an OEM. The OEM usually brands its machines by placing a copyright notice within the BIOS code. An example is the AT&T PC 6300, which is manufactured by Olivetti. Olivetti purchases the BIOS for its machine from Phoenix Software Associates. So what is the resulting copyright notice inside the user's 6300? It is the string "OLIVETTI," followed by some text.

Copyright notices thus far have been an unofficial method of determining a machine's manufacturer. The method is not 100 percent reliable, however, since the manufacturer might decide, for whatever reason, to change the location or actual string of the copyright notice. To prevent problems with your users, we have provided some software escape hatches. When your program cannot locate the copyright, the software will default to its generic-machine mode. However, some of your users might not be satisfied with the resulting loss of performance, so we also suggest that you incorporate into your program a method for the user to set the machine's compatibility level. Here are three examples of how to do that.

First, you can let your user input a slash option such as /IBM when invoking your software with its command string, as in

```
yourprm /IBM
```

A good example of a program that uses the slash-option approach is Microsoft's SYMDEB.

Second, you can incorporate an "It's a compatible" override as part of an optional installation process. Finally, you can let your user set compatibility as part of the DOS environment. For example,

```
set compatibility = IBM
```

The use of any of these methods in your program lets those users who need more performance obtain it. When a new machine appears on the market, advanced users will be able to use that machine to its fullest potential.

An example of a C-language implementation of a features table is presented in listing 1. [*Editor's note: Only listings 1, 2, and 3 are reproduced here. The entire set of listings* (1 *through* 9) *is available for downloading. See the note at the end of this article.*] In that example, machine characteristics are defined as bit flags in the variables FEATURES and VIDEO_FEATURES.

You should develop your own set of bit flags for the features your program needs to use. These bit flags are bits that you can set either off or on and that exist within a word. For example, if we set bits 1, 4, and 8 of a word "on" while leaving the remaining bits "off," the value of that word is 13 hexadecimal. Since we are interested in determining only if particular bits within the word are set, the value of the word is not important. Instead, we extract the bits that we are interested in by using a mask. Our sample programs in the listings illustrate how the mask is used.

Some of your programs might require information about the compatible's operating system version or the availability of certain BIOS calls. We will not discuss the detection of this additional information here, but we

(continued)

Listing 1: A *sample features table, as described in the article.*

```
/*

*/

/*
   This code contains a C language Features Table which contains the location
   and copyright string that uniquely identify a machine.  In addition to the
   copyrights, the bit fields for the  FEATURES and  VIDEO_FEATURES variables
   are defined. Note that this code is compiled with the Lattice  C  Compiler
   version 2.15, using -md -n options.  Copyright  (c)  1986  Dan Jacobs  and
   Joel Rosenblum for public, unrestricted use.
*/

/* bit flags for FEATURES */

#define IBMPC          0x0100  /* IBM PC, XT, Portable, */
#define IBMPCAT        0x0200  /* IBM AT */
#define IBMCOMPAT      0x0400  /* IBM PC BIOS Compatible */
#define IBM_CONVERT    0x0800  /* IBM Convertible */
#define GENERIC        0x1000  /* Assumed generic PC */
#define NO_DMA         0x2000  /* Machine has no DMA */
#define WANG           0x4000  /* Wang PC special case*/
#define TIPROF         0x8000  /* TI Professional PC special case */
#define CPU_88         0x0001  /* 8088, 8086 processor */
#define CPU_186        0x0002  /* 80188, 80186 processor */
#define CPU_286        0x0004  /* 80286 processor */
#define CPU_V20        0x0008  /* V20, V30 processor */
#define NDP            0x0010  /* 8087, 80287 math coprocessor */

/* bit flags for VIDEO_FEATURES */

#define CGA            0x0001  /* IBM Color Graphics Adapter */
#define MONO           0x0002  /* IBM Monochrome Adapter */
#define HERCULES       0x0004  /* Hercules Monochrome Adapter Card */
#define PGA            0x0008  /* IBM Professional Graphics Adapter */
#define EGA_MONO       0x0010  /*  w/Monochrome Monitor */
#define EGA_COLOR      0x0020  /*  w/Color Monitor */
#define EGA_HIGH       0x0040  /*  w/High Resolution Color Monitor */
#define UNKNOWN        0x0080  /* Unknown graphics type */
#define ANSI           0x0100  /* ANSI.SYS installed */

/* Additional bit fields may also be defined, please see TABLE 1 for suggestions */

struct machine_info {
    char    *logo;  /* Unique copyright string */
    long    addr;   /* String memory location  */
            /* Note: actually (char *) must be (long) to pass Lattice C */
    int type;    /* Machine attributes */
} feature_table[] = {

/*      copyright notice, physical address, pctype */

    { "IBM", 0xFE00EL, IBMPC|IBMCOMPAT},      /* All IBMs */
    { "COMPAQ", 0xFFFEAL, IBMCOMPAT},         /* All Compaqs */
    { "Corona", 0xFE00F, IBMCOMPAT},          /* Old version Corona */
    { "Corona", 0xFE01A, IBMCOMPAT},          /* Version 3.10 ROM Corona (also Phillips) */
    { "M.P.C.", 0xFDB2D, IBMCOMPAT},          /* New Columbia */
    { "Columbia", 0xFF768, IBMCOMPAT},        /* Old Columbia */
    { "Eagle PC", 0xFFFAA, IBMCOMPAT},        /* Eagle PC */
    { "Eagle PC", 0xFF810, IBMCOMPAT},        /* Eagle PC Plus */
    { "Zenith", 0xFB000, IBMCOMPAT},          /* Zenith Data Systems */
    { "Zenith", 0xFC2FF, GENERIC},            /* Zenith 100 */
    { "MITSUBISHI", 0xFC02A, IBMCOMPAT},      /* Sperry PC and Leading Edge */
    { "TVS", 0xFE003, IBMCOMPAT},             /* TeleVideo */
    { "OSM", 0xFFFF5, IBMCOMPAT},             /* OSM Rom Version 3.6 or later */
    { "OLIVETTI", 0xFC050, IBMCOMPAT},        /* AT&T-IS PC 300 and Xerox  */
```

(continued)

```
                                              /* NOTE: AT&T is not supporting V1.0 ROMs */
    { "WANG", 0xFFFC2, WANG|GENERIC},         /* WANG Professional */
    { "ADDS", 0xFC050, IBMCOMPAT},            /* Applied Data Digital Systems Model PC/I */
    { "CROS", 0xFE000, IBMCOMPAT},            /* Seattle Telecom Turbo Boards */
    { "PCPI", 0xFE00F, IBMCOMPAT},            /* Personal Computer Products */
    { "TAVA", 0xFE018, IBMCOMPAT},            /* Tava PC */
    { "Tandy", 0xFC02B, IBMCOMPAT|NO_DMA},    /* Tandy 1000 has no DMA without memory upgrade */
    { "Tandon", 0xFC013, IBMCOMPAT},          /* Tandy 1200 */
    { "Texas", 0xFE022, TIPROF},              /* TI Professional V1.23 & V2.11 SYSROM */
    { "American", 0xFE004, IBMCOMPAT},        /* American PC lookalike */
    { "STD", 0xFE00EL, IBMCOMPAT},            /* STD Turbo Boards in IBMs */
    { "STD", 0xFFFEAL, IBMCOMPAT},            /* STD Turbo Boards in COMPAQs */
    { "TOMCAT", 0xFE028, IBMCOMPAT},          /* Tomcat AT clone */
    { "WYSE", 0xFC003, IBMCOMPAT},            /* WYSE PC BIOS Version 1.08 */
    { "Hewlett-Packard", 0xF0024, IBMCOMPAT}, /* Hewlett-Packard Vectra AT Compatible */
    { "Morrow", 0xFE073, IBMCOMPAT},          /* Morrow Pivot II & Zenith 171 Desktops */

    /* Additional machines are added to the list starting here */

    { NULL, NULL, 0}
};
```

Table 1: A *summary of some bit-field considerations, information that programs might require before they can run on* IBM PC–*compatible systems.*

CPU-related features:
- detection of the primary processor in the machine
- detection of the processor's speed
- detection and use of coprocessors

Video-related features:
- present video type(s)
- present video mode
- installation of ANSI.SYS video device driver
- ability to use IBM expanded-video character set

Operating system–related features:
- availability of certain BIOS-level calls
- DOS version check

Disk-related use and detection:
- floppy and/or hard disk drive type
- floppy and/or hard disk drive size
- detection of floppy disk drive mode
- ability to use interrupt 13h calls
- DMA detection

have provided a summary of some bit-field considerations for use in the FEATURES variable in table 1.

The definitions are then followed by the copyright notices that appear in a structure containing the location and unique identifying string for some sample machine BIOS ROMs. Note that each defined machine in the table contains its own set of characteristics that are then placed in the bit-flag variable.

Two machines, the Wang PC and the TI Professional, are important examples of how you can use the table to deal with some unusual compatibility considerations. For example, the Wang PC requires clearing the direction flag before making disk I/O calls from assembly language routines. This problem does not occur when making the I/O calls from most high-level languages since, in these languages, the direction flag is usually left in the increment position. The TI Professional requires a substitution of interrupt 4Eh in place of any assembly language interrupt 13h direct disk I/O calls. Thus, listing 1 defines the special bit flags WANG and TIPROF. If your program needed to use any of these calls on one of these two machines, the defined bit flag would handle the branch within your program. Some examples of use of the bit-flag branch to control program performance optimization are contained in the Detecting Video Type section of this article.

The sample features table in listing 1 also shows how you might determine the presence of a turbo board. The copyright notice was given for an STD turbo board used in an IBM or Compaq PC. Again, once it detects the board, your program could act accordingly. Of course, your program could also incorporate detection for other installed circuit cards using their copyright notices.

In summary, the equipment features table places all the burden of compatibility and machine optimization in one convenient place. If a computer is not on the list, the program assumes it is generic. Otherwise, the capabilities of the machine are already "known" and your program would automatically use them. For new or previously unknown machines, your user must either accept the automatic generic-machine mode or override it by providing the program with performance optimization. Therefore, as a service to your users who prefer to use software as it comes off the shelf, you have a responsibility to keep your features table as up-to-date as possible. Perhaps the features table will become a public domain standard for use by all programmers.

USING THE FEATURES TABLE

Now that you have developed a features table, how do you use it in your code? Listing 2 contains a C-language routine that uses the features-table structure defined in listing 1 to determine machine compatibilities. The routine reads the copyright notice, if it can locate one, and sets the bits within the variable FEATURES. The routine also calls separate functions that set additional bits within FEATURES and VIDEO_FEATURES. Your program's code then checks the appropriate bit within the variable to determine if a particular ability exists for the machine on which your software is currently operating.

It is important that the routines in your program that use the features variables exist at the lowest level of your code. The reason for this is so that the rest of your program will sit above the machine's hardware and be oblivious to the equipment present. Your program will execute the appropriate routines based on the information contained within the variables. For example, suppose your software could speed up its disk access by using BIOS interrupt 13h calls. If FEATURES indicated that the machine your software is currently operating on is 100 percent IBM-compatible, then you would use the BIOS interrupt; otherwise, you would use DOS interrupt calls 25h and 26h to access the disk. In effect, you create a device-independent interface for your program. If you later find that you need to define another FEATURES bit or you need to extend the length of the FEATURES variable, you will be able to make the change with a minimum of recoding.

Now that we have defined the bits

(continued)

Listing 2: *C-language routine that uses the features table of listing 1 to determine machine compatibility.*

```
/*

*/

/*
   This code shows  how the Features Table is used to set up
   the bit flags  in the FEATURES  variable.  Once  FEATURES
   is  set  for  the  current  machine,  your  other program
   modules can  use it to  determine what  section  of  code
   should be executed to yield the best program performance.

   Copyright (c) 1986 Dan Jacobs and Joel Rosenblum

   Compiled using Lattice C ver 2.15, using -md -n options
*/

unsigned int video_features;   /* global variable which holds video attributes */

unsigned int set_features()
{
     char *cp;                    /* Pointer */
     struct machine_info *p;      /* Features Table Structure */
     unsigned int feature;        /* FEATURES bit field variable */

     /* Assume the PC is generic to start */
     feature = GENERIC;           /* default to generic */

/*
   A pseudo code example of how to override the automatic set of FEATURES
   assuming that either a slash option  or a DOS environment variable is
   set.  Your actual code will depend upon how you do the parsing.  See
   the  section  on using the  machine's copyright notice to determine
   compatibility  in our text.

begin pseudo code example --

     if ((/IBM entered on command line) |
         (compatibility = IBM is in the environment)) {
         feature = IBMCOMPAT;
         goto cpu_test;
     }
-- end pseudo code example */

     for (p = feature_table; p->addr != NULL; p++) /* If next table entry is NULL, end loop */
         if (strncmp((char *) p->addr, p->logo, strlen(p->logo)) == 0) {
             feature = p->type;
             break;
         }

     if (feature & IBMPC) {           /* IBM Personal Computers */
         cp = (char *) 0xFFFFE;        /* physical address 0FFFF:E */
         switch (*cp) {
             case 0xF9:  /* IBM Convertible */
                 feature |= IBM_CONVERT;
                 break;
             case 0xFC:       /* IBM AT */
                 feature |= IBMPCAT | CPU_286;
                 break;
             case 0xFD:  /* IBM PC JR */
                 feature |= NO_DMA;
                 break;
             case 0xFE:  /* IBM XT or Portable */
             case 0xFF:  /* IBM PC */
                 break;
             default:
                 break;  /* unknown IBM type */
```

(continued on page 190)

that make up the variables, the next sections will show you the details behind setting those flags. These examples illustrate how your programs can detect such features of your machine as its processor, effective clock speed, and video display. These routines are the foundation for the creation of your own hardware-independent modules.

DETERMINING CPU TYPE

Software that is dependent upon processor type needs to determine under which processor it is operating. Examples include operating system software that might require the use of certain processor modes such as the Intel 80286's protected mode or the use of the PUSHA instruction on the 80186.

Listing 3 gives a C-callable assembly language routine that you can use to determine the presence of the Intel 8088/8086, 80186, and 80286 processors and the NEC V20 and V30 processors, so you can set the corresponding bit in FEATURES.

Your program's performance might improve by detecting and using a math coprocessor. Examples include programs with heavy trigonometric or floating-point operations such as statistical analysis and speech-processing software. Two methods for detecting a math coprocessor are in listing 4.

Finally, it might be important to determine the processor's clock speed. Timing loops are an important part of communications software, and the assembly language procedure in listing 5a lets you set processor-speed-independent timing loops. Listing 5b shows an example of how to use the timing routine.

DETECTING VIDEO TYPE

Automatic video detection should be an almost universal part of your software if you want to display any of the IBM extended character set or bit-mapped graphics on the video display. Further, automatic display-type determination eliminates placing the burden of video-display installation

(continued)

on the user. Of course, a feature that lets users override this display determination, similar to the ones described in the copyright-notice section of our article, could be incorporated into your program.

Video detection starts with determination of the active display-adapter type. The five major adapter types are IBM Monochrome Adapter, Hercules Graphics Card, IBM Color Graphics Adapter (CGA), IBM Enhanced Graphics Adapter (EGA), and IBM Professional Graphics Adapters (PGA). The procedure in listing 6 detects these adapter types and sets the appropriate performance bits in the variable VIDEO_FEATURES.

The performance bits in VIDEO_FEATURES activate code within your program, which can then take advantage of the selected display adapter's features. Programs that allow use of the EGA's colors, for instance, could be set active when that adapter type is detected. You could also use VIDEO_FEATURES bit flags to politely notify your user that a particular display is not present if, for instance, your software absolutely requires the use of that display.

If none of the above display adapters is in the compatible's hardware, the display might still have the ability to position the cursor directly on the screen. Direct cursor positioning lets screen displays appear without scrolling. Displays with this capability are ANSI-compatible. ANSI compatibility implies that the ANSI.SYS device driver has been installed by the user as a part of the CONFIG.SYS file on the compatible machine. If you incorporate the code contained in listing 7 into your program, the program will be able to directly check whether ANSI.SYS has been installed on the user's machine.

In addition to determining ANSI compatibility, you might want to take advantage of the IBM extended character set so that you can design screen displays and menus to look better. Screen enhancements such as character blinking, underlining, and boldface might also be possible. We

(continued)

```
        }
    }

    /* add the cpu type to FEATURES -- see listing 3 */
    feature = cputest(feature);

    /* check for numeric data processor -- see listing 4 */
    feature = test_ndp(feature);

    /* add the video display type to VIDEO_FEATURES -- see listing 6 */
    video_features = video_test(feature);

    /* check if  ANSI.SYS is present -- see listing 7 */
    if (check_ansi()) {
            video_features |= ANSI;
        } else {
            putch(0x0D);  /* This cleans up any garbage left on the screen */
            putch(' ');   /* by the ANSI check if ANSI.SYS  is not present */
            putch(' ');
            putch(' ');
            putch(' ');
            putch(0x0A);
            putch(0x0D);
        }

        return (feature);
    }
```

Listing 3: A *C-callable assembly language routine for determining the type of microprocessor used in an* IBM PC *compatible.*

```
; Cputest.asm is the Lattice C-callable assembly language routine that determines
; the machine's processor type. Copyright (c) 1986 Dan Jacobs and Joel Rosenblum

        name    cputest         ;determine CPU type
        include dos.mac         ; Lattice C memory model configuration macro
                                ; In this case it is a copy of dm8086.mac

; processor type equates
CPU_88     equ 01H        ; Intel 8088 - 8086
CPU_186    equ 02H        ; Intel 80188 - 80186
CPU_286    equ 04H        ; Intel 80286
CPU_V20    equ 08H        ; NEC V20 - V30

        PSEG

comment\**********************************************************************

NAME
        cputest
SYNOPSIS
        unsigned int cputest (features)
        unsigned int features;          see definition of machine type
DESCRIPTION
        returns features with the proper active CPU type or'ed in

***************************************************************************\

                public  cputest
cputest         proc    near

                push    BP              ; save the frame pointer (if called from C)
                mov     BP, SP
                                        ; next, save the passed existing features
                mov     AX, 4[BP]
```

(continued)

PC-DESK
TAKES YOU BEYOND SIDEKICK

PC-DESK. The Ultimate in Desk-Top Management

Now, finally at your command. A completely integrated word processor, calendar/reminder, name/address/phone database and directory. Letter/label/report printer, mailmerge, invoice system and printing calculator.

PC-Desk does just about everything you need. It's a powerful and easy-to-use tool that reduces your work and makes your business life easier. And, it does more than hundreds of higher-priced programs.

The Most Powerful Feature

PC-Desk automatically prepares your letters, invoices and memos.

It's fast and easy to send individually typed, personalized letters, either singly or by the hundreds. Just select the names you want. Tell PC-Desk which letter to send, and it does the rest.

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PC-Desk is simply spectacular. Users say, "This is the way software ought to be!" Try it for 60 days. If you're not completely satisfied, return it for a full refund.

Free Updates, Free Support.

That's right. Free updates. (Remember, if you already own PC-Desk, send for your free update to version 6.5.)

And, if you ever need help, just call us. We'll talk you through it.

Look At Everything You Get!

Easy Instructions
Step by step directions on the screen. You'll always know what codes to use. Even if you're new to computers, you'll be efficient right away.

Calendar/Reminder
24 reminders per day. Reminder days are highlighted. Put the cursor on any day. . . all your reminders pop up. See a full month at a time. Flick back and forth between months. Print reminders with a single keystroke. You're organized and you'll stay organized.

To Do List
Tracks up to 20 projects. You'll never forget what you need to do.

Word Processor
Full-featured. . .why use any other word processor? PC-Desk gives you professional-looking documents. . .with bold, underlining, centering, and justification. Word wrap, block move, search, margin settings. And no waiting for screens to come up with Turboscreen.

Personal Address Book
Automatically printed in a pocket-sized format. Cross-indexed by company name. Breast-pocket holder free when you order PC-Desk.

Database
Outstanding organization and flexibility. Easy to access and maintain. Name, address, phone number (work and home), salutation, title, date, variables for automatic printing, comments, and more. Sort on zip, or alphabetically by name or company. Search, scroll through, change or delete. Select names for group mailings. Make notes on client contact. Print your rolodex, envelopes, (with return address too), letterheads, invoices, labels, entire name and address file.

Mail Merge
Fully integrated with database. Letters with up to four variables.

Calculator
Print your calculations. Pops up into word processor. Hex, binary, and octal for programmers.

Memory Partitioning
Lets you flip back and forth between PC-Desk and other programs. Cut and paste.

Logs
Client billing, computer use, telephone, and expense logs. Great for tax records! Print monthly statements with total time and expenses. Edit your logs. With auto-dialer calls are logged automatically.

Auto-Dial
Save time! Auto-dial any phone number in your database. Choose work or home number.

Encrypt
Protect your files from prying eyes.

DOS Functions
Copy, delete, print, view, renamefiles easily.

On-Screen Clock

Manual
Full instructions.

Not Copy Protected

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```
            push    AX
        ; check for  8088 or 8086  by using the  SHR instruction  since the
        ; 8088 and 8086 do not mask cl with 07H before executing the shift.
            mov     CL, 20H
            mov     AX, 1
            shr     AX, CL
            test    AX, AX          ; if after the shift AX is the same
                                    ; as before, it's an 8088 - 8086 or V20 - V30
            jnz     check_80186     ; else, continue checking other Intel CPUs
        ; check for V20 or V30 by detecting if PUSHA is a valid instruction
        ; on the NEC CPUs
            mov     BX, SP          ; save SP
            pusha
            cmp     BX, SP          ; if SP has not been decremented, then
            je      is_88           ; it's an 8088 - 8086
            popa                    ; else, we restore registers
            mov     AX, CPU_V20
            jmp     return
is_88:      mov     AX, CPU_88
            jmp     return
check_80186:
        ; check for the 80188 or 80186 by detecting if SP is updated
        ; before or after it is pushed.
            push    SP
            pop     BX
            cmp     BX, SP
            je      is_286          ; if updated after, it's an 80286
            mov     AX, CPU_186     ; else, it's an 80186 or 80188
            jmp     short return
is_286:     mov     AX, CPU_286

return:     pop     BX              ; recall saved features
            or      AX, BX          ; and or cputype into other features bits
            pop     BP
            ret
cputest     endp
            ENDPS
            end
```

```
 ┌──────────────────────────┐        +---------------------------+
 │ IBM extended characters  │        | Standard ASCII characters |
 └──────────────────────────┘        +---------------------------+

     100 percent IBM PC                   Generic MS-DOS
   compatible display box                  display box
```

Figure 1: *Two boxes drawn by the routine in listing 8, on a system that has the IBM extended character set available (left) and on a system that does not and uses only ASCII characters (right).*

assume that a machine has an extended character set if it has the IBMCOMPAT bit set in the variable FEATURES.

The sample program in listing 8 shows how to draw a simple box that could take advantage of the machine's ability to use the IBM extended character set. The draw_box routine uses the IBMCOMPAT bit flag contained in FEATURES to determine which character set can be displayed. Figure 1 shows the difference between boxes drawn with the two sets.

The draw_box routine uses a routine called move_cursor, which is contained in listing 9. Whereas draw_box uses a bit flag set in FEATURES, move_cursor relies more directly upon the video hardware. Thus, it uses bit flags set in VIDEO_FEATURES, as well as a bit set in FEATURES. Move_cursor then moves the cursor to the position row, column. It decides which method is needed to move the cursor on your particular machine without burdening the calling program with the task.

Note that if your program detects the presence of ANSI.SYS operating on a machine that is IBMCOMPAT and sets screen attributes using BIOS-level video calls, then it should not use the low-level video DOS calls to display additional text. To do so will overwrite the attributes you have just set with what ANSI.SYS believes the attributes to be. Complicated prob-

(continued)

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Incorporating processor- and speed-detection procedures into your program allows for run-time performance determination of the PC compatible. Based on that run-time analysis, you could enable sections of optimizing code in the program by setting your program's "performance bit flags." For example, a multiuser spreadsheet program that allows for multiple users only if operating on an 80286-based system could determine if the processor type was an 80286. If so, a flag within the software could be set that allows multiuser capability. Then detection would proceed to determine the presence of a math coprocessor. If an 8087 or 80287 was detected, a bit would enable use of the hardware-based math routines. Finally, your device time-out loops could be adjusted according to the results of the processor-speed check. Combining this analysis with the screen display lets your spreadsheet program allow charts and plots to appear on the screen, if possible.

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Editor's note: The listings from this article are available on disk, in print, and on BIX. *See the insert card following page 176 for details. Listings are also available on* BYTEnet. *See page 4. Listings 1, 2, 5b, 7, 8, and 9 are C source code and are available as the file* PERPROPC.C*; listings 3, 4, 5a, and 6 are assembly language code and are available as the file* PERPROPC.ASM. *You will need the Lattice C compiler or a compatible C compiler to use the source code listings.* ■

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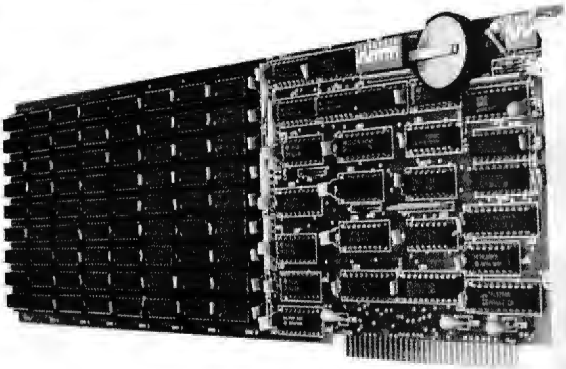

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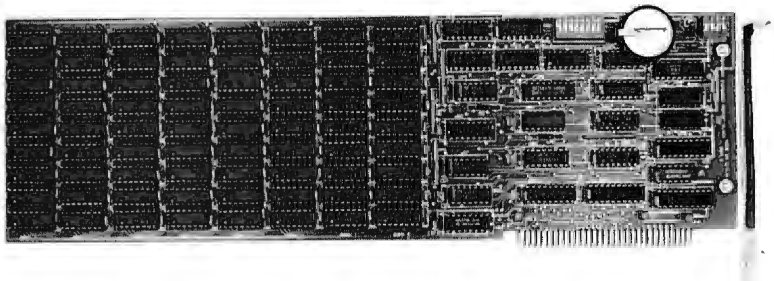

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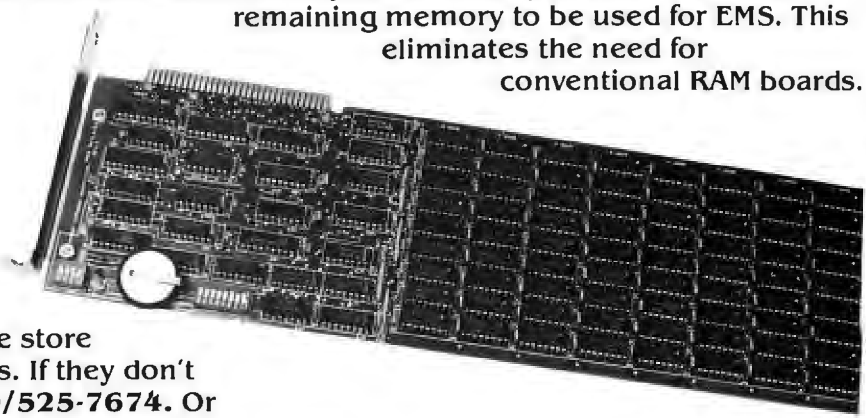

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Inquiry 55

RAM-LOADABLE CHARACTER SETS FOR THE IBM PC

How to create and use RAM-based character fonts

BY RICHARD WILTON

MOST IBM PC users take for granted the size and shape of the characters on their video displays. However, the newer video display adapters from IBM and Hercules let you change the font of the displayed characters, as well as the set of displayable characters, without compromising the display's speed or clarity.

The ability to display characters of arbitrary size and shape helps programmers make the user interface more natural. For example, a word-processing program can display characters exactly as they will appear on the printed page. Foreign-language alphabets, mathematical symbols, and simple graphics elements can all appear on a single screen.

Almost all the video display adapters available for the IBM PC can display some sort of customized character set (see table 1). Some adapters provide more built-in support for custom character sets than others. In general, a greater amount of hardware and firmware support simplifies character-set software and delivers greater speed.

There are two general approaches to displaying customized character sets on an IBM PC. One is to define and display each character with special software routines. The other is to load a table containing formatted descriptions of each character into RAM where a hardware character generator can display them. I will focus on programming for such RAM-loadable fonts. I'll explain how to create them and how to apply them on commonly available IBM PC video adapters.

ALPHANUMERIC CHARACTERS

A close look at the characters on your video display reveals that each one is composed of a group of dots. A hardware or software character generator puts the dots on the screen in the patterns that you see as individual characters.

To display alphanumeric characters using an IBM PC video adapter, you must store the code for each character in a buffer in the adapter's video display RAM. Data bytes in the video display buffer represent these character codes. Each 8-bit byte from 0 to 255 (0 to 0FF hexadecimal) is interpreted as a character code that corresponds to a single character in an extended ASCII character set.

Every IBM PC video adapter includes a hardware character generator that displays the dot pattern corresponding to the character codes in the video display buffer. The dot patterns are stored in an 8K-byte table in ROM and are indexed by the character code. Thus, for each character code in the video display buffer, the character generator copies the corresponding dot pattern to the video display screen (see figure 1).

SOFTWARE CHARACTER SETS

Many IBM PC video adapters support one or more *all-points-addressable* (APA) display modes that let you place individual dots directly on the display. Such adapters can interpret the data in the video display buffer as a bit stream that corresponds to the appearance of points on the screen. You can draw characters on the display by setting the appropriate bits in the video display buffer.

[*Editor's note: There are 7 programs that illustrate many of the concepts explained in*

(continued)

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Table 1: *Support for custom character sets on video display adapters.*

	APA graphics	BIOS support for APA graphics characters	RAM-loadable character sets
MDA	no	no	no
CGA	yes	yes	no
PCjr	yes	yes	no
EGA	yes	yes	yes
HGC	yes	no	no
HGC Plus	yes	no	yes

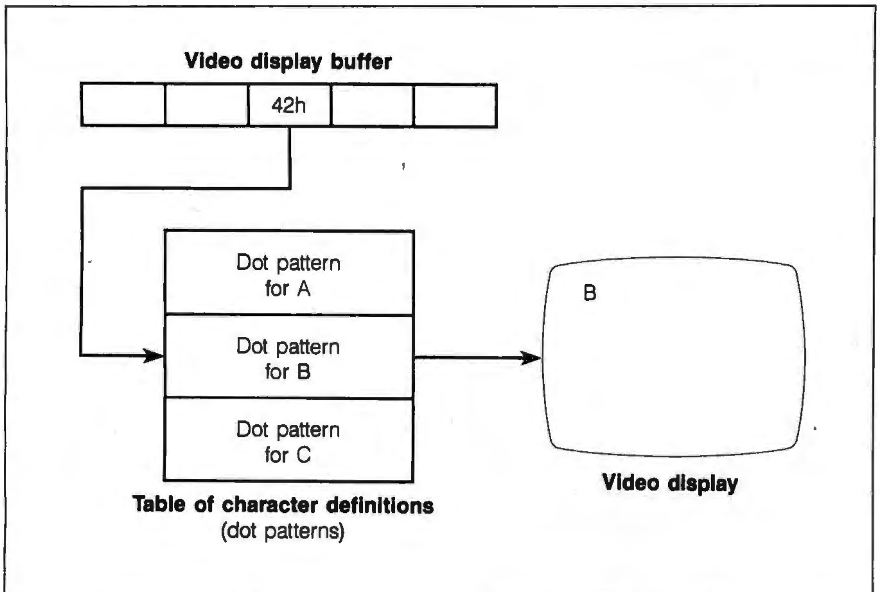

Figure 1: A *block diagram for an alphanumeric character generator.*

this article. They are available on disk, in print, and on BIX. *See the order card following page* 176 *for details. Listings are also available on* BYTEnet. *See page* 4.]

Because it is under software control, this table-driven technique is extremely flexible. The characters you draw can be virtually any size and shape. Using a software character generator is also the best way to mix text with graphics images because you have point-by-point control over arcs, lines, and other graphics elements as well as text characters.

IBM's Color Graphics Adapter supports a software character generator in its ROM BIOS. The routine uses the address in interrupt vector 1Fh [*Editor's note: For the remainder of the article, all interrupt vectors and addresses will be in hexadecimal.*] to locate a character-definition table for ASCII characters 80 through FF. If you store the address of your own character-definition table in this interrupt vector, the BIOS character-generator routine will use your character set for ASCII characters 80 through FF hexadecimal (see the program CSLS2.ASM for an example).

Unfortunately, the BIOS definitions for ASCII characters 00 through 7F hexadecimal are always taken from a table in ROM at address F000:FA6E. Thus, you still need to do some special programming if you want to customize the first 128 ASCII characters, 00 through 7F.

However, IBM's Enhanced Graphics Adapter lets you define all 256 characters for APA graphics. The address of your character-definition table is passed to the BIOS using interrupt 10h, function 10h. When the BIOS is subsequently called upon to display graphics characters, the BIOS routine uses your character-definition table in RAM rather than its default table in ROM.

Whether you write them yourself or use the ones provided in IBM's ROM BIOS, such APA software character generators are much slower than an alphanumeric hardware character generator. One reason is that you might need to write a considerable amount of code to implement a practical character-set generator. Even in assembly language, executing a sizable subroutine just to display a character of text can significantly slow down an application. Also, you have to manipulate much more data in the video display buffer when you draw each character explicitly. Lastly, software runs much more slowly than hardware.

RAM-LOADABLE CHARACTER SETS

A reasonable compromise adopted by IBM on the EGA and by Hercules on the Graphics Card Plus is to implement a hardware character-set generator that can use a table of character definitions that you load into RAM rather than store permanently in ROM. This approach does not provide as much flexibility as the use of a software character generator but preserves the speed advantage of using a hardware character generator.

Using a RAM-loadable character set requires that you accomplish three programming tasks. First, you must create a table containing the dot-pattern definitions for your character set. Second, you must load the character-definition table into RAM. Third, you have to program the video adapter's CRT controller to display your characters.

CHARACTER-SET DEFINITION

To define a character set, you create an ordered list of the dot patterns that

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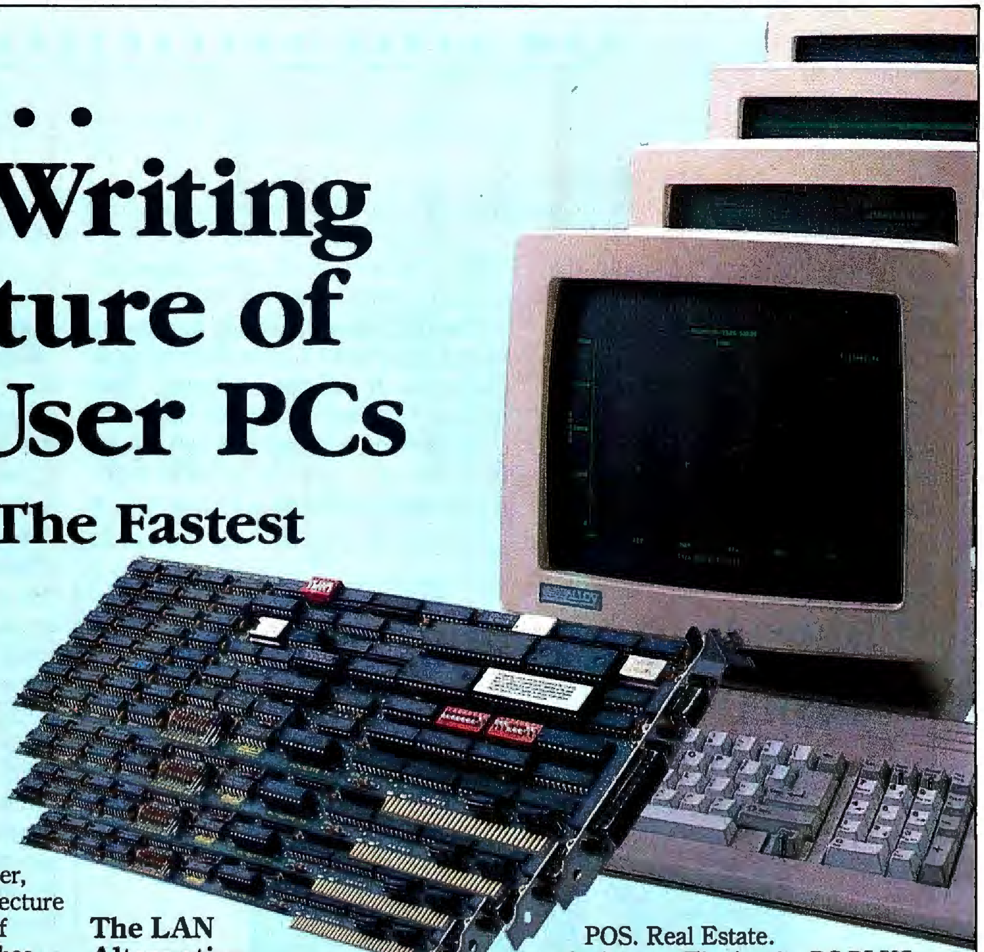

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make up the characters. Usually, the order in which the characters appear corresponds to the ASCII character sequence. Of course, many applications demand the use of other character-set sequences. For example, you might want to use the EBCDIC character sequence, a foreign-language character set, or even a set of graphics "tiles" that you could piece together to form larger graphics images.

The HGC Plus character generator uses a table in RAM that defines each character in exactly 16 bytes. This means that the maximum size of a character in the table is 8 dots wide (the size of 1 byte) by 16 dots high. If you wish to define a character set in which the characters are less than 16 dots high, you need to pad each character definition out to a total of 16 bytes. When you program the HGC Plus's video controller to display characters that are less than 16 rows high, the extra padding is ignored.

The EGA's character-generator table is similar except that it has a 32-byte-per-character format. This means that character sets that utilize a small dot matrix contain a significant amount of padding. For instance, a table that defines an 8- by 8-dot character set would contain 75 percent padding.

For this reason, the EGA's ROM BIOS provides a routine that loads a table that includes no padding between characters. If your characters are defined in an 8- by 6-dot matrix, for example, each character definition is exactly 6 bytes long. If you save character-set definitions in disk files, this "compressed" format can save a fair amount of space. Also, since the ROM BIOS character-definition tables are stored in a compressed format, you can use the same EGA BIOS routine to load them into RAM as well. (The programs CSLS4.ASM and CSLS5.ASM contain examples of compressed and padded character-definition tables.)

Mapping Character-Generator RAM

You have to know exactly where in RAM to store your character-set definition table. Because the architecture of RAM differs among video display adapters, the way you load your character set into RAM is hardware-dependent.

All IBM PC video display adapters are designed with the video display refresh buffer located in RAM, built onto the adapter itself. When you use RAM-loadable character sets, this on-board RAM is partitioned so that a portion is used to store the character-set definition table. The method of partitioning reflects the underlying architecture of the adapter's on-board RAM.

The HGC Plus can use the 64K bytes of RAM from B000:0000 through

B000:FFFF as a video display buffer. However, when you use a RAM-loadable character set, only the first 16K bytes serve as the display buffer. The remaining 48K bytes, starting at B000:4000, can contain your character-set definition table.

IBM's EGA has a different RAM layout. Individual pixels are represented by corresponding bits in four parallel bit planes. All four bit planes occupy the same range of addresses in the 8088's address space. Each plane is individually addressable by modifying the contents of special registers on the EGA.

The EGA's alphanumeric character generator uses only one of the four parallel bit planes as a display refresh buffer. One of the other three bit planes is then used to store up to 32K bytes of character definitions for the character generator.

LOADING A CHARACTER-SET DEFINITION

Since different video adapters have different hardware configurations of video RAM, you must tailor your font-loading routines to the hardware you use. This task is simpler on the EGA with its fairly complete ROM BIOS support for loading character-definition tables into video RAM. On the HGC Plus, you must write your own software routines to load a font into RAM.

As you have already seen, the EGA and the HGC require that your character-definition table reside at a particular location in video RAM. On the HGC Plus, this location is at B000:4000 (see figure 2a). You can copy the table to this location from somewhere else in memory. (The program CSLS5.ASM shows an example of the copy operation.) If your character-definition data is stored in a disk file, however, you can read the data directly from the file to B000:4000. You can use MS-DOS function 3Fh of interrupt 21h to accomplish this.

Since the HGC Plus lets you use all 48K bytes of the on-board RAM between B000:4000 and B000:FFFF for your table, you can define up to 3072

(continued)

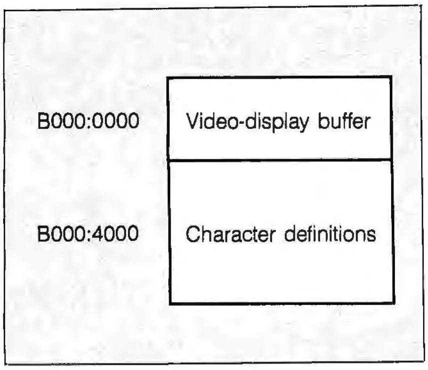

Figure 2a: *Video RAM configuration for the Hercules Graphics Card Plus.*

(49152/16) characters in a single table. However, the IBM PC BIOS and PC-DOS are capable of displaying only the first 256 characters. You can display all 3072 characters at one time only by changing the way character codes are stored in the video display buffer (this will be discussed further under "Extended Character Sets").

You must restrict the size of your character-definition table if your HGC Plus is installed in a system with another video adapter such as the IBM CGA, which uses RAM beginning at B800:0000 (B000:8000). In this case, you must limit your character-definition table to the 16K bytes between B000:4000 and B000:8000. This is done by resetting bit 1 of the HGC Plus's configuration switch (I/O port 3BF). Using only 16K bytes lets you define up to 1024 characters in your table.

On the EGA, you can load your character definitions in up to four RAM locations in bit plane 2 of the EGA's on-board RAM (see figure 2b). The maximum size of each character-definition table is 8K bytes (256 characters times 32 bytes per character). The actual number of character tables you can load at one time depends on the amount of RAM on your EGA: One RAM-loadable character set is supported for every 64K bytes of RAM on the card. Thus, the basic 64K-byte EGA provides enough RAM for only one table, while the fully loaded 256K-byte card supports four character-definition tables at once (see figure 3).

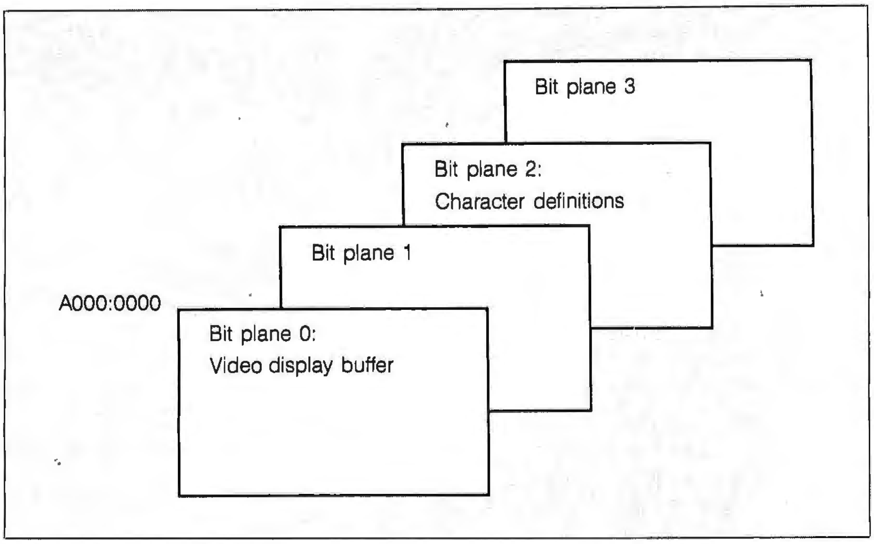

Figure 2b: *Video RAM configuration for IBM's Enhanced Graphics Adapter.*

Starting address		Total EGA RAM
A000:0000	8K character definitions	64K
	(Unused)	
A000:4000	8K character definitions	128K
	(Unused)	
A000:8000	8K character definitions	192K
	(Unused)	
A000:C000	8K character definitions	256K
	(Unused)	

Figure 3: *Bit plane 2 of the EGA's character-set RAM.*

Although you can define only 256 characters in each table, you can maintain up to four such tables in EGA RAM at once and display characters from any two of them at the same time. In other words, you can load as many as 1024 characters into RAM and display 512 of them at once.

The addresses of the 8K-byte tables are at 16K-byte increments in segment A000 (i.e., A000:0000, A000:4000, A000:8000, and A000:C000). Of course, if you want to write to these locations directly, you must selectively enable only bit plane 2 and disable the other three bit planes by programming the adapter's Sequencer Map Mask register. However, you may use EGA BIOS interrupt 10h, function 11h, to copy a character-definition table properly from any arbitrary address in RAM to any of the four available locations in bit plane 2.

PROGRAMMING THE VIDEO CONTROLLER

The third task you must accomplish in order to use a RAM-loadable character set is to program your video dis-

(continued)

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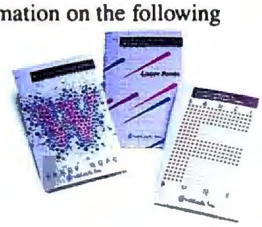

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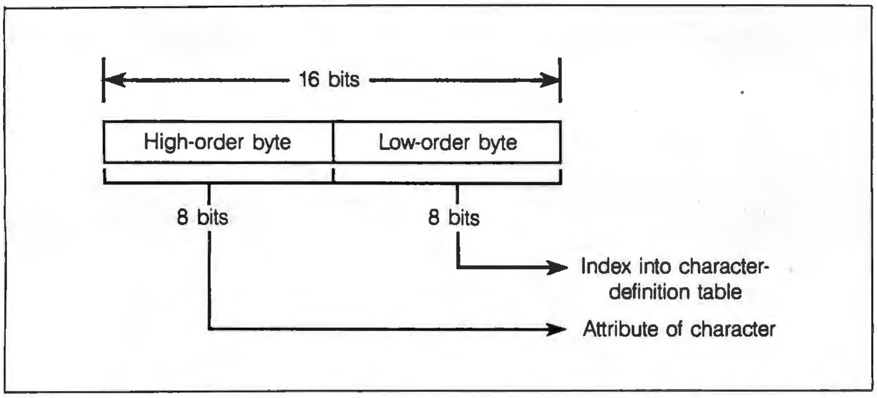

Figure 4a: *The video display buffer mapping of the alphanumeric modes of* IBM's Monochrome Display Adapter, CGA, *and* EGA, *and the Hercules Graphics Card Plus.*

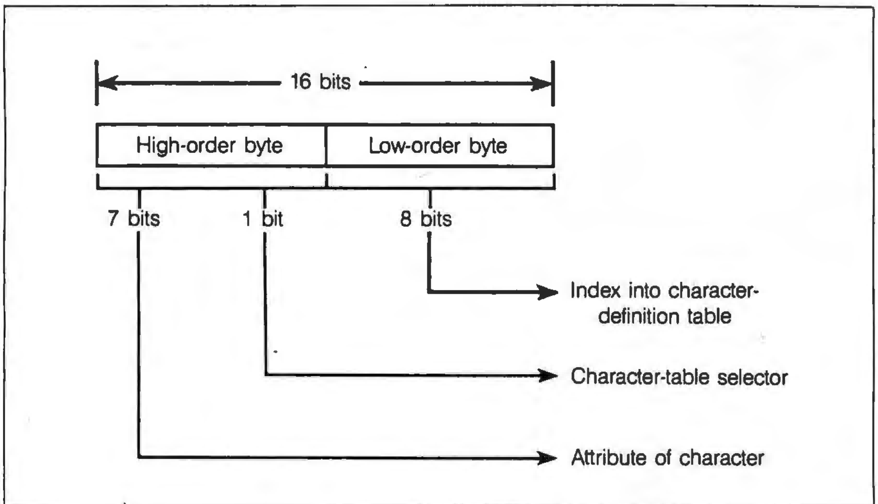

Figure 4b: *The video display buffer mapping of* IBM's EGA *extended character set. Bit 3 of the high-order byte selects one of two 256-character tables.*

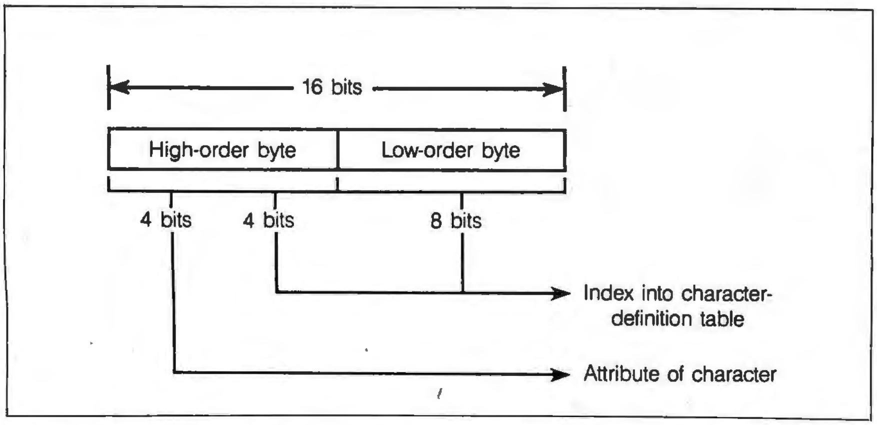

Figure 4c: *The extended character set of the* HGC Plus *video display buffer map. Bits 0 to 7 of the low-order byte are appended to bits 0 to 3 of the high-order byte to form a 12-bit index into the character-definition table.*

play adapter's CRT controller. On the EGA, the CRT controller circuitry resides in a special LSI chip with 27 internal registers. The HGC Plus uses a Motorola 6845 plus a proprietary chip that adds an additional 3 registers for controlling RAM-loadable font configurations.

The way you configure the CRT controller on the EGA and the HGC Plus depends primarily on the height of the characters in your character set. Hercules provides a table of register values for its CRT controller. Your program must explicitly load each of these values into the proper CRT controller registers.

Similarly, the EGA's CRT controller must be programmed to reflect the character height. In particular, the Maximum Scan Line, Cursor Start, Cursor End, Vertical Display Enable End, and Underline Location registers must be updated. Again, your task is simplified by an EGA ROM BIOS routine (interrupt 10h, function 11h). The BIOS routine calculates the correct register values given the number of bytes per character in your character-definition table and programs the CRT controller accordingly.

NINE-DOT-WIDE CHARACTERS

Although the height of the characters you define may vary, you might expect their width to be restricted to eight dots, since this is the number of bits in each byte of your character-definition table. However, both the HGC Plus and the EGA can be programmed to put 8-dot-wide characters on the screen in a 9-dot-wide matrix. The extra space between characters improves their appearance on a green IBM monochrome display.

To do this on the HGC Plus, you must set bit 1 in CRT controller register 14 hexadecimal. On the EGA, you reset bit 0 of the Sequencer Clocking Mode register. The EGA BIOS routines set this bit for alphanumeric display modes on a color monitor (8-dot-wide characters) and reset the bit for a monochrome monitor (9-dot-wide characters).

A subtle built-in function of both

(continued)

adapters relates to the use of the block-graphics characters, specified with character codes B0 through DF hexadecimal in IBM's PC character set. You can concatenate these characters to draw horizontal lines on the display. When they display characters in a 9-dot-wide matrix, the EGA and the HGC Plus copy the rightmost dot of all block-graphics characters into the extra space between characters. This ensures the continuity of horizontal lines.

EXTENDED CHARACTER SETS

When 8-bit codes represent characters in the video display buffer, a maximum of 256 (2^8) different characters can be displayed at one time. To display more characters than this, you must find a way to use character codes that are larger than 8 bits.

When IBM PC video adapters display text, 16 bits (one word) of data are actually stored in the video display buffer for each character on the screen. Usually, 8 of these bits encode the ASCII character number, while the other 8 bits specify attributes such as the character's color, intensity, blinking, or underlining (see figure 4a). The HGC Plus and the EGA use one or more of the 8 attribute bits to extend the range of character codes and thus increase the number of displayable characters.

On the EGA, the character-generator hardware can use bit 3 of the high-order byte to toggle two 256-character tables (see figure 4b). Which two of the four possible tables are actually used is determined by programming the EGA's Sequencer Character Map Selector register. Although it is possible to program this register directly, EGA ROM BIOS function 11h will perform this function for you.

On the HGC Plus, the character-generator hardware can use the low-order 12 bits of the 16-bit word as an index into the character-definition table at B000:4000 (see figure 4c). The character generator interprets character codes in this way when you set bit 2 of CRT controller register 14 hexadecimal. (The program CSLS7.ASM demonstrates this technique.)

In order to use the extended character sets on either adapter, you must write software routines to store character codes and attributes in the display buffer in the appropriate format. Unfortunately, software that uses extended character sets on the EGA will not format character codes and attributes correctly for the HGC Plus, and vice versa. Furthermore, all the IBM PC's BIOS routines assume that the video buffer is formatted for only 256 character codes (as in figure 4a). Programs that perform video output with BIOS calls or with PC-DOS calls (which in turn call the BIOS) will not

(continued)

run properly if your adapter is configured to display an extended character set.

UPDATING BIOS RAM

When you change the height or width of your character set, you implicitly change the screen's logical dimensions. The usual screen dimensions are 80 characters across by 25 characters down. Consider what happens when you use 8 by 8 characters on a screen that usually displays 9 by 14 characters, such as the green monochrome display: Your screen now displays 90 characters across and 43 characters down.

Although the ROM BIOS and PC-DOS are not always flexible enough to function correctly with screen dimensions other than 80 by 25 or 40 by 25, you can preserve a great deal of function by updating the status values stored by the BIOS in segment 40. In particular, several different BIOS routines use the words at 0040:004A (CRT_COLS) and 0040:004C (CRT_LEN).

PROBLEMS AND PITFALLS

I've alluded to one obvious problem with the use of RAM-loadable character sets: namely, that neither PC-DOS nor the ROM BIOS was designed to handle character sets of different-size characters. Also, neither DOS nor the BIOS can support the modified video buffer format required for extended character sets. When the usual DOS and BIOS video output routines are used with an extended character-set configuration, garbage characters appear on the display. The only solution is to be certain that an appropriate character set is available when control is transferred out of your application to DOS or to a BIOS video output routine.

A related problem crops up in a windowing or multitasking environment when a coresident program or an alternate task takes control of the display. Your program's character set and CRT controller configuration might be incompatible with those expected by some other task. At present there is no agreed-upon way to coordinate character set and video status between tasks. The problem might be solved with some type of global video status table or by a memory-resident display manager, but any such approach would have to be agreed upon by software developers to become usable.

Despite such potential pitfalls, the availability of RAM-loadable character sets in moderately priced video hardware should encourage their use by software developers. The reasonable compromise between the flexibility of dot-addressable graphics and the speed of a hardware character generator provides a way to improve the user interface in many applications. ■

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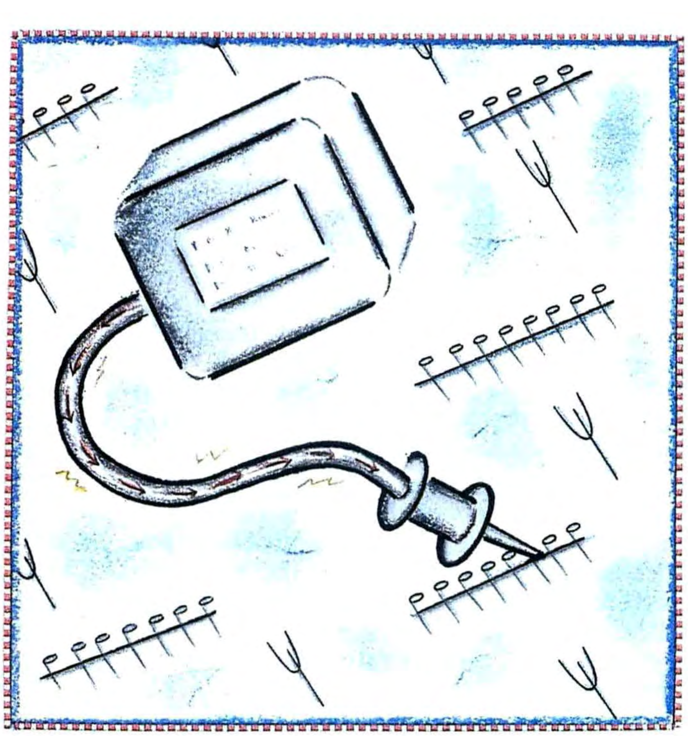
SPEEDING UP THE PC AT

Without spending a fortune, you can dramatically increase the AT's potential

BY BRIAN K. ROEMMELE



YOU CAN INCREASE the standard 6-MHz CPU speed of the IBM PC AT to 8 MHz with relatively low-cost modifications and replacement parts. All the critical components are socketed and easy to replace. You can obtain speeds faster than 8 MHz after testing and identifying the components that are not capable of higher speeds. How involved the speedup is depends on how fast you want your AT to go. The modifications can range from a simple crystal change to changing the CPU, RAM, and clock-generator chip as well as the crystal. Also, you will need to consider the speed limitations of any expansion boards you have in the system. I will explain how you can speed up your AT and describe the possible negative effects. [*Editor's note: See the "Benchmarks" text box for the results we got when speeding up one of* BYTE's ATs.]

It is rare to find a system that has so much upgrade potential with so little cost investment. The generous performance margins that Intel built into its chips, along with the predictable quality of the components on the AT's motherboard, let you increase performance without causing problems. Also, evidence suggests that the AT was originally designed for an 8-MHz CPU speed. First, the crystal is socketed rather that soldered, which is unusual for microcomputers. Second, in the schematics in the IBM *Technical Reference Manual* (Part #1502494, first edition, March 1984) the SysClk, ProcClk, and PClk traces all reference an 8-MHz bus, system frequency, and a 16-MHz crystal.

CRYSTALS

With a new crystal, you can increase the speed of your AT to 8 MHz. But the crystal you buy must be of high quality. The socket used to hold the AT's crystal requires an HC 25– or HC 33–type container. It is tempting to buy a low-cost wire-leaded HC 18 type and solder on nonpliable pins so you can mount it into the socket. In my tests, this method proved to be unreliable over the long term.

Standard HC 18– and HC 25–type crystals that you can find at local electronics stores might not be able to produce the stable and clean output many chips need to operate above the manufacturer's specifications. This is important for reliable operation when running the AT above 8 MHz.

You should buy an HC 25 military-specification-type crystal because of its stable frequency over temperature —better than 0.0005 percent +/– frequency deviation. The mil-spec crystals can cost twice as much as the lower-quality crystals and might be more stable than necessary, but the more stable frequency source will prevent damage to system components.

80286 MICROPROCESSOR

The 80286 is one of the most critical components when you are increasing the AT's system frequency. Intel's testing system works with a 35 percent upper performance margin when related to temperature, current, and frequency capabilities. Intel designed the 80286 to ultimately yield 10-MHz devices in volume production, but in early production runs Intel was able to produce only 6-MHz devices; this might be why the AT came out as a 6-MHz machine. Intel rates the 80286 by inducing an 85°C case

(continued)

Brian K. Roemmele is the president of Ariel Computer Corporation (Box 866, Flemington, NJ 08822, (201) 788-9002), *maker of an* IBM PC AT *speed-up kit.*

ILLUSTRATION BY ALEXA GRACE

temperature with a stable and clean power source. The chip's resulting coefficient at 3.3 power dissipation will qualify its frequency capabilities. The AT's power supply produces a relatively stable, clean current. The surrounding ambient temperature (35 to 52°C) within the AT's case is rarely close to the 85°C case temperature used to rate the 80286.

Considering Intel's test safety margin and the CPU's relative temperature, 8-MHz operation from the 80286-6 is safe. On average, consider 9.5 MHz to be the maximum frequency of the 6-MHz device. The radiated temperature from the 80286-6 running with an 8- to 9-MHz clock stabilizes well below the chip's maximum specifications. Although I successfully ran some ATs with stock 80286-6s at 10 MHz, I would not recommend this unless you monitor the CPU's temperature and check the system regularly.

In the tests I ran, I saw no evidence of lower mortality of the 80286-6, provided it receives a reliable, stable clock frequency. The gates that directly see the input frequency could theoretically suffer unpredictable performance or damage from wide and continuous frequency shifts. The damage is usually to the gates of the chip. If you don't want to worry about running in the safety margins of an 80286-6, you can replace the CPU with an 80286-8 or 80286-10. Since this chip is socketed, it is a simple upgrade.

82284 Clock Generator

The Intel 82284 clock generator divides the raw frequency from the crystal or frequency synthesizer in half, which stabilizes the frequency. The AT's standard 12-MHz crystal yields a 6-MHz processor and system frequency. The same test rating performed on the 80286 is performed on the 82284, resulting in the same coefficients. Intel designed this device to yield 8- to 10-MHz devices in volume production. In the AT, you can easily expect 10-MHz operation from this chip. In some ATs this chip is socketed, and you can replace it with a faster device. The chip will need replacing if you want to bring the AT above 11.5 MHz.

RAM Chips

The AT waits one CPU cycle before it performs a read or write to the RAM or a read to ROM. This wait state is wired in by the hardware and does not increase when you increase the CPU frequency. In fact, the period of wait decreases proportionally to the increase in frequency. You can approximately calculate the needed RAM nanosecond rating by dividing two into the CPU frequency (e.g., 2/6 = .3333, or 333 nanoseconds).

To arrive at an accurate result, you need to include the wait state (1/CPU frequency) and overall capacitance and propagation delays. IBM's *Technical Reference Manual* lists all RAM as 150 ns or better for the system board. The standard 128K-bit piggy-back 150-ns RAM is adequate up to a 9.5-MHz CPU speed. At 10 to 11 MHz, 120 ns is required; above that, 100-ns RAM should cover any other frequency that the rest of the system can handle. Because of increased capacitance and propagation delays, the RAM that populates memory-expansion cards should be at least 120 ns at frequencies above 8 MHz.

80287 Math Coprocessor

The standard 80287 math coprocessor receives one-third of the actual crystal frequency. On the standard 6-MHz AT, this works out to 4 MHz. For system frequencies below 10 MHz, the normally heat-sensitive 80287 should not experience any dramatic temperature increases. With a system speed of 10 MHz, the 80287 is running at 6.6 MHz, which is far enough beyond the Intel 5-MHz specification that an 80287-8 should be used.

Various Chips

The 74ALSxxx-series TTL logic chips covering approximately 60 percent of the system board and the Intel 82288 bus controller are the final limiting factors after you have considered or replaced all other components. They are both capable of approximately 11.5-MHz operation, but beyond that you should replace them. This is difficult because they are soldered into place. The extra 1 or 2 MHz you could gain might not be worth the heat and circuit-board damage that you could cause during desoldering.

RAM Boards

The quality control enforced by IBM on the chips that form the system board is predictable. After months of observing and testing, I have arrived at a reliable success rate in speeding up ATs. This is not the case for boards supplied by outside vendors. Some slow boards, just by being connected to the system bus, could cause the whole machine to lock up. RAM boards are particularly sensitive. To date there are no Lotus/Intel/Microsoft Expanded Memory Specification memory boards that run at or above 9 MHz. Some are not even capable of running at 8 MHz.

Most memory-board limitations can be traced to PAL (programmable array logic) chips, slow delay lines, and slow 74LSxxx-series chips. Standard RAM boards are more likely to be compatible. For example, the IBM 128K-byte memory board and the AST Advantage can run at 10 MHz, although the manufacturers don't support these capabilities. I have used the AST Advantage in ATs running at 12 MHz populated with 100-ns RAM chips. Other RAM boards are capable of fast CPU speeds. Working with the manufacturer or dealer in a trial-and-error process to find a suitable board would be the best way to identify boards capable of operating at high speed.

Monitor Boards

Monitor boards, like memory boards, suffer from wide variations in the system frequencies at which they can operate. Some older boards designed specifically for the PC might not work correctly in even a 6-MHz AT. Most monitor boards now manufactured specify their maximum system frequency capabilities. All of IBM's display cards can operate at up to

10-MHz CPU speeds. Monitor boards rarely reference the CPU frequency.

OTHER BOARDS

Printer and RS-232C ports, if designed to IBM's recommended specification, do not limit the AT's maximum frequency capabilities. A few low-priced imported boards have failed in 8-MHz systems. They interface to the system bus with slow 74LSxxx TTL chips. Timing (data rates) for the printer and RS-232C ports is usually derived from an autonomous frequency source unrelated to the CPU frequency.

Modem boards are a little more sensitive to a faster system. All Hayes internal modem products perform correctly at 10 MHz. Older or low-quality modem boards seem to fail above 8-MHz CPU speeds. Most boards designed for AT-class systems should not show any major problems; when in doubt, contact a knowledgeable engineer at the manufacturer.

FLOPPY AND HARD DISK DRIVES

The fixed disk/floppy disk controller card that comes with the AT can run at 12.5-MHz. The hard disk drives I have tested work fine at faster CPU speeds. However, the 1.2-megabyte floppy disk drive experiences some errors at or above 9 MHz.

Approximately 45 percent of the systems I tested reported a "Drive not ready error" during first-time drive access or during a copy or format. In many cases this error can be traced to an optimization for 8-MHz CPU and bus frequencies in the BIOS and PC-DOS 3.1 and 3.2.

PC-DOS and the BIOS set up a timing loop to wait for the drive to respond after being prompted with a signal. The loop time decreases while the drive's reaction time stays the same, causing the drive to sometimes fail to report "Drive ready" to the DOS/BIOS. Fortunately, you can press R for retry until the drive is ready. [*Editor's note: Ariel sells a patch to the* BIOS *to watch for the drive log-on.*]

HARD DISK INTERLEAVE

If you increase the CPU speed above 8 MHz, you can change the hard disk interleave. The 3:1 interleave on the standard IBM-supplied 20-megabyte drive is optimized for 6- to 8-MHz CPU speeds. At a CPU speed of 9 MHz or faster, a 2:1 interleave is better. You can change the hard disk interleave with IBM's Advanced Diagnostics found in the *Hardware Maintenance and Service Manual* (Part #1502242). You can expect a performance increase of 30 to 50 percent from a drive with a 2:1 interleave and a CPU speed of 9 MHz or above.

SOFTWARE

Software for MS-/PC-DOS systems rarely intentionally uses the CPU frequency as a critical reference. Theoretically, software that assumes a particular CPU speed could pose an uncorrectable problem, although you can readjust some software defaults that assume a particular CPU speed. For example, in some terminal-emulation programs you might need to increase the time-out default before carrier detect in auto-dial mode.

Timed screen sequences and timed screen menus might need adjustment, if it's possible. Some copy-protection techniques assume a particular system speed and will create a problem. Ashton-Tate seems to be the only company using this form of time-based copy protection.

ERRORS

The AT's POST (power-on self-test) investigates all the critical points of concern when increasing the CPU frequency. Running the standard IBM AT diagnostics disk continuously for the first 5 to 10 minutes after finalizing on a frequency should magnify conditions that the POST might have missed. During the testing of the monitor card in some systems, diagnostics might report a 501 error. This is due to IBM's technique for testing a specific function on the monitor board and does not represent any failure of the hardware.

Table 1 lists some of the errors that POST and diagnostics report, with a brief explanation and recommendation for correction. If the system fails to respond at less than 8-MHz CPU speeds, it is most often traced to a

(continued)

Table 1: *Some errors that POST and diagnostics report if some component fails when you increase the* IBM AT's *processor speed.*

Error	Description
Parity check 1 and 2 error	The RAM is too slow in responding to the CPU access cycle (install 120- or 100-ns RAM chips).
164 memory-size error	Usually attributed to an expansion RAM board that cannot handle the current CPU frequency.
201 system-board error	A general error—it usually means that under this system setup the current CPU speed is too fast for various chips on the system board (difficult to correct). It might also be an 80286 that is borderline failing.
System activity but no information on your screen	Generally relates to an incompatible display board.
No system activity or display	This is usually an 80286 failure. It can also represent a failure of the various chips on the system board.
Drive not ready error (abort, ignore, retry)	This can be traced to the BIOS, DOS, and the drive itself. You can retry until the drive is ready.

BENCHMARKS

BY EVA WHITE

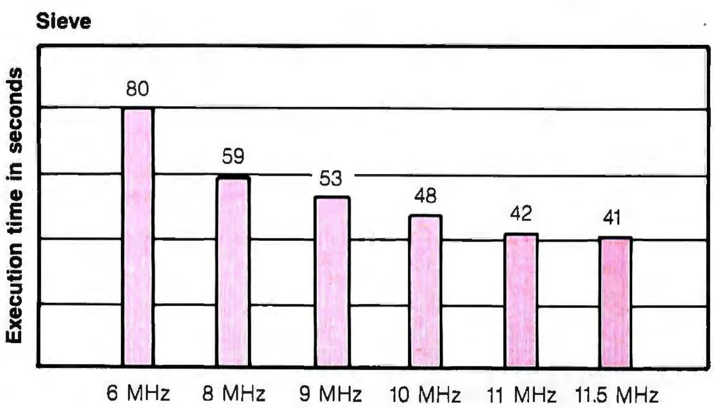
I tried some of Brain Roemmele's techniques to speed up one of BYTE's IBM PC ATs. I wanted to run benchmarks at six different speeds, so rather than buy six crystals, I opted for Ariel Corporation's variable frequency synthesizer (VFS), XCELX. It replaces the 12-MHz crystal in the AT.

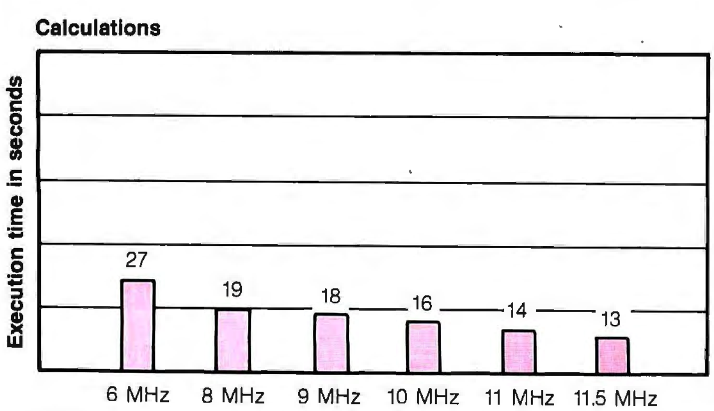
The VFS is a silver box (about 2 by 1 by 1 inch) that you mount with Velcro to the AT's power-supply case. Three wires and a control panel with variable resistor and toggle switch come out of the frequency synthesizer box; the red wire plugs in beside the wire in pin 1 of the P58 power connector, the black wire plugs in beside the wire in pin 1 of P59, and a wire with a hook-clip is attached to one of the leads of the empty crystal socket. The variable resistor lets you adjust the CPU speed, and the toggle switch engages either the standard (6 MHz) operation or the variable-speed CPU operation. The panel mounts in the rear of the AT (between the card slots and the fan). The control panel is bolted in place of the utility plate. The control knob and toggle switch stick out the back of the AT's case, preventing you from replacing the plastic rear cover. An adhesive label goes over the control panel to give you approximate CPU speed. A program included with the XCELX software called Tuneup gives a more accurate value for the CPU speed. I used it to set the CPU speed for the benchmark tests.

The CPU speed knob was too easy to turn. If you had to reach behind the machine, you could accidentally brush against the knob, turn it past the speed that the machine could handle, and cause a crash. To be on the safe side you can flip the toggle switch to standard mode, adjusting any cables behind the machine.

The Benchmarks for a standard AT were identical to those I ran with the synthesizer in standard mode (6 MHz). I flipped the toggle switch and was able to crank up the standard AT to 9 MHz before the machine froze. Then I replaced the CPU with an 80286 rated at 12.5 MHz and replaced the standard RAM with 100-ns RAM, both supplied by Ariel Corp. I ran the Sieve and Calculations programs at different speeds; the results are shown in table A. (See *Inside the IBM PCs*, Fall 1985, pages 200–201 for the listings of the Sieve and Calculations programs.) The speed increase going from 6 to 8 MHz was dramatic. While speeding up the machine beyond 8 MHz results in a noticeable decrease in execution times, it becomes less attractive when you have to replace the CPU and memory. Still, it's neat to see the AT running at 11.5 MHz. So far our speeded-up AT has been running the Sieve continuously for four days and is still working fine.

Table A: *Sieve and Calculations benchmarks run on an* IBM PC AT *at various* CPU *speeds. The benchmarks at* 9 MHz *and below were performed on an* AT *with all stock equipment except for a frequency synthesizer. For those tests at* 10 MHz *and above,* 512K *bytes of* 100-*ns* RAM *and a* 12.5-MHz 80826 *were installed. The* 80287 *was not accessed during these tests.*





Eva White is a BYTE *technical editor. She can be reached at* BYTE, *One Phoenix Mill Lane, Peterborough,* NH 03458.

memory or monitor board not designed for anything above 6 MHz.

DAMAGE

With all the components I have mentioned, permanent circuit or chip damage is unlikely when you are increasing the CPU frequency. Provided the frequency is reliable and stable, the worst that you can expect is a reported error or the system refusing to come up altogether. A chip either fails entirely or does not work normally. Heat-related damage might occur from prolonged use of a borderline device or use of an unstable frequency reference. The borderline problem is possible but unlikely. By selecting a lower frequency when you suspect this, you will make damage less likely.

IBM'S WARRANTY

As of this writing, IBM has made no official statement on the effect that increasing the system frequency will have on the company's one-year limited warranty. Officially, IBM doesn't encourage any activity of this type; unofficially, many IBM engineers and salespeople have been performing and recommending the upgrade. The dealer seems to have the final word on the warranty question.

IBM'S NEW ROM

The Model 239 30-megabyte hard disk system is not capable of increased CPU speeds with just a crystal replacement. Because of the popularity of increasing the CPU frequency, IBM chose to alter the ROMs in the new system. The affected ROMs have date codes beginning in June and July 1985. The alteration is a time-based loop in the first 500 lines of code in the BIOS's POST portion. The loop will determine if the CPU speed is greater than 6.6 MHz. If it is greater, the code will perform a branch that will purposely seize the system. The system will not beep or report any errors. (Newer ROM releases will produce two beeps.) I had considered a sophisticated ROM patch using mapped-in RAM or ROM to the code area. However, such a solution is complicated, inelegant, and would have introduced more vulnerability to the system as a whole.

I have come up with an easy fix for the ROM check. If you maintain a 6-MHz frequency to the 80286 for at least 10 seconds after power-up, the POST sees the standard AT frequency. Slowly and uniformly increasing the frequency to the system's maximum speed circumvents the ROM's investigations. A crystal switch selector would lock up the system if switched while the system was running. Debouncing only marginally im-

(continued)

proves the crystal switch design. A variable-frequency synthesizer proved to be the only reliable option.

It was relatively easy to design a frequency synthesizer that will automatically handle the procedures for getting around the ROM check. The timing loop for detecting an increase in system frequency is activated only during power-up and during a Ctrl-Alt-Del key combination. If you add an extra connector to a chip that receives this interrupt, the frequency synthesizer resets so that the required 6-MHz CPU speed is maintained during restart of POST.

Unlike crystals, which are passive devices, the frequency synthesizer is an active device that produces a continuum of frequencies; it allows increasing and decreasing of frequency while the system is running. This makes it easy to adjust the system for top performance. A variable resistor-based circuit offers the widest possible range of frequencies from which to choose.

NEW 8-MHZ AT

As I write this, IBM is beginning to ship the new Model 339 and 319 8-MHz system. It uses the same Type 2 system board found on most Model 239s. This board requires 256K-bit memory chips rather than the 128K-bit devices the Type 1 board used.

The differences are that the CPU is an 8-MHz marked part, the crystal is a 16-MHz device, and the ROMs (date beginning November 1985) have a loop that senses the CPU speed and causes them to seize on frequencies above 8.6 MHz. I have used a frequency synthesizer in an unmodified system up to and above a 10-MHz CPU speed.

CONCLUSIONS

If you are using an IBM PC AT with 512K bytes of RAM, a 20-megabyte fixed disk, and an IBM monochrome adapter, you can replace the 12-MHz crystal with a 16-MHz crystal without replacing other components. You might even be able to push the 80286-6 to 9 MHz with an 18-MHz crystal. Using a 20-MHz crystal, you would need to replace the CPU. With a 22-MHz crystal you would need to replace the CPU and RAM. At 24 MHz, you would need to replace the CPU, RAM, 82284 and 82288 chips, and possibly some 74ALS TTL chips.

Electronics manufacturers test and rate their products to perform predictably and reliably within their stated guidelines. Normally you should not design products that use components close to or above the manufacturer's specifications. Under most circumstances, I believe this is a good rule to follow, but the AT has a large safety margin; I have found that the benefits of improving its speed greatly outweigh the potential drawbacks. ■

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Using Assembly Routines in MS-FORTRAN Programs

Improve the speed of your FORTRAN code

BY MARK DAHMKE

IN THE COURSE of developing a large program, it is often necessary to call assembly language routines to make a critical task efficient or to gain access to features that are machine-specific or not implemented well in a high-level language. To that end, I'll present some mechanisms for dealing with the problem of passing parameters and managing the programming environment when working with Microsoft FORTRAN and 8086-family assembly language. The examples presented here are written in Microsoft assembly language and should work correctly with any version of the assembler.

The FORTRAN Environment

Microsoft FORTRAN, Pascal, and C have many common features in terms of their environment, parameter passing, and data structures. Many of the examples shown here will work well with all these languages, but the emphasis in this article will be on Microsoft FORTRAN.

The Microsoft FORTRAN run-time environment is shown in figure 1. Depending on which version of FORTRAN you are using, there may be some minor differences. FORTRAN begins by allocating memory at the first available low address and places the code segment (all user-generated code and library routines) there. All segments that are part of a group must reside in the same 64K-byte block of memory, due to the segmentation scheme of the 8088 and the 8086. For example, all FORTRAN subroutines compiled together (from one source file) are treated as a group. Thus, you could create a program with 256K bytes of code by compiling the main program and subroutines in four pieces, then linking them.

Similarly, blocks of constants and variables are put in groups that cannot exceed 64K bytes each. The most frequently used of these is the DGROUP, which includes all constants, variables, and unnamed common blocks and strings. If a program becomes so large that the data space exceeds 64K bytes, you must move variables and arrays into common blocks; unfortunately, common blocks are less efficient to address. The DGROUP also contains stack space and heap space used by FORTRAN.

Due to the 8088 and 8086 family's segmented address space scheme, you must establish addressability before reading or writing memory or you will likely cause your system to crash. "Establishing addressability" means loading one of the segment registers with a 16-bit pointer to the base of the block of memory you want access to. Figure 2 shows how this works. The CS, DS, and SS registers establish addressability for code, data, and stack segments, respectively. The ES register is for an "extra segment" that allows you to copy data from one segment to another. The segment registers hold the most significant 16 bits of a 20-bit address. This is added to the "offset" address specified in the instruction. For example, the CS and IP (instruction pointer) registers always point to the current instruction. Addresses of this form are denoted as CS:IP or "segment plus offset."

Parameters passed to subroutines must include the segment portion of the address if the constant or variable

(continued)

A contributing editor for BYTE, *Mark Dahmke owns a consulting business and has had three books published by* BYTE Books/McGraw-Hill. *He can be reached at* P. O. Box 80266, Lincoln, NE 68501.

ILLUSTRATED BY MARY ANN SMITH

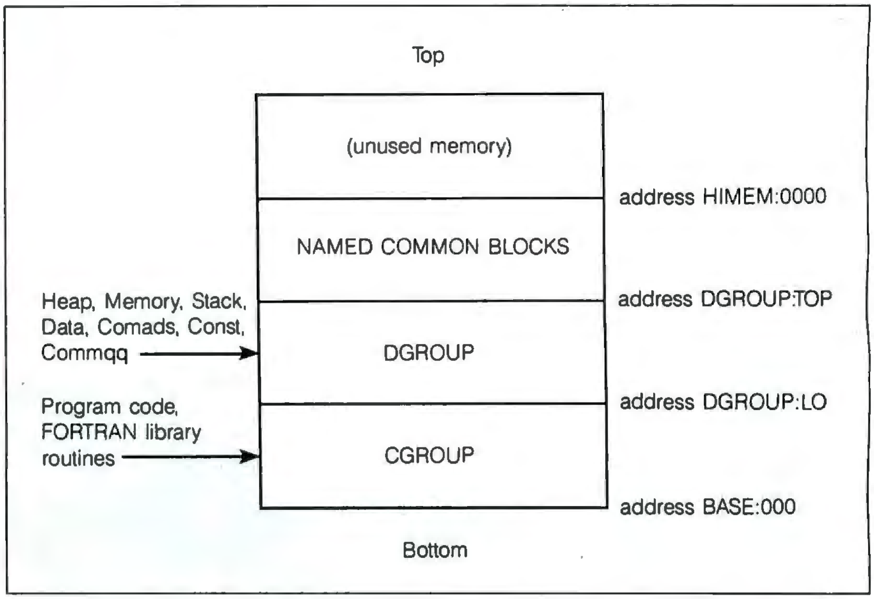

Figure 1: MS-FORTRAN *run-time memory organization.* FORTRAN *sets up two major areas, the code group and the data group. You may need additional groups for named common blocks. Due to the segmented address scheme of the* 8086 *family,* 4*-byte addresses (segment plus offset) are required for most parameter passing to subroutines.*

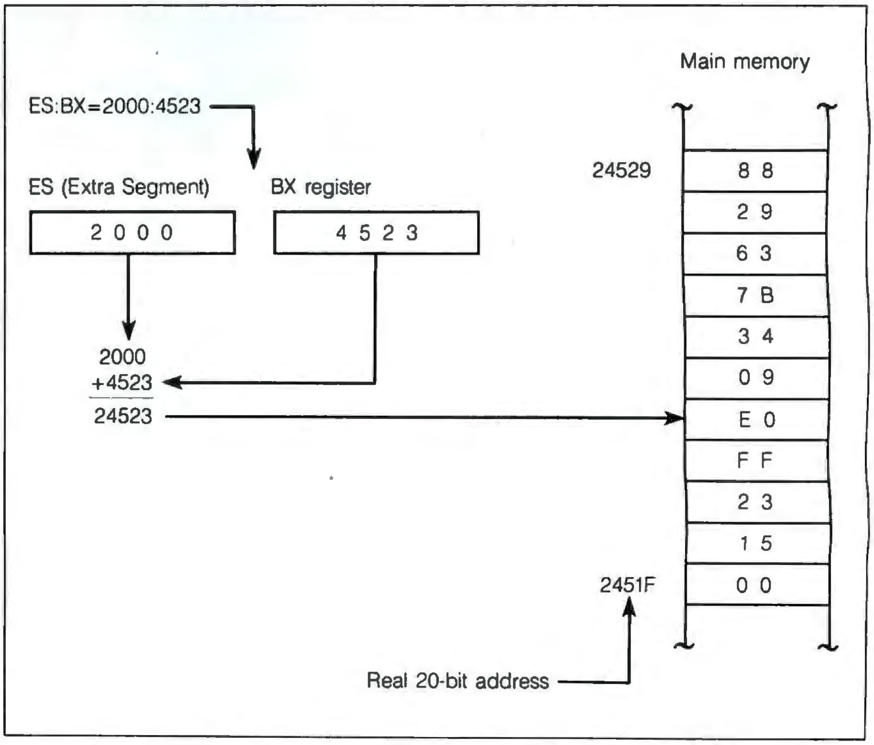

Figure 2: *Establishing addressability. Assuming that* ES *and* BX *have been loaded with* 2000 *and* 4523*, respectively, the instruction* MOV AX,ES:[BX] *would cause the value* 09E0 *to be loaded into* AX. *If interpreted as an* INTEGER*2 *number,* 09E0 *would equal* 2528 *in decimal.*

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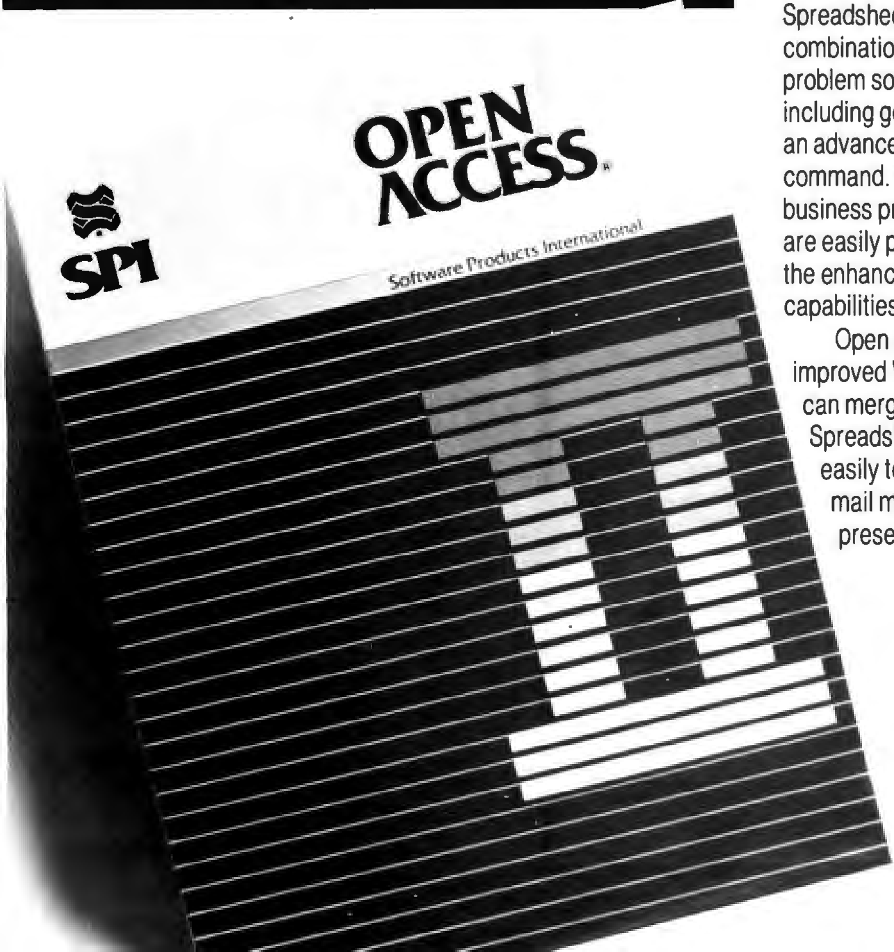

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is not considered local to the subroutine. Since it is almost impossible to tell in advance whether the DS or ES register will be correctly loaded before calling the routine, FORTRAN always passes the segment and offset to a subroutine.

PASSING PARAMETERS

Two cases must be dealt with in FORTRAN: functions and subroutines. In both cases, FORTRAN uses the call-by-reference method for passing parameters, even for constants and expressions. This method makes it easier to write assembly language programs, since the values being passed are always addressed in the segment-plus-offset format.

For both functions and subroutines, the parameters are placed on the stack in the order in which they appear in the parameter list of the calling program. Figure 3 shows the stack before a call to a sample function. In the case of functions, results are returned in registers if the result is defined as an integer or single-precision real number. If the result is 16 or fewer bits long, it is assumed to be in the AX register upon return. If the result is declared INTEGER*4 or REAL*4, it will be in the AX,DX pair. If a number is double-precision (REAL*8), the result must be returned in a dummy variable created by the calling program. The offset address of this variable is in the stack at location BP+6.

SUBROUTINES

All variables passed to subroutines and all results returned from subroutines are passed as parameters in the call list. Figure 4 shows how the stack is loaded prior to calling the sample subroutine shown.

ENTRY AND EXIT REQUIREMENTS

As shown earlier, the addresses must be obtained from the stack and placed in segment and offset registers to gain access to the value of the variable. This can be confusing, especially if the stack contains many parameters. All addressing is done on the basis of the base pointer (BP) register.

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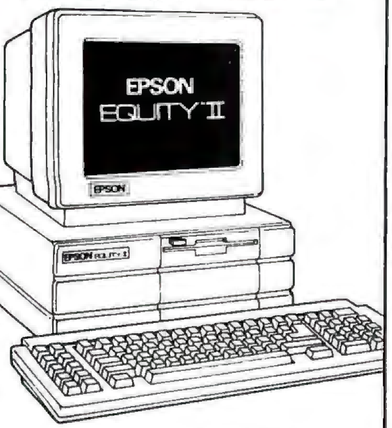

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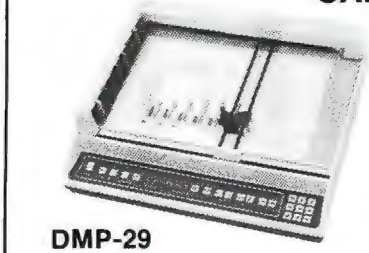

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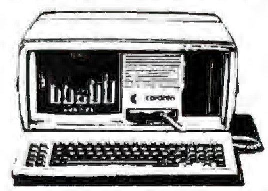

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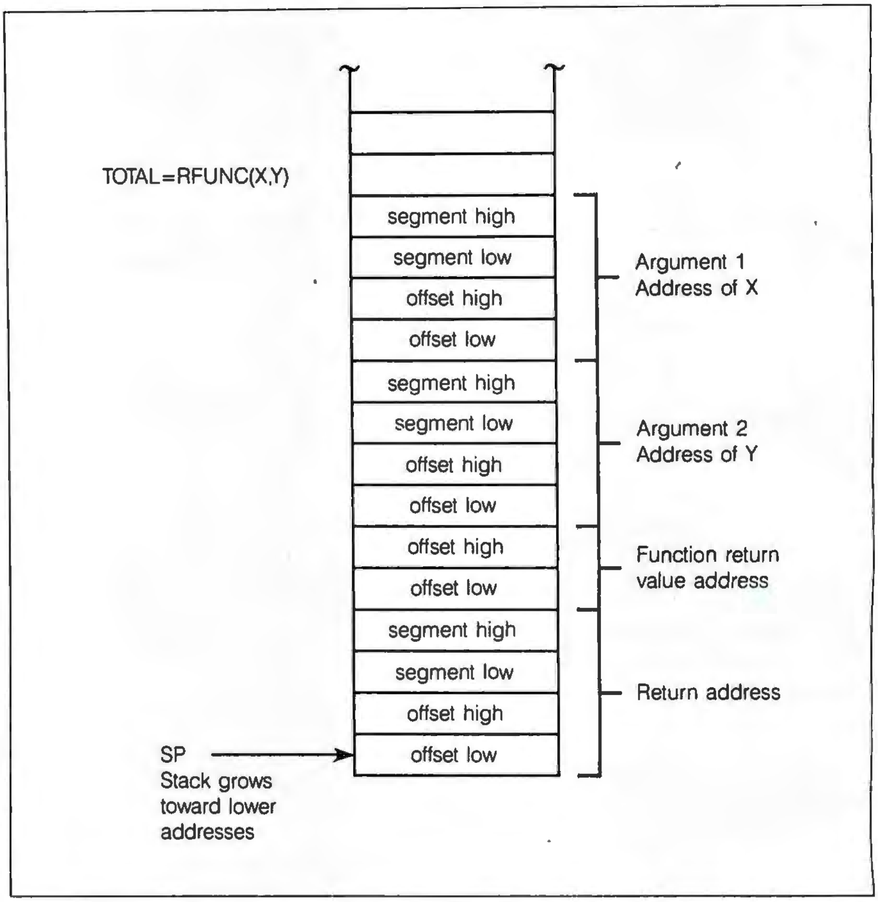

Figure 3: *The stack segment before a function call. All argument addresses are pushed onto the stack prior to a subroutine or function call. Four bytes are required to store each address in the segment-plus-offset format.*

To simplify the process of computing offsets, I wrote the macros shown in figure 5.

SETFRAME (see listing 1) performs the housekeeping tasks needed to gain access to the stack. The frame pointer must be saved, so it is in the same location when returning to the calling program. Also, the stack pointer (SP) must be loaded into the BP so that the offset address to the parameters will be correct.

The GETPARM macro solves the problem of getting an address and putting it in the ES:BX register pair. The first argument of GETPARM is the number (counting from the left) of the parameter you want to retrieve. The second argument specifies the total number of parameters in the call list. For example, if the call CALL SUBR(A,B,C) were made from a program, and you wanted to retrieve the address of the variable C, you would enter GETPARM 3,3, which would return the address of the third of three parameters. Listing 1 shows the instructions generated for all three parameters in the call list of this sample program. [*Editor's note: Listing 1 and the sample assembly language subroutines discussed below are available on disk, in print, and on* BIX. *See the insert card following page* 176 *for details. Listings are also available on* BYTE*net. See page* 4.]

The third macro shown in figure 5 is for housekeeping at the end of a subroutine. POPRET will make sure the SP and BP registers are returned to their starting values and that the correct number of bytes is popped off the stack before returning. This is necessary because the calling program

(continued)

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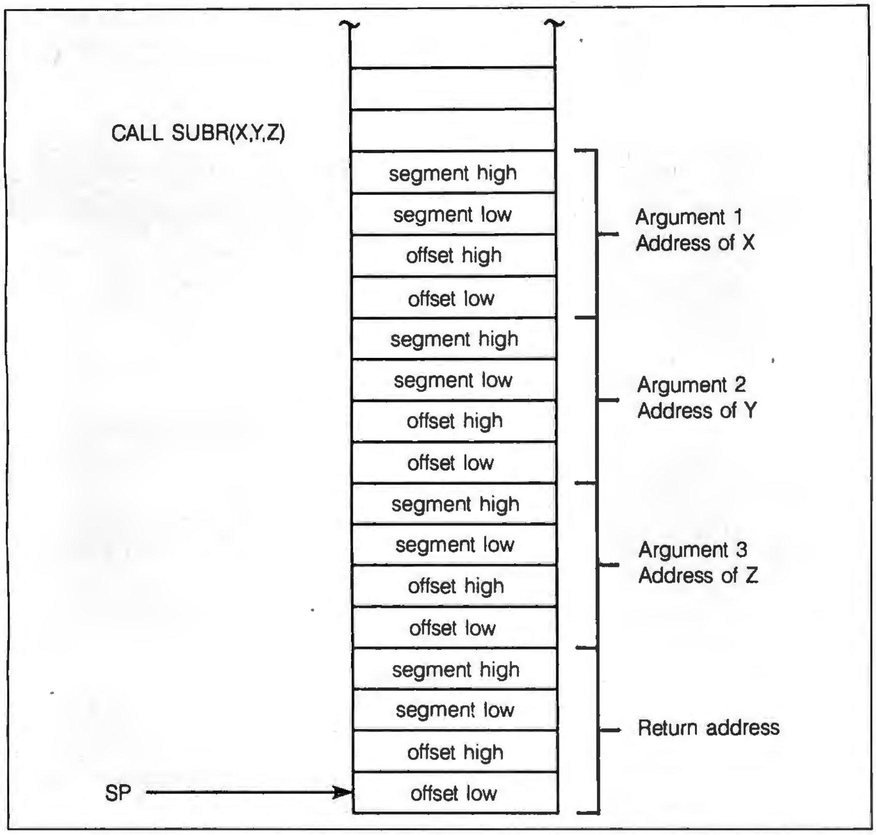

Figure 4: *The stack segment before a subroutine call.*

assumes that the stack is the same as it was before setting up for the subroutine call. The only argument given to POPRET is the number of parameters in the call list. In this example, four parameters were passed, so you would code POPRET 4. After 16 bytes are popped off the stack, a FAR return instruction is executed, which passes control back to the caller.

EXAMPLES

I have written four sample subroutines. The first two, SRCHF and SRCHN, allow a calling FORTRAN program to scan the current directory for filenames. These subroutines use the old DOS function calls that use FCBs (file control blocks) instead of the newer DOS functions, which use file handles.

SRCHF and SRCHN are almost identical, except that SRCHF locates the first matching directory entry and SRCHN finds subsequent matching entries. SRCHF is called just once, while SRCHN can be called repeatedly to get subsequent filenames that may or may not be identical to the first one returned.

(continued)

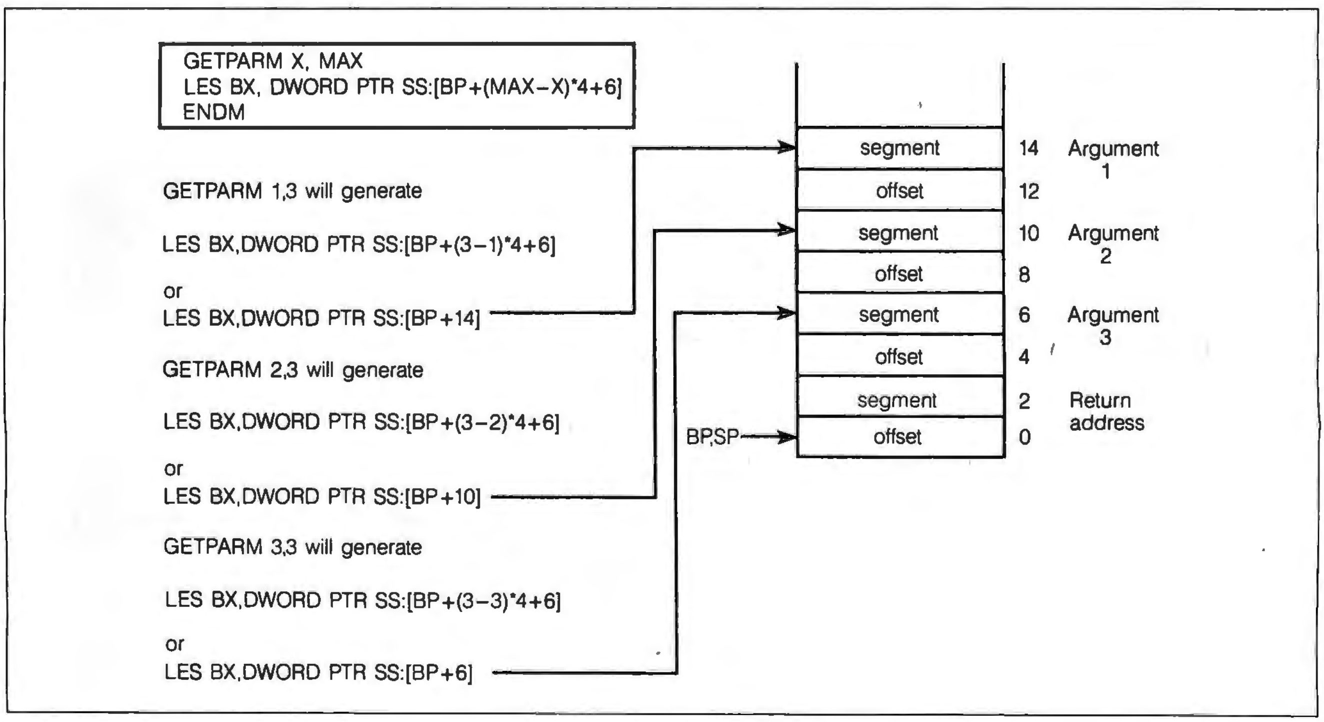

Figure 5: *Utility macros that simplify parameter handling in assembly language subroutines.*

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COMPATIBILITY:			
▲ FULLY SOFTWARE/ HARDWARE COMPATIBLE	YES	NO	NO
▲ NO SOFTWARE PATCHES NEEDED	YES	NO	NO
▲ IBM EGA COMPATIBLE	YES	NO	YES
▲ LOTUS/INTEL EMS COMPATIBLE	YES	NO	YES
▲ NETWORK COMPATIBLE	YES	NO	YES
▲ STANDARD 8088 MODE	YES	YES	NO
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▲ MULTIPLE VDISKS	YES	NO	NO
▲ MULTIUSER OPTION	YES	NO	NO
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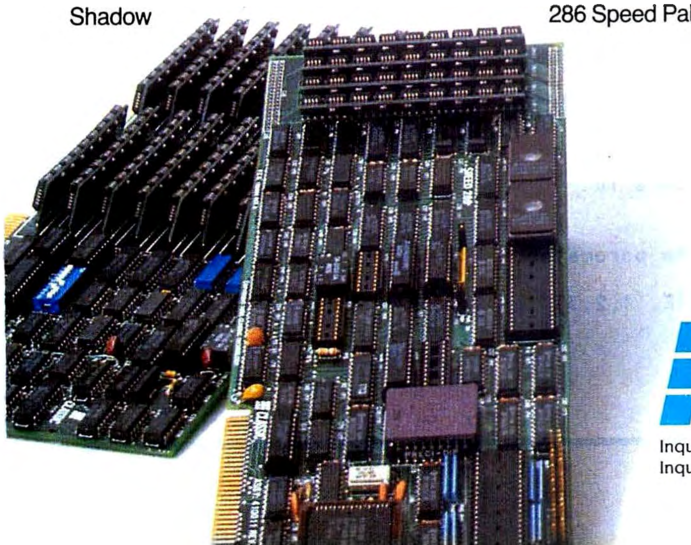
▲ INCLUDES 1 MB MEMORY	YES	YES	NO
3-YR. WARRANTY:	YES	NO	NO



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Because these two routines are nearly identical, I will describe only SRCHF in detail. The calling FORTRAN routine must load a string with the filename to be matched. This name may include question mark (?) as a wildcard, but not an asterisk (*). While the asterisk is a valid wildcard in many DOS commands, this low-level function call doesn't recognize it. Normally the asterisk is parsed by the calling program and converted into question marks.

The calling program must pass two other parameters: the drive code and an empty string in which the requested filename is returned. The drive code is an integer that corresponds to the disk drive letter (1 = A:, 2 = B:, 3 = C:, and 0 = default).

Upon receiving control, the SRCHF routine retrieves the drive code value. The GETPARM 1,3 macro looks into the stack and finds the double word pointer for the drive code, which is returned in the ES:BX register pair. The next instruction gets the value of the drive code and stores it in the AX register. The FCB template must be initialized with the drive code and filename. The next instruction copies the least significant byte of the drive code (all that really matters anyway) into the first byte of the FCB.

Next, a GETPARM 2,3 macro retrieves the pointer to the second of three parameters passed to SRCHF—the filename itself. The filename must be stored as 11 characters with no period separating the filename from the file type. For example, the filename SAMPLE.DAT would be stored as SAMPLE_ _DAT. A second pointer is set up to copy these 11 bytes from the FORTRAN string to the filename area of the FCB. The length is loaded into CX, and a REP MOVSB instruction performs the copy automatically.

After the FCB is loaded, DOS must be told where to find the buffer that will hold the resulting FCB. This is done through the SET DMA ADDRESS function call. Finally, a call to the SEARCH FIRST function will cause DOS to check the directory and return either a matching filename or an error code. If a filename is found, an error code of zero will be returned, along with the filename in the same 11-byte format as described earlier. If no files are found, the subroutine returns a single question mark in the first character of the returned filename string.

GETDIR AND CHDIR

The subroutine GETDIR returns the current directory name. Three parameters are required: an empty string to store the resulting directory name, the drive code, and an error code variable.

This routine first gets a pointer to the character string and stores the segment and offset in STRING_SEG and STRING, respectively. After load-

(continued)

Listing 1: *The* GETPARM *macro loads the* ES:BX *pair with the address of a parameter from the subroutine call list. The first argument of the macro is the number (counting from the left) of the desired parameter in the call list. The second argument* (X,MAX) *is the maximum number of parameters in the call list.*

```
;  SETFRAME:  Sets the environment upon entry to a subroutine.
;
SETFRAME MACRO
        PUSH    BP                  ;SAVE FRAMEPOINTER ON STACK
        MOV     BP,SP
        ENDM
;
;  POPRET:    Restores the BP register and returns to the
;             calling FORTRAN routine after cleaning up the
;             stack.
;
POPRET  MACRO   NPARMS              ;RETURN FROM SUBR.  NPARMS=NUMBER OF PARMS
        POP     BP
        RET     NPARMS*4
        ENDM
;
; GETPARM: returns a pointer to a parameter in the call list.
;
;       Operands:  X = the number of the desired parameter
;                MAX = the maximum number of parameters in
;                      the call list.
;
;       Result: The ES:BX register pair points to the parameter.
;
GETPARM MACRO   X,MAX               ;PARAMETER NUMBER (IE. 1,2,3)
        LES     BX,DWORD PTR SS:[BP+(MAX-X)*4+6]
        ENDM
;
;
```

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ing the drive code into the AX register, the string segment and offset addresses are loaded into the DS:DX pair, and DOS function 47h is called. This function stores the full directory name in the string space but will not add a leading backslash (\ ) or drive letter and colon to the name. Thus, if you are currently in the directory C: \ MAIN \ SAMPLE, this subroutine will return the string MAIN \ SAMPLE. Also, the string will be terminated with a null or zero byte. After the DOS function call, the return code is stored in the third variable and returned to the calling program.

CHDIR (change directory) is almost identical to GETDIR, but the input directory name can be fully qualified, including a drive code, colon, and leading backslash character, just as you would enter it in the DOS CD command. The string must be terminated with a null or zero byte to be accepted, though.

THE GETDFS SUBROUTINE

The GETDFS (get disk free space) routine returns information about the disk drive. Three values are returned, indicating the number of bytes per sector, sectors per cluster, and the number of free clusters on a disk. With these three values, you can calculate the number of free bytes easily. The values are returned to the calling program in INTEGER*2 variables, but if the three are multiplied to get free space in bytes, you must use an INTEGER*4 variable to hold the result. If the value returned in the fourth argument of the call list (ICLUST) is equal to −1 (0FFFF hexadecimal), an error condition has resulted.

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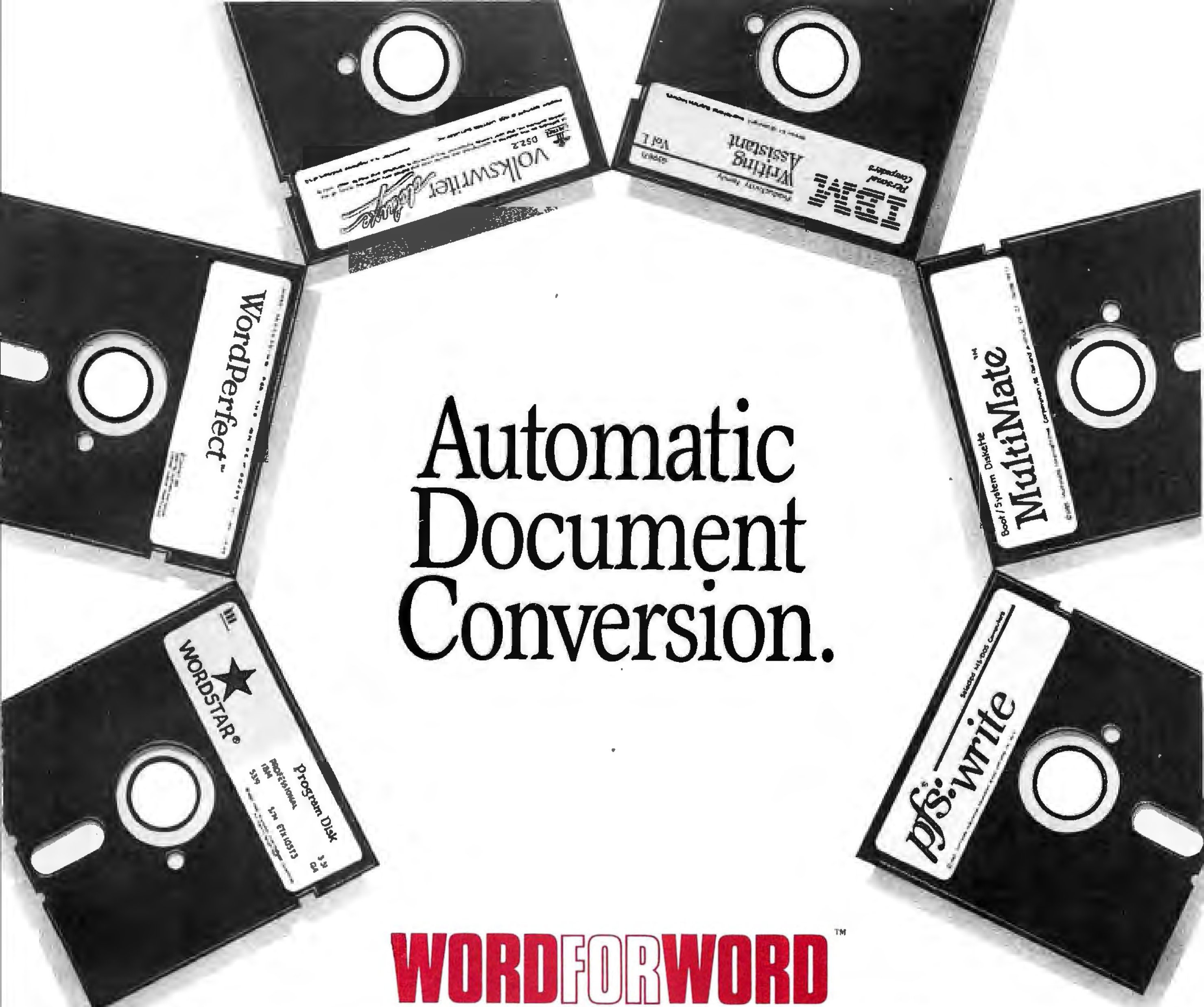

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9:08: *"Hit any key. Where's the 'any' key?"*

9:47: *"So that's how you create a file."*

10:26: *"And they all laughed when I sat down at the computer."*

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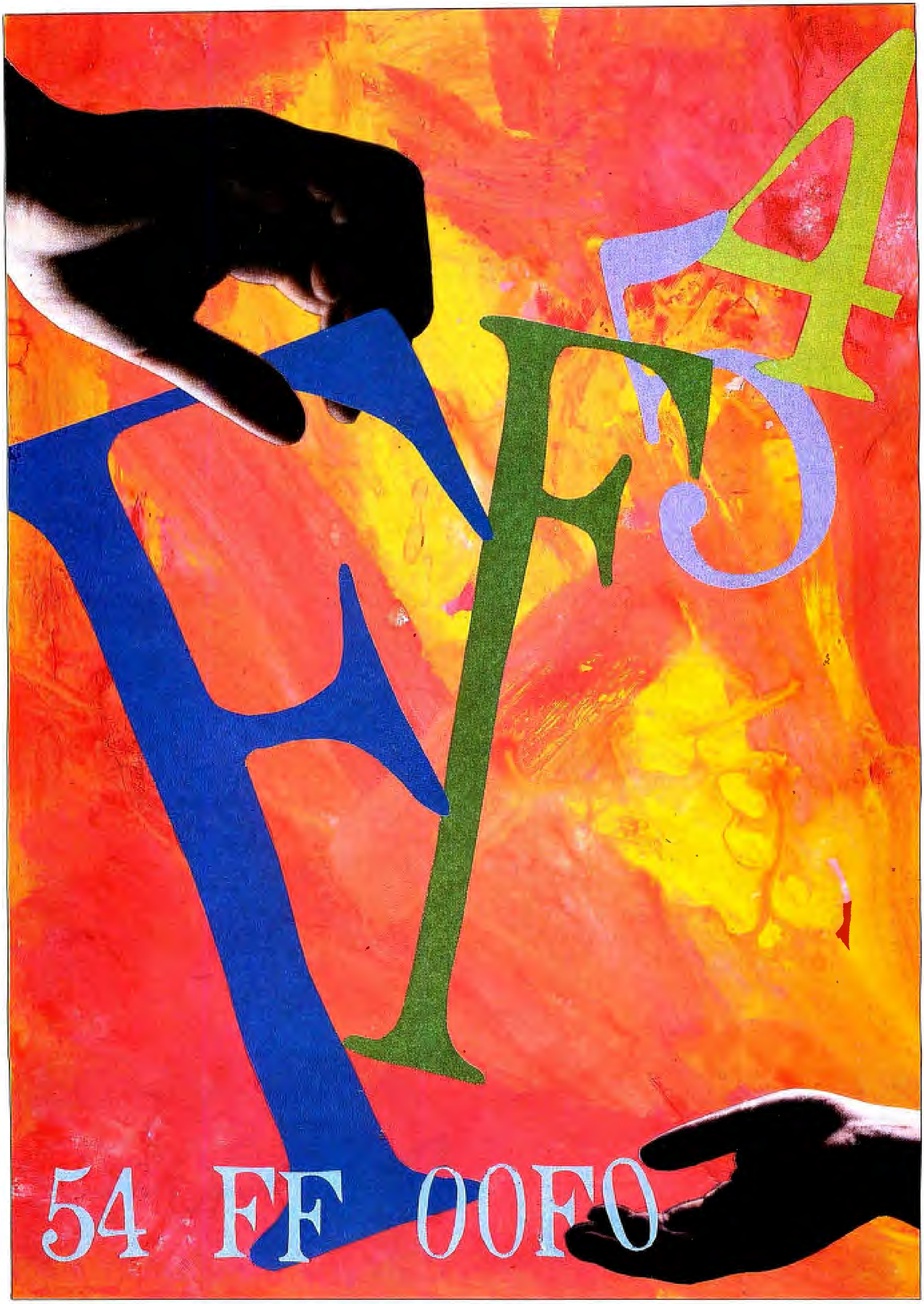

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MEMORY MANIPULATIONS

PART 1: ARABIC VERSUS ROMAN

Making sense out of FATs and other reversed addresses

BY ALAN R. MILLER

Editor's note: Alan Miller explains two ways to manipulate the memory of the IBM PC. Part 1 clarifies the ordering of addresses. Part 2 discusses how to adjust the size of memory.

READING HEXADECIMAL numbers larger than one byte presents a problem that is rooted in the difference between the Arabic language, which is written from right to left and from which our numbers come, and the Roman language, which is written from left to right and from which our letters come. In our number systems—whether binary, hexadecimal, or decimal—the value of each digit position increases as you move from right to left, in the Arabic style. For example, in the decimal system, the tens are positioned to the left of the units, and the hundreds to the left of the tens.

Unfortunately, it has become the custom to display successive hexadecimal bytes in the Roman fashion, from left to right. Thus, although the 16-bit binary number 1010 1101 0101 0111 is equivalent to the hexadecimal number AD57, when this number is written as two bytes, the order is reversed to give 57 AD. Now the low byte, 57, is on the left, and the high byte, AD, is on the right. Notice the inconsistency of this form. The two characters of *each* byte are shown with the high nybble on the left and the low nybble on the right in Arabic style. However, *successive* bytes of the number are given with the low byte on the left and the high byte on the right in Roman style.

FINDING THE PORT ADDRESSES

You can observe the reversed display on the IBM PC by using the DOS program DEBUG. Execute DEBUG by typing its name and then pressing the Return key. When you see the minus-sign prompt, display two lines in hexadecimal notation by entering the command D0:400L20, then press the Return key. You should see something like the display in figure 1, corresponding to the first 32 bytes of the BIOS data area. The first symbols give the beginning address of 400 hexadecimal that was requested.

The first item at address 400 is the 16-bit address of the serial port. The two bytes are shown as F8 03. However, you need to reverse these two bytes to find the real address of the serial port, which is 3F8 hexadecimal. Similarly, the addresses of the two parallel ports start at address 408. After you reverse the byte pairs, the values BC 03 78 03 give the port addresses 3BC and 378. While this might seem confusing, the comforting rule is that the higher, and therefore more significant, half of the address resides higher in memory than the lower half.

Consider the next line at address 413. The two bytes at this location give the maximum amount of available RAM in K bytes. The reversed bytes 80 and 02 become 280 hexadecimal or 640K bytes.

THE INTERRUPT VECTORS

The first 1024 bytes of IBM PC memory (0 to 400 hexadecimal) contain 256 four-byte addresses that point to subroutines or data located somewhere in memory. These addresses are numbered from 0 through FF hexadecimal and are known as interrupt vectors. The hardware directly accesses some of these vectors. For example, when you type information at the keyboard, an electrical signal interrupts the microprocessor and directs it to the address given at 24 hexadecimal, which is for interrupt 9. The address there points to a keyboard-service routine in the ROM BIOS near the top of memory. After the keyboard routine completes its work, it returns control to the interrupted program.

If you use DEBUG to look at the first 12 interrupt vectors by giving the command D0:0L30, you will see something similar to figure 2. Each group of four bytes represents one interrupt vector. For example, interrupt 5 activates the PrtSc routine. When you hold down the Shift key and press the PrtSc key, the microprocessor branches to the address given at location 14 hexadecimal. The data there is shown as 54 FF 00 F0, which after reversal represents the address F000:FF54. Again, the display is inconsistent. The two characters in each byte have the higher half on the left and the lower half on the right in Arabic fashion. However, successive bytes are arranged with the higher bytes on the right and the lower bytes on the left in Roman fashion. Notice

(continued)

Alan R. Miller is a BYTE contributing editor and the author of Assembly Language Techniques for the IBM PC (Sybex, 1986). *These two articles are adaptations of information from that book. Alan is a professor at New Mexico Institute of Mining and Technology (Metallurgy Department, Socorro, NM 87801), where he has taught materials science, thermodynamics, electrical engineering, and programming methods. He holds a Ph.D. in engineering from the University of California at Berkeley.*

that if the display's second line were in reverse order (i.e., in Arabic fashion), you would see the contents of figure 3a. Then you could more easily read the four interrupt vectors shown in figure 3b. The address for interrupt 5 is now the second one from the right.

```
0000:0400  F8 03 F8 02 00 00 00 00-BC 03 78 03 00 00 00 00
0000:0410  7F 82 00 80 02 40 02 00-00 00 32 00 32 00 64 20
```

Figure 1: *An example of DEBUG's display of the first 32 bytes of the BIOS data area.*

```
0000:0000  E8 4E 2E 01 F0 01 70 00-C3 E2 00 F0 F0 01 70 00
0000:0010  F0 01 70 00 54 FF 00 F0-47 FF 00 F0 47 FF 00 F0
0000:0020  DF 01 6F 0B 2F 01 4A 10-DD E6 00 F0 DD E6 00 F0
```

Figure 2: *An example of DEBUG's display of the first 12 interrupt vectors.*

```
F0 00 FF 47 F0 00 FF 47-F0 00 FF 54 00 70 01 F0 0000:0010
```

Figure 3a: *The second line of figure 2 shown in reverse order (i.e., in Arabic fashion).*

```
F000:FF47  F000:FF47 – F000:FF54  0070:01F0
```

Figure 3b: *The four interrupt vectors described in figure 3a.*

```
xxxx:0170  C0 04 4D E0 04 4F 00 05-51 20 05 53 40 05 55 60
```

Figure 4a: *An example of DEBUG's display of the FAT. (The xxxx value is unimportant.)*

```
4C 4D 4E 4F 50 51 52 53 54 55
```

Figure 4b: *The actual FAT numbers shown in figure 4a.*

```
60 55 05 40 53 05 20 51-05 00 4F 04 E0 4D 04 C0
```

Figure 4c: *The FAT display from figure 4a shown backward.*

```
6 0 55 0 54 0 53 0 52 0 51-0 50 0 4F 0 4E 0 4D 0 4C 0
```

Figure 4d: *The display in figure 4c with the nybbles split. Note that the FAT for a floppy disk uses three nybbles per entry.*

THE FILE ALLOCATION TABLE

A more serious problem occurs with the file allocation table (FAT), a set of numbers that shows where each part of a file is located on the disk. Floppy disks and hard disks smaller than 20 megabytes use a 12-bit FAT, while larger disks use a 16-bit FAT. (A 20-megabyte hard disk uses a 12-bit FAT with DOS 2.x and a 16-bit FAT with DOS 3.x.) You can inspect the FAT for the floppy disk in drive A by giving the DEBUG command LDS:100 0 1 2. The first parameter to the load command is the offset address in memory where the FAT will be loaded (100 hexadecimal). The next parameter, 0, requests drive A; 1 is starting sector number, and 2 is the number of sectors.

After the FAT is loaded, you can examine it with the command D170L10. You will see something like the contents of figure 4a. Although it is not readily apparent, the FAT numbers in figure 4a are those in figure 4b. It is more obvious if you display the line backward (figure 4c) and then split the nybbles (figure 4d). Remember, the FAT for a floppy disk uses 12 bits, or three nybbles, per entry. When read from right to left (Arabic style), the bytes appear as in figure 4b.

Several authors have criticized the FAT's backward design. However, the design is correct; the problem lies in mixing Arabic and Roman notation. We have accepted the system of Arabic numerals, which is backward to us, without question. However, we insist on displaying successive bytes in Roman fashion from left to right. In this way, we scramble 12-bit, 16-bit, and 32-bit numbers in our displays.

Microsoft compromises by reversing the 16-bit addresses but then runs the bytes together to indicate that they are reversed. Consider a typical assembly listing that shows

```
E9 02DC    JMP done
```

The value E9 hexadecimal is the 8088 code for JMP, and the number 02DC hexadecimal is the relative distance to be jumped. However, if you look at a hexadecimal display of this instruction, you would see E9 DC 02. The DC

(continued)

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Listing 1: ADUMP.ASM, *a program designed to display bytes in Arabic fashion from right to left. (Note that this is written to be executed in a* .COM *file.)*

```
        PAGE    ,132
        TITLE   ADUMP

COMMENT *
  Display a portion of memory in hex and ASCII
  Successive hex bytes are reversed in Arabic fashion
  Usage:
        ADUMP
        ADUMP  400      ;offset
        ADUMP  5300 0   ;segment, offset
  Macros: @d_char, @ucase, @write_r
  INT 21h function 8
 *
        IF1
        INCLUDE mymac.lib
        ENDIF

blank   EQU     32
cr      EQU     13
esc     EQU     1Bh
lf      EQU     10
period  EQU     46
up_arr  EQU     72                  ;up cursor
down_ar EQU     80                  ;down cursor
pg_up   EQU     73                  ;previous screen
pg_dn   EQU     81                  ;next screen

code    SEGMENT
        ASSUME  CS:code, DS:code
        ORG     5Dh
param1  DB      ?                   ;parameter 1
        ORG     6Dh
param2  DB      ?                   ;parameter 2

        ORG     100h
strt:
        @write_r <OFFSET mes1>
; set segment and offset to zero
        XOR     SI,SI               ;zero offset
        MOV     ES,SI               ;segment
; check if parameter was entered
        MOV     DI,OFFSET param1
        CMP     BYTE PTR [DI],blank ;anything?
        JZ      t_lines
; convert parameter from ASCII hex to binary in SI
        CALL    get_hex
        MOV     SI,DX
; check if second parameter was entered
        MOV     DI,OFFSET param2
        CMP     BYTE PTR [DI],blank ;anything?
        JZ      t_lines
        MOV     ES,SI
; convert parameter from ASCII hex to binary in SI
        CALL    get_hex
        MOV     SI,DX
;-----------------------------------------------
; start display of 16 lines
; ES has segment, SI has offset
;-----------------------------------------------
t_lines:
        @write_r <OFFSET mes2>
        MOV     CX,21               ;lines
```

(continued)

byte is located between the E9 and 02 bytes. This would be much clearer if we displayed the data with the order of the bytes reversed, as in

02 DC E9   JMP done

or

JMP done   02 DC E9

AN ARABIC DISPLAY

The assembly language program ADUMP.ASM (listing 1) is designed to make your hexadecimal displays easier to read by giving the bytes in Arabic fashion from right to left. To run ADUMP.ASM, you need the macros given in MYMAC.LIB (listing 2); notice that the macro names begin with @. (If you don't have a macro assembler, you must put the corresponding code at each place in the program. But then be careful to change the dummy variables and to remove the INCLUDE directive near the beginning. ADUMP.ASM is described in my book *Assembly Language Techniques for the IBM PC*, Sybex, 1986.) [*Editor's note*: ADUMP.ASM *and* MYMAC.LIB *are available on disk, in print, and on* BIX. *See the insert card following page 176 for details. Listings are also available on* BYTE*net. See page 4.*]

After you assemble ADUMP.ASM, if you execute it without parameters, you will see a listing similar to the one in table 1. The display begins at address 0, and so it includes the BIOS interrupt vectors. For example, the PrtSc vector at address 14 hexadecimal can now be clearly seen as F0 00 FF 54 or F000:FF54.

You can press the down arrow key to see the next line or the PgDn key to see the next page. To view another area of memory, execute this program with one or two parameters. If you provide only one parameter, the display begins at that hexadecimal offset from the beginning of memory. For example, to see the BIOS data area, you use the parameter 400. If you provide two parameters, the first is the segment address and the second is the offset within that segment.

ADUMP.ASM contains routines for

(continued)

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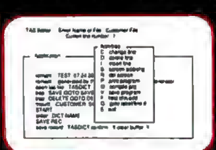

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```
n_line:
        @d_char cr
        @d_char lf
; display address and 16 hex bytes
        CALL    do_hex
; display ASCII
        CALL    do_ascii
        ADD     SI,16           ;next line
        LOOP    n_line
; wait for keyboard input
        CALL    get_in
        CMP     AL,esc          ;quit?
        JZ      done            ;yes
        CMP     AL,cr           ;next page?
        JNZ     not_cr          ;no
        JMP     t_lines
not_cr:
        CMP     AL,pg_dn
        JNZ     not_pd
        JMP     t_lines         ;next page
not_pd:
        CMP     AL,up_arr
        JNZ     not_ua          ;prev line
; back up pointer one line and redisplay
        SUB     SI,22*16
        JMP     t_lines
not_ua:
        CMP     AL,pg_up
        JNZ     not_tl          ;prev page
; back up pointer one page and redisplay
        SUB     SI,42*16
        JMP     t_lines
not_tl:
        MOV     CX,1
        CMP     AL,blank
        JZ      n_line          ;next line
        CMP     AL,down_ar
        JZ      n_line          ;next line
done:
        INT     20h
; translation table binary to ASCII hex
hex_tab DB      '0123456789ABCDEF'
;*******************************************
; Convert binary number in AL to hex and
;  and display on screen
; Input:        AL = byte
;*******************************************
outhex  PROC
        PUSH    DX
        MOV     DL,AL           ;save
        REPT    4               ;times 16
        SHR     AL,1
        ENDM
        CALL    outhx           ;high half
        MOV     AL,DL           ;get back
        CALL    outhx           ;low half
        MOV     AL,DL           ;restore
        POP     DX
        RET
outhex  ENDP
;********  End outhex  ******************
;******************************************
; convert four bits in AL to hex and
; display on screen
;******************************************
```

```
outhx   PROC
        AND     AL,0Fh              ;low 4 bits
        PUSH    BX
        MOV     BX,OFFSET hex_tab
        XLAT    hex_tab
        @d_char AL                  ;display
        POP     BX
        RET
outhx   ENDP
;********  End outhx  ********************
;*****************************************
; Convert ASCII hex to binary
; Input:        DI points to string
; Output:       DX = binary value
;*****************************************
get_hex PROC
        PUSH    AX
        XOR     AX,AX               ;zero
        MOV     DX,AX               ;DX too
g_hex2:
        MOV     AL,[DI]
        SUB     AL,'0'              ;make binary
        JL      g_hex_b             ;too low
        CMP     AL,10
        JL      g_hex_g             ;ok
        @ucase                      ;make upper
        SUB     AL,'A'-'9'-1        ;adjust for A-F
        JL      g_hex_b             ;too low
        CMP     AL,15
        JG      g_hex_b             ;too large
; add new character to sum
g_hex_g:
        REPT    4
        SHL     DX,1
        ENDM
        ADD     DX,AX
        INC     DI
        JMP     g_hex2              ;next char
; end of string
g_hex_b:
        POP     AX
        RET

get_hex ENDP
;*************  End of get_hex  **********
;*****************************************
; display address and 16 hex bytes
; Input:        SI = pointer
; Output:       SI is 16 larger
;*****************************************
do_hex  PROC
        MOV     DI,SI
        ADD     DI,16
        PUSH    CX
        MOV     CX,16               ;one line
next_ch:
        DEC     DI                  ;next
        MOV     AL,ES:[DI]
        CALL    outhex
        PUSH    BX
        MOV     BL,blank
; put a minus sign at quarter points
        MOV     AX,DI
        AND     AL,0fh
        JZ      not_min             ;line end
        AND     AL,3
```

(continued)

```
        JNZ     not_min
        MOV     BL,'-'              ;minus
not_min:
        @d_char BL
        POP     BX
        LOOP    next_ch
        POP     CX
        @d_char blank
; display address at right side
        PUSH    BX
; display segment address
        MOV     BX,ES
        MOV     AL,BH
        CALL    outhex              ;high half
        MOV     AL,BL
        CALL    outhex              ;low half
        @d_char ':'                 ;colon
; display offset address
        MOV     BX,SI               ;offset
        MOV     AL,BH
        CALL    outhex              ;high half
        MOV     AL,BL
        POP     BX
        CALL    outhex              ;low half
        RET
do_hex  ENDP
;************* End of do_hex ************
;*****************************************
; display 16 ASCII bytes
; control characters shown as period
; extended character translated to ASCII
;
; Input:        SI = pointer
;*****************************************
do_ascii PROC
        @d_char blank
        @d_char blank
        MOV     DI,SI
        PUSH    CX
        MOV     CX,16               ;one line
next_as:
        MOV     AL,ES:[DI]
        AND     AL,7Fh              ;make ASCII
        CMP     AL,7Fh              ;DEL?
        JZ      d_per               ;yes
        CMP     AL,blank            ;too small?
        JNB     nbl
d_per:
; change to period
        MOV     AL,period
nbl:
        @d_char AL
        INC     DI                  ;next
        LOOP    next_as
        POP     CX
        RET
do_ascii ENDP
;************* End of do_ascii **********
;*****************************************
; wait for character from keyboard
; don't echo on screen
; if extended code, two calls are made
;
; Output:       AL = character
;*****************************************
```

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```
get_in  PROC
        MOV     AH,8
        INT     21h
        OR      AL,AL              ;zero?
        JNZ     get_2              ;no
; get extended code
        INT     21h
get_2:
        RET
get_in  ENDP
;************* End of get_in  **********
mes1    DB      '    Arabic display--Hex goes from'
        DB      ' right to left',cr,lf
        DB      ' Active keys are: down and up'
        DB      ' arrows, PgDn, PgUp, and Esc$'
mes2    DB      cr,lf,lf,' F  E  D  C  B  A  9  8'
        DB      '  7  6  5  4  3  2  1  0  SEGM'
        DB      ' ADDR  0123456789ABCDEF$'

code    ENDS
        END     strt
```

Table 1: *Arabic display of* BIOS *interrupt vectors. If you execute the* ADUMP *program without parameters, you will see an output listing similar to this.*

Arabic display—Hex goes from right to left
Active keys are: down and up arrows, PgDn, PgUp, and Esc

F	E	D	C B	A	9	8 7	6	5	4 3	2	1	0	SEGM ADDR
00	70	01	F0-F0	00	E2	C3-00	70	01	F0-01	2E	4E	E8	0000:0000
F0	00	FF	47-F0	00	FF	47-F0	00	FF	54-00	70	01	F0	0000:0010
F0	00	E6	DD-F0	00	E6	DD-10	4A	01	2F-0B	6F	01	DF	0000:0020
00	70	01	F0-F0	00	EF	57-C8	00	08	49-F0	00	E6	DD	0000:0030
00	70	09	AB-F0	00	F8	41-F0	00	F8	4D-F0	00	F0	65	0000:0040
0B	6F	01	64-F0	00	E8	2E-F0	00	F8	59-F0	00	E7	39	0000:0050
00	70	01	EA-F0	00	FE	6E-00	70	0A	DD-F6	00	00	00	0000:0060
F0	00	00	00-00	00	05	22-F0	00	F0	A4-F0	00	FF	53	0000:0070
0A	9A	01	3C-0A	9A	01	2F-10	67	03	5C-01	2E	12	C3	0000:0080

Listing 2: MYMAC.LIB, *a macro-definition library.*

```
@d_char MACRO   par?
;; display par? on video screen
;; Usage:   @d_char  AL          ;;from register
;;          @d_char  '*'         ;;constant
        PUSH    DX
        MOV     DL,par?
        MOV     AH,2
        INT     21h
        POP     DX
        ENDM
@ucase  MACRO
        LOCAL   notup?
;; Macro to change AL to upper case
;; Usage:  @ucase
        CMP     AL,'a'           ;;uppercase?
        JB      notup?           ;;yes
        AND     AL,5Fh           ;;make upper
notup?:
        ENDM
```

(continued)

```
@write  MACRO    text?
        LOCAL    around,mesg
;; Macro to embed version number
;; Usage:        @write  'title, date'
        PUSH     DX
        PUSH     AX
        MOV      AH,9             ;;write string
        MOV      DX,OFFSET mesg
        INT      21h
        POP      AX
        POP      DX
        JMP      SHORT around

mesg    DB       text?,'$'
around:                   ;;write
        ENDM
@write_r MACRO   addr?
;; display text at location addr?
;; text must end with $
;; Usage:    @write_r <OFFSET p_ver>

        PUSH     DX
        MOV      DX,addr?
        MOV      AH,9
        INT      21h
        POP      DX
        ENDM
```

converting binary to hexadecimal and hexadecimal to binary. The binary-to-hexadecimal routine uses the 8088 XLAT instruction and a simple table of hexadecimal values for the conversion.

You can back the display up one line by pressing the up arrow key and back it up one page by pressing PgUp. Unfortunately, these operations refresh the entire screen, so they are time-consuming. It would be faster if the information were written directly to the video screen; then the screen would be instantly updated. This technique is also described in my book.

FINALLY

There is considerable confusion between Arabic and Roman styles in reading hexadecimal addresses. However, with the help of ADUMP.ASM or a similar program, you can make such addresses more logically readable.

PART 2: ADJUSTING MEMORY SIZE

Making it smaller—or larger

IT IS POSSIBLE to decrease or increase the amount of memory available for program execution on the IBM PC. Everyone can find reasons for increasing memory, but there are also reasons why you might want to decrease it.

REDUCING THE MEMORY SIZE

Although the IBM PC can, in principle, address about 1 megabyte of memory, DOS versions 2.x and 3.x are limited to a maximum of 640K bytes for program execution. Many programs can use all 640K bytes. However, while several commercial programs won't operate with this much memory, they will run correctly with less, usually 512K bytes or fewer. Furthermore, if you attempt to run one of these programs with the full 640K bytes, you will get the confusing error message "Insufficient memory." You can solve this problem by reducing the effective memory size of your PC temporarily while you run these programs.

One way to reduce memory size is to install a RAM disk. However, if you have a PC AT, it would be better to install a RAM disk in addition to the regular 1 megabyte of memory using a board such as the AST Advantage. Then you can still have 640K bytes of RAM for program execution.

You can also reduce the memory size by creating a resident program. When a program begins execution, DOS gives it all the remaining RAM. If that program terminates normally through interrupt 20h or function 4Ch of interrupt 21h, DOS recovers the allocated RAM for the next program's use. However, if a program terminates with DOS interrupt 27h, DOS reserves a portion of memory, and the effective memory available for the next program is reduced accordingly. This technique is commonly utilized for installing device drivers such as a print spooler or a RAM disk program.

The program in listing 3, FILL.ASM, allocates a 64K-byte block of memory; it does not execute any code in this space. You also need the macro library, MYMAC.LIB (see listing 2 in "Arabic versus Roman" on page 241), since the program uses the macro @write. [*Editor's note*: FILL.ASM, MYMAC.LIB, *and* MEM704.ASM *are available in a variety of formats. See the insert card following page* 176 *for details.*] If you have 640K bytes of memory available, you might occasionally need to run this program.

You can run the DOS CHKDSK.COM program to determine the amount of available memory. For example, if you have 640K bytes, you will see a display such as

```
655360 bytes total
  memory
618464 bytes free
```

If you assemble and execute FILL.ASM, you will see the expression "Memory reduced 64K bytes" on the screen. You should run the CHKDSK.COM program again to verify that the memory has been reduced:

```
655360 bytes total
  memory
552912 bytes free
```

FILL.ASM begins with assembler directives and comments; the INCLUDE directive tells the assembler to look in the library you created, MYMAC.LIB, for the macros. Since FILL.ASM assembles into a .COM file, you set the instruction pointer to 100 hexadecimal with the ORG statement. The executable instructions begin with the @write macro, which displays the "Memory reduced . . ." message.

The program contains only two more microprocessor instructions: MOV and INT. MOV places the resident code length in the DX register; INT terminates the program with DOS interrupt 27h, leaving 64K bytes resident. The assembler calculates the resident length by using the labels pg_len and strt.

INCREASING THE MEMORY TO 704K BYTES

The maximum amount of RAM that DOS can normally use is 640K bytes, ending with segment 9000 hexadecimal. Since the video-screen memory

(continued)

ILLUSTRATED BY MIRIAM SCHAER

begins at segment B000, an unused 64K-byte block of memory is at segment A000. The program MEM704.ASM (listing 4) lets you expand DOS into this segment so that 704K bytes are available to your programs. Of course, you can't use this program unless you have memory in segment A000. Therefore, you might need to add another memory board. Some memory boards, such as the AST SixPak, can't be addressed in this region, while others, like the IBM 64/256 board, can. After adding the new memory and addressing it to the A000 segment, you must run MEM704.ASM to reset the internal indicators for maximum RAM memory to 704K bytes. You don't need to change the switches on your system board that specify memory size.

MEM704.ASM does several things. It increases the maximum memory size, stored in the BIOS data area at 413 hexadecimal (or 40:13), and sets the new memory to zero to avoid parity errors. After making these changes, the program initiates interrupt 19h so the PC will reload DOS. Finally, it checks to make sure that it doesn't perform these services a second time.

First, MEM704.ASM establishes the segment in the BIOS data area at 40 hexadecimal (bios_d). Then it defines the offset (in this segment) of the maximum memory size stored at location 13 hexadecimal (mem_siz). The code segment begins by checking the word at 413 to see if the value stored there is already 704K (2C0 hexadecimal). (This will be the case after the program has reset the computer with interrupt 19h.) If so, the program terminates because this is the second time it has been run. However, if this is the first time the program has executed, it checks to see if the computer has 704K bytes of memory installed.

To determine whether any memory exists at the A000 segment, the program writes the pattern 55 hexadecimal, an alternating sequence of zeros and ones, at the beginning of the A000 segment. Then it reads back the value to see if it is correct. Next, it writes the value AA, an alternating se-

Listing 3: FILL.ASM, *a program to reduce the size of addressable memory. (Note that this is written to be executed in a .COM file.)*

```
        PAGE    ,132
        TITLE   FILL part of memory

COMMENT *
  Program to fill part of memory with
  resident program (some programs will
  not run when there is too much memory).
  Macros: @write
  INT 27h
 *
cr      EQU     13
lf      EQU     10

        IF1
        INCLUDE mymac.lib
        ENDIF

code    SEGMENT
        ASSUME  CS:code, DS:code
        ORG     100h

strt:
   @write    <cr,lf,' Memory reduced 64K bytes'>
;-------------------------------------------------
; quit and stay resident
;-------------------------------------------------
        MOV     DX,OFFSET strt-OFFSET pg_len
        INT     27h                 ;done
pg_len  LABEL   BYTE

code    ENDS
        END     strt
```

Listing 4: MEM704.ASM, *a program to increase addressable memory from 640K to 704K bytes. (Note that this is written to be executed in a .COM file.)*

```
        PAGE    ,132
        TITLE   704K - set memory to 704K bytes
COMMENT *
   Increase memory to 704K bytes by changing
   BIOS data word at 40:13 hex
   Set new memory to zero
 *
cr      EQU     13
lf      EQU     10

        IF1
        INCLUDE mymac.lib
        ENDIF

old_siz EQU     640             ;old mem size
new_siz EQU     704             ;new mem size
new_seg EQU     0A000h          ;704K segment

; BIOS data area
bios_d  SEGMENT AT 40h
        ORG     13h
mem_siz LABEL   WORD            ;memory size
bios_d  ENDS
```

You can increase or decrease the PC's memory to do what you want.

```
code     SEGMENT
         ASSUME  CS:code,DS:code, ES:bios_d
         ORG     100h
strt:
; point to memory size in BIOS data area
         MOV     AX,bios_d            ;zero
         MOV     ES,AX
         MOV     SI,OFFSET mem_siz
; check if already run
         CMP     WORD PTR ES:[SI],new_siz
         JNE     ok
         INT     20h                  ;quit
; check for memory at A000 hex
ok:
         MOV     BX,ES                ;save ES
         MOV     AX,new_seg
         MOV     ES,AX                ;ES=A000
         XOR     DI,DI                ;offset
         MOV     AX,55AAh             ;01010101
         MOV     ES:[DI],AH           ;55 hex
         CMP     AH,ES:[DI]           ;ok?
         JNZ     no_mem               ;no
         MOV     ES:[DI],AL           ;AA hex
         CMP     AL,ES:[DI]           ;ok?
         JNZ     no_mem               ;no
; set memory size for 704K bytes
         MOV     CX,ES                ;save ES
         MOV     ES,BX                ;ES=40
         MOV     WORD PTR ES:[SI],new_siz
         MOV     ES,CX                ;ES=A000
; fill new memory with zeros
         XOR     AX,AX                ;zero word
         MOV     DI,AX                ;zero location
         MOV     CX,8000h             ;32K words
         REP     STOSW                ;do it
         @write  <' Memory now 704K bytes',cr,lf>
         INT     19h                  ;reboot system
; no memory at A000 hex, terminate without change
no_mem:
         @write  'No memory at A000 hex, aborting'
         INT     20h

code     ENDS
         END     strt
```

quence of ones and zeros, and again checks for the correct value. If the program can't read back the values it stored, it concludes that there is no memory at the A000 segment. The program displays an error message and aborts.

If 704K bytes of memory are present, the program changes the BIOS word at 413 to 2C0, sets the memory in segment A000 to zero, writes the message "Memory now 704K bytes" on the screen, and reboots with interrupt 19h.

This "new" memory needs to be set to zero because the IBM PC uses parity-checked memory. Each 8-bit byte has an associated ninth bit that is used for a parity check. The sum of the 9 bits *must* have zero parity. When any byte is read, the parity bit is checked to see that there is no error. However, this scheme works properly only if the parity bits are set correctly on start-up. You can accomplish this by writing a zero in each memory location.

The system sets memory parity only up through 640K bytes. Therefore, the new memory in the A000 segment will not automatically be set to even parity. If you try to read from the new memory before setting its parity, you will get a parity error and your computer will lock up. However, if you first fill the new memory with zeros, it will pass subsequent parity checks.

MEM704.ASM sets the new 64K bytes of memory to zero with the store-string instruction (STOSW). It points the ES:DI registers to the beginning of segment A000, sets the AX register to zero, sets the CX register to 64K bytes (8000 hexadecimal, or 32K, words), and combines the REP instruction with the STOSW string instruction. After you run MEM704.ASM, your programs can use as much as 704K bytes of memory. You might want to establish a 360K-byte RAM disk with the DOS VDISK program. If you do, you will still have 344K bytes of usable memory.

If you run CHKDSK.COM after establishing a 360K-byte RAM disk, you will see a display such as

```
720896 bytes total memory
281472 bytes free
```

Since 1K bytes equals 1024 or 2^{10} bytes, 704K bytes equals 720,896 bytes. You can also think of this as 11 segments (0 through A) of 64K bytes, or 65,536 bytes, each.

While this technique works properly with both the monochrome and the graphics adapter, there is a potential problem. The IBM Extended Graphics Adapter uses part of the A000 segment. Therefore, you cannot use this technique when you have an EGA installed in your computer.

In Conclusion

As you can see, you can adjust the amount of memory on the IBM PC to fill your needs. Within limits, you can increase it—or decrease it—to do what you want to do. You aren't necessarily stuck with what comes on the system. ■

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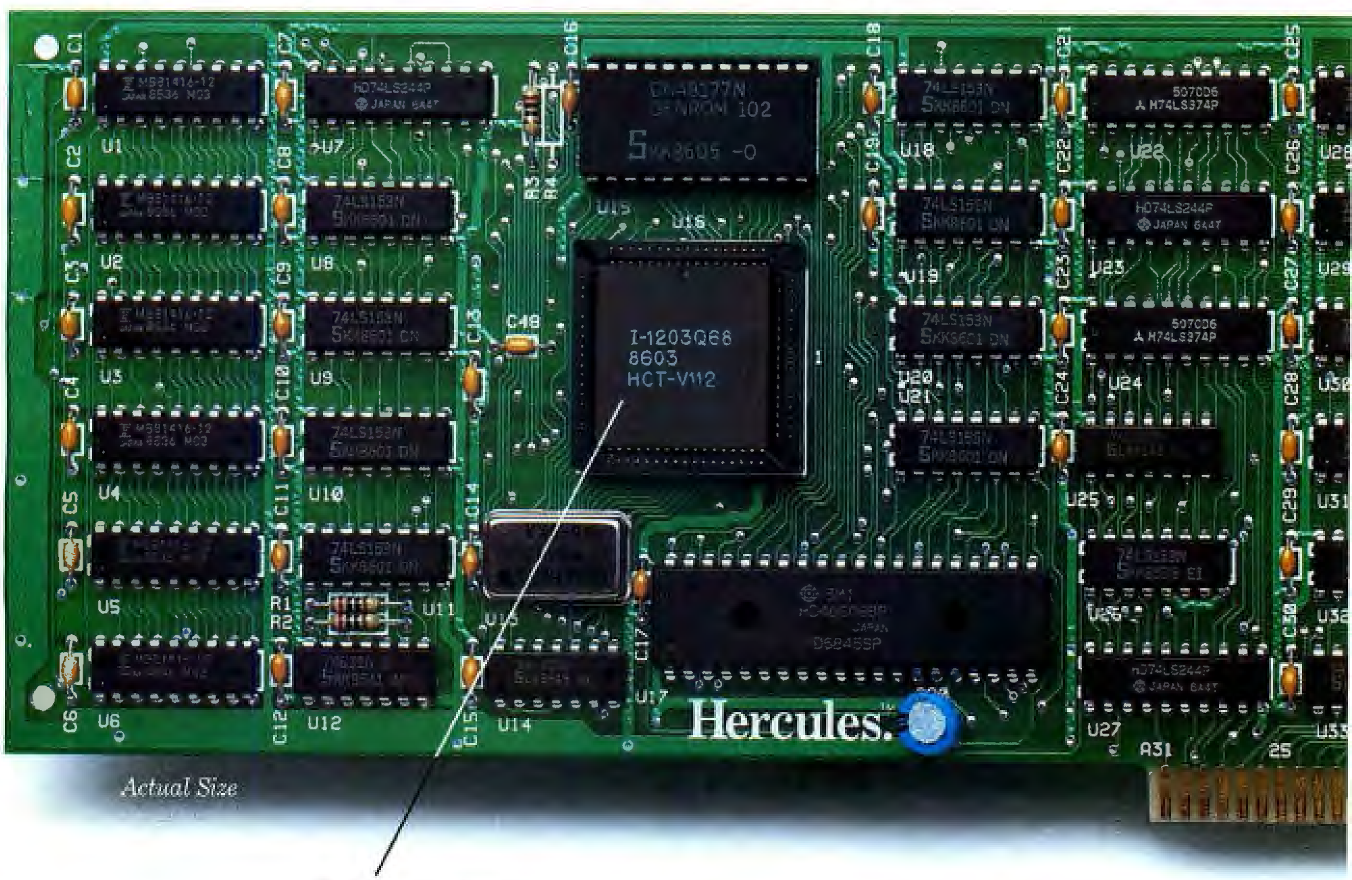

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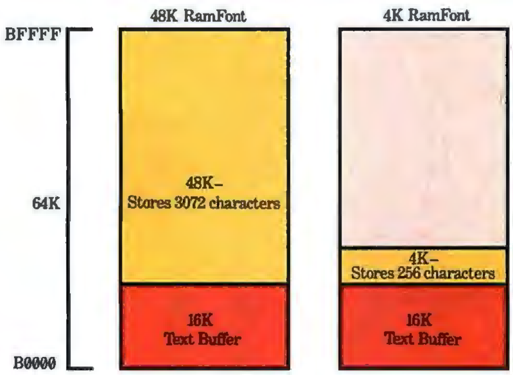

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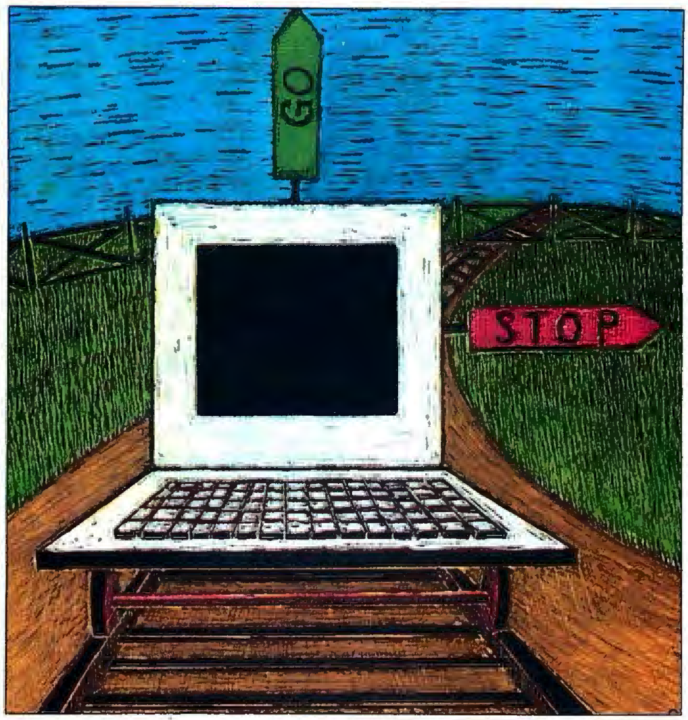
WRITING ASSEMBLY LANGUAGE INTERRUPT ROUTINES

A description of interrupts on the PC and examples of some interrupt handlers

BY WILLIAM J. CLAFF

THIS IS A GUIDE for IBM PC programmers interested in writing assembly language interrupt routines. I will briefly discuss the concept of an interrupt, followed by some programming examples.

You can think of interrupt routines as subroutines called by the hardware or the operating system. Implementing interrupt routines is an advanced topic in programming that requires a high degree of understanding of the computer's existing interrupt structure and hardware. I am assuming that you are familiar with the basics of assembly language programming for the IBM PC.



INTERRUPTS ON THE 8088

The Intel 8088 microprocessor has 256 interrupts that are dispatched through the interrupt-vector table located at 0000:0000 hexadecimal. This table is treated as a zero-based array of the interrupt routines' double-word addresses. The two types of interrupts are hardware and software.

The hardware interrupt is aptly named. The CPU, or external circuitry attached to the CPU, generates hardware interrupts. When a hardware interrupt occurs, it suspends the code that is currently executing so the interrupt routine can be called.

The software interrupt is not so aptly named. The execution of the INT instruction generates software interrupts. Since the code is not suspended at an arbitrary location as it is during a hardware interrupt, the term "interrupt" is a misnomer. In effect, INT behaves much like a subroutine call.

Many early microcomputer systems had no software-interrupt capability. This concept was first introduced in the Intel 8080 with the RST (restart) instruction. The 8080's interrupts are usually controlled by an Intel 8259 Programmable Interrupt Controller (PIC) that lets you associate a hardware interrupt with each of the eight RST interrupts. Intel took a different approach with the 8085; it included three hardware interrupts with no corresponding software interrupt. It wasn't until the 8086 that Intel recognized the value of stand-alone software interrupts.

HARDWARE INTERRUPTS

Hardware interrupts are either internal or external. Internal hardware interrupts are generated from within the CPU; external hardware interrupts are generated by circuitry outside the CPU. On the IBM PC, the 8259 PIC manages external interrupts.

SOFTWARE INTERRUPTS

Software interrupts have three levels: BIOS interrupts, DOS interrupts, and application-program interrupts.

IBM intended the BIOS interrupts to be the sole means of accessing the hardware. Unfortunately, due to incomplete functionality and speed considerations, many programs manipulate the hardware directly. Such programs are less likely to work with "IBM-compatible" computers.

DOS interrupts are intended as the sole means of accessing the DOS

(continued)

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ILLUSTRATED BY CLAUDIA TANTILLO

The interrupt-intercept routine remembers the original interrupt routine.

resources. Fortunately, most programs abide by the intent of the DOS software-interrupt interface.

The application-program interrupts are those used by programs executed by the DOS (e.g., BASIC). You must be aware of these interrupts in order to permanently install a new interrupt routine. Although many interrupts are unused, only interrupts 60h through 67h are officially available.

INTERRUPT LEVELS

To illustrate the various interrupt levels, I want to consider the PC's keyboard. The three keyboard-related interrupts are the external hardware interrupt, the BIOS software interrupt, and the DOS software interrupt.

A DOS software interrupt that involves the keyboard (e.g., function 1h) will use the BIOS software interrupt 16h to interface with the hardware. The INT 016H routine polls memory locations it shares with hardware interrupt 9h. When you press a key, you generate an interrupt 9h. The INT 009H routine stores the keystroke in the shared buffer; the INT 016H routine senses the arrival of the keystroke and returns the key to DOS.

REPLACEMENT VS. INTERCEPT

An interrupt-replacement routine is one that replaces an existing interrupt routine. An INT 023H (control/break) handler would be of this type.

Rather than replacing an existing interrupt routine, the interrupt-intercept routine remembers the original interrupt routine. It might or might not pass control through to the original routine. Most keyboard macro programs are of this type. They do not replace the BIOS INT 009H routine (the keyboard-interrupt handler) but field the hardware interrupt first and decide whether or not to use the

(continued)

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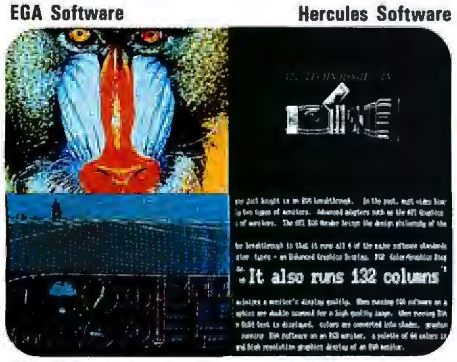

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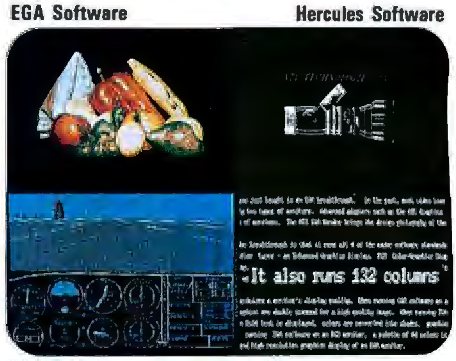

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Listing 1: *Source code for the* PRTSC *program. The include file,* PSP.INC, *is in listing* 2.

```
;=======INTERRUPT VECTOR STRUCTURE
VECTOR  STRUC
REGIP   DW      ?
REGCS   DW      ?
VECTOR  ENDS
;=======KEYBOARD SHIFT FLAG RECORD
RIGHT   EQU     00000001B
;=======CODE SEGMENT
CODE    SEGMENT
;*******EXECUTION STARTS WITH THIS PIECE
        ASSUME  CS:CODE,DS:CODE,ES:CODE,SS:CODE
; PROGRAM SEGMENT PREFIX
        INCLUDE PSP.INC
; LABEL FOR END STATEMENT
IP      LABEL   NEAR
        JMP     SHORT START
;*******INTERRUPT INTERCEPT PIECE
        ASSUME  CS:CODE,DS:NOTHING,ES:NOTHING
        ASSUME  SS:NOTHING
ORG05   VECTOR  <>              ;ORIGINAL INT
                                ; 005H VECTOR
;-------INTERCEPT ROUTINE
INT05   PROC    FAR
        PUSH    AX
        MOV     AH,002H         ;GET KEYBOARD
                                ; FLAGS FROM BIOS
        INT     016H
; TEST FOR RIGHT SHIFT KEY
        TEST    AL,RIGHT
        POP     AX
        JNZ     INT05X
; NOT DOWN, DO ORIGINAL INT 005H
        JMP     ORG05
INT05X  LABEL   NEAR
        IRET
INT05   ENDP
;*******INITIALIZATION PIECE
        ASSUME  CS:CODE,DS:CODE,ES:CODE,SS:CODE
START   LABEL   NEAR
;-------GET INT 5 VECTOR AND SAVE IN ORG05
        PUSH    ES
        MOV     AH,035H
        MOV     AL,005H
        INT     021H
        ASSUME  ES:NOTHING
        MOV     ORG05.REGIP,BX
        MOV     ORG05.REGCS,ES
        POP     ES
        ASSUME  ES:CODE
;-------SET INT 5 VECTOR TO INT05
        MOV     AH,025H
        MOV     AL,005H
        MOV     DX,OFFSET INT05
        INT     021H
;-------FREE MEMORY ALLOCATED TO THE ENVIRONMENT
        PUSH    ES
        MOV     AH,049H
        MOV     ES,ENVIRONMENT
        ASSUME  ES:NOTHING
        INT     021H
```

BIOS INT 009H routine as well.

In fact, most interrupt routines are (or should be) interrupt-intercept routines. For example, some word processors will replace the keyboard interrupt and not pass control through to other programs "watching" the keyboard.

So far, I have been careful to differentiate hardware from software, internal from external, and BIOS from DOS interrupts. However, the type of interrupt routine is usually implied in the interrupt number. For the balance of this article, I will not distinguish between interrupt types unless there is an ambiguity.

PRTSC

Listing 1, PRTSC.ASM, is a handy interrupt-intercept routine. [*Editor's note: The listings in this article are available on disk, in print, and on* BIX. *See the insert card following page* 176 *for details. Listings are also available on* BYTEnet. *See page* 4.] It intercepts interrupt 5h (the print-screen interrupt) and passes control through to the original print-screen routine only if you are not holding down the right Shift key. This eliminates accidental print-screen functions caused by careless typists and abetted by the adjacent placement of the Shift and Print Screen keys on the IBM PC and PC XT keyboards.

PRTSC begins by defining VECTOR and RIGHT. VECTOR is a structure for holding an interrupt-vector address. RIGHT is a bit in KB_FLAG that is described in the ROM BIOS data area.

The CODE segment is divided into three sections: the entry code, the intercept-routine code, and the initialization code. Note that the ASSUME statements at the top of each piece properly convey the segment-register values. In particular, the only known segment-register value at the top of the intercept piece is CS= SEG CODE. I will describe the sections of the CODE segment in order of execution.

ENTRY CODE

The entry code starts with an INCLUDE of the file PSP.INC, as shown in listing 2. This file represents the layout of the program segment prefix (PSP). PRTSC uses the value of ENVIRONMENT (it needs this to free the memory allocated to the environment). IP is a LABEL for the END statement and must be at offset 00100 hexadecimal. There is no need for an ORG 00100H statement, since the PSP occupies 00100 hexadecimal bytes. The only executable code in the entry code is a jump to the START LABEL of the initialization code. Since you jump over the interrupt-routine code, the initialization code will be highest in memory.

```
        POP     ES
        ASSUME  ES:CODE
;-------TERMINATE PROTECTING MEMORY BELOW START
        MOV     DX,OFFSET START
        INT     027H
CODE    ENDS
        END     IP        ;NOTE IP FOR EXE2BIN
```

Listing 2: *Layout of the program segment prefix.*

```
;=======PROGRAM SEGMENT PREFIX
                    INT     020H          ;INT 020H
TOP_OF_MEMORY       DW      ?
                    DB      ?             ;IOCTL
                    DB      5 DUP(?)      ;DOS_JMP
TERMINATE           VECTOR  <>
CTRL_BREAK          VECTOR  <>
CRITICAL_ERROR      VECTOR  <>
                    DW      ?             ;USED BY DOS
                    DB      20 DUP(?)     ;USED BY DOS
ENVIRONMENT         DW      ?
                    DW      7 DUP(?)      ;USED BY DOS
                    DB      20 DUP(?)     ;UNUSED ?
DOS_CALL            PROC    FAR
                    INT     021H          ;INT 021H
                    RET                   ;RET
DOS_CALL            ENDP
                    DB      9 DUP(?)      ;UNUSED ?
FORMATTED_AREA_1    DB      16 DUP(?)
FORMATTED_AREA_2    DB      16 DUP(?)
                    DB      4 DUP(?)      ;UNUSED
UNFORMATTED_LENGTH  DB      ?
UNFORMATTED_AREA    DB      127 DUP(?)
```

INITIALIZATION CODE

This section uses DOS functions 35h (GET) and 25h (SET) to retrieve and modify the interrupt 5h vector. The original interrupt 5h vector is saved for use by the intercept routine.

Note the careful use of ASSUME statements. Good assembly language programming requires strict adherence to this rule: Any statement changing the value of a segment register must be immediately followed by the appropriate ASSUME statement.

The next piece of code frees the memory that is allocated to the environment. This memory is usually freed when the program terminates; however, INT 027H (the terminate-and-stay-resident interrupt) does not free this memory. Finally, the termination interrupt is executed, returning to DOS. The memory before the LABEL START is reserved so that subsequent programs do not overlay the interrupt routine. The IP on the END statement is required for EXE2BIN to work properly. As noted earlier, IP must have a value of 00100 hexadecimal.

INTERCEPT-ROUTINE CODE

Control passes to the code at location INT05 whenever an INT 005H is executed. (Interrupt 5 is a BIOS interrupt that is often replaced by executing the DOS program GRAPHICS.) INT05 checks the keyboard-shift flags using a BIOS interrupt. If the right Shift key is held down, the routine simply exits with an IRET. If the right Shift key is not held down, control is passed to the previous interrupt 5h routine.

ASSEMBLING PRTSC

To assemble PRTSC and produce a usable program file, execute the following commands:

```
MASM PRTSC;
LINK PRTSC;
EXE2BIN PRTSC PRTSC.COM
```

Do not be alarmed by any message from the linker concerning the stack segment, since .COM files cannot have a stack segment. To use PRTSC, type PRTSC on a line by itself in your AUTOEXEC.BAT file.

NESTED INTERCEPT ROUTINES

PRTSC does not detect whether or not you have already installed the intercept routine. The installation of additional PRTSC routines causes no problems, except that each installation uses memory. There is no standard for the identification of intercept routines. Therefore, detection of reinstallation is not a trivial matter. Although it is probably too late to take hold, I propose the following interrupt-routine standard:

```
NAME      DB      '   '
NEXTRTN   VECTOR  <>
ROUTINE   PROC    FAR
          ...
ROUTINE   ENDP
```

The ROUTINE is preceded by the VECTOR NEXTRTN, where VECTOR defines a structure consisting of a segment/offset double word. NEXTRTN

(continued)

Listing 3: *Source code for the* CLK *program.*

```
;=======VECTOR STRUCTURE
VECTOR   STRUC
REGIP    DW      ?
REGCS    DW      ?
VECTOR   ENDS
;=======DATA SEGMENT
DATA     SEGMENT PUBLIC 'DATA'
CLKDIV   DW      ?         ;<- USER PROVIDED DIVISOR
         PUBLIC  CLKDIV
                           ; ACTUAL DIVISOR ...
CLKDIVH DW      ?         ;...(HIGH WORD)
CLKDIVL DW      ?         ;...(LOW WORD)
CLKMOD   DW      ?         ; DIVISOR MODULUS
; USER-PROVIDED NEAR PROCEDURE
CLKRTN   DW      ?
         PUBLIC  CLKRTN
INT08    VECTOR  <>        ;INTERCEPTED INT 008H VECTOR
DATA     ENDS
;=======STACK SEGMENT
STACK    SEGMENT STACK 'STACK'
STACK    ENDS
;=======CODE SEGMENT
CODE     SEGMENT PUBLIC 'CODE'
         ASSUME  CS:CODE,DS:DATA,ES:DATA,SS:STACK
         EXTRN   SEGCODE:WORD     ;<- CODE SEGMENT
         EXTRN   SEGDATA:WORD     ;<- DATA SEGMENT
;*******CLKRATE CLOCK RATE SETTING ROUTINE
CLKRATE PROC     NEAR
;-------LOAD COUNTER 0 OF THE 8259
         PUSH    AX
         MOV     AL,00110110B
         OUT     043H,AL
         POP     AX
         OUT     040H,AL
         XCHG    AH,AL
         OUT     040H,AL
         XCHG    AH,AL
         RET
CLKRATE ENDP
;*******CLKPRO  CLOCK PROLOGUE
CLKPRO   PROC    NEAR
         PUBLIC  CLKPRO
         PUSH    AX
         PUSH    DX
;-------INITIALIZE CLK VARIABLES
         XOR     AX,AX
         CALL    CLKRATE
         MOV     CLKDIV,AX
         MOV     CLKDIVH,1
         MOV     CLKDIVL,AX
         MOV     CLKMOD,AX
         MOV     CLKRTN,OFFSET CLKNUL
;-------SAVE CURRENT INTERRUPT VECTOR
         PUSH    ES
         MOV     AH,035H
         MOV     AL,008H
         INT     021H
         ASSUME  ES:NOTHING
         MOV     INT08.REGIP,BX
         MOV     INT08.REGCS,ES
         POP     ES
         ASSUME  ES:DATA
;-------INSTALL INTERRUPT INTERCEPT VECTOR
```

(continued)

points to the next routine in the intercept-routine chain. If there is no next routine, NEXTRTN is VECTOR <–1,–1>. NEXTRTN is preceded by an eight-character name.

If this standard were in place, the installation code could start at the original interrupt-vector location, follow the interrupt-routine chain, and determine whether or not to install the intercept. The linked list could also be manipulated to modify the priorities of routines vying for a common resource.

CLK

Listing 3, CLK.ASM, is a module containing code to assist in managing the Intel 8253 Programmable Interval Timer. This chip has three counters. Counter 0 generates interrupt 8h, counter 1 triggers dynamic memory refreshes, and counter 2 drives the cassette port or speaker. They count at a rate determined by the system crystal frequency of 14.31818 megahertz.

Designers of the PC chose this value because, when divided by 4, it produces a 3.58-MHz rate for television color burst. When divided by 3, it produces a 4.77-MHz rate for the Intel 8088. When divided by 12, it produces a 1.19-MHz rate for the Intel 8253. The counter chip has 16-bit counters that count down to 0 (a 0 value is equivalent to 65,536 decimal). The 1.19-MHz rate divided by 65,536 produces the 18.2-Hz signal that triggers the interrupt 8h handler.

Interrupt 8h

Interrupt 8h has three responsibilities. First, it updates a count that represents the system time. Second, it decrements the count for the floppy disk head load. This controls when the head is retracted and the LED light goes off; the head is kept against the disk until this count reaches 0. The count is reset on every disk access, thus reducing disk access time if a new read or write request arrives while the head is still loaded.

Third, interrupt 8h does an INT 1CH (timer tick), letting you provide a

(continued)

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The CLK module lets you run counter 0 at almost any rate.

routine to be executed 18.2 times per second. To run counter 0 at a rate other than 65,536, you need to write an intercept routine that calls the original interrupt routine at the rate of 18.2 times per second. The CLK module lets you run counter 0 at almost any rate.

CLK WALK-THROUGH

The CLK module starts with my ubiquitous VECTOR structure. The DATA segment contains several values. CLKDIV is the interrupt rate that the user desires. CLKDIVH and CLKDIVL are the high and low portions of the current divisor. CLKMOD is the number of 1.19-MHz clock ticks since the last true interrupt 8h. CLKRTN is the user-provided NEAR procedure, to be called on every interrupt 8h. INT08 is the original interrupt 8h vector.

I have defined a STACK segment, even though the SS register is not used, so that the ASSUME SS:STACK statement can be coded. Defining all known segments is a good programming practice.

The CODE segment begins with the proper ASSUMEs and with two EXTRN (external) definitions. In particular, the interrupt routine needs SEGDATA to locate the DATA segment.

CLKRATE is a utility routine that sets the counter 0 divisor value.

CLKPRO is the CLK-module prologue routine. It calls CLKRATE to ensure that counter 0's divisor is set to 65,536. The DATA segment values are initialized, and the current interrupt 8h VECTOR is saved in INT08. Finally, CLKPRO installs CLKINT as the interrupt 8h intercept routine.

CLKEPI is the CLK-module epilogue

(continued)

```
        PUSH    DS
        MOV     AH,025H
        MOV     AL,008H
        MOV     DX,OFFSET CLKINT
        MOV     DS,SEGCODE
        ASSUME  DS:CODE
        INT     021H
        POP     DS
        ASSUME  DS:DATA
        POP     DX
        POP     AX
        RET
CLKPRO  ENDP
;*******CLKEPI  CLOCK EPILOGUE
CLKEPI  PROC    NEAR
        PUBLIC  CLKEPI
        PUSH    AX
        PUSH    DX
;-------RESET CLOCK DIVISOR TO 65536
        XOR     AX,AX
        CALL    CLKRATE
;-------RESET INTERRUPT VECTOR
        PUSH    DS
        MOV     AH,025H
        MOV     AL,008H
        LDS     DX,INT08
        ASSUME  DS:NOTHING
        INT     021H
        POP     DS
        ASSUME  DS:DATA
        POP     DX
        POP     AX
        RET
CLKEPI  ENDP
;*******INTERRUPT ROUTINES
        ASSUME  CS:CODE,DS:NOTHING,ES:NOTHING
        ASSUME  SS:NOTHING
;*******CLKINT  CLOCK INTERRUPT INTERCEPT ROUTINE
CLKINT  PROC    FAR
        PUSH    AX
        PUSH    DS
        PUSH    ES
;-------ESTABLISH ADDRESSABILITY
        MOV     DS,SEGDATA
        ASSUME  DS:DATA
        MOV     ES,SEGDATA
        ASSUME  ES:DATA
;-------DO USER ROUTINE.
        CALL    CLKRTN
;-------CHECK FOR ROLL-OVER OF 65536 CYCLES
        MOV     AX,CLKDIVL
        ADD     CLKMOD,AX
        MOV     AX,CLKDIVH
        ADC     AX,0
        JNZ     CLKINT8
;-------NOT TIME YET, SKIP ORIGINAL INTERRUPT
        MOV     AL,00100000B
        OUT     020H,AL
        JMP     CLKINT7
;-------DO THE ORIGINAL INTERRUPT.
CLKINT8 LABEL   NEAR
        PUSHF
        CALL    INT08
CLKINT7 LABEL   NEAR
;-------CHANGE DIVISOR IF SO REQUESTED
        MOV     AX,CLKDIV
```

(continued)

```
         CMP     AX,CLKDIVL
         JE      CLKINTX
         CALL    CLKRATE
         MOV     CLKDIVL,AX
         CMP     AX,1
         MOV     CLKDIVH,0
         ADC     CLKDIVH,0
CLKINTX  LABEL   NEAR
         POP     ES
         ASSUME  ES:NOTHING
         POP     DS
         ASSUME  DS:NOTHING
         POP     AX
         IRET
CLKINT   ENDP
;*******CLKNUL   INITIAL USER PROVIDED ROUTINE
CLKNUL   PROC    NEAR
         RET
CLKNUL   ENDP
CODE     ENDS
         END
```

Listing 4: *Source code for the* DEMO *program.*

```
;=======VECTOR STRUCTURE
VECTOR   STRUC
REGIP    DW      ?
REGCS    DW      ?
VECTOR   ENDS
;=======PSP SEGMENT
PSP      SEGMENT AT 0FFFFH
; PROGRAM SEGMENT PREFIX
         INCLUDE PSP.INC
PSP      ENDS
;=======DATA SEGMENT
DATA     SEGMENT PUBLIC 'DATA'
         EXTRN   CLKDIV:WORD
         EXTRN   CLKRTN:WORD
COL      DB      0          ;COLUMN
DIR      DB      1          ;DIRECTION
LEFT     DB      ?          ;NUMBER LEFT
COLS     DB      ?          ;LAST COLUMN (0 RELATIVE)
SPEED    DW      1000000000000000B      ;SPEED MASK
DEEPS    DW      0000000000000001B      ;BACKWARDS!
DATA     ENDS
;=======STACK SEGMENT
STACK    SEGMENT STACK 'STACK'
         DW      128 DUP(?)
STACK    ENDS
;=======CODE SEGMENT
CODE     SEGMENT PUBLIC 'CODE'
         ASSUME  CS:CODE,DS:PSP,ES:PSP,SS:STACK
         EXTRN   CLKEPI:NEAR
         EXTRN   CLKPRO:NEAR
DOSCALL  VECTOR  <>         ;WILL POINT TO
                            ;  PSP:DOS_CALL

SEGCODE  DW      CODE       ;CODE SEGMENT
         PUBLIC  SEGCODE
SEGDATA  DW      DATA       ;DATA SEGMENT
         PUBLIC  SEGDATA
IP       LABEL   NEAR       ;EXECUTION STARTS HERE
```

(continued)

routine. It also calls CLKRATE to ensure a divisor of 65,536. Then, CLKEPI resets the interrupt 8h interrupt vector to its original value.

CLKINT

CLKINT is the CLK-module interrupt-intercept routine where the work is done. Note again that the program initially assumes nothing except CS= CODE. CLKINT establishes the location of the DATA segment and the extra segment by loading DS and ES with SEGDATA. It then calls the user-provided NEAR procedure, whose address is in CLKRTN. If CLKRTN does not finish before the next timer interrupt, an interrupt might be lost because the hardware keeps track of an interrupt's occurrence only—not how many times it has occurred. The current counter's divisor represents the number of 1.19-MHz ticks that have passed since the last interrupt. This value is added to CLKMOD.

A carry indicates a rollover past 65,536. If there is no rollover, the 8259 is notified that the interrupt has been processed. If there is a rollover, the intercepted interrupt 8h is called. In order to call an interrupt routine, you must precede that call with a PUSHF instruction. Finally, the routine checks to see if the user has requested a different divisor since the previous interrupt and, if so, sets the new divisor.

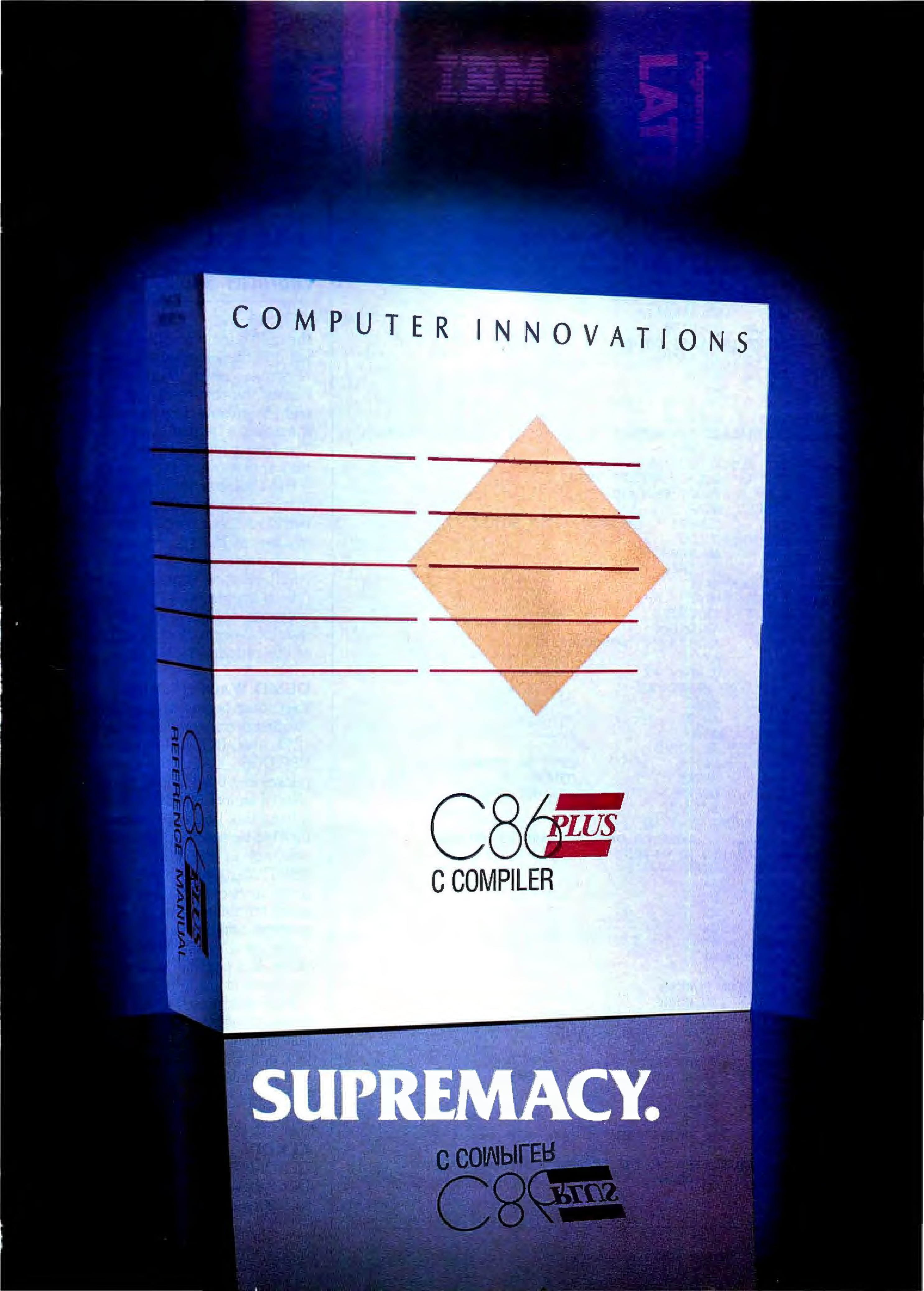
CLKNUL is a null interrupt routine used as the initial value of CLKRTN.

I have used the CLK module for interrupt-driven music at varying tempos and to invoke C procedures as background tasks. Unfortunately, a full-blown example of its use is beyond the scope of this article. However, the DEMO program described below hints at some of its potential uses.

DEMO

Listing 4, DEMO.ASM, is a program that graphically verifies the operation of the CLK module. It writes characters to the top line of the screen until you press the Escape key. The characters are displayed left to right until

(continued)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```
;-------SETUP DOSCALL VECTOR
        MOV     DOSCALL.REGIP,OFFSET DOS_CALL
        MOV     DOSCALL.REGCS,DS
;-------SETUP DS AND ES REGISTERS
        MOV     ES,SEGDATA
        ASSUME  ES:DATA
        MOV     DS,SEGDATA
        ASSUME  DS:DATA
;-------DETERMINE LAST COLUMN
        MOV     AH,00FH
        INT     010H
        DEC     AH
        MOV     COLS,AH
        MOV     LEFT,AH
;-------INITIALIZE CLK MODULE
        CALL    CLKPRO
;-------SET CLOCK ROUTINE
        MOV     CLKRTN,OFFSET INT08
        JMP     SHORT SETRATE
MAINX   LABEL   NEAR
        CALL    CLKEPI   ;DEINSTALL CLK MODULE
;-------RETURN TO DOS
        MOV     AH,000H
        CALL    DOSCALL
;-------SET CLK RATE
SETRATE LABEL   NEAR
        MOV     AX,SPEED
        OR      AX,DEEPS
        AND     AX,1111111100000000B
        SHL     AX,1
        MOV     CLKDIV,AX
;-------WAIT FOR KEYSTROKE
KEY     LABEL   NEAR
        MOV     AH,0
        INT     016H
        CMP     AL,01BH
        JE      MAINX              ;EXIT ON ESCAPE
        ROR     SPEED,1            ;OTHERWISE,
        ROL     DEEPS,1            ; CHANGE SPEED
        JMP     SETRATE
;*******INTERRUPT ROUTINE
        ASSUME  CS:CODE,DS:DATA,ES:DATA,SS:NOTHING
; NEAR PROC CALLED BY INT08
INT08   PROC    NEAR
        PUSH    AX
        PUSH    BX
        PUSH    CX
        PUSH    DX
        PUSH    BP
        PUSH    SI
        PUSH    DI
;-------POSITION CURSOR
        MOV     AH,002H
        MOV     BH,0
        MOV     DH,0
        MOV     DL,COL
        INT     010H
;-------DERIVE CHARACTER FROM TIME OF DAY
        MOV     AH,0
        INT     01AH
        MOV     AL,DL
        AND     AL,00111111B
        ADD     AL,' '
;-------PUT CHARACTER ON THE SCREEN
        MOV     AH,00AH
```

(continued)

When the clock rate is 36.4 Hz, each character shows twice.

the right edge is reached and right to left until the left edge is reached. Any keystroke other than an Escape causes the rate to change. The first eight keystrokes double the rate until it reaches a frequency of 2329.6 Hz. The next eight keystrokes halve the rate until it returns to 18.2 Hz.

The character to display is chosen from the lower-order bits of the system clock. Since the system clock runs at a rate of 18.2 Hz, the initial output is of consecutive characters in the ASCII collating sequence. When the rate is increased to 36.4 Hz, each character shows twice. This verifies that the system clock is still running at the proper 18.2-Hz rate.

DEMO WALK-THROUGH

Execution begins at the LABEL IP. The first two statements set up a VECTOR called DOSCALL that points to PSP:DOS_CALL. This documented but seldom-used field in the PSP consists of an INT 021H and a FAR RET. Calling this VECTOR causes an INT 021H to be executed with the CS register set to the PSP. Since calling PSP:DOS_CALL meets all the requirements of DOS functions 0h (program terminate) and 31h (terminate process and remain resident), you never need to use INT 020H or INT 027H. It is possible to make an .EXE file resident using this technique.

At initialization, DEMO sets up the segment registers and determines the last display column. It then calls the CLK prologue routine and informs the CLK module that INT08 is the routine to be called at the rate determined by CLKDIV.

CLKDIV

CLKDIV is derived from SPEED and DEEPS using some unnecessary but fun bit-twiddling. SPEED contains a

(continued)

Fast ANSI Console Driver


```
          MOV     BH,0
          MOV     CX,1
          INT     010H
;--------UPDATE COLUMN
          MOV     AL,DIR
          ADD     COL,AL
          DEC     LEFT
          JNZ     SHOWX
          NEG     DIR
          MOV     AL,COLS
          MOV     LEFT,AL
SHOWX     LABEL   NEAR
          POP     DI
          POP     SI
          POP     BP
          POP     DX
          POP     CX
          POP     BX
          POP     AX
          RET
INT08     ENDP
CODE      ENDS
          END     IP
```

single bit and is rotated right on each keystroke. DEEPS is the reverse of SPEED; it contains a single bit (which is the mirror image of SPEED) that is rotated left on each keystroke. When SPEED and DEEPS are combined via an OR operation, a single bit is in each byte. To set CLKDIV, the program isolates the upper byte and doubles its value. This produces divisors from 10000 down to 02000 hexadecimal in powers of two.

Main Loop

The main loop processes keystrokes. If the keystroke is not an Escape, it cycles CLKDIV as described above. If the keystroke is an Escape, it calls the CLK prologue routine and the program is terminated.

INT08

When INT08 is called, it first pushes all registers. BP, SI, and DI are pushed because INT 010H does not preserve these registers. Next, the routine positions the cursor and derives the character to be displayed from the time of day. It sends this character to the CRT and updates the column number. Finally, INT08 restores all the registers and returns control to the CLK module.

I have used only BIOS interrupts in this program because it is difficult to use DOS interrupts within a hardware-interrupt routine. This is because DOS is not reentrant.

Assembling DEMO

The steps in assembling DEMO are

```
MASM   DEMO;
LINK   DEMO+CLK;
```

To execute the DEMO program, simply enter DEMO.

Conclusion

In this article, I have covered the major aspects of writing interrupt routines for the IBM PC family. You should be able to successfully tackle writing your own interrupt routines by building on this foundation. ■

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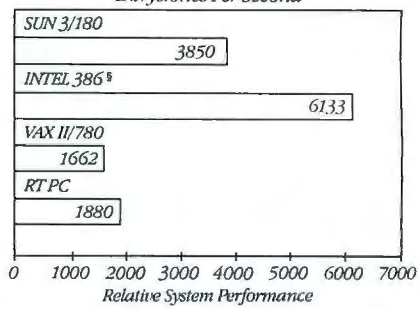

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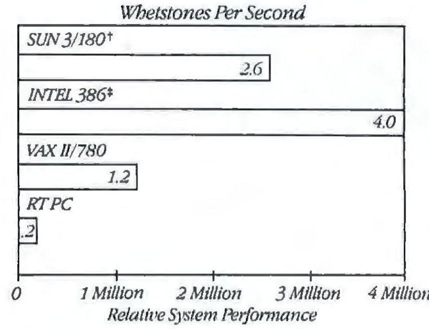

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C VERSUS ASSEMBLY—C PLUS ASSEMBLY

C provides portability and assembly functionality without the pitfalls of assembly code

BY TOM HOGAN

IS C A BETTER choice than assembly language for professional programming tasks? C has a reputation for being portable, easy to write, very fast, and difficult to maintain. Assembly has a reputation for being compact, difficult to write, lightning fast, and impossible to maintain.

While the reputations of C and assembly language have some factual basis, it is easy to find examples that don't fit them. Some C programs are definitely not portable, and some C applications run faster than others written in assembly. Assembly can be written to be readable, as can C (see "Easy C" by Pete Orlin and John Heath, May BYTE). This discussion should clarify matters.

My bias is in favor of C because applications can be written more quickly with C than with assembly. My experience is in developing a C graphics library for the IBM PC. Since the hardware is barely adequate for real-time low-resolution graphics applications, I had to write some assembly code to get acceptable performance. In doing this, I became familiar with the C-to-assembly language interface.

I will compare C with assembly by discussing their relative speed, the suitability of one versus the other for complex applications, real-world products that were written in each language, the comparative popularity of products written in each, which applications absolutely require assembly language, and techniques to help you write assembly functions to work with your C programs.

C's portability is one of its supposed advantages over other languages. Assembly language is not portable, although cross-assemblers can aid in moving code to new architectures. High-level languages like FORTRAN and Pascal have built-in I/O capabilities that limit their portability. C lacks any I/O functions, but every C compiler I am aware of comes with a library that supplies these.

A bigger problem with high-level languages is that most compilers are supersets of the language. If a program relies heavily on a compiler's nonstandard features, it is not going to port easily to another compiler. C avoids this by not including much in the language. If a programmer needs a special function, he writes it himself or buys a commercial library package.

One dilemma C programmers often face is whether to sacrifice speed or portability. If the application must run independently of the hardware (under UNIX, for example), portability is more important. If the application is written for a single architecture, speed is the priority.

C programs are not necessarily portable, but you can write them to be portable, and you must take great care to ensure this. Generally, you reduce a program's portability if you introduce assembly language to improve its speed. The resources and overhead of MS-DOS, for example, are too limiting for highly interactive commercial applications to rely on them (or on the standard library that relies on them), so assembly language is used for video output instead of MS-DOS routines. For example, writing text through DOS is much too slow when you have to update an entire screen for a full-screen editor.

(continued)

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ILLUSTRATED BY KAREN STOLPER

C VERSUS ASSEMBLY

Comparing C programs written for speed with assembly programs produces mixed results.

If you compare well-behaved C programs (such as UNIX applications) with programs written in assembly, you might conclude that assembly is much faster than C. However, comparing C programs written for speed with assembly programs produces mixed results.

An article written by Mark Edwards and titled "Programming Editors, Programmable Editors" in the November 1985 issue of Dr. *Dobb's Journal* rated the speed of different editors for various applications. The editors written in C included BRIEF, EC, EMACS, and Epsilon. [*Editor's note*: BRIEF *and* Epsilon *are written primarily in* C *with assembly routines to optimize performance.* EC *and* EMACS *are written entirely in* C.] Those written in assembly were Pmate, VEDIT PLUS, and XyWrite II Plus. Editors written in C had by far the fastest times in the following categories: search and replace (EC), change ASM comments to C (EMACS), and brace count macro (BRIEF). In file I/O, XyWrite came in first, followed closely by Epsilon, with the rest of the editors quite far behind. Pmate had the fastest load time, although EC was a not-too-distant second.

In the macro benchmark, editors written in assembly were at least an order of magnitude slower than the editors written in C that took first and second place. Screen handling had a three-way tie for first place with a C editor and two assembly editors.

The upshot of all this is that the language in which a program is written matters less than its implementation where speed is concerned. The

(continued)

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2201 Lively Boulevard, Elk Grove Village, IL 60007. Phone: 312/364-1180. TLX: 280-803 editors written in C were generally faster than those written in assembly. There were two reasons for the performance advantage: The editors written in C could be written faster initially, so the author could spend more time improving performance; and a complex design can be implemented in C much more easily than it can in assembly.

You might argue that C programs cannot be fast because they have too much high-level language overhead compared with assembly. Who cares whether or not C has overhead? The question is, "Can I make my C program run like greased lightning?" The answer is, "Yes, if you know what you are doing." The whole question hinges on program design and how well you can write code—not on how efficient your compiler is (although more efficient code is without question desirable).

Let's look at how C programs can be made about as fast as assembly programs. Assume that both the C program and the assembly program use the same algorithm, the algorithm causes the C program to spend 95 percent of its time in 5 percent of the code, and the C program is unacceptably slow. An experienced C programmer can rewrite the time-intensive 5 percent of the C code in assembly, often achieving a several-fold improvement in performance. Thus, the final program will run about as fast as if it had been written entirely in assembly.

In the world of commercial applications, speed is often crucial to success. Part of the reason for the success of Turbo Pascal (written in assembly) is that it is more fun to use than competitive products. Today, people complain that WordStar 2000 (written in C) is slower than the original WordStar (cross-assembled from 8080 assembly), although WordStar 2000 does a lot more.

Assembly advocates tout early successes like dBASE II and WordStar to show that the most popular programs are written in assembly. I submit that assembly was used because it was the

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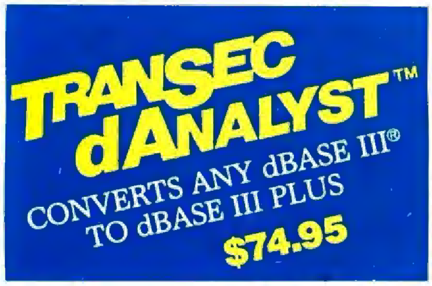

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One overlooked factor is the inverse relation between speed and the time required to write a program.

best tool available at the time. It offered very good speed in the finished applications and produced compact code (important on 8080 systems where memory was limited). Also, users were willing to put up with buggy software because there wasn't a lot of software available.

Now that excellent implementations of C are available, many programmers are choosing them over assembly. Another important reason for using assembly has vanished—compact size. Personal computers tend to have at least 512K bytes of memory, so a program's compactness is less important than it was on 8080 systems. Compactness will become less important as systems have increasing amounts of memory.

Assembly is less attractive as a programming language because programs written in it tend to have more bugs than those written in other languages. Fast programs don't help you get a job done more quickly if they are buggy. Programs written in C help you get the job done faster because the program is more robust (that is, less likely to crash), resulting in less downtime. So a program's useful speed can be as important as its execution speed.

One overlooked factor is the inverse relation between speed and the time necessary to write a program. This is hard to quantify, because it assumes that if you have more time to work on a program you will find a faster algorithm. It is this factor that lets some C programs run faster than their as-

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sembly language counterparts. Even programmers who favor assembly language admit that assembly programs take longer to write than C programs.

A general rule of thumb is that it takes about the same amount of time to write a line of source code no matter which language you use. (Scaling factors enter in if you want precise results, but the general rule is adequate for my argument.) Because it typically takes me three lines of assembly code to generate the equivalent of one line of C, I will estimate that it takes about three times as long to write a program in assembly as it does in C.

The cost to a company that uses assembly as its primary programming language is twofold. Assuming salaries for C and assembly programmers are comparable, the company spends three times as much on programmers' salaries as it would if its programmers wrote in C. And competitors who use C will beat it to market and get plenty of time to establish their products.

As far as maintenance goes, programs written in assembly are more difficult (translate "expensive") to maintain for commercial developers. Naturally, the extra cost is passed along to the consumer.

Some people assert that assembly has a more complete set of instructions than C. I disagree—assembly has a much *finer* set of instructions than C. Assembly gives the programmer much tighter control of program flow. However, it interfaces so nicely with C that you might say that the C instruction set includes assembly's instruction set. As far as addressing memory goes, C provides about everything you need. (The only really necessary data types that C lacks are an 8-byte BCD data type for accounting packages and an 8-byte long for high-resolution graphics.)

C has much more powerful software tools than assembly because of all the support products for C programmers. There are more than 15 professional C compilers, plus many source-level debuggers, general C libraries, C

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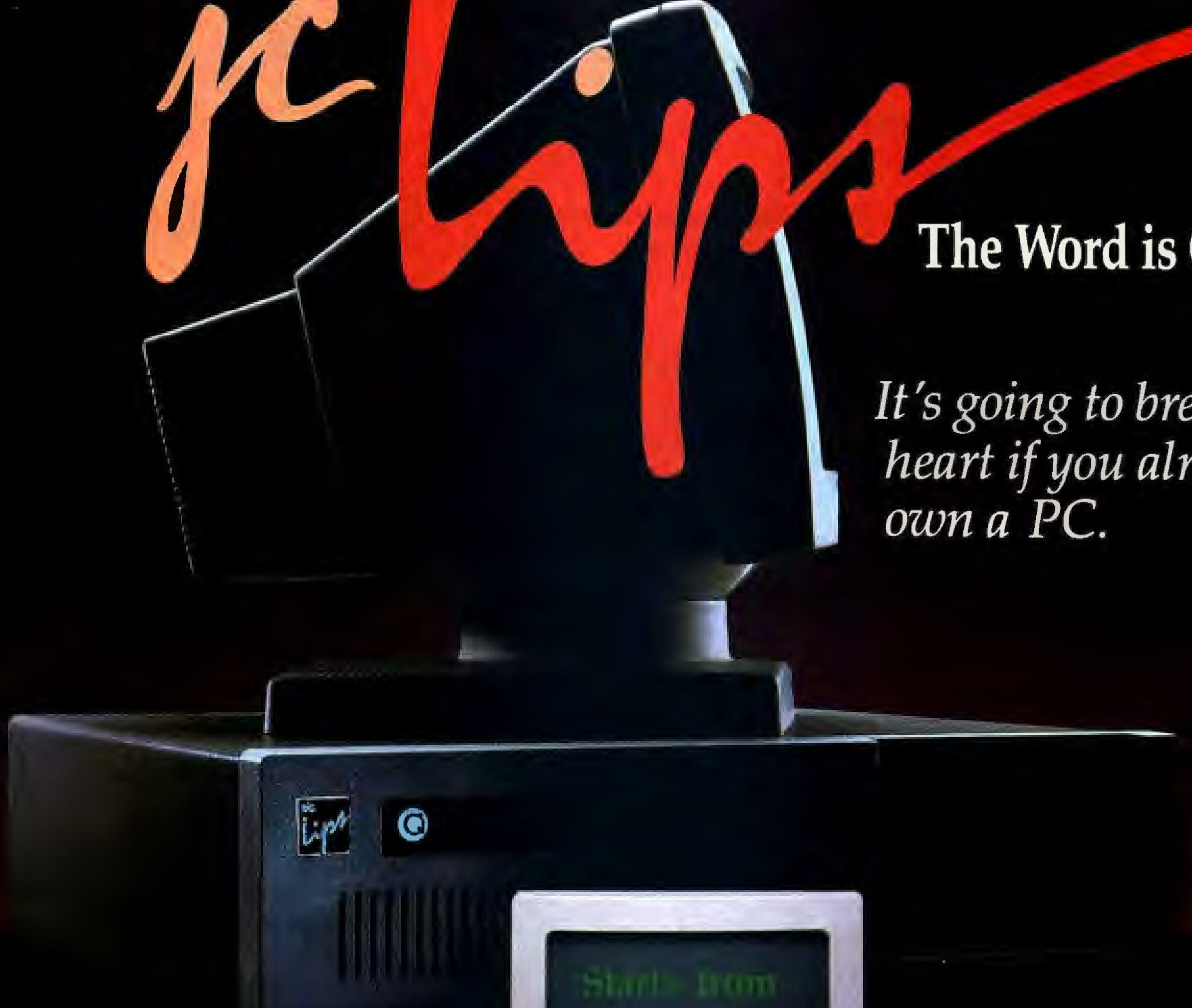

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C's rich programming environment is probably the most important reason to choose it as a development language.

libraries that emulate commercial database managers, interpreters, lint checkers, editors that offer special C support, translators that convert source code from other languages to C, and teaching tools to help novice C programmers learn C. The rich programming environment for C is probably the most important reason to choose C as a development language.

Assembly just doesn't have the support. Support products include Microsoft's Macro Assembler, other miscellaneous assemblers, cross-assemblers, and a few symbolic debuggers. Its support is sparse when compared with C's.

One assembly writer was surprised to learn that a C programmer went to the trouble to write his own I/O routines. He thought that a C compiler was supposed to do that. His error is instructive in the philosophy behind C: The compiler is deliberately kept sparse so that you can tailor I/O routines to your needs. Many C programmers write their own routines eventually. The standard library just gets you up and running under MS-DOS.

Having covered the disadvantages of assembly, I want to point out two instances where it has distinct advantages over C. Where memory is extremely limited, C might not be able to produce code that will fit. Assembly's compactness may be the deciding criterion. Another case is when very high-performance software is needed and the program doesn't spend most of its time in a small sec-

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tion of the code. In this case it might be easier to write the whole application in assembly.

SUPPLEMENTING C WITH ASSEMBLY

Although I have presented C and assembly in an opposition format, I would like to show how assembly can complement C. Of the C programs written for the PC architecture, most are written in the small-data model. Accordingly, if a program needs to access areas outside of the program's data space, such as video RAM, it needs to use assembly routines.

C doesn't provide access to some of the 8088's hardware resources. If a program needs to access a system interrupt or a port, you must use assembly. Generally, the C compiler library includes assembly functions that do these things. Sometimes these resources are inadequate, requiring you to write assembly code.

If a program's performance is too slow, you will have to write certain portions of the code in assembly. Assembly provides access to the fast 8088 block write/search commands (REPZ, REPNZ with MOVS, SCAS, CMPS, or STOS) that C lacks. Again, the compiler library typically provides C functions using fast block writes/searches, but they might not do what the programmer needs.

HOW ASSEMBLY INTERFACES WITH C

Let's look at what C programmers have to take into consideration when writing assembly routines. The C programmer who is starting to write assembly code for use by C programs will run into several obstacles, one of which deals with segments. C compilers take care of all the linkage information so you don't have to worry about code and data segments. Assembly isn't so nice: You have to make sure the assembly code includes instructions that match the output of the C compiler to tell the linker where code and data are to go.

Some C compilers add an underscore before or after public names. When you write public functions or reference static data in assembly code, be sure to add a leading or trailing underscore (as required by your compiler) to its name. Should you forget the underscore, you will probably get an error message from the linker about unresolved external names.

C compilers assume that the contents of certain registers will be saved. In the small-data model, most compilers require that all segment registers be saved. In the large-data model, the ES register doesn't need to be saved, but the contents of all other segment registers need to be saved. If the compiler implements register

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variables, the SI and DI registers might need to be saved. BP needs to be pushed and popped if you use it to address the stack (which you do if you need to pass arguments to the function).

Assembly routines address these arguments as offsets of the base pointer. The difficulty with addressing arguments as numeric offsets is that it is easy to become confused as to just what [BP + 18] is pointing at. The offset is different for the small- and large-code models, because in the large-code model the segment number—as well as the offset—must be in the return sequence. The small-code model requires only the offset. In the large-data model, pointers are 4-byte quantities. To load pointers passed as arguments on the stack into a register requires an LES or LDS instruction. In the small-data model, a simple MOV will suffice.

Sometimes your assembly function will need to return a value. Generally, integers are returned in the AX register. The way pointers are returned is variable, depending on the compiler and whether you are using the small- or large-data model. Longs may be returned in AX and BX or in AX and DX (which is standard DOS convention). Chars are returned in AL. Doubles are returned in AX, BX, CX, and DX. One compiler returns near pointers in a different register than integers—a mistake in my opinion, because many C programmers don't explicitly declare functions to return pointers.

USING A MACRO ASSEMBLER

You can make writing assembly for C a good deal easier when you use a macro assembler. You should combine standard patterns into macros. For example, the prologue to starting a function called FN_INT in the small-code model is

```
PUBLIC FN_INT
FN_INT PROC NEAR
```

As an example, you could write a macro called FN_PROLOGUE (this macro won't work with version 1.0 of

(continued)

MASM because of a bug):

```
FN_PROLOGUE MACRO NAME
PUBLIC NAME
NAME PROC NEAR
ENDM
```

Then, if you wanted to write FN_INT, you could start with

```
FN_PROLOGUE FN_INT
```

Most compilers put the first argument passed to a function at [BP + 4] in the small-code model (remember, the return address and BP register—two words—are commonly pushed onto the stack upon entering a function). Let's define a constant, ARG_BASE, which points at the first argument passed to the assembly function:

```
ARG_BASE EQU BP + 4
```

To make sure you address the stack properly, you can create other constants (assuming the small-data model):

```
INTEGER = 2
POINTER = 2
LONG = 4
LONG_PTR = 4
FLOAT = 4
DOUBLE = 8
CHAR = 2 ; although chars are
         ; 1-byte values, com-
         ; pilers promote
         ; them to integers
         ; before pushing them
         ; on the stack
```

With these defined, you can address the first element on the stack with the expression [ARG_BASE]. If the first argument is a pointer, you can address the second argument with the expression [ARG_BASE + POINTER], and so on.

For those of you who use a compiler that adds an underscore before or after public names, an operator in the Macro Assembler that you will find invaluable is &. For example, if you want to append an underscore to a function called FN_INT, you would say FN_INT&_. This can be handy when you are creating macros. You might want to modify my first example using this trick.

WRITING FAST-EXECUTING ASSEMBLY CODE

If you've decided to use assembly routines to improve the performance of your C program, here are some hints to make these parts of your code as fast as possible.

Keep your variables in registers. The difference between MOV REG, REG and MOV REG, MEMORY is theoretically a factor of eight. In practice, the execution of many small, fast instructions limits the speed because time is spent moving the instructions into the prefetch queue.

You normally have six registers to work with—AX, BX, CX, DX, SI, and DI. Any variables that you can guarantee won't exceed the value of 255 can be kept in AL, AH, BL, BH, and so on. This means you could have up to 10 variables in registers. For most functions, this is more than adequate.

Write large code. This might sound like

(continued)

Listing 1: A *faster way to multiply a byte variable by the value* 80.

```
MOV  AX, VARIABLE    ; 3 bytes, 14 clocks
MOV  CL, 4           ; 2 bytes,  4 clocks
SHL  AX, CL          ; 2 bytes, 24 clocks
MOV  BX, AX          ; 2 bytes,  2 clocks
SHL  AX, 1           ; 2 bytes,  2 clocks
SHL  AX, 1           ; 2 bytes,  6 clocks -- prefetch queue
                     ; is empty before the instruction
                     ; is executed
ADD  AX, BX          ; 2 bytes, 14 clocks -- 4 clocks/byte
                     ; for the BIU to put the instruction
                     ; in the queue plus 2 clocks to
                     ; execute it
```

Listing 2: A *routine to move a row of text into the screen buffer.*

```
      MOV  CX, 40            ; 40 WORDs to search
      MOV  DI, BUFFER        ; DI points at the buffer
      MOV  SI, SCREEN_OFFSET ; SI points at the screen offset
START:
      MOV  AX, [DI]          ; 14 clocks -- get two chars from the buffer
      AND  AX, 07F7FH        ;  4 clocks -- turn off the high bits
      MOV  [SI], AX          ; 14 clocks -- put the chars into screen RAM
      ADD  SI, 2             ;  4 clocks -- the next two chars in the buffer
      ADD  DI, 2             ;  4 clocks -- the next two chars in screen RAM
      LOOP START             ; 17 clocks -- continue until CX is zero
```

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Inquiry 27

Listing 3: *A routine to search for a byte using the* compare string block *instruction.*

```
        MOV    CX, 128          ; SEARCH 128 BYTES
        MOV    AL, VALUE        ; VALUE TO BE FOUND
        MOV    DI, OFFSET       ; START OF MEMORY TO SEARCH
REPNZ   SCASB                   ; 15 clocks/repetition,
                                ; plus 2 clocks per
                                ; execution of prefix.
```

Listing 4: *The same search routine without using block instructions.*

```
        MOV    CX, 128          ; SEARCH 128 BYTES
        MOV    AL, VALUE        ; VALUE TO BE FOUND
        MOV    AH, AL           ; SAME VALUE IN AH
        MOV    DI, OFFSET       ; START OF MEMORY TO SEARCH
        DEC    DI
TOP:
        INC    DI               ;  2 clocks
        MOV    AL, AH           ;  2 clocks
        SUB    AL, [DI]         ; 14 clocks
        LOOPNZ TOP              ; 19 clocks
```

heresy, but it's true in many cases. Here's an example in which larger code runs faster than smaller code. Suppose you want to multiply a byte variable by 80 and can guarantee no overflow. One way to do it is

```
MOV AX, VARIABLE ; 3 bytes
                 ; 14 clocks
MOV BL, 80       ; 2 bytes
                 ; 4 clocks
MUL AL, BL       ; 2 bytes
                 ; 70–77 clocks
```

This produces 7 bytes of code that takes 88–95 clocks to execute.

Listing 1 shows a much faster way. The code is 15 bytes long and takes about 66 clocks to execute. It is about twice as much code as the previous example and runs about a third faster. (The comparison assumes that the prefetch queue is full at the beginning of each example.) This finding runs counter to what some experts say—that the larger a program is, the slower it runs.

Michael Abrash had an interesting observation in his article on how using fast shift and rotate instructions can actually slow execution time (see "Bit Rotation Speeds," *PC Tech Journal*, May 1986). Although Intel gives a time of two clocks for the instruction SHL AX, 1, if the instruction isn't already in the prefetch queue, it will take eight clocks to fetch the instruction and two clocks to execute it—five times what the book says. You empty the queue quickly with those fast two or three clock instructions. It might be faster to use the shift or rotate instructions with the CL register.

A corollary of "write large code" is "avoid elegance." Brute-force routines run faster than routines that rely on a lot of decision making. Those conditional jumps aren't cheap. (The idea that more code runs faster also applies to C, although at a higher level. You might have two similar routines that are optimized to be fast at specific tasks instead of one general, slower routine.)

Suppose you want to move a row of text into screen RAM from a buffer and turn off the high bit. You could write the code shown in listing 2. Each iteration of the loop takes 57 clocks. The total time to process 80 characters is 2280 clocks, which doesn't include the overhead from having to refill the prefetch queue after each jump. Look what happens when you use more code:

```
    MOV   CX, 20
    MOV   DI, BUFFER
    MOV   SI, SCREEN__OFFSET
START:
    MOV   AX, [DI]        ; 14 clocks
    AND   AX, 07F7FH      ;  4 clocks
    MOV   [SI], AX        ; 14 clocks
    MOV   AX, [DI + 2]    ; 14 clocks
    AND   AX, 07F7FH      ;  4 clocks
    MOV   [SI + 2], AX    ; 14 clocks
    ADD   SI, 4           ;  4 clocks
    ADD   DI, 4           ;  4 clocks
    LOOP  START           ; 17 clocks
```

The total time for this loop is 1780 clocks. You can continue the process by moving four words at a time instead of two. For four words, the total time is 1530 clocks. The advantage decreases significantly as more time is spent inside the loop. Figure that the overhead is 23 clocks times the number of iterations.

Take advantage of block instructions. The 8088 instruction set includes instructions that can search a block of memory for a byte or word value, or write a byte or word value into a block of memory. These instructions execute much faster than code that uses instructions that search a byte or word at a time. For example, the code in listing 3 searches for VALUE beginning at OFFSET. Assuming that the code searches the entire 128 bytes without finding VALUE, the code will take about 1950 clocks. The equivalent code that doesn't use block instructions is shown in listing 4. The set of instructions in listing 4 takes over twice as long to execute as the previous set (37 clocks per repetition versus the previous 15).

Count the clocks. Use short instructions if possible. Be aware of how instructions modify flags so you don't use a TST or CMP if the flags already contain the information you need to do a conditional jump. Use one-word instruction instead of two byte instructions if possible. The list of tricks to speed up code goes on and on.

One key idea is: Learn the 8088 instruction set. Another is: Don't be afraid to use unconventional tricks. Often, merely setting up a nonintuitive array of data to drive the decision making will reduce code size and increase the speed. This will work in your C code as well. ■

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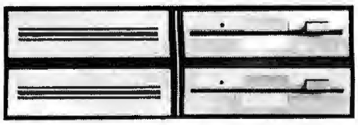

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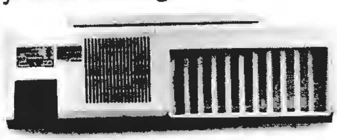

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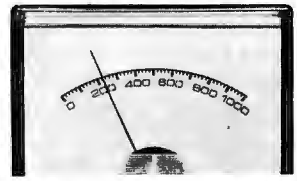

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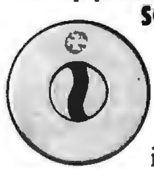

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pascal/turbo #244, from billn (Bill Nicholls)
a comment to message 221

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BillN.

pascal/turbo #268, from jdow (Joanne Dow)
a comment to message 262

At the risk of getting fried for the "C"isms here, this is a very partial listing of the ANSI x3.64 commands. Hope they help.
<^_^>
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c.language/tips #48, from jdow

And printf("\0x1b[%dJ", parameter) will:

```
parameter  action
0          erase to end of screen
1          erase from start to current (including
           current)
2          as noted clear screen leaving cursor in
           place
```

And printf("\0x1b[%dK", parameter); is the same with line replacing screen.
printf("\0x1b[%d;%dH); can be: printf("0x1b[H"); for home cursor or printf("\0x1b[%dH", line); works, as does printf("\0x1b[;%dH", column);

```
cursor     sequence
  up       \0x1b[A
  dn       \0x1b[B
  rt       \0x1b[C    (make last two lines "\x1b" into
                      "\0x1b")
  lt       \0x1b[D
```

Note that a parameter can squeeze into the string just after the "[" for a rep count.

index = \0x1bM
reverse index = \0x1bD

And then we get into the attributes that I won't get into because I am not sure what they'd be implementing. I believe the general sequence would be "\0x1b[%d;%d;...%dm" (any sensible number of %d's in there separated by ";" will work). If the parameter is "0" then all attributes are canceled.
These are ANSI x3.64 defns that, hopefully, they followed in ANSI.SYS but I have no PC to try them on. I'm just reading my terminal defns.
<^_^>

THE EOF( ) FUNCTION

pascal/turbo #1036, from mwelch (Mark Welch)

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To try to cut down execution time, I've been using

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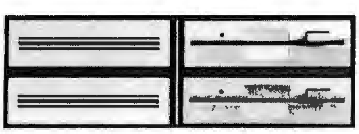

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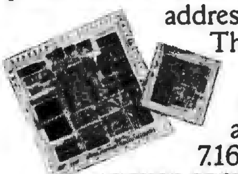

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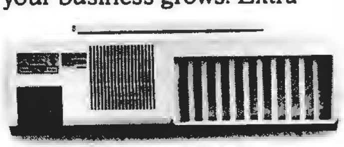

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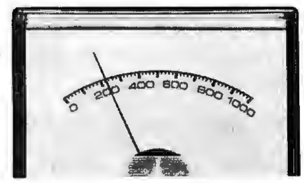

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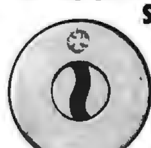

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BIX is the BYTE Information Exchange, BYTE's continuous electronic conferencing system. The following excerpts represent conversations taking place on BIX over a number of months and in a number of different conferences. The common ground for all is, of course, the IBM PC. The conferences represented this month are IBM AT, Pascal, Assembler, and BASIC. For information on how to join BIX, see the advertisement on page 320.

IBM PC AND COMPATIBLES

As the most powerful member of the IBM PC family, the PC AT receives a good deal of attention on BIX. In the following excerpts, an address space is explored.

ADDRESS SPACE E000:0000

ibm.at/at.hardware #353, from tanstaafl (Dana Cline)

Does anyone know if the 64K bytes starting at E000:0000 is used for anything? On my AT, Debug reads changing garbage there. I think it is mapped to an empty ROM socket. I need to use it for a video board and don't know if it will work reliably. Any ideas?

ibm.at/at.hardware #354, from cjackson (Craig Jackson)
a comment to message 353

The only uses I've ever heard of for that area are the PCjr ROM cartridge slots. One is at D000 and the other at E000. IBM presumably will evaluate new uses for this space as the PCjr becomes less of an issue.

ibm.at/at.hardware #355, from rschnapp (Russell L. Schnapp)
a comment to message 353

This area can be used for onboard BIOS ROM. I don't think the AT has any dedicated purpose for E000:0.

ibm.at/at.hardware #369, from tanstaafl
a comment to message 353

I've investigated the E000:xxxx address space on my AT and found some interesting things. The results make me wonder about the sanity of Debug. I'm using a video board that looks like RAM to the system. I jumpered it to fit in segment E. When using the Debug fill command, no matter what I fill with, it sets the RAM to FFs. When I display that area, it shows garbage. However, the garbage changes. Not only that, a Debug display does not match the hex to the ASCII. The left side has FEs and 5As, while the characters are "<" and "s" (and periods). 5A is "Z", so why does Debug display it wrong?

As far as E000 reserved for BIOS ROM, there is none there that I can find. Does it map to the empty sockets on the motherboard? A Debug dump of D000 shows different stuff, and D000 works for the video board. According to all the manuals, both D and E segments are reserved, unused. AST Research uses D and E to page in their Enhanced Memory Spec memory. What do they know about this area?

ibm.at/at.hardware #383, from rschnapp
a comment to message 369

It appears that E000:0 does, in fact, map to the spare ROM sockets on the AT motherboard. We have Golden Bow disk map chips in our ATs, and when I looked at E000:0, I found their copyright notice (doubled up, of course).

I haven't checked the tech specs yet, to find out if E000 is still available if you don't plug in ROM chips in those sockets.

PASCAL

The Pascal conference is consistently one of the busiest on the system. The following conversations cover a number of topics including setting screen attributes, errant EOF markers, a data compression technique (this is a simple technique in the best hacker tradition), and replacing console output drivers.

SCREEN ATTRIBUTES FROM PASCAL

pascal/turbo #221, from rlang (Robert Lang)

This question breaks down into two parts. First, since Turbo Pascal doesn't have an Inverse or Blink command similar to LowVideo and NormVideo, I have been playing around with attribute bytes. The way I currently do it is to create an absolute variable:

```
  MonoScreen : array [ 1..25, 1..80, 1..2 ] of char
absolute $B000:0000;
```

And one for Color screen at $B800. Then I write into Row, Col, 2 for the attribute byte, the code I want. It works but violates every rule on writing generic software. Is there a way I can use an interrupt or ms-dos call to set an attribute byte that will work on all MS-DOS machines? One that is as simple to use as assigning to an array the Row, Col and either char or attribute byte? (Perhaps a procedure with arguments?)

Second, Microsoft Word does something on a monochrome screen I didn't think could be done. When a bold letter, word, etc., is highlighted it appears in inverse, but with a bold background. (Bold in this case implies intensity on.) Whenever I set the intensity bit on, it only works for foreground, that is, the character, not the background. I just double-checked this and MS Word does in fact have two different intensity inverse backgrounds. Anyone know how they can set background on intense? Could they be using a different character set where the character is the background and the foreground is the shadow of the character? If I knew how, I would love to get a copy of the screen bytes as in the adapter when I have some bold text highlighted with MS Word. I would really like to be able to get intense inverse in my TP program. Granted it is an aesthetic issue, but if MS Word can do it, then there has to be a way in TP.

Sorry about length of question, but I am way over my head and could use any help anyone might offer.
Rob Lang

pascal/turbo #232, from rlang
a comment to message 221

My objective is to be MS-DOS-specific, not IBM PC-specific. My assumption (!?) is that if I keep to generic TP procedures and functions, then I can run my software on other machines. Inherent in this assumption was the capability of the MS-DOS machine to be able to display on the screen

```
  Normal Text  ( Intense )
  Dim Text     ( LowVideo )
  Inverse
  Blinking
```

and hopefully any one of the permutations (inverse blinking of high intensity text!?).

Perhaps this assumption is incorrect for all MS-DOS machines and I should admit defeat now and stick with PC-specific software?
Rob Lang

(continued)

pascal/turbo #244, from bilin (Bill Nicholls)
a comment to message 221

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```
cursor     sequence
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  rt       \0x1b[C    (make last two lines "\x1b" into
                      "\0x1b")
  lt       \0x1b[D
```

Note that a parameter can squeeze into the string just after the "[" for a rep count.

index = \0x1bM
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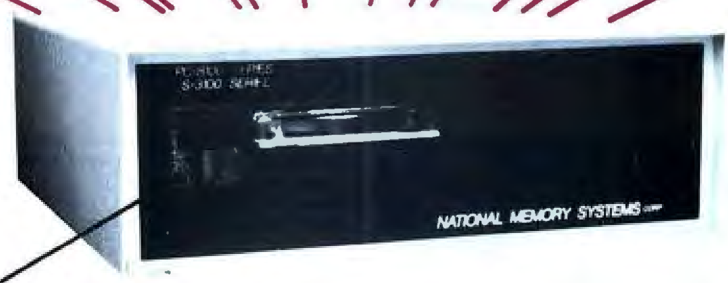

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the Execution Timer from the Turbo Power Utilities, and after much agony I've found the single largest bottleneck: the Turbo eof() function. While each call to it takes only a *very* short time, my program calls it very often (2716 times for a typical run), and it takes longer than most other functions. As a result, it accounts for about 30% of the program's total execution time.

Is there any way to cut down on the number of calls to eof() or to speed up eof() or, conversely, to use some other routine?

The code segment in question is:

```
...
var  f: file of char; (* can't be text, since I need to
know exact file pos *)
...
repeat
...
until eof(f);
...
```

pascal/turbo #1053, from jimkeo (Jim Keohane)
a comment to message 1036

Invert.pas speedup via blockread

Mark, the following reduced time for inverting a file from 3.40 seconds to 1.27. See "Now" calls for start-stop time displays.conds.   - Jim

PS- If garbage past the ^Z in the last block is a problem, then the "for i:=0 to 127" could be changed to "for i:=0 to last" where last was set by a "scan" for ^Z in the current block. See very fast "scan" function in Turbo #757.

PPS- To reduce mem requirements, I would move "Text:S" to end of record description. Then, instead of New(recptr) I would use GetMem(recptr,sizeof(recptr^)-WordLength+Length(St)); That way, if St="HEAD", you save 10 bytes of memory!

```
{==========added for DOS time call================}
type intregs = record
               case integer of
0:(ax,bx,cx,dx,bp,si,di,ds,es,flags:integer);
               1:(al,ah,bl,bh,cl,ch,dl,dh:byte)
             end;
procedure time(var
hours,minutes,seconds,hundredths:integer);
var r:intregs;
begin
 r.ah:=$2c;
 msdos(r);
 hours:=r.ch;
 minutes:=r.cl;
 seconds:=r.dh;
 hundredths:=r.dl
end;

procedure now;
var h,m,s,hs:integer;
begin
 time(h,m,s,hs);
 writeln(h,':',m,':',s,':',hs)
end;

{================ADDED to InvertFil==============}

{p.s. changed fil to just 'file', not 'file of char'}

var block:array[0..127] of char;
    j,k:integer;

Begin   (* InvertFil *)
```

(continued)

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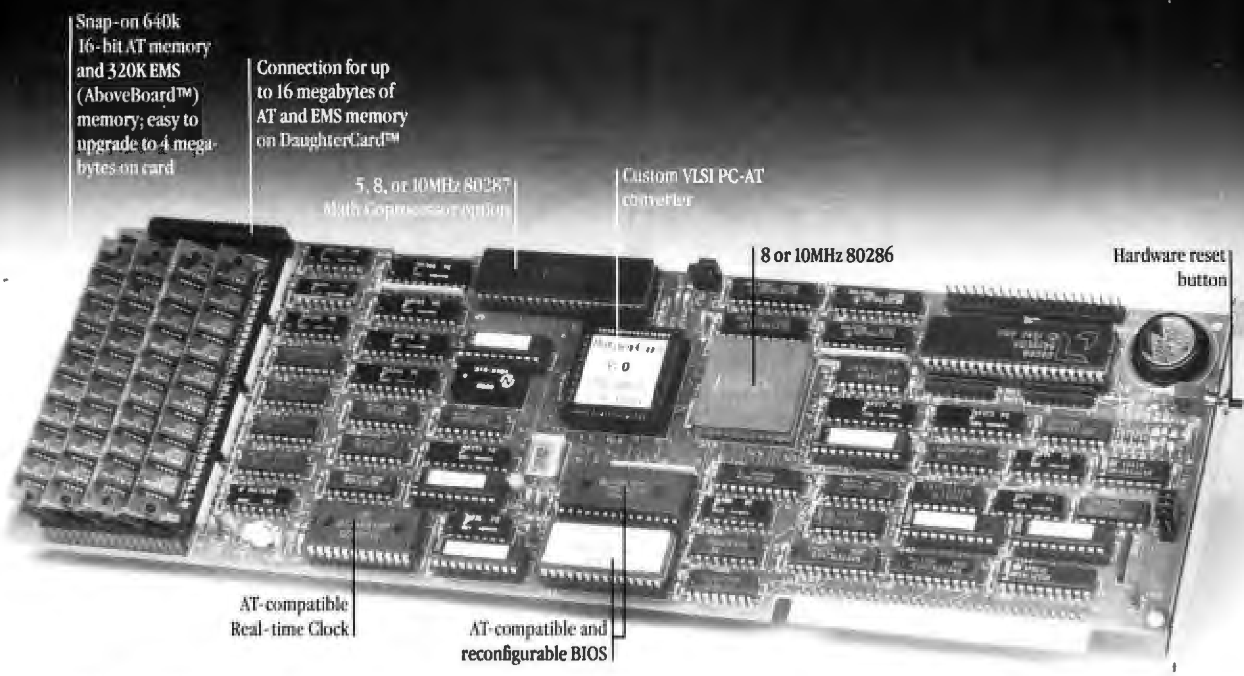

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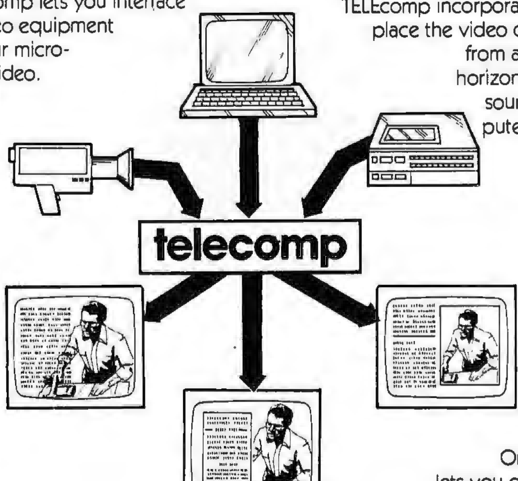

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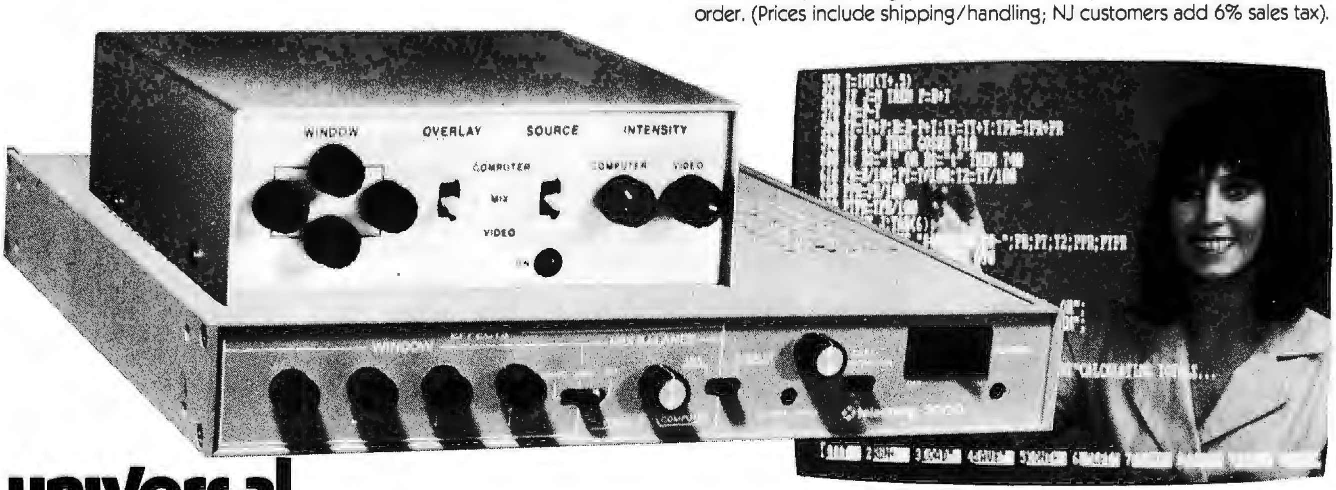

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Inquiry 291

```
  Writeln('Invert: ',FN); (* let user know what file
we're fiddling with *)
  NumFiles := NumFiles + 1;
  If NumFiles > MaxFiles (* remove this when FileList
is a linked list *)
    then begin (* crash impolitely, trashing all work
done so far *)
           writeln('Too many files inverted: maximum is
',MaxFiles);
           Halt;
         end
    else FileList[NumFiles] := fn;
  Assign(fil,fn);
  Reset(fil);
  St := '';
  Now;          {display time to 100ths sec}
  k:=0;                                      {block no}
  blockread(fil,block,1,j);                  {read first
block}
  while (j=1) do
  begin
  for i := 0 to 127 do                       {128 bytes
per block}
  begin
      c:=block[i];
      If ((c >= 'A') and (c < 'z'))
         and ((c >= 'a') or (c <= 'Z'))
        then st := st + UpCase(c)
        else if (Ord(St[0]) > 0)
          then
            begin
              matchKey := false;
              case st[1] of
                'A': matchKey := (st = 'A') or (st =
'AND') or (st = 'AN');
                'I': matchKey := (st = 'IN') or (st =
'IS') or
                                 (st = 'IT') or (st =
'ITS');
                'N': matchKey := (st = 'NOT');
                'O': matchKey := (st = 'OR') or (st =
'ON') or (st = 'OF');
                'T': matchKey := (st = 'THE') or (st =
'TO');
                'Y': matchKey := (st = 'YOU');
              end; (* case *)
              if matchKey
                then
                  St := ''
                else
                  begin
                    New(StPtr);
                    StPtr^.F := NumFiles;
                    StPtr^.FilPosPtr :=k+i-ord(st[0]);
{FilePos out}
                    StPtr^.Next := Nil;
                    AddWord(St,StPtr);
                    St := '';
                  end;
           end;
  end;
  k:=k+128;  {add in 128 bytes per block}
  blockread(fil,block,1,j)    {read next and j=1 if
more}
  end;
  Now;
  Writeln('  Done Inverting ',FN);
End; (* InvertFile *)
```

Data Compression Tricks

pascal/turbo #624, from jimkeo

This is a CORRECTION/REPLACEMENT for msg #619, now withdrawn.

You have a VERY LARGE data file filled with REAL numbers, what can ya do? Well, here's what SOME can do. Turbo REALS take 6 bytes. That's a lot of precision

(continued)

and a big range. Suppose your numbers can be held in an integer. "But my numbers are outside the range -32768..32767," you say. Well, do ya need them kept exactly or just to a certain precision? Like for graphing purposes. Turbo REALS have an 8-bit signed exponent and a 40-bit signed fraction. The following code has 2 routines called "i2r" and "r2i" which swap numbers between integer and real. The integers are really mini-reals with a 5-bit UNSIGNED exponent and an 11-bit UNSIGNED fraction. The example assumes positive so I don't need that 1 bit for exponent sign. The fraction sign only is negative when the value is less than 2. I get around this by adding 2 in "r2i" and subtracting 2 in "i2r" thus saving another bit. The "integers" can now hold values into the BILLIONS (mebbe I shudda called this a sneakie). The precision is to the nearest 16th when number less than 613, nearest 8th when less than 1025, nearest whole number when less than 4094, nearest even number when less than 8190 and so on. Depending on your needs the below routines might save you a lot of disk space, disk I/o time and RAM! You can always modify the routines to return a 3-byte structure (as a proc, not func) and can thus add greater range and/or more precision and still save 50%!

I use the routines all the time in stock market applications and in many graphics applications. Hope they're useful to you. - Jim Keohane

P.S. The routines are in a program that asks you to enter numbers, then shows you what that number becomes after packing and after unpacking. Use the program with the range of numbers your application requires to see if it is adequate. I have other data compression techniques I'll post. Send me mail if you have a particular data type in question (strings, chars, etc.).

```
program tr;
type both = record case integer of
            0:(r:real);
            1:(b:array[0..5] of byte)
            end;
     str3=string[3];

var r:real;i:integer;

function r2i(r:real):integer;
var x:both;
    i:integer;
begin
x.r:=r+2;
i:=(x.b[0] and $1f) shl 11; {5 lsb of exponent}
i:=i or ( (x.b[5] and $7f) shl 4); {hi 7 bits of
precision}
i:=i or (x.b[4] shr 4); {lo 4 bits of precision}
r2i:=i
end;

function i2r(i:integer):real;
var j:integer;x:both;
begin
x.r:=0;
x.b[0]:=$80 or ((i shr 11) and $1f);
x.b[5] := (i shr 4) and $7f; {hi 7 bits precision}
x.b[4] := (i and $000f) shl 4; {lo 4 bits precision}
i2r:=x.r-2
end;

begin
repeat
write('enter real number.....');readln(r);
writeln('orig=',r:12:6,' int=',r2i(r),'
packed/unpacked=',i2r(r2i(r)):12:6);
until r=0;
end.
```

Extra advantage: The mini-reals have the bit pattern eeeeehhhhhhhllll where eeeee is a 5-bit exponent,

(continued)

hhhhhhhllll is the fraction broken into high & low significant parts. This means that for real #s less than 2**15-3 (32765) the mini-real retains the same order as the full real. If you wanna test for >, <, =, <=, or >= you can using the mini-real (integer) and not have to convert back to Turbo REALS before every comparison.

Replacing Console Output Driver

pascal/ms.pascal #36, from mcmahon (Steve McMahon)

I'm working with MS Pascal 3.31 (Microsoft's, not IBM's version) and would like to find out if there is any way to replace the console output mechanism in such a fashion that the full Write library can still be used.

What I'm after is something like Turbo's ability to use the ConOutPtr to replace the built-in, underlying console output procedure with another.

This version of MS Pascal has the console output seemingly inextricably linked with the DOS2 file system functions. That's fine if you're willing to accept slow console output that can be killed (along with the program) by an inadvertant control-c from the keyboard, but not OK for anything else.

I'd like to get it to use DOS function 6 for output for program versions to be used on generic MS-DOS machines and the IBM BIOS functions on program versions for use on IBMs. Do I have to give up the write, writeln procedures to do this?

Any help will be much appreciated.
Steve McMahon

---

pascal/ms.pascal #37, from johnm (John McLaughlin)
a comment to message 36

How about using (or writing) a C-type "printf" function with varying numbers of arg's. "printf" may be in pascal.lib, but if not, it would be fairly easy to write. I'm a heavy MS Pascal user.

johnm, portland, or.

---

pascal/ms.pascal #38, from mcmahon
a comment to message 37

The point of finding a way to replace just the driver is to avoid the work of having to redo the terminal I/O routines. If I have to redo them, I'd probably go with a variety of special-purpose routines (e.g., WriteString, WriteLn, WriteInt ... a la Modula-2) rather than one big, relatively non-portable one.

But, there >>must<< be some way to accomplish the driver replacement. If Microsoft really buried the console I/O inextricably in the file system it seems to me they've compromised the possibility of porting code by forcing the use of non-standard constructs to achieve adequate terminal communication.
Steve McMahon

---

pascal/ms.pascal #41, from jsprowl (Jim Sprowl)
a comment to message 36

Steve, you should write your screen routine in assembler and link it into your Pascal program as an "extern" function. I wrote a full VT100 emulator that also emulates the DOS ANSI.SYS device driver. It includes Pascal callable entries that let me pass in single characters as well as LSTRINGS. I use ANSI standard escape sequences to position the cursor, etc. If you write an assembly language procedure to accept an LSTRING, watch out -- Microsoft Pascal passes an LSTRING with two words, not one, pushed on the stack.

(continued)

The first word is the LSTRING length, and the second word is its address within the DATA segment. This is not documented anywhere that I can find. There are some good examples in the IBM Pascal manual of how to pass parameters to an assembly language program.

Assembly language functions are really simple -- just place the return argument in the AX or AL register, if I remember correctly. Make sure to pop off just the same number of bytes as Pascal pushed onto the stack, or the computer will head off into never-never land.

If you pass a byte to an assembly language routine by value, the byte will be placed on the stack along with a byte of padding so that a word is placed on the stack -- caveat emptor!

Let me know if you would like some sample code.

---

pascal/ms.pascal #43, from mcmahon
a comment to message 41

Thot sounds wonderful, but ...

What I was really after was a way to replace the terminal output driver and retain the ability to use all the compiler magic of the Write/WriteLn routines. Writing assembler EXTERN routines is no particular problem: I've done lots before and would have to do another to do what I'm proposing. Except that what I'm proposing doesn't seem to be possible, judging from the reaction here.

To re-iterate:

In Turbo, you can replace the console output driver with a statement like:

```
ConOutPtr := Ofs( MyReplacementRoutine );
```

where MyReplacementRoutine is a function that takes a character as a value parameter. So, in Turbo, you can write a little inline code to handle an alternative console output technique, initialize the ConOutPtr at the top of the program and forget about it!

I guess Microsoft doesn't believe we'd really like to use the Write/WriteLn routines for anything other than slow, redirectable output!

Steve McMahon

ASSEMBLY

Though high-level languages have gotten the lion's share of publicity in the last few years, assembler remains the language tool of choice for many applications. The Assembler conference on BIX has topics covering most of the popular microprocessors in use today. These excerpts from the 8088 topic cover screen writing attributes and writing custom interrupt handlers.

REPLACING DOS INTERRUPT HANDLERS

assembler/cpu8088 #27, from leroy (Leroy Casterline)

I am an experienced C programmer and have come to the point in my life where learning 8088 ASM is necessary. I need to write a few routines in ASM to be called from (Lattice) C and am looking for pointers (no pun intended) to good sources of learning material or any tips you folks would be willing to share with me.

I need to write a couple of interrupt service routines (pref in C) and must come up with a method of replacing the DOS interrupt handlers with pointers to

(continued)

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the C functions that will actually process the interrupt. I need to write a general-purpose routine that will allow me to specify the interrupt number to replace and a pointer to the C function. Anyone had experience with this?

Thanks in advance,
Leroy

---

assembler/cpu8088 #28, from barryn (Barry Nance)
a comment to message 27

Leo Scanlon's "IBM PC & XT Assembly Language: A Guide for Programmers" is a decent text on the subject.

I could put about 60 lines of assembler code here that replaces an interrupt vector (part of a program I wrote). Want it?

---

assembler/cpu8088 #29, from hvanderbilt (Henry Vanderbilt)
a comment to message 28

Somebody's bound to get some good out of it. Put it up!

---

assembler/cpu8088 #30, from barryn
a comment to message 29

OK, you asked for it. (Seriously, it's a code fragment from a GRAPHICS.COM-type replacement that I wrote for the Okidata 92/93 printers. It is about 60 lines long, so, for those not wanting it, you can skip the next message. BTW, pardon that it occurs in uppercase; I apologize in advance.)

---

assembler/cpu8088 #31, from barryn

```
TITLE: Code fragment for interrupt replacement
;
;        INITIALIZATION CODE (NOT PART OF RESIDENT)
;
         INIT_CODE:
              ASSUME  CS:CODE
              PUSH    DS                ; set up DOS
                                        return
              MOV     AX,0
              PUSH    AX
;
;             IF WE'VE BEEN HERE BEFORE, THEN
;             SAY SO AND EXIT GRACEFULLY.
;             (JUST RETURN TO DOS; WE'RE ALREADY
;             RESIDENT)
;
              ASSUME  DS:INT_5_LOC
              MOV     AX,INT_5_LOC      ; establish
              MOV     DS,AX             ; addressability
;
              MOV     DX,INT_5_OFS
              ASSUME  DS:CODE
              MOV     AX,CS
              MOV     DS,AX
              MOV     AX, OFFSET MAIN_ROUTINE
              CMP     AX,DX             ;BIOS interrupt
                                        in place?
              JNE     P010_CONTINUE ;yes, go ahead &
                                        replace
;
              MOV     DX, OFFSET ERRMSG
                                      ;no,say'already
                                      here'
              MOV     AH,9H
              INT     21H
;
              RET              ;FAR RETURN TO DOS
;
;        outline of initialization logic:
;             1. REPLACE INTERRUPT 5 VECTOR ADDRESS
;                    (WITH ADDRESS OF
;                    MAIN_ROUTINE)
```

(continued)

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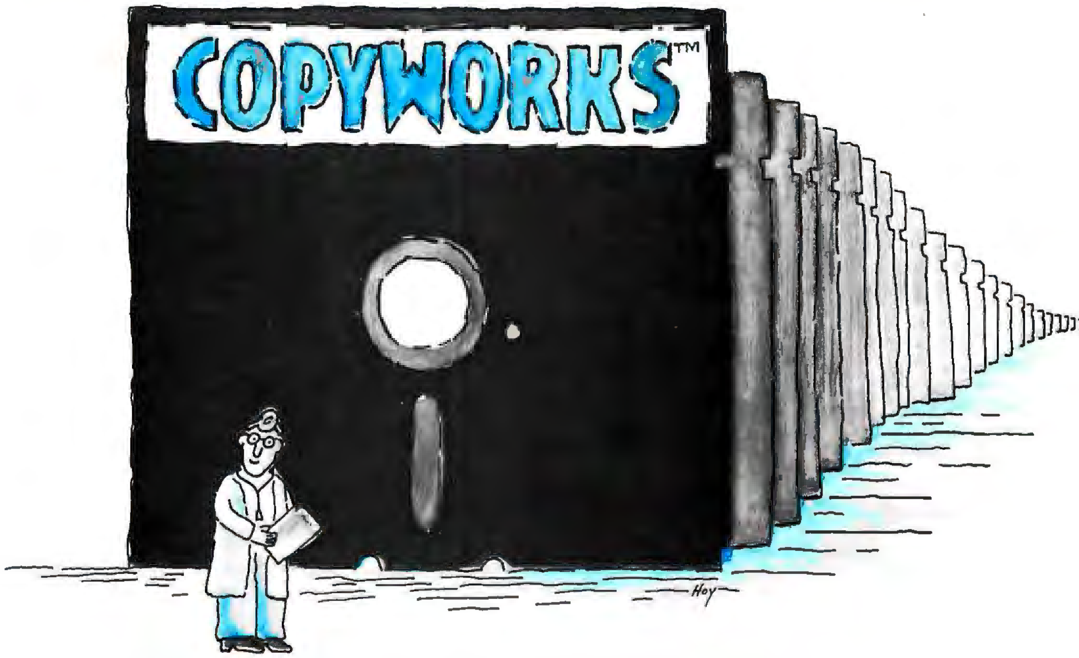

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```
;               2. SAY HELLO TO THE PERSON WATCHING THE
                   SCREEN
;               3. SET PRINT SCREEN STATUS FLAG = ZERO
;               4. TERMINATE BUT STAY RESIDENT
;
P010_CONTINUE:
;
;       replace the int 5 vector
;
                MOV     AX, OFFSET MAIN_ROUTINE
                MOV     DX,AX
                MOV     AL,05H
                MOV     AH,25H
                INT     21H
;
;       say hello
;
                MOV     DX, OFFSET HELLO
                MOV     AH,09H
                INT     21H
;
;       set print screen status flag byte to zero
;
                ASSUME  DS:XXDATA
                MOV     AX,XXDATA
                MOV     DS,AX
                MOV     AX,0
                MOV     STATUS_BYTE,AL
;
;       terminate but stay resident
;        (last address of resident portion is
INIT_CODE)
;
                MOV     DX, OFFSET INIT_CODE
                INT     27H
;
```

BASIC

The BASIC programming language remains one of the most popular ways of getting things done on a micro. The BASIC conference on BIX contains questions, answers, and statements covering problem solving, design philosophy, and programming style using BASIC. Two conversations follow, the first on the FIELD statement in Microsoft BASIC and the second on tips for a compact bit-counting program.

THE FIELD STATEMENT

basic/misc #46, from btonkin (Bruce Tonkin)

I have often heard that Microsoft BASIC users are intimidated by the FIELD statement. I wasn't, and most of the people I have talked to have not been, either. They might not be representative, though. Would any of you like to see the FIELD statement abolished? If so, what would you replace it with? I'd like to hear some comment, especially from people with limited knowledge of BASIC.

basic/misc #48, from dmick (Dan Mick)
a comment to message 46

I sure wish one could *easily* and *clearly* FIELD a file buffer with an array, without having to go through the "dummy variable" crap you usually have to, like so:

```
FOR I=1 TO 256:FIELD #1, (I-1) AS DUM$, 1 AS
CHAR$(I):NEXT I
```

Why not a syntax like FIELD #1, 256 AS A$() and let BASIC take care of it? (A minor quibble, but otherwise FIELD makes a lot of sense and is a good way to read other language datafiles, like FORTRAN.)

(continued)

A$(), #1, 256 BY 1? Or FIELD #1; A$(256) BY 1? Maybe even FIELD #1, A$(1-256) BY 1 or FIELD #1, 1 AS A$(256)

Is the horse dead yet? (smirk) Is it obvious I've read Pascal and PL/I? (grin,chuckle)

---

basic/misc #51, from btonkin
a comment to message 50

Your examples would seem ambiguous, syntactically. The nice thing about the CFIELD statement is that you could have an integer array specify the individual FIELD lengths. It's not clear that any of yours could do the same. Further, A$(256) already has a meaning in BASIC; using it the way you did would be, er, confusing at best. How would you like FIELD #1, USING F(), A$() Where F() is an array holding the field lengths, and A$() is the array of separate fields, in order?

No, I don't think the horse is dead yet. Kick 'im again, Dan.

---

basic/misc #52, from dmick
a comment to message 51

I have an even better thought. How about having the FIELD statement continue from the last statement unless you add the option ,CLEAR or ,NEW to the parameter list? No, better would be a CLEAR FIELD or CLEAR FILENUM statement. Although if you close & re-open the file, the field is cleared, right? How about that? Is there really any reason FIELD should not mean continue specifying the map of this buffer from the last FIELDed position? (Except for compatibility with older code, which I admit is not a trivial exception.) Perhaps a new statement like CFIELD *is* the best option. Or maybe I should have just thought about it for 10 minutes before saying *any* of this.

---

basic/misc #53, from btonkin
a comment to message 52

Sounds like a good idea, except . . . I think there may be a problem with the "of this buffer" part. Could make for horrendous problems in compiled programs, especially given the possibilities of a GOTO statement mucking things up. The other problem I see is one involving multiple FIELD statements, all to the same buffer, existing at the same time. I use that one a lot, depending on how I want to look at the data at the time. If FIELD meant "continue from last fielded location," it would screw up multiple allocations for sure. I'm pretty sure CFIELD isn't the optimal solution, though. Someone's bound to think of something better. Any more ideas?

---

basic/misc #54, from barryn
a comment to message 53

(timidly...) I kind of like the way it works now. If I have to redefine part of a record, I can use the FIELD statement the way you've described. If I want to have multiple FIELD statements that want to follow one another across a record, I just put a FillerX$ item at the beginning of each new FIELD statement whose size exactly covers the already-defined portion of the record.

---

basic/misc #55, from btonkin
a comment to message 54

No need to be timid. Your approach is exactly what I've been doing for years. Still, it seems like rather a waste, and in interpreted BASIC you end up having to watch to make sure you don't make the filler longer than 255 characters (boom! string too long). That latter problem means you've got to use multiple dummy strings explicitly in the FIELD statement for long records, and the line length limitation will eat you up pretty soon.

(continued)

In compiled BASIC under CP/M, you have the same problem; no string can be longer than 255 characters. If you want to write transportable programs, you end up with scads of useless dummy variables cluttering up the code, and FIELD statements that look like their nearest ancestor was spaghetti.

So, the question: what should we do instead?

---

basic/misc #59, from bwaldheim (Bill Waldheim)
a comment to message 46

Bruce, I've been programming in BASIC (Microsoft & GW) for about as long as you have and I agree. The FIELD statement didn't cause me any problems once I became comfortable enough in BASIC to start messing around with files. The beauty of BASIC is that I could write little 10-line programs of the "Gee, I wonder if this'll work" type. I think some beginners have the mistaken idea that they must write useful code right from the start, but that ain't the way to really learn anything. The machines may lock up, but they don't blow up. And avoiding the FIELD statement won't make life any easier later on when writing let's say an accounting program that accesses 50 to 100 accounts. Having to scan them all from the beginning via a sequential type file will really spoil what might otherwise be a good program. So to all you novices out there, jump in and get your feet wet and DON'T be afraid of making mistakes. That's part of the learning process!!!

Bill Waldheim

---

basic/misc #60, from bwaldheim

Bruce, I'm putting these comments in as I scan the new messages, so that's why there are two from me. The CFIELD sounds like a sensible solution to me. As far as clearing things out, as was mentioned in an earlier message, I wish BASIC had a dBASE-type CLEAR statement that you could use to DISCREETLY release variables from memory instead of the shotgun it now has. How sweet it would be!

Bill

---

basic/misc #61, from btonkin
a comment to message 60

A possible way to work around the CLEAR statement would be a CHAIN that allowed an EXCEPT for variables you wanted killed. Often, I get programs where CHAIN ALL is too inclusive, and COMMON is far too much of a pain.

COUNTING "ON" BITS IN A WORD

basic/one.liners #15, from jimkeo

I forget where exactly on BIX this problem was first posed. The problem was to code a routine that calculated the number of one (1) bits in a word. One solution was to use each byte of the word as an index into a 256-byte table preset with the appropriate counts. Another solution that I suggested is the following: Function fnbt(I) returns the number of bits

(continued)

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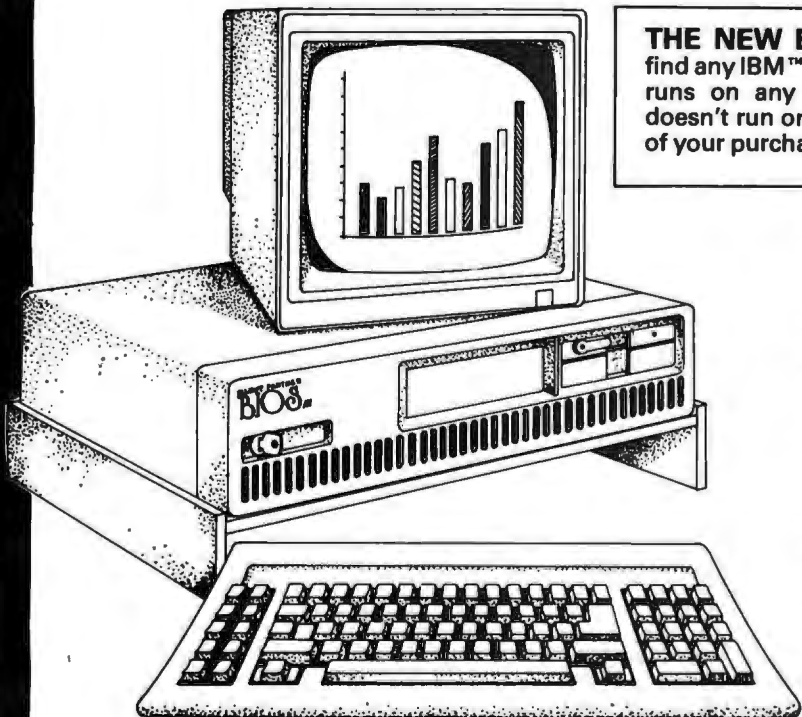

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>Count Bits...
   Touche! Juan. I guess I got a little carried away with functions. - Jim

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basic/one.liners #18, from btonkin
a comment to message 16

Elegant solution, Juan! All I'd change in that one would be the part that reads B=INT(B/2). Better would be B=B\2; it does the same thing!

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basic/one.liners #19, from jimkeo
a comment to message 18

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   - Jim Keohane
   PS- Taken from C code posted by rfoxmich in soft.eng/algorithms #80

```
10 GOTO 80
20 K=0
30 IF B=0 THEN RETURN
40 K=K+1
50 IF B=&H8000 THEN RETURN
60 B=B AND (B-1)
70 GOTO 30
80 INPUT "Number....",B
90 GOSUB 20
100 PRINT K
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basic/one.liners #20, from juan
a comment to message 18

Now that is interesting. "\" you say? OK, I'll try it. What follows is a THREE liner. Believe it or not, it is a full implementation of the Quicksort algorithm. To call it, fill array LN$() with the elements to be sorted and set N to the maximum element to go up to when sorting. On return LN$(N) will be sorted!

```
1000 S=1:STACK(S)=1:STACK(S+1)=N:WHILE
S>0:L=STACK(S):R=STACK(S+1):S=S-2:WHILE
L<R:I=L:J=R:X$=LN$((L+R)/2):WHILE I<=J:WHILE
LN$(I)<X$:I=I+1:WEND:WHILE X$<LN$(J):J=J-1:WEND:IF I<=J
THEN SWAP LN$(I),LN$(J):I=I+1:J=J-1
1010 WEND:IF I<R THEN S=S+2:STACK(S)=I:STACK(S+1)=R
1020 R=J:WEND:WEND:RETURN
```

   Enjoy.
   |1|
   PS- If LN$() is very big, then dimension STACK() out to about 20 or 30, not much more, since by that point you should write an assembly language version.
|1|

---

basic/one.liners #21, from juan
a comment to message 19

As a matter of fact, I think it can. Try this out:

```
  10 K=0:WHILE (B<>0) and (B<>&H8000):K=K+1:B=B and (B-
1):WEND
```

it should work, but I don't guarantee it. I just winged that one.
|1|

---

basic/one.liners #22, from jimkeo
a comment to message 21

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---

basic/one.liners #23, from juan
a comment to message 22

Question: Why do you need that &H8000 anyways?
|1|

---

basic/one.liners #24, from jimkeo
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>&H8000 test
Otherwise, ya get OVERFLOW with "B-1" when B=&H8000 (-32768). Of course, you can disable OVERFLOW as I think I mentioned with the example. - Jim

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An Attack on the Public Domain

ms.dos/other #464, from dondumitru (Donald Dumitru)

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WARNING! WARNING! WARNING! WARNING! WARNING! WARNING!

   The program ARC513.COM is a TROJAN! It will alter the boot sector on your hard disk, preventing you from booting from your HD until you do a PHYSICAL FORMAT! Do *not* run this program! If you see it posted on a BBS, tell the sysop about it! I am attempting to track down the source of the copy that I have - wish me luck.

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   Donald
   PS- But it definitely does things to your hard disk. I ran it *twice*, and had to do a physical format after each run.

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ms.dos/other #469, from dondumitru
a comment to message 467

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7313 Grove Road, Frederick, Maryland 21701 in I that are ON (0 thru 16). It has application where individual bits are used as switches and you wish a count.

— Jim Keohane

```
1 DEF FNB1(I)=(I AND &H5555)+((I\2) AND &H5555)
2 DEF FNB2(I)=(FNB1(I) AND &H3333)+((FNB1(I)\4) AND
&H3333)
3 DEF FNB3(I)=(FNB2(I) AND &HF0F)+((FNB2(I)\16) AND
&HF0F)
4 DEF FNBB(I)=(FNB3(I) AND &HFF)+((FNB3(I)\256) AND
&HFF)
5 DEF FNBT(I)=FNBB(I AND 32767)-(I<0)
6 print fnbt(32767),     fnbt(-1),     fnbt(255),
fnbt(0)
7 REM          15          16          8          0
```

---

basic/one.liners #16, from juan (Juan Orlandini)
a comment to message 15

```
1 CIXI=0:FOR IXI=1 TO 16:CIXI=(B AND
1)+CIXI:B=INT(B/2):NEXT IXI:B=CIXI:RETURN
```

Now that is what I call a ONE-LINER. It counts the number of bits in a word. Just set B equal to the word and then call it. B will return the number of bits on. By the way, this comes directly from a Pascal program that I wrote.

|1|

Moderator of the Osborne Conference.

---

basic/one.liners #17, from jimkeo
a comment to message 16

(continued)

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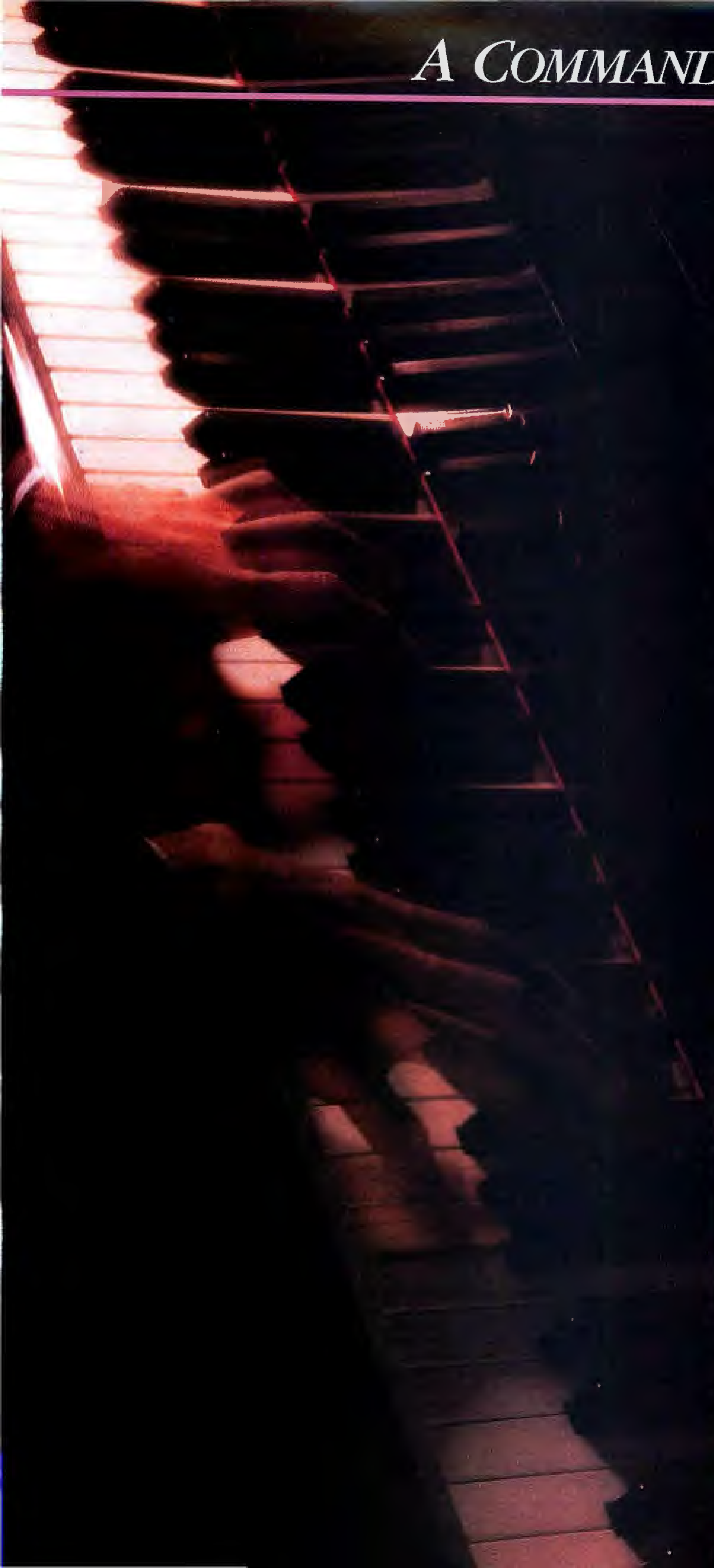

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S>0:L=STACK(S):R=STACK(S+1):S=S-2:WHILE
L<R:I=L:J=R:X$=LN$((L+R)/2):WHILE I<=J:WHILE
LN$(I)<X$:I=I+1:WEND:WHILE X$<LN$(J):J=J-1:WEND:IF I<=J
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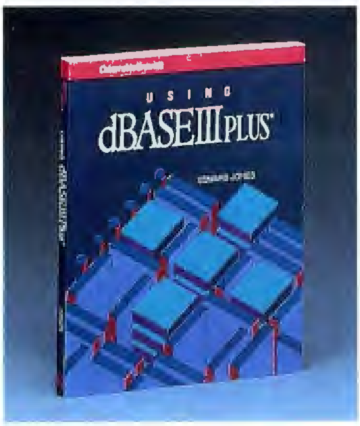

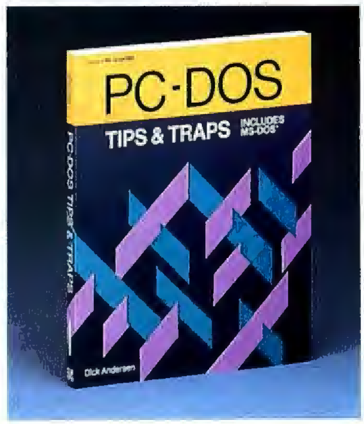

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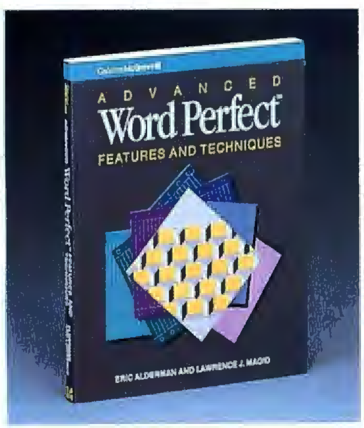

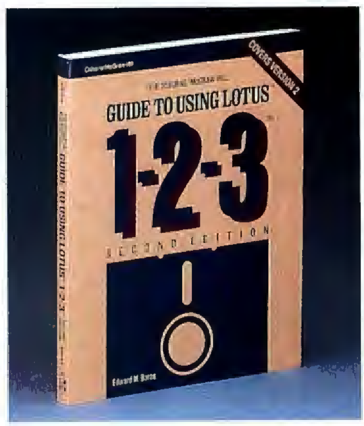

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hacked (meaning that it was not a legitimate release of ARC), and that it was possibly a trojan.

That night, I went back by the BBS where I had seen ARC513.COM and downloaded it. After backing up my hard disk, I ran it. Surprise! It looked just like any other ARC and professed to be version 5.13, created in late April. I had it extract some library files, etc., with no problems. So I rebooted. Surprise! The system locked up after attempting to read from the hard disk, and I had to power down. I let it try to boot from the HD twice more (with duplicate results) before stuffing a floppy in to boot from. The hard disk was *still* accessible, with no apparent change. All data was available. I just couldn't boot from it. So I did a DOS (logical) FORMAT and tried to boot from the HD - lockup. I tried FDISK, FORMAT, reboot, lockup. I did a low-level format, FDISK, FORMAT, reboot, success! (I would sure *hope* so!) I ran the bugger again, and again had to resort to low-level formatting to boot from my hard disk.

My best guess is that it alters bootstrap code in the boot sector. FDISK will detect that there *is* a boot record on the HD and so doesn't rewrite the bootstrap code but just updates the partition table. FORMAT doesn't touch the boot sector at all. So you have to do a low-level format to erase the boot sector, forcing FDISK to completely rewrite it, etc. This is just a guess.

Observations: The company that produces ARC distributes .COM files - these .COM files have the executable code as well as documentation in them, and they unpack themselves when run. The executable code is *always* an .EXE file. (They have stated that executable .COM versions of ARC are hacked and thus are against the licensing agreement.) This trojan is an executable .COM file. Its approximate size is 33792 bytes (having been rounded up from XMODEM transfer). The first couple of bytes in the file are -9C 55 56 8C CD 83-. This should help identify any other copies of it that are around.

I still have a copy of it. If anybody *really* wants to have a chance at debugging through it (I don't think I have the skill to get too far), they should BIXmail me.
Donald

---

ms.dos/other #473, from dmick
a comment to message 472

I have that too, and it's short enough so I could upload ASCII .ASM source or Debug instructions. What it does is intercept INT 13 calls to disk units >3 (hard disks) and if it's a write, returns the error that means "write-protected disk in drive." You must reboot to remove, but it works for most things. I don't know if it's foolproof, though. I suppose one could always call C800: at some offset to do the same thing as an INT 13h, and bypass the resident WPTHD. Or maybe some other wizard knows if (besides that) there's another commonly-used way to write to the disks than INT 13? It seems pretty low-level and possibly what the Debug interrupts use for "w" command. I'll investigate that and report back. Meanwhile, here's the hex dump of WPTHD, which you may use to create a .COM file that will do the above.

```
0000H  EB 1A 00 00 00 00 80 FC 03 75 0C 80 FA 03 76 07
0010H  B8 00 03 F9 CA 02 00 2E FF 2E 02 01 BB 4C 00 B8
0020H  00 00 8E C0 26 8B 47 02 26 8B 1F 8E C0 8B FB BE
0030H  06 01 B9 08 00 F3 A6 75 04 B4 4C CD 21 89 1E 02
0040H  01 8C 06 04 01 BA 06 01 B8 13 25 CD 21 BA 1C 01
0050H  B1 04 D3 EA 42 B4 31 CD 21 00 00 00 00 00 00 00
```

Since I've got SideKick up, here also is the Debug unassembly. And I commented it (that's why this is the second try).

```
6237:0100 EB1A      JMP   011C          ;to install
                                        ;routine
6237:0102 0000      ADD   [BX+SI],AL    ;holds old int
                                        ;vector offset
6237:0104 0000      ADD   [BX+SI],AL    ;and segment
6237:0106 80FC03    CMP   AH,03         ;write?
6237:0109 750C      JNZ   0117          ;no, skip
6237:010B 80FA03    CMP   DL,03         ;disk unit >=3?
6237:010E 7607      JBE   0117          ;no, skip
6237:0110 B80003    MOV   AX,0300       ;wrtprot error
6237:0113 F9        STC                 ;cy=error
6237:0114 CA0200    RETF  0002          ;get rid of
                                        ;callers flags
6237:0117 2E        CS:
6237:0118 FF2E0201  JMP   FAR [0102]    ;go to previous
                                        ;int 13
6237:011C BB4C00    MOV   BX,004C       ;install - 0:4c
                                        ;is int 13 vec
6237:011F B80000    MOV   AX,0000
6237:0122 8EC0      MOV   ES,AX
6237:0124 26        ES:
6237:0125 8B4702    MOV   AX,[BX+02]
6237:0128 26        ES:
6237:0129 8B1F      MOV   BX,[BX]
6237:012B 8EC0      MOV   ES,AX
6237:012D 8BFB      MOV   DI,BX
6237:012F BE0601    MOV   SI,0106
6237:0132 B90800    MOV   CX,0008       ;check first 8
                                        ;bytes of isr
6237:0135 F3        REPZ
6237:0136 A6        CMPSB
6237:0137 7504      JNZ   013D          ;if not same,
                                        ;do install
6237:0139 B44C      MOV   AH,4C         ;same,
                                        ;terminate
6237:013B CD21      INT   21
6237:013D 891E0201  MOV   [0102],BX     ;store old
                                        ;vecadd
6237:0141 8C060401  MOV   [0104],ES
6237:0145 BA0601    MOV   DX,0106       ;install ours
6237:0148 B81325    MOV   AX,2513
6237:014B CD21      INT   21
6237:014D BA1C01    MOV   DX,011C       ;term and stay
                                        ;res
6237:0150 B104      MOV   CL,04
6237:0152 D3EA      SHR   DX,CL
6237:0154 42        INC   DX
6237:0155 B431      MOV   AH,31
6237:0157 CD21      INT   21
```

Okay? I know nobody asked, but....

---

ms.dos/other #474, from barryn
a comment to message 473

Gosh, that'll be even faster than a RAM disk for output files! <grin>

Seriously, the only other way besides INT 13 (and DOS function calls, of course, which use INT 13) to access a disk would be to write low-level code to send commands directly to the disk controller.

I have no idea how you'd even begin to protect against that kind of code.

---

ms.dos/other #475, from dondumitru
a comment to message 474

To protect against *all* attempted access to your hard disk, do what I did while I was debugging through ARC513.COM a bit more today - remove the hard disk. Of course this has the disadvantage of preventing you from *reading* from the HD as well, but in some cases...

I'm gonna type in that WPTHD program and see if it works.
Donald

(continued)

ms.dos/other #479, from petewhite (Pete White)
a comment to message 471

I'm trying to find that same program. It doesn't really "write protect," but I guess that's terminology. It gives a warning when any attempt is made to the hard disk and refuses to do so. I KNOW I have it, but on which section of my board? System (the Cul-De-Dac) is getting too big!

ms.dos/other #483, from wgivens (Wayne Givens)
a comment to message 475

A thought, Don - if that ARC513.COM is messing up the boot record (IBMBIO.COM and IBMSYS.COM?), you can unhide them and do a compare to verify/deny this. If bad, just strip all attributes, do a copy, and remark them as wo, sys, and hidden. If this works, then you know where the bugger is attacking. Otherwise....sigh.
Wayne

ms.dos/other #488, from dmick
a comment to message 483

The "boot record" is a reserved sector on the hard disk that contains partition info, which is bootable, size, etc., and is read (by the hard disk BIOS?) at bootup only. If IBMBIO and IBMSYS were the problems, one could do a SYS or something to redo. I assume Don tried that or has some other indication that the boot record was the problem.

ms.dos/other #489, from dondumitru
a comment to message 483

No! No! It's screwing up the hard disk PARTITION RECORD, which is located outside of the DOS partition (outside of *any* partition). Even Norton utilities won't read it!

ms.dos/other #490, from chrisd (Chris Dunford)
a comment to message 489

BIOS will read it. Using Debug, you can set the registers to read track 0, head 0, sector 0 and do an INT 13 to read the sector into memory someplace. You can then fix it in memory and write it back out.

ms.dos/other #491, from dmick
a comment to message 490

Sure, BIOS will (through Debug, I'd think). So will DOS interrupts....are they 25 and 26h? I never can remember.
Surprising that Norton won't. I guess I never tried it.

Actually, IBM calls that the boot record/partition table. They say a fixed-disk boot record (normally either the DOS loader or a code frag that prints the msg "Non-system disk") consists of the normal boot record PLUS a partition table. They both (being contiguous) reside in the first sector of the disk, that is, sector 0, cylinder 0, head 0. Try getting at it with Debug's L command, Don; it works 'cause I've snooped there before. The L command uses that DOS interrupt (it's 25h, absolute disk read) but makes it a lot easier to do than writing your own code fragment. It'd be interesting to see just what happened as a result of running ARC, just to get some clue as to whether it was a deliberate trojan or what.

BTW, I've seen it on several other boards since you told us all about it. Those who are members might take a look and leave a msg for the sysop if you find it.

ms.dos/other #494, from dondumitru
a comment to message 491

The DOS interrupt *won't* read the boot record - they only allow access to the DOS partition. Any sector number you pass to DOS interrupts is the logical sector in the DOS partition - not the physical sector on the disk.

The hard disk is set up as follows:
The first physical sector has the fixed-disk master boot record in it. This boot record has some bootstrap code in the front, as well as the partition table after. It is loaded into memory (by BIOS) and given control. It looks at its own boot record for a bootable partition, loads that partition's boot record into memory, and gives *it* control. This last step is the first step with diskettes. They don't load a master boot record into memory to find the bootable partition, 'cause they only have *one* partition.

Norton utilities won't read the master fixed-disk boot record (probably) because NU uses DOS interrupts for I/O (so it will work on MS-DOS machines, not just PCs).

What ARC513.COM seems to do is screw up the master fixed-disk boot record's bootstrap code. But it leaves enough of it there so that FDISK thinks it's OK and doesn't bother rewriting it - just updates the partition table at the end.

[The last paragraph is an educated guess!]
Donald

ms.dos/other #524, from dmick
a comment to message 523

Well, let's theorize together. If 1) a program has no INT 13s 2) no obvious DOS writes (INT 21 calls or INT 25 or 26h), and 3) doesn't do any IN or OUT inst. or, if it does, none to the disk board ports, then is the only other way to do it to do one of those by modifying code on the fly? One could use one of the debugging utilities that execute code like an interpreter to breakpoint mem accesses, port accesses, specific interrupts, etc., to stop any Trojan if there's no other way to write to the disk. Let me recap in a bit more organized fashion what ways I think you have to stop:

1) INT 13h (or only some...can look at subfunction in AX to check)
2) DOS calls (INT 21h, several functions...INT 26h)
3) IN's and OUT's to disk ports...I guess the important ones are the hard disk ports, since you can run floppies with write-protect tabs and if you lose 'em who cares anyway.

Is there another way to make the hard disk controller write to the disk? Or is there any other way besides writing to the hd to bung it up?

ms.dos/other #525, from dondumitru
a comment to message 524

All three of those methods are (reasonably) easy to check for in small files. In larger files, it might take a little more time to search through (but would still be worth it). The problem is large files with self-modifying code - can you imagine trying to run that 37K+ ARC513.COM through an intepreter?!! That would be a lot worse than "go out for coffee while its running." Maybe if you had an AT (or a 386-based machine) you could put the CPU in protected mode so self-modifying code wouldn't work. Then if the CPU sets a flag when self-modification is tried, you could check it for an indication. But *lots* of programs would be trapped by the protected mode (any program with data in the same segment as code...*lots*). Other ideas? ■

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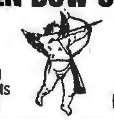

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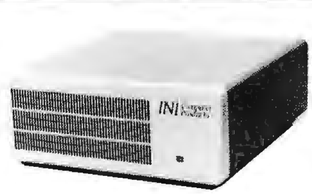

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MONO/GRAPHICS/PRN (HERC)	54
TTL MONITOR W/SWIVEL	96
(1) 360K FLOPPY	92
PARTS	$535
ASSEMBLY & TEST	64
	$599
20 MEG HARD DISK W/CONTROLLER	425

AT COMPUTER

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80286 MOTHER BOARD W 512K RAM	595
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30 MEG 40 MSEC HARD DRIVE	615
EGA CARD	295
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XT PORTABLE $995

640K MOTHER BOARD
640K RAM
MULTI I/O CARD
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SERIAL,
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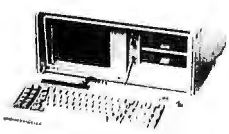

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XT-640K TURBO 4.77/8 MHZ W/OK	99
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384K MULTI-FUNCTION (AST 6 COMP) OK	69
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AB SWITCH BOX W/64K BUFFER (1:2 or 2:1)	94
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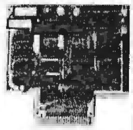

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Inquiry 50

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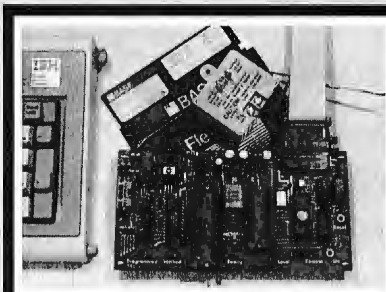

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Two systems from TEC allow the IBM PC/XT/AT to be used as a complete development system for the Motorola 6805 series single chip microcomputers. Model MCPM-1 supports the MC68705P3,P5,U3,U5, R3, & R5 chips. Model MCPM-2 supports the MC1468705F2 & G2 cmos versions. Both systems are priced at $495 and include a cross assembler program, a Simulator/Debugger program and a programming circuit board with driver software. One serial port required.

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1.2 Megabyte, PC-compatible
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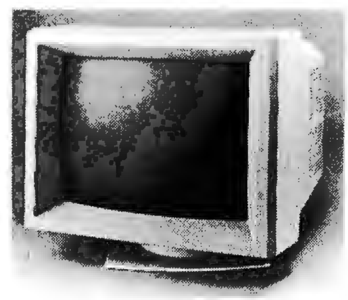

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Inquiry 170

38¢ Each is all you have to pay for the best 5.25" Double Sided, Double Density diskettes to be found!

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Don't buy junk.

DISK WORLD!™ has always been the price and quality leader in diskettes.

Our SuperStar™ diskettes are fully certified to at least 65% clipping levels, far in excess of the ANSI and IBM™ standard of 40%.

Furthermore, SuperStar™ diskettes have jackets of at least 8-mils, as opposed to the 6-mil jackets offered by other low-priced brands. (And, believe us, jacket thickness makes a big difference in whether or not you will get read/write errors on your machine.)

SuperStar™ 3.50" diskettes are all licensed by Sony™ Corporation, the inventor of the 3.50" diskette standard, and meet their exacting standards.

All SuperStar™ diskettes carry a FULL LIFETIME WARRANTY against manufacturing and material defects.

Finally, all SuperStar™ diskettes are manufactured in the United States...not in Hong Kong, Taiwan, Pago Pago or other strange and exotic places where the standards of quality might not be quite as high.

In short, SuperStar™ diskettes are equal or superior to such famous brand names as 3m™, TDK™, Fuji™, Maxell™ and just about any other brand you can name!

SuperStar™ diskettes simply cost half as much or less.

The truth about diskette prices, brand names and some other unpleasant facts of life.

There are exactly two kinds of diskettes: good and bad.

The brand name...or absence of a brand name...on a diskette doesn't mean a thing in terms of quality.

Neither does the price.

For example, let's take a hard look at 3M™ diskettes, a brand which we have carried for more than three years.

During that time, we sold more than $ 6,500,000 worth of these diskettes...and that's one hell of a lot of diskettes.

Until very recently, we were proud to market 3M™ brand diskettes. Now we don't advertise them and actively discourage people from buying them.

Why?

Well, here's a quote from the July 21, 1986 Business Week magazine (page 107): "The disks have been plagued by quality problems recently..."according to one industry expert.

And a radical change in 3M's pricing policies has resulted in exactly the same diskette being sold at prices ranging from 29 to 89 cents, depending on who you were.

Not exactly a fair deal for anyone...except 3M™ which, according to Business Week earned a mere $ 73,000,000 in profits on magnetic media in 1985...mostly at your expense and ours while "(t)he diskettes have been plagued by quality problems recently..."

Counterfeiting and The Hong Kong Connection.

If the life of a diskette purchaser weren't bad enough already, there are now two more problems to contend with.

Counterfeiting is the newest game in town for the "let's get rich quick" crowd.

At least two mail order companies are currently operating very comfortable businesses offering "famous brand name" diskettes at unbeatable prices.

The prices ought to be unbeatable, since these two companies simply take an inferior diskette and slip into a Tyvec™ sleeve which they have printed to be an exact duplicate of the "famous brand name", slap on a forged manufacturer's label to the diskette and make a very tidy profit...without regard to the harm they are causing the end user.

Finally, there is now a wave of cheap, poorly made diskettes pouring in from the Orient, mostly Hong Kong. We are not talking about reputable brands such as Sony™ or Fuji™: we are talking about diskettes which are being turned out in sweatshops on outmoded equipment with little or no regard for quality control.

They show up in this country under a variety of names at extremely attractive prices. Prices so attractive, in fact, that your savings on buying these diskettes may just about pay for the cost of replacing your drives after you use them for a while.

90,000 DISK WORLD!™ customers really tell the story.

DISK WORLD!™ serves more than 90,000 customers throughout the United States and now the world. More and more major corporations, universities and governmental bodies have switched over to our SuperStar™ brands because they recognize that SuperStar™...with DISK WORLD!'s integrity standing behind it...offer absolutely the best combination of HIGH-QUALITY and LOW PRICE.

In short, DISK WORLD!™ and SuperStar™ are unbeatable.

Over the past three years, we've sold more than 30,000,000 diskettes.

Our return rate has been less than 1/10,000th of 1%.

Those two facts speak for themselves.

When every bit counts, it's SuperStar™!

We don't have to boast of imaginary factories employing "floppy phreaks", advertise diskettes for 39¢...if you buy 10,000 of them, offer "2 for 1" replacement guaranties or engage in any of the other hokum schemes designed to part you from your money.

Nor do we have to offer you "famous brand name" diskettes at inflated prices that don't offer you any more in quality, but do manage to support fleets of corporate jet aircraft and executive retreats in Minnesota and Canada.

We simply deliver the best for less.

More than a million diskettes a month flow out of our warehouse under the SuperStar™ "non-name". As noted, fewer than 1/10,000th of 1% of these are returned for any reason.

And that should say it all: SuperStar™ means far more for far less.

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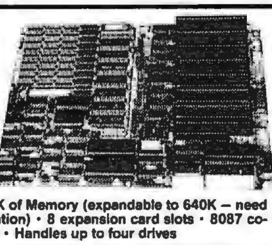
IBM-Special (Includes the 9 items listed above)........ **$549.95**

IBM PC XT Compatible Motherboard



SALE!

• Comes with Zero-K of Memory (expandable to 640K — need 128K RAM for operation) • 8 expansion card slots • 8087 co-processor capability • Handles up to four drives

The whole board comes complete (including BIOS ROM) with system board, specifications and schematics. Ideal for engineer or OEM applications! Size: 12"L x 8½"W x 15/16"H • Wt. 2 lbs.

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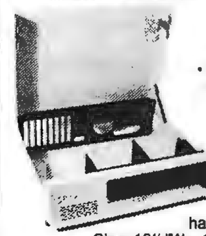

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• Metal housing and chassis with coating & anti-static treatment
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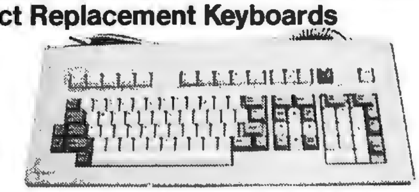

• Enhanced PC/XT keyboard (equivalent to Keytronics™ 5151) • Separate cursor and numeric keyboard • Typewriter style layout: easier to learn! • LED indicators • Ready-to-go, complete with schematic & instructions • Color: off-white • Size: 20"L x 8½"W x 1½"H

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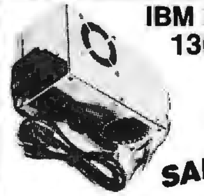

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• Input: 100V-130V @ 47Hz • Output: +5VDC @ 15A, −5VDC @ 0.5A, +12VDC @ 4.2A, −12VDC @ 0.5A • Plug compatible connectors • Fits into IBM PC • Built-in fan • Weight: 6 lbs. • Size: 9½"L x 5½"W x 4⅝"H • Spec. included

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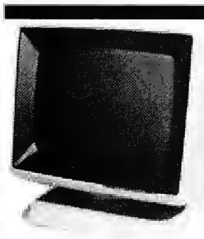
MONITOR



12" Green Monochrome Monitor for IBM PC

FEATURES:
• TTL input • Band width: 20MHz
• Input impedance: 75 Ohm
• Resolution: 800 lines at center
• Power consumption: 30 watts
• Complete with tilt/swivel monitor stand
• Weight: 19 lbs • Size: 14.5"W x 16"D x 16.5"H

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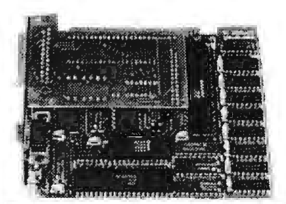

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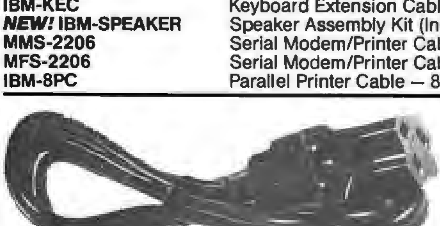


Monitor Adapter Power Cable

Enables user to plug any monitor into your IBM Power Supply
(IBM-PS — See above)

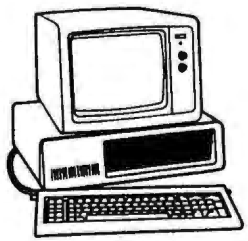
MCable........................ $9.95

Inquiry 147

JADE XPC or XPC-AT

- 640K of RAM
- 4.77 MHz 8088
- 7 MHz turbo mode
- 135 watt power supply
- 360K disk drive
- Floppy disk controller
- 5151-style keyboard
- 8 expansion slots
- PC-style case
- 90 day warranty

$588



- 1 MB of RAM
- 6 MHz 80286
- 8 MHz turbo mode
- 200 watt power supply
- 1.2 MB disk drive
- Floppy/hard disk controller
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- 8 expansion slots
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$1288

OPTION #1
Two disk drives
Mono graphics card
Parallel printer port
Amdek 310A monitor

XPC $898 XPC-AT $1698

OPTION #2
20 MB hard disk
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Parallel printer port
PGS MAX-12E monitor

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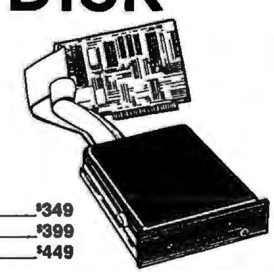
OPTION #3
20 MB hard disk
Color graphics card
Parallel printer port
Hitachi hi-res color monitor

XPC $1388 XPC-AT $1998

HARD DISK DRIVE

$349



10 MB Kit	$349
20 MB Kit	$399
20 MB hard disk card	$449

20 MB HI-SPEED HARD DISK FOR YOUR AT

$399

Limited quantity.

30 MB Hi-speed	$695
40 MB Hi-speed	$895
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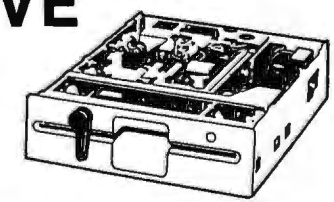
QUME DISK DRIVE

- Double sided
- Double density
- 360K for PC

$69



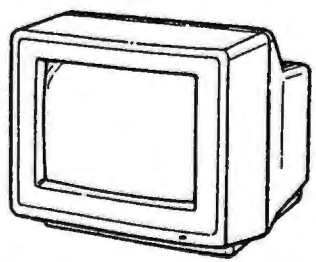
Teac FD55 BV	$109
Tandon TM100-2	$109
1.2 MB for AT	$149

HIGH RESOLUTION COLOR MONITOR

$269

List Price $699

Free PC RGB cable included



- IBM PC color graphics compatible
- High resolution 640 x 240
- Excellent dot pitch .38 mm
- 16 true colors, 2000 characters
- Accepts standard RGB input signals
- Non-glare picture tube
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MICROSPEED FAST 88
7 MHz TURBO CARD FOR YOUR PC

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- Uses no slots
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- No wait states
- External switch
- Reset switch

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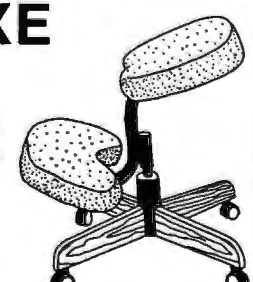

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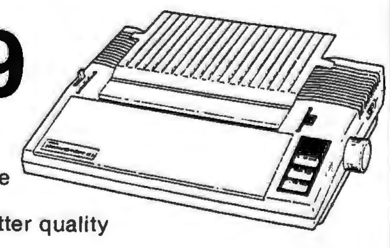

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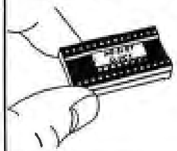

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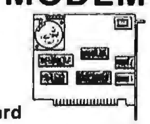

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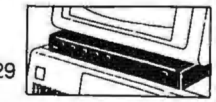

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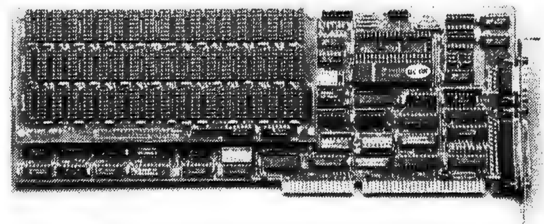

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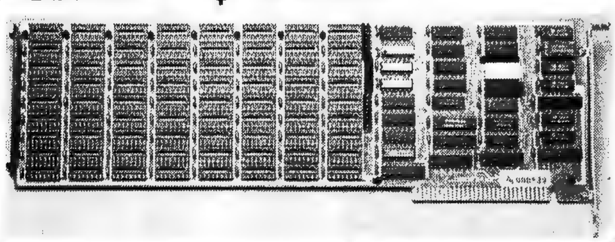

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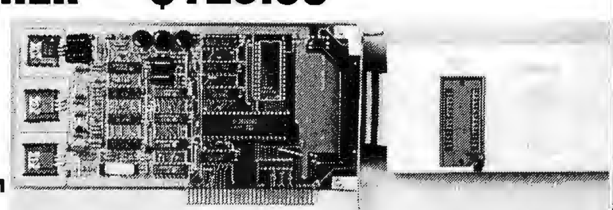

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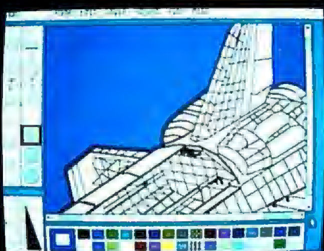
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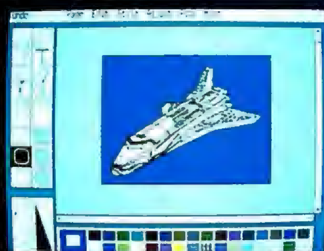
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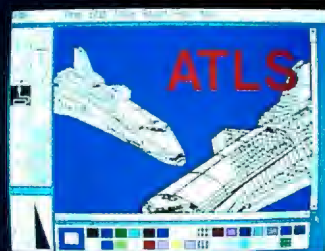

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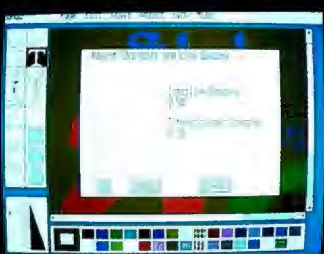
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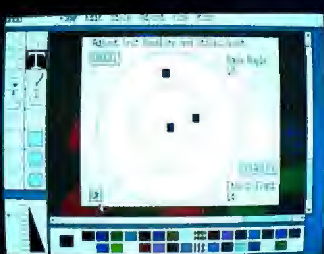
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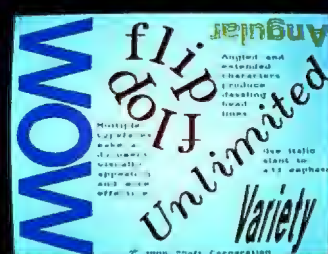

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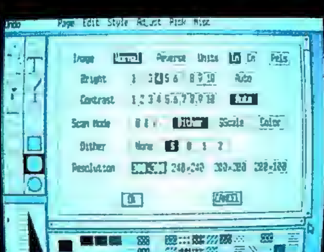
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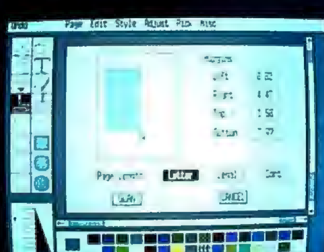
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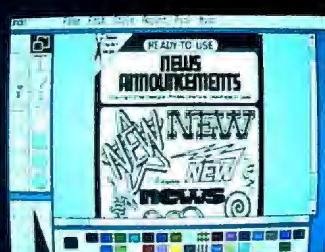

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