BYTE

THE SMALL SYSTEMS JOURNAL®

JANUARY 1987 VOL. 12, NO. 1

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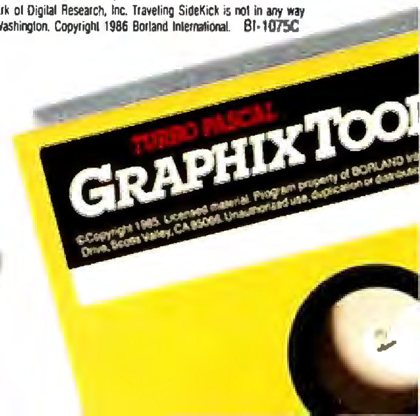

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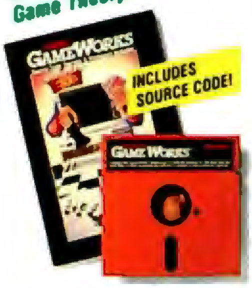

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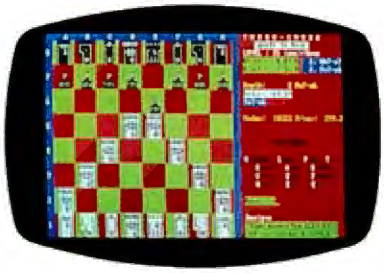

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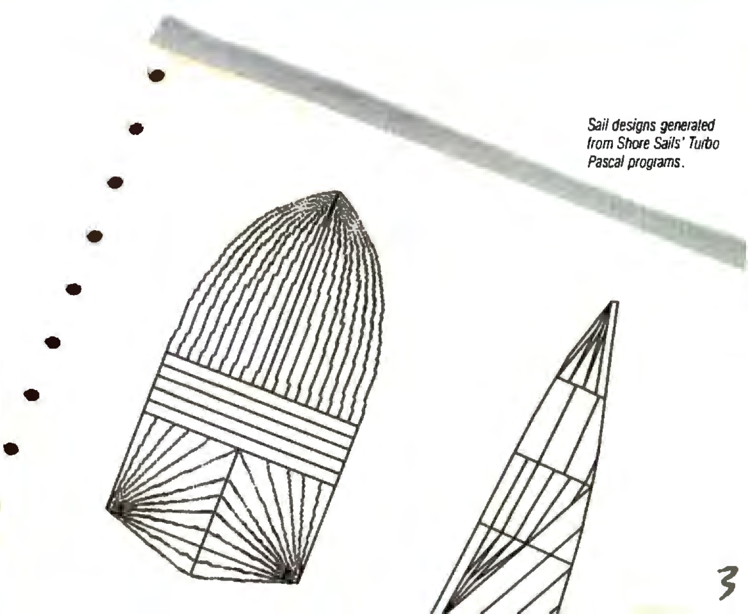

Sail designs generated from Shore Sails' Turbo Pascal programs.

OFFICIAL RULES - BORLAND INSTANT WINNER GAME

1. NO PURCHASE NECESSARY: To participate, you may obtain a game card inserted into the October, November, December, or January issue of the following magazines: PC World; Byte; PC Tech Journal; PC Magazine. You may also obtain a game card by mailing a self-addressed, stamped envelope to: Borland International Game Card, P.O. Box 870, Wilton, CT 06897. (Washington State residents send self-addressed envelope.) Limit one game card per stamped request. All requests must be received by January 15, 1987.

2. TO PLAY: Remove the rub-off area on the game card to reveal what prize or rebate offer you have obtained.

3. PRIZES/ REBATES: Beneath the rub-off area one of the following prizes may be revealed: Trip for Two to America's Cup Races or $10,000; 1986 Suzuki 4W Samurai Convertible or $6,895; AST Turbo Laser; Toshiba 1100 Portable Computer; Toshiba 3100 Portable Computer; AST Sixpakpremium; AST Advantagepremium; AST3G Pak; AST Rampage; AST Rampage AT; Free Borland Product, or you may obtain the following rebate offer: $10 rebate offer on any individual product or $15 rebate offer on any single advertised Borland bundle (See rule #11 for prize details).

4. PRIZE CLAIMS: If you obtain one of the prizes stated in Rule #3, sign your full legal signature on the game card and send via certified mail (copy should be made for your records) along with your name and address to: Borland International Prize Claim, 196 Danbury Road, Wilton, CT 06897. All prize claims must be received or postmarked by February 15, 1987. (See Rule #12 for Trip for Two to America's Cup exception.)

5. REBATE CLAIMS: Rebates are good for products purchased from September 5, 1986 through March 31, 1987. The $10 rebate is good for any individual Borland product and the $15 rebate is good for any advertised Borland software bundle. To receive your rebate you must return your completed license agreement from the manual, this game card and dated proof of purchase to: Borland International, Game Card Rebate, 4585 Scotts Valley Drive, Scotts Valley, CA 95066. Upon receipt of the license agreement, game card and proof of purchase, Borland will send your check. Rebate is not valid with any other rebate or promotion offered directly from Borland.

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8. ELIGIBILITY: Participation is open solely to residents of the United States 18 years of age and over, except employees and agents of Borland International, service agencies, and individuals engaged in the development, production, or distribution of game materials, The Merritt Group, Inc. and their immediate family or members of their households. Void in Vermont and where prohibited by law.

9. GAME SCHEDULE AND AWARD OF PRIZES: The Borland Instant Winner Game will commence on or about September 5, 1986 and end on January 30, 1987. It will officially end, however, when all game pieces are distributed. Verified game prizes will be awarded within thirty (30) days from the date of their receipt for verification at the Official Redemption Center. A major prize winners' list can be obtained by sending a stamped, self-addressed envelope to: Borland Instant Winner Game Winners' List, P.O. Box 7089, Wilton, CT 06897.

10. ODDS CHART: The odds of winning prizes are based upon obtaining the one rare game piece among the applicable number of game pieces.

PRIZE	Qty.	Total Value	Odds of Winning
Trip for Two to America's Cup or $10,000	1	$ 10,000.00	1 in 6,458,000
Suzuki 4W Samurai Convertible JA or $6,895	2	$ 13,790.00	1 in 3,229,000
AST Turbo Laser	1	$ 4,995.00	1 in 6,458,000
Toshiba Portable Computer	2	$ 6,898.00	1 in 3,229,000
AST Memory Boards	25	$ 15,025.00	1 in 258,320
Borland Products	1,000	$149,000.00	1 in 6,458
OVERALL TOTAL	**1,031**	**$199,708.00**	**1 in 6,264**

All remaining game cards will contain a $10 rebate good on any individual Borland product or a $15 rebate good toward any advertised Borland software bundle.

11. PRIZE DETAILS: Trip for two to America's Cup Races (or $10,000) will include coach seating round trip airfare on regularly scheduled commercial airline from San Francisco, California to Perth, Australia and up to two weeks hotel accommodations in Perth, Australia plus $4,500 spending cash. Winners will be responsible for obtaining visa, passport, and all other travel documents. Trip does not include meals, taxes, excess baggage charges and other hotel charges. Minor must be accompanied by parent or legal guardian.

Suzuki 4W Samurai Convertible JA Standard Equipment Package (or $6,895), verified winner will be responsible for all registration, insurance, and licensing fees. AST Turbo Laser; Toshiba Portable Computer Model #T1100; Toshiba Portable Computer Model #T3100; AST Memory Boards and Free Borland Products are non-substitutional except by sponsor due to product availability and all warranties and guarantees are subject to manufacturers terms. All prizes are non-transferrable. Winning consumer is responsible for all local, state and federal taxes.

12. SECOND CHANCE SWEEPSTAKES: There are two Second Chance Sweepstakes drawings scheduled to be conducted on December 31, 1986 and February 28, 1987. Random drawing from all entries received by December 30, 1986 will award trip for two to America's Cup Races (or $10,000). Random drawing from all entries received by February 26, 1987 will award two (2) Suzuki 4W Samurai (or $6,895). All remaining prizes that are unclaimed after February 15, 1987 will remain unclaimed. Send entry to: Second Chance Entry P.O. Box 870 Wilton, CT 06897.

If you have any questions concerning the Borland Instant Winner Game, call: 1-800-451-4471.

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Build Your Own Database Applications!

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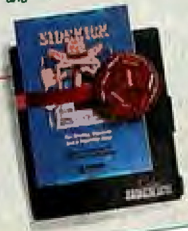

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Inquiry 427 →

EDITORIAL

Two Brief Conversations with Ben Rosen

With the arrival of the 68020 and the 80386, we've heard a lot of people saying most users don't need the power of a 32-bit processor. We've heard this sort of thing before. Back in the mid 1970s, some technically astute people said things like, "I wouldn't know what to do with 16K bytes if I had it," and "You ought to be able to do anything in 8K bytes." Programs like VisiCalc and WordStar made everyone realize that 64K bytes of RAM has its uses.

When 16-bit processors arrived in the early 1980s, more than a few experts said, "A Z80 and 64K bytes can do anything anybody needs." But Lotus 1-2-3, Framework, Javelin, Reflex, Paradox, Q&A, and dozens of other products have shown that an 8088 and 640K bytes can do things an 8-bit processor can't.

Since the introduction of the Macintosh, and especially since the Macintosh Plus gave that 68000-based system adequate memory and mass storage for its graphics environment, software developers have given us glimpses of what 16-bit processors with a large linear address space can do. Can you imagine products like Excel, STELLA, Balance of Power, PageMaker, and More running on a Z80 with 64K bytes?

But how can we be sure that the move from 16 bits to 32 will be as important as the move from 8 bits to 16? As it turns out, Ben Rosen is an interesting gauge of this.

Ben is not easily impressed. His venture capital firm, Sevin-Rosen Management, has been involved in some of the most successful start-up companies in personal computing, including Lotus, Compaq, and Ansa. He has seen a million proposals from start-up companies.

At the Personal Computer Forum in Phoenix in early 1986, I ran into Ben during a coffee break. He was outside on the patio, thinking aloud about the talk he was to give the next day. Many people from the software community were questioning whether there was room in the market for any new software products, no matter how good. I asked Ben what he would do if Mitch Kapor walked into Sevin-Rosen seeking funding then, in early 1986, rather than years earlier. "That's an interesting question," Ben said with a smile. He seemed intrigued with the prospect of a product like 1-2-3 being turned down. This was a depressing commentary on the opportunities in software in the heyday of the IBM PC AT.

I bumped into Ben Rosen again last November at COMDEX in Las Vegas. We were in the Quarterdeck booth watching software run under Quarterdeck's DESQview environment on a Compaq 386. The machine was simultaneously running a desktop publishing program under GEM, a CAD program under Windows, and another application written for TopView.

Ben said, "We're beginning to see proposals for new application software products for the 80386. There are going to be some very nice things written for that chip."

"AI?" I asked.

"That, and other things," he said. He refused to be drawn out further.

With the 32-bit processors, as with the 16-bit processors before them, we will all find we need them as soon as software developers have had time to exploit the new chips. How will developers break new ground? There are many possibilities: in the graphical user interface, in natural language, in communications, and so on.

But developers *will* break important new ground. When a seasoned venture capitalist like Ben Rosen finds proposals interesting again and attributes this to the 80386, we can all be sure that the 32-bit processors will make possible some improvements in software much more dramatic than the great increases in speed that have already been observed. You better begin to budget now for a machine that will run the software that's coming.

—Phil Lemmons
Editor in Chief

Free BIX Accounts for Apple IIGS Event

When Apple announced the Apple IIGS on September 15, 1986, BIX was ready with the full text of our technical preview (which also appeared in the October 1986 BYTE). By the end of that week, we had added Apple's price list, additional information, and ongoing commentary by the IIGS engineers and three average BIX users who had final prototype IIGSs! The weeks that followed were very exciting because of the quality and quantity of information that passed among all these BIX users.

Unfortunately, Apple had problems shipping the new computer and its associated software, and interest in the BIX topics waned because nobody had one. We offered month-long free access to BIX to the first 10 Apple IIGS owners who called, but nobody did.

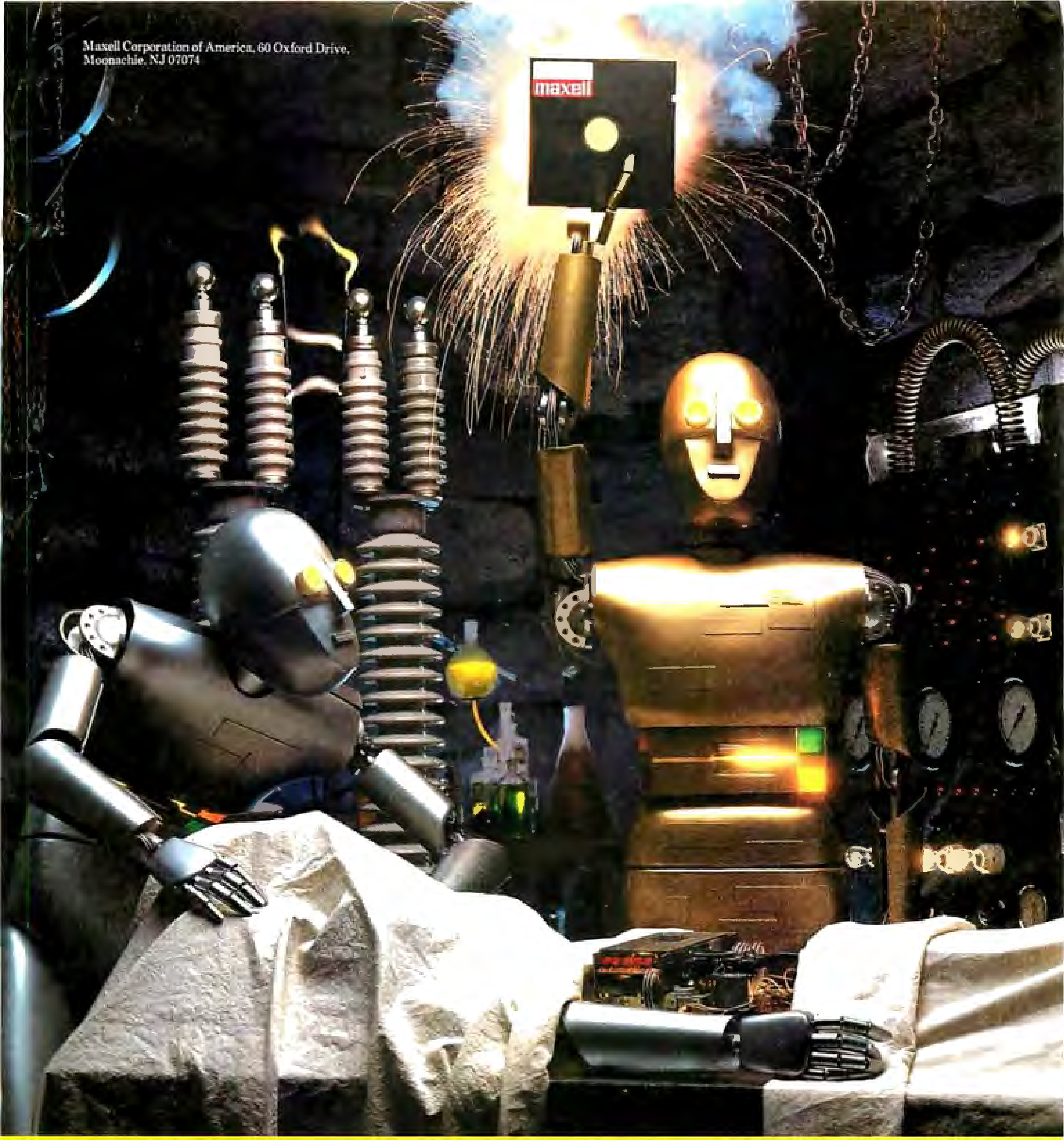
Apple should be shipping lots of the IIGS by the time you read this, so we're making our offer again. If you have just bought an Apple IIGS, are not a commercial IIGS product developer, and are interested in participating in the Apple IIGS special event, please call Curt Franklin at BYTE at (603) 924-9281. The first 10 people who call will get free BIX access for a month. We look forward to continuing the extremely rich dialogue among BIX users about this new computer.

The beginning of 1987 will see several new conferences and special events on BIX. Among those currently scheduled for a January debut is a new conference concentrating on application software written to take advantage of the new 80386-based microcomputers. The conference, apps386, will allow users and developers to discuss new possibilities and problems of software for the 80386.

A special event coming up in the CAD conference will look at how microcomputer-based CAD is shaping up, in terms of functionality and ease of use, against freestanding CAD systems.

The conference on computers and the handicapped will host a special event on the current state of adaptive hardware and software.

With the Department of Defense allotting an ever-larger budget for programs in Ada, a BIX event in the Ada conference will examine the compilers currently available for microcomputers and the implications of greater Ada usage for the microcomputer programming community.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MICROBYTES

Staff-written highlights of developments in technology and the microcomputer industry.

Microlithography Process Packs Memory Circuits with 1 Million Transistors

A microlithography process developed at the IBM Almaden Research Center (San Jose, CA) has enabled researchers to build memory circuits with more than a million transistors packed into an area the size of the top of a pencil eraser. Circuit lines in these chips are typically 1 micrometer wide, or about 1/100th the width of a human hair. Equivalent circuit lines on standard 256K memory circuits average about 3 micrometers wide.

What makes this much miniaturization possible is a new photosensitive polymer consisting of diazonaphthoquinone molecules dissolved in phenolic resins. While traditional polymers are sensitive to ultraviolet lights that have wavelengths of 400 to 450 nanometers, the new polymer is photosensitive to wavelengths of 300 to 350 nanometers. The shorter wavelengths enable engineers to more tightly focus the image and create the smaller circuit lines.

A typical fabrication process begins with a wafer of silicon substrate material coated with a thin-metal, oxide-based film. The photosensitive polymer (called a "resist") is applied to the thin film, then overlayed with a pattern (or "mask") representing the circuit lines. Next, the wafer is exposed to ultraviolet light. During the subsequent photodeveloping, the exposed resist is dissolved, leaving polymer lines on top of the thin film that represent the circuit lines. The wafer is then etched to remove portions of the thin film not protected by the resist. The result is a "double layer" of metal and polymer that represents the circuit lines. Finally, the polymer resist is stripped away, leaving only the metal circuit lines on the silicon substrate.

The first computers to implement the 1-million-transistor circuits will be IBM's 3090 series.

Hardware Builders Showing Preference for TI's Graphics Chip Over Intel's

After a wait-and-see period, several hardware developers are announcing graphics products based on Texas Instrument's 32-bit TMS34010 graphics microprocessor rather than on Intel's 82786 graphics coprocessor. Although neither chip manufacturer would supply a list of third-party products based upon their respective processors, a survey of developers indicated a preference for the TI chip.

Part of the TMS34010's attraction was summed up by one representative of a display manufacturer, who said that "while the TI processor is somewhat more expensive, it is very versatile and more programmable." According to Joe Meshi of Conographic Corp. (Irvine, CA), "The TI chip is vastly more powerful than the Intel one." Conographic's TMS34010-based product, the ConoVision 2800, supports resolution of up to 2880 by 1024 pixels.

The programmability of the TMS34010 allows developers to design "soft" RAM-based cards that can be configured by downloading a command set to the board so that the software sees a "different" board in different situations.

Video-7 (Milpitas, CA), another developer of graphics enhancers, also evaluated both processors and selected the TI chip. One issue Video-7 took into account was applications software that will be developed for the new 32-bit microcomputers. "The TI chip is more difficult from a hardware point of view," said Video-7's Greg Reznick, "but it is easier for software developers." Video-7 plans on shipping the Host Graphics Interface, its first product based on the TMS340 family, early this year.

One firm using Intel's chip, Quadram (Norcross, GA), claimed its new graphics board would be the first of its kind to use the 82786. The

continued

Nanobytes

Phoenix Technologies (Norwood, MA) is developing its 80386-based VP/ix virtual PC environment for Microsoft's UNIX-based XENIX System V/386. Phoenix said its VP/ix will enable IBM PC–compatible applications to run on 386 machines, without change, as tasks under XENIX. Because VP/ix emulates a PC hardware environment, any program that runs on a PC should be able to run under VP/ix, Phoenix said. . . . **Cylink** (Sunnyvale, CA) has brought out a 40-pin CMOS chip that can implement public-key encryption algorithms, including RSA and SEEK. Cylink says the CY1024 Key Management Processor interfaces easily to any microprocessor. The company claims the chip can perform 1000-bit modular exponentiation in less than 1 second. A single chip handles integers as long as 1028 bits; 16 chips can be cascaded to accommodate integers as long as 16,384 bits. . . . Looking for a **secure job** that starts at an average of $36,000 and could pay three times more than that? According to a study by Cornell University, all you have to do is get a doctorate in computer science and engineering. The study says U.S. schools can't produce the Ph.D.s fast enough to fill demand at universities and in industry. . . . **Sperry** (Blue Bell, PA), a.k.a. **Unisys**, is going to include Intel's 80287 numeric coprocessor as standard in its PC/IT. For the past year, the math chip has been available for the IT as a $375 option. . . . **OmniTel** (Fremont, CA) said it will soon start shipping its PC board that contains four 1200- or 2400-bps Hayes-compatible modems. The NetComm Quad 1200 ($1249) and Quad 2400

($1799) go in IBM PC XTs, ATs, or compatibles connected on a LAN. OmniTel said the boards eliminate the expense of having to put a modem in every station in a local network.... **Heath Co.** (Benton Harbor, MI) donated the original Heathkit H-8 computer to the Smithsonian Institute.... A small quarterly newsletter called the **PostScript Language Journal** sells for $15 a year. Contact Pipeline Associates, 39 East 12th St., New York, NY 10003.... Speaking to the Boston Computer Society, former apostle of psychedelic drugs **Timothy Leary** talked about the potential to put "performance books" on-screen that let you play "as if" with thoughts just as spreadsheets let you play "what if" with numbers. He now heads his own software firm called Futique Inc. (Los Angeles). "Life," Leary said, "is a menu-driven universe."

board, code-named HPG, features a resolution similar to that of the IBM PGC—up to 640 by 480 pixels with as many as 256 colors out of a palette of 16 million possible colors. But unlike the PGC, it will work with four different monitors: CGA, EGA, and MultiSync-type monitors, and the IBM Professional Graphics Display.

The firmware will allow programmers to access graphics capabilities in four ways: via routines in Quadram's own QBIOS, GSS's DGIS, Digital Research's GEM, or Microsoft's Windows.

A prototype was scheduled to be shown at COMDEX; production units should be available in February. Name and price hadn't been set at press time, but a spokesperson said the price would be just slightly more than that of a standard EGA board.

Some Makers of Laser Printers Switching to NS32000

Several laser printer manufacturers are quietly turning away from Motorola's 68000 microprocessor and replacing it in their products with members of National Semiconductor's 32000 family of chips, particularly the 32016 and 32032. According to engineers who have compared the chips for laser printer applications, the NS32000 is more attractive because it has a 32-bit ALU for math and graphics processing, more powerful bit-manipulation capabilities, 35 percent smaller object code requirements, 32-bit floating-point arithmetic for halftones and shading, memory-to-memory address ing of large arrays of data, and lower-cost memory devices.

While National Semiconductor representatives would not reveal which companies are adopting the 32000 chip, they did say that several companies were to announce changes by the end of 1986. Dataproducts led the way several months ago with its LZR 2630 laser printer; however, other Dataproducts printers continue to use the 68000 chip.

The processor change should be transparent to users, but software houses may have to convert assembly language portions of their products.

Electronic Cameras Store Photos on Floppies; Computer Interfaces in the Picture

Electronic "still-video" cameras that take pictures and put them on a floppy disk look from the outside like regular 35mm single-lens reflex models. (Canon, Nikon, Fuji, Minolta, Konica, Panasonic, and Polaroid showed samples at the Photokina trade show in Cologne, Germany.) But inside is a CCD image chip with moderate sensitivity to light. The cameras record still-video images in analog mode on a 47mm floppy disk, using a 51-track format that major camera and electronics companies have agreed upon as a standard. The disk can store 50 pictures at video field resolution or 25 at frame resolution (twice as many scan lines); track 51 is a data track.

Disks can be erased for new shots. Photojournalists can put the disk into a modem-type transmitter and send pictures to a newspaper almost immediately. (The reliability of the miniature 3600-rpm disk drive in the cameras will be a major factor in their success or failure.) Pictures are viewed by putting the disk in a playback unit that connects to a television. (No cameras shown thus far provide playback viewing.) Since the playback unit outputs a standard video signal, images can be captured with frame-grabber boards and used in graphics programs. Sanyo and Sharp are working on still-video computer interfaces, but no details were yet available.

For computer graphics, the main advantage of still-video cameras may be their ability to stop action for sharper images, thanks to shutter speeds of up to 1/1000th of a second and electronic flash synchronization.

Aldus, Microsoft, and Scanner Makers Adopt TIFF

In an attempt to standardize the use of scanned images in desktop publishing, Aldus Corp. (Seattle) and Microsoft Corp. (Redmond, WA), along with scanner manufacturers DEST Corp. (Milpitas, CA) and Datacopy Corp. (Mountain View, CA), have said they'll support the Tag Image File Format (TIFF) standard. According to a memorandum prepared jointly by Aldus and Microsoft, the purpose of TIFF is to "promote the interchange of digital image data" by organizing and codifying the definition and usage of digital data. The hope is that software developers creating scanning or painting programs will have the programs generate TIFF files that can later be incorporated into desktop publishing documents.

A TIFF file has three parts: a header, a field directory, and the data. Within the file, each field is identified by a unique tag that tells what the field means. Fields are used to define data architecture, photometrics (to determine the visual meaning of the data), resolution, document context, string handling, and storage management. Most images can then be described by a few fields. A typical binary image from a scanner or paint program, for example, might be defined by file type, image width, image length, and photometric interpretation.

continued

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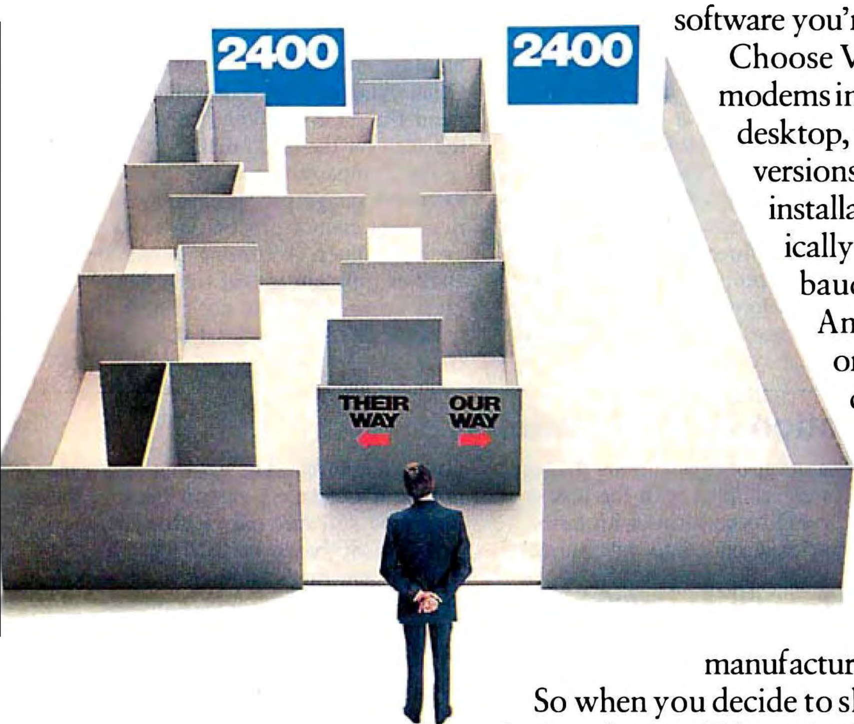

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Error-Correction Technology Allows 2.5 Gigabytes on Videocassette

While several companies are offering tape drives that can store up to 120 megabytes of data, Digi-Data Corp. (Jessup, MD) says it has perfected a technique to store 2.5 gigabytes on a standard T-120 videocassette. The company's Gigastore is a modified Panasonic VCR with one recording head used for writing to the tape, while another head checks the error-correction code of the data that has just been written. The company claims its technique offers an error rate of less than 1 bit in 10^{23}.

The tape drive will be designed to run in streaming mode at a rate of 7.2 megabytes per minute. It can be connected to a PC with a Pertec-style nine-track controller card. The Gigastore will be available early this year for $4780.

Micros Used to Color Black-and-White Classics

Although people might argue about adding color to old black-and-white movies, most will admit that the technology used is impressive. What's even more impressive is that much of the work, involving gigabytes of data, is done by microcomputers. And it's ironic that some of the colorization is done by a black-and-white computer—Apple's Macintosh.

Color Systems Technology (Marina del Rey, CA) has colorized such classics as *Miracle on 34th Street* and *Yankee Doodle Dandy.* Its process first transfers the black-and-white film to 1-inch videotape, then adds color with a Sony videotape recorder. A custom-built host computer, based on Intel's 80186 microprocessor, feeds signals to the recorder. Four Macintoshes are connected to the host and used as drawing stations. A fifth Mac serves as an intelligent console.

Colorization Inc. (Toronto) has added color to *Topper* and *Night of the Living Dead.* Colorization uses a dedicated videographics processor called the Dubner CBG-II, widely used to generate graphics during television sports coverage. The Dubner uses an 8-bit 8080 processor, along with a 2901 bit-slice processor, and stores information on Iomega 10-megabyte disks. Colorization has approximately 4500 10-megabyte disks of data.

According to Wilson Markle, president of Colorization, the company has begun to use IBM PC ATs for some of the work. The AT, equipped with a Matrox NTSC video board, is used for painting and some "in-between" work. Other ATs, running Lotus Development Corp.'s Symphony, keep track of the data on the 4500 disks.

The company would like to use ATs for more image processing, but the machines cannot process video as fast as the Dubner. According to Markle, another problem is that most PC graphics products are not compatible with the NTSC broadcast standard.

Allen at Work on 'New Generation of Applications'

Paul Allen, who along with Bill Gates founded Microsoft Corp., has formed a new software company that's developing applications software for 80286- and 80386-based PCs. Allen told Microbytes Daily that his firm, Asymetrix (Bellevue, WA), is designing software to take advantage of future versions of DOS and Microsoft Windows.

Allen was short on specifics but did describe the development project as "a new generation of applications that are more closely coupled with the task a user is trying to perform, with business knowledge built into the application."

"It will overlap some existing categories," Allen continued, "but the way it delivers will be in a totally different way, like comparing C to assembler. The user will deal with problems at the conceptual level he likes to deal with; it's a very high level approach to problem solving. The environment I'm talking about hasn't existed because the operating software hasn't been there."

An 80286-based or IBM PC AT-style system that's running in protected mode will be a minimum hardware configuration for using the Asymetrix product, which is not expected to be published until sometime this year at the earliest. The software will perform better on 80386-based systems, Allen noted.

Intel's 32-bit Bus Seen on 80386 Computers

In the quest for a bus that makes the best use of the capabilities of the 80386, several companies—including PC's Limited (Austin, TX) and ALR (Irvine, CA)—have turned to a bus based on one developed for internal use by Intel (Santa Clara, CA). When contacted about the bus and its specifications, Intel managers admitted they had supplied the bus, along with the Intel motherboard, to a number of vendors. They said it was developed out of necessity for internal development at Intel. One manager drew parallels between the making of the 32-bit bus and the initial Multibus. Both were developed to meet internal needs and were later released to other companies only when customers ran into difficulty coming up with their own bus in time to meet delivery schedules.

Intel spokespersons refused to release any technical details or specifications on the bus.

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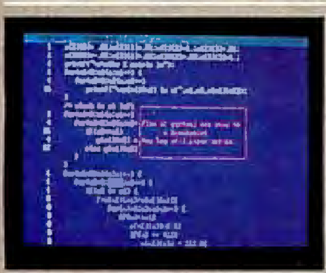
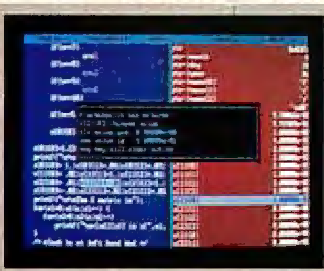
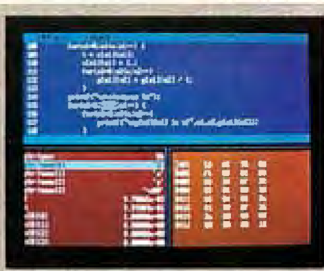


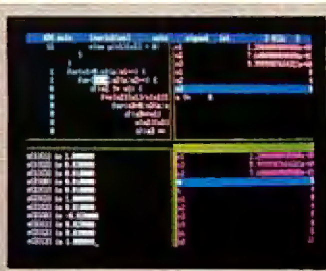
Source window with profile count showing number of times each statement has executed. Pop up message indicates break point has been hit



Source and variables windows shown side by side. Pop up message indicates that a watch point condition has been satisfied.



Source, variables, and memory window. Memory window lets you view any area of memory using any data type.



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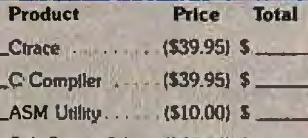

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The Ideal Programming Language

This letter is in agreement with the one from Ronald J. Perrella in October 1986 ("Combining Languages," page 22).

Perrella is absolutely right when he says that the programming discipline has essentially remained static. We are still using antiquated tools in our high-technology activities. This inefficiency is being proliferated by the "traditional" methods of teaching computer science. As an appalling example, in one of my programming courses we were not allowed (*allowed*, mind you) to use a calculator on a test. While I do not propose that we become dependent upon calculators and forget how to do long division, to deny programmers the use of this tool is almost criminal. Do we deny carpenters the use of power drills lest they forget how to use the brace and bit?

Perrella states that the goal of the programmer is not to use a specific language but to produce a program, one that, I would add, is as efficient as possible. There is too much emphasis on programming and not enough on producing a program. Loyalty to a single language produces headaches, but an open mind produces solutions.

I agree wholeheartedly that what programmers need is a good programming *environment*, not another PL/I. I have begun to think about such an environment and in my mind I call it IDEAL. Since no language can be a top performer in every category, the languages in IDEAL would each excel at certain functions and be easily linkable. Each would compile to an object code conforming exactly to some standard. Object modules could then be linked freely to form independently executable programs.

But this is minor. Several languages can already be linked in exactly this way. The major function of the IDEAL system would be to simplify the processes of coding, debugging, and documenting programs. An auto-coding utility might allow the programmer to develop a program as a flowchart-like structure and would then fill in the code when a suitable level of detail is reached. This code need not be in any particular language; it could be generated directly as object code, making the module available to all of the languages on the system. A screen generator working with the auto-coder would produce input and output screen formats and code. These I/O modules could also be accessed by any language on the system.

The second part of IDEAL would be the debugger. This should give the programmer the ability to control the execution of any independent program *or* object module. The programmer should be able to begin and halt execution at will by single-stepping, setting breakpoints, or perhaps simply by a keystroke. During halts all registers, symbol tables, and stacks should be easily viewable and changeable. Two additional helpful features would be the ability to view and alter any memory locations and a trace of program execution.

The proper role of documentation has always been unclear. Contrary to the thinking of some, there is a definite limit to the value of internal documentation (i.e., comments). The proper choice of identifiers makes many languages almost self-documenting as far as the actual coding goes. Programs written with the IDEAL coder would, by the very nature of the process, be self-documenting. The argument for internal documentation is that it facilitates future revisions. If a change is so great that a little study of the code does not provide an answer, let the program or module be rewritten. Patching old code like a worn-out tire makes for dinosaurs; let the program be reborn as a sleek, modern animal, taking advantage of new insights and new technology.

More effort should be put into user documentation. There are only a few good user's manuals in comparison to the total number. On-disk tutorials and demonstrations are an effective supplement to printed documentation. The IDEAL system could include the capability to create such helps by taking snapshots of programs or recording keystrokes. A user documentation development tool could use a template to help programmers be comprehensive and consistent.

I would seriously like to develop the IDEAL system, but it may be too big a project for a poor calculator-deprived programmer with only a pencil.

J. David Reynolds Jr.
Makanda, IL

Easy C Naysayer

Sincere appreciation for printing the letter by John A. Rupley (September 1986, "Easy C: Is the Easy Way the Best Way?" page 22). If C is to retain its efficiency and portability, then it must have a standard that is comprehensive to all C programmers. The current X3J11 ANSI committee is still establishing that standard; it is following recommendations from many vendors of C compilers. There is always room in a program for embellishments or "my way," but let's have a common foundation known to all and let that foundation be the starting point for the new and upcoming C programmers.

Charles W. Atran
Fife, WA

Proving the Properties of 2^n

Robert C. Arp Jr.'s Programming Insight "A Useful Property of 2^n" (October 1986) has inspired me to observe, in another example of lateral thinking, an amazing property of the decimal system we use every day. Looking at several examples of integers of various magnitudes, I figured out that simply by inspection I was able to determine the number of hundreds, tens, or units in the integer. I haven't tried this with larger numbers yet, but I'll bet this technique will generalize to thousands and even millions and billions!

Is this the same magazine that published C. A. R. Hoare's excellent article on the mathematics of programming?

Carla Marceau
Ithaca, NY

In his interesting and valuable article, Robert C. Arp Jr. has chosen to rest his case on empirical verification "within the limits of [his] calculator" and not to offer proof.

In the world of engineering problems, this is quite sensible and legitimate. Nevertheless, some BYTE readers may be interested in the following simple proof.

continued

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Because BYTE receives hundreds of letters each month, not all of them can be published. Letters will not be returned to authors. Generally, it takes four months from the time BYTE receives a letter until it is published.

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If a sum of different integer powers of 2 is divided by an integer power of 2, Arp's proposition says that the integer part of the quotient will be odd if the divisor is also one of the addends, and it will be even if it is not. Or, in Arp's symbols, if $Y = \Sigma 2^i/2^n$, then $[Y] \bmod 2 = 1$ if n is one of the i's, and 0 otherwise (the square brackets mean "integer part of" the enclosed expression).

Expanding the sum,

$$\Sigma 2^i = 2^{i_1} + 2^{i_2} + \ldots + 2^{i_k},$$

the quotient becomes

$$Y = 2^{i_1 - n} + 2^{i_2 - n} + \ldots + 2^{i_k - n},$$

where the terms are of three types only:

type 1: a fraction less than 1—namely, if $i < n$;
type 2: a power of 2 greater than 1—namely if $i > n$;
type 3: exactly 1—namely, if $i = n$.

Terms of type 1 can never influence the integer part of Y because even the sum of the *infinite* geometric series $½ + ½^2 + ½^3 + \ldots$ has 1 as its upper limit.

Terms of type 2 are even integers. Their sum is also even.

Type 3 can occur only once (or not at all) since all the i's are supposed to be different and at most only one of them can equal n.

Thus, since adding 1 to an even number results in an odd number, $[Y]$ is odd only if 2^n is one of the addends. For example (and without loss of generality),

$$\text{if } i_1 = n, \text{ then } Y = 1 + \sum_{p=2}^{k} 2^{i_p}/2^n.$$

This proves Arp's proposition and the limits of his calculator may be exceeded safely when using his algorithms.

Dr. Rudi Borth
Don Mills, Ontario, Canada

[Editor's note: *A number of other readers submitted proofs similar to Professor Borth's. The following letter was unusual in its use of assembly language to prove the theorem.*]

Robert C. Arp Jr.'s use of a number to store flags is common to assembly language programmers. Any ordered group of flags can be taken as a number. The proof of Arp's theorem,

$$[\text{INT}(\frac{\Sigma 2^i}{2^n})] \text{ MOD } 2 = \begin{cases} 1 & \text{when } 2^n \text{ is an addend of } \Sigma 2^i, \\ 0 & \text{otherwise} \end{cases}$$

continued

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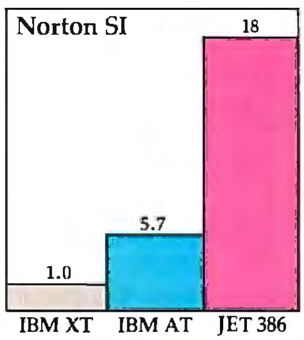

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LETTERS

is evident in the following segment of 6502 code from a program of mine, which determines if 1 of 24 flags is set.

On entry, the flags are temporarily stored low to high in FLAG through FLAG+2 and the flag number desired is in the X register. On exit, the carry bit C (rotated off bit 0 of FLAG) is the desired flag.

```
; 0->bit7->bit6->...bit0->C
ROTATE  LSR  FLAG+2
; C->bit7->bit6->...bit0->C
        ROR  FLAG+1
; C->bit7->bit6->...bit0->C
        ROR  FLAG
        DEX       ; X=X-1
; Go to ROTATE if X>=0
        BPL  ROTATE
```

Since division by 2^n is the same as rotating right n times, this divides the number in FLAG through FLAG+2 by 2^{n+1}, where bit 0 is flag 0 with $n = 0$. Arp's method would divide by 2^n and leave the flag in question in bit 0 of FLAG. Thus, the result would be odd if and only if the flag bit was set.

This can be extended to any base. Arp's conclusion can be generalized

$$[\mathrm{INT}(\frac{\Sigma b^i}{b^n})] \mathrm{MOD}\ b = \begin{cases} 1 \text{ when } b^n \text{ is an addend of } \Sigma b^i, \\ 0 \text{ otherwise.} \end{cases}$$

(The result of the modulo b operation will always be 0 or 1 because when any Σb^i is represented in base b, it will look like a binary string.) Arp's method looks new because he manipulates binary flags from decimal representations.

Phil Goetz
Ellicott City, MD

MC68000 Microprocessor and Descendants

I appreciate the broad analysis in "A Comparison of MC68000 Family Processors" by Thomas L. Johnson (September 1986), but the statement in his conclusion that "... for user code, all family members are 100 percent upwardly compatible for object code..." is not entirely correct. The "move from status register" available on the 68000/68008 to read the condition code register will cause a privileged instruction violation on the 68010/68020. The alternative instruction on the latter processors is a new "move from condition code register" instruction. To write user-state code that reads the condition code registers in a upwardly and downwardly compatible manner is unwieldy to say the least. Motorola engineers should be aware of the fact that the family is only 99.98 percent upwardly compatible.

Kim Kempf
Ankeny, IA

Objections to C

Although I certainly appreciated the overall value of his article "Atari ST Software Development" (September 1986), I was disturbed that Michael Rothman included a routine written in C that (to be nice) was garbage. Not only will the code not produce the desired result—formatting a single-sided floppy disk—it is also written in the wrong language. I realize that these are strong allegations, but I believe the following will sufficiently document my position.

If you actually typed in and executed Mr. Rothman's code and then chose "Show Info..." from the File menu, you would discover a disk that had zero bytes used and zero bytes free!

This confusing and anomalous situation is the result of initializing all the tracks on side 0 with the value of $E5E5. Tracks 0 and 1, which, in addition to the boot sector (track 0, sector 1), contain directory information, *must* be initialized to $0000. In short, even though the disk is devoid of directory entries, it is, in essence, full. (GEMDOS is dumb.)

One further note. The situation above applies only to side 0. On side 1 of a double-sided disk, all tracks must be initialized to the standard value. This partially explains why a double-sided disk has more than twice the storage of a single-sided one.

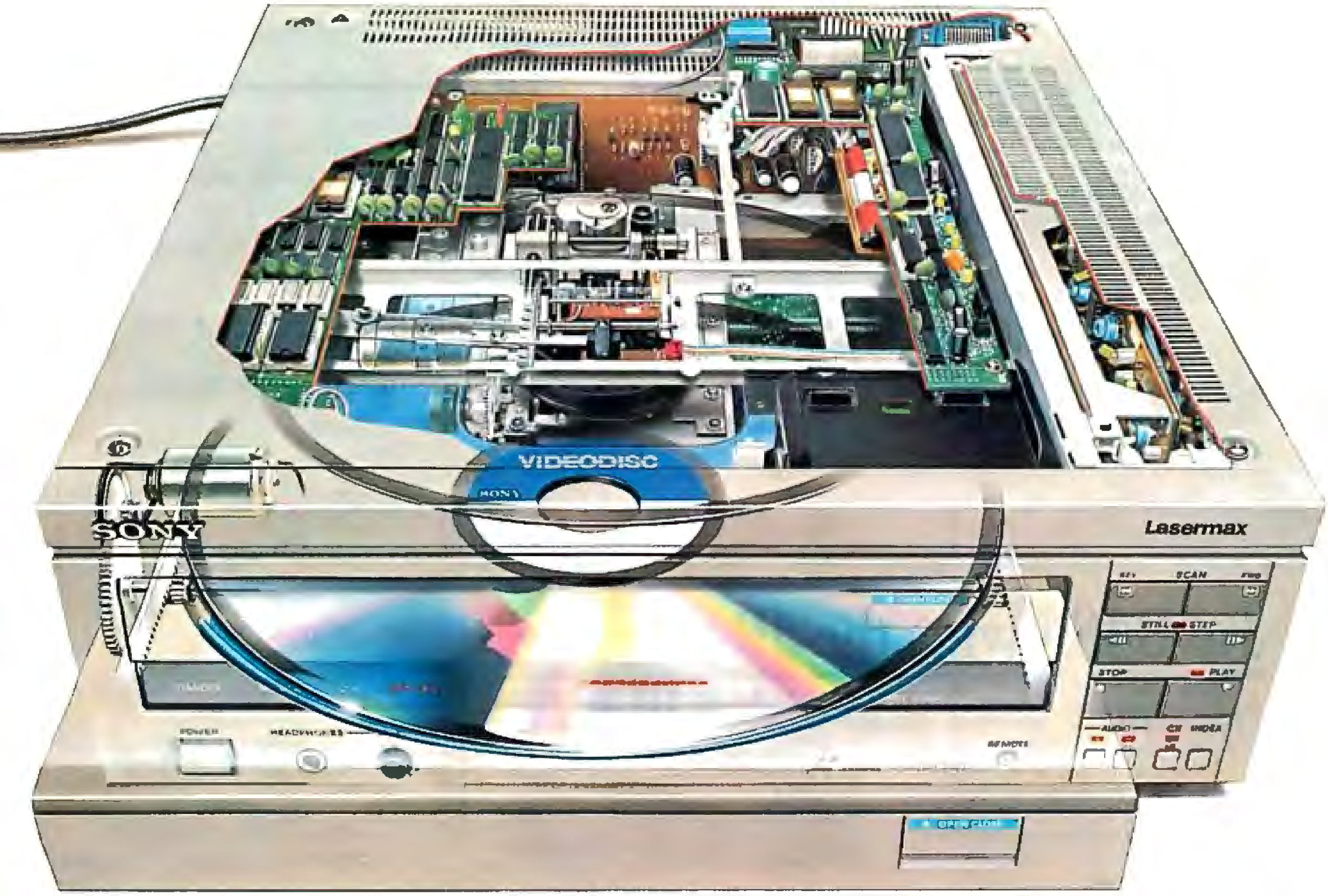
I realize that my assertion that the author used the wrong language opens me to charges of arrogance, but I stick by it. I do not have anything against C as a language; to the contrary, one of the strongest points in its favor is the ease of including assembly language segments in a program. It is no more difficult to write XBIOS (or GEMDOS or BIOS) calls in assembly language than it is in C, and it results in more readable source code and more compact, faster-executing object code.

Two other arguments in favor of using assembly are that C contains an assembler, and if you write these calls in C, you must write a "trap handler" in assembly for each of the aforementioned families of calls. In other words, it makes more sense to me to write the overall program in C and write the calls in assembly. (See listing 1.)

Some seasoned 680xx programmers may wince at my specifying the .W (word) length in the code. Even though every assembler I am familiar with automatically defaults to this value, its inclusion guarantees portability from one assembler to another. In addition, it helps me as a programmer to remember the length of the argument.

In conclusion, I consider it curious that

continued



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an author of Mr. Rothman's obvious stature would trade on his good name by submitting untested code to a magazine, especially to a magazine with such a high reputation as that of BYTE. I would certainly be interested in seeing his response to this letter.

Thank you for giving me the opportunity to set the record straight.

Maloney
Van Nuys, CA

The author's reply:

Mr. Maloney is correct that it is necessary to initialize tracks 0 and 1 to all zeros. In the original of this routine, this was done in the last parameter to the Flopfmt *call (page 230) which should be:*

i<2 ? 0 : VIRGIN

Somewhere in the course of revising the routine after it had been tested, the first part of the parameter got lost. My apologies for any inconvenience.

While we're on the subject, one other error cropped up in the same listing. In

continued

Listing 1: *The following assembly code will correctly format both sides of a double-sided disk in drive A.*

```
FLOPFMT MOVE.Q  #1,D7
   ;SIDE ONE

LOOP_S  MOVE.W  #79,D6
   ;(TRACKS/SIDE) -1

LOOP_T  MOVE.W #$E5E5,
        (SP)
   ;VIRGIN

        TST.W   D7
   ;IS THIS SIDE ZERO?

        BNE     CONT
   ;IF NOT, THEN BRANCH

        CMPI.W  #2,D6
   ;IS THIS TRACK 2-79?

        BPL     CONT
   ;IF SO, THEN BRANCH

        ADDQ.L  #2,SP
   ;ALIGN STACK POINTER

        CLR.W   -(SP)
   ;VIRGIN FOR TRACKS
   ;0-1

CONT MOVE.L #$87654321,
        -(SP)
   ;MAGIC

        MOVE.W  #1,
        -(SP)
   ;INTERLEAVE

        MOVE.W  D7,
        -(SP)
   ;SIDE

        MOVE.W  D6,
        -(SP)
   ;TRACK

        MOVE.W  #9,
        -(SP)
   ;SECTORS/TRACK

        CLR.W   -(SP)
   ;DRIVE A

        CLR.L   -(SP)
   ;DUMMY ARGUMENT

        PEA     BUFFER
   ;ADDRESS OF BUFFER

        MOVE.W  #10,
        -(SP)
   ;FORMAT FLOPPY
   ;DISK

        TRAP    #14
   ;CALL XBIOS
```

continued

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```
       ADD.L    #26,SP
;ALIGN STACK
;POINTER

       TST.W    DO

;DID ERROR OCCUR?

       BMI      ERROR
;IF SO, TAKE BRANCH

       DBRA D6,LOOP_T
;NEXT TRACK

       DBRA D7,LOOP_S
;OTHER SIDE
```

the Flopwr *call on page 232, the parameter* SIDENO *actually should be* devno.

With the two errors fixed, the routine is in its correct form. In this form, it has been in use in our company's ST products for over a year and has produced no problems.

As to Mr. Maloney's assertion that C is not the correct language for the routine: This is what a colleague of mine calls a "religious" question—that is, it has to do with what you believe in. There is certainly something to be said for writing many low-level routines in assembly. However, I used C in the article for two reasons: I thought more people would be able to read a C example than one in 68000 assembly, and the ST Developer's Package provided by Atari has a strong C bias and includes the trap handlers that Mr. Maloney mentions, hidden in bindings that make trap calls look just like calls to C library functions. So there is no additional work for the C programmer.

Michael Rothman
Cambridge, MA

FIXES

EXE Only

In our July 1986 issue, on page 178, at the end of David McNeill's article "Analog Circuit Analysis," it was incorrectly stated that the program he discussed is available in a variety of formats. In fact, only the executable code is available and it runs only on the Commodore 64. We regret any inconveniences that this error may have caused.

Noncommercial ZCPR3

David McCord of Echelon Inc. has pointed out to us that the source code for the ZCPR3 operating system mentioned in the "CP/M Hall of Fame" (October) is available for noncommercial use only. Any commercial use of ZCPR3 requires permission from Richard Conn (the program's author) or Echelon Inc. (885 North San Antonio Rd., Los Altos, CA 94022, (415) 948-3820). Also, other forms of ZCPR3 marketed by Echelon as automatic installation versions are completely proprietary.

Bridger Mitchell and Derek McKay also wrote in, carrying the banner for MEX, NSWP, and NULU, which all carry the same copyright as ZCPR3.

Much public domain software is distributed in a "copyrighted, noncommercial duplication permitted" form. You should always consult a public domain package's accompanying documentation for details on permissions its author is granting.

Expanded Price

The price of $295 for the Levco One+ One memory-expansion kit (November 1986, page 250) is in error. Levco has informed us that the price is $395. ■

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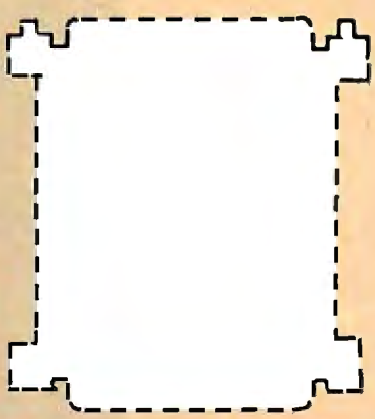

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Zenith Data Systems introduced its first 80386-based machine, the Z-386, claiming it has a performance rate of 4 million instructions per second. The Z-386's central processor has a clock speed of 16 MHz with zero wait states. ZDS will sell the Z-386 in two configurations. The Model 40 comes with a 40-megabyte hard disk, a 1.2-megabyte floppy disk, and six open expansion slots; suggested retail price is $6499. The Model 80 has 80 megabytes of storage; suggested retail price is $7499.

The Z-386 has 10 bus slots: six "true" 32-bit (three of which are unoccupied), two 16-bit, and two 8-bit. It also comes with a Winchester/floppy disk controller, serial and parallel ports, and sockets for 80287 or 80387 coprocessors.

Zenith said the machine will be available early this year and will ship with MS-DOS 3.2 and Microsoft Windows. Contact Zenith Data Systems, 1000 Milwaukee Ave., Glenview, IL 60025, (312) 391-8860.
Inquiry **550.**

Kaypro Corporation announced a trio of machines based on Intel's 80386 microprocessor. The basic version, called the Kaypro 386 Model A, has a 1.2-megabyte floppy disk drive and 512K bytes of RAM; its price is $4995. The Model E has a 1.2-megabyte floppy disk drive, 1 megabyte of RAM, and a 40-, 130-, or 170-megabyte hard disk. The Model E will sell for $6295 to $8595, depending on storage capacity. The Model-N Network File Server comes packaged with a 170-, 280-, or 380-megabyte hard disk drive, at prices ranging from $14,950 to $19,950.

The Kaypro 386 runs on a 16-MHz 80386 microprocessor.

Each model is equipped with either a monochrome, CGA, or EGA display. All three units can be expanded to handle as much as 660 megabytes of hard disk storage and 16 megabytes of RAM. For high-speed backup, Kaypro will sell 60-megabyte cartridge tape units. Contact Kaypro Corp., 533 Stevens Ave., Solana Beach, CA 92075, (619) 481-4300.
Inquiry **551.**

Four for the 386

Phar Lap Software announced 386/ASM, an assembler for the Intel 80386 microprocessor. The assembler enables you to create assembly language programs for the 80386 on the IBM PC, VAX, and UNIX systems.

You can assemble multiple source modules separately and combine them using Phar Lap's linker program. A macro processor lets you create your own instruction sequences that can be called by name. You can also group common symbol directives in a file and then assemble them into source files as needed. According to Phar Lap, symbols can be up to 31 characters and can contain uppercase and lowercase characters. The company reported that on an IBM PC AT, you can assemble over 3000 source lines per minute.

Accompanying 386/ASM are two utilities. Minibug is a real- and protected-mode debugger for the 80386. RUN386 loads and executes 80386 protected-mode applications. Both utilities require a PC-compatible system equipped with an 80386 CPU running MS-DOS.

The program costs $495. For more information, contact Phar Lap Software Inc., 60 Aberdeen Ave., Cambridge, MA 02138, (617) 661-1510.
Inquiry **552.**

The program 386/Link is a linker from Phar Lap that combines relocatable object modules created by 386/ASM into a single executable file. The linker features external symbols, which when used in an 80386 instruction enables the assembler to partially assemble the instruction, without specifying the address of the symbol. The linker fills in the address at link time.

The Intel Absolute Hex Format is produced by 386/Link.

Requirements of 386/Link include an IBM PC or compatible with 256K bytes of RAM and MS-DOS or PC-DOS 2.0 or later. It will also run on a VAX or MicroVAX running VMS 3.0 or higher.

The linker also costs $495; you can contact Phar Lap at the address above.
Inquiry **553.**

Virtual 86 machine architecture support for the Compaq Deskpro 386 is incorporated into the most recent release of DESQview. Version 1.3 of the multitasking operating environment was announced by Quarterdeck Office Systems. The program acts as a virtual machine manager that allocates resources such as memory and processor time to several programs simultaneously.

DESQview version 1.3 sells for $99.95 and runs on IBM PCs, XTs, ATs, or compatibles, as well as on the Compaq Deskpro 386.

For more information, contact Quarterdeck Office Systems, 150 Pico Blvd., Santa Monica, CA 90405, (213) 392-9851.
Inquiry **554.**

continued

PC-MOS/386 is a DOS-compatible multiuser operating system, announced by The Software Link.

The operating system is available in single-user multitasking, 5-user multitasking, and 25-user multitasking versions.

PC-MOS/386 MT, the single-user version, costs $195 and provides concurrency for multiple applications running on the same 80386 system.

PC-MOS/386 Multiuser-5, also a multitasking system, costs $595 and allows up to five users to run applications at dumb terminals linked to an 80386 system. PC-MOS/386 Multiuser-25, priced at $995, is the same as the Multiuser-5 system but allows up to 25 users to be linked at one time.

According to The Software Link, PC-MOS/386 supports the four modes of the 80386 chip. By supporting the 32-bit protected mode and enhanced instruction set of the 80386 chip, the operating system enables you to create new applications. Support of the real mode and virtual 80386 mode enables you to use DOS application software, while also taking advantage of the operating system's multiuser capability.

The operating system includes support for record and file locking, intertask communication through the NETBIOS protocol, print spooling, remote-modem access, usage statistics, nested batch files, and security at the user, file, and directory levels.

The Software Link reports that Summit Software Technology's BetterBASIC/386, which is a multitasking superset of BASICA, is bundled with PC-MOS/386.

Contact The Software Link Inc., 8601 Dunwoody Place NE, Suite 632, Atlanta, GA 30338, (404) 998-0700.
Inquiry **555.**

PC-MOS/386 supports the four modes of the 80386 chip.

80386 Boards for PC XT and AT

Quadram's Quad386 XT, a coprocessor board for the IBM PC XT and compatibles, is based on a 16-MHz 80386 microprocessor. The board features 1 megabyte of 32-bit memory using 256K-bit DRAMs and offers an additional 2 megabytes of memory via an optional daughterboard. It can hold an 80287 math coprocessor and has 96K bytes of image memory and 32K of direct cache memory.

The board supports expanded memory applications, allowing them to execute in its 32-bit memory. Disk-caching software is bundled with the board, which fits in a single slot in the computer.

With 1 megabyte of memory, the board sells for $1495; the daughterboard with 2 megabytes costs $795. Contact Quadram Corp., One Quad Way, Norcross, GA 30093-2919, (404) 923-6666.
Inquiry **556.**

Seattle Telecom & Data, maker of 80286-based accelerator boards for the IBM PC, announced a 16-MHz 80386-based board for the PC AT. The STD-386 accommodates 2 to 16 megabytes of dual-ported memory and will hold an 80387 math coprocessor when that chip becomes available. Currently, a daughterboard provides an 80287 coprocessor.

The board is compatible with 8086 and 80286 hardware and software and supports the AT's real and protected modes. It runs in both 6- and 8-MHz ATs and, according to the company, may work in AT compatibles running at other clock speeds.

Prices range from $3200 to $3700 depending on the amount of memory. The board occupies a single full-length expansion slot and has a ribbon-cable connector that plugs into the 80286 socket on the motherboard. Contact Seattle Telecom & Data Inc., 12277 134th Court NE, Suite 205, Redmond, WA 98052-2429, (206) 820-1873.
Inquiry **557.**

Also designed for the IBM PC AT and compatibles is Intel's Inboard 386/AT. In conjunction with its 16-MHz 80386, the board uses a high-speed memory cache to boost performance. It can hold up to 1 megabyte of memory and has a socket for an 80387 math coprocessor, although this chip is not yet available; in the meantime, the company is offering a 10-MHz 80287 math coprocessor. The basic board sells for $1995; with 1 megabyte of memory, it costs $2495. An optional piggyback board holds an additional 1 megabyte ($645) or 2 megabytes ($1145) of memory.

According to the company, the Inboard is fully compatible with existing 8088- and 80286-based hardware and software. When control software that uses the 80386's virtual 86 mode is developed, the board will run several existing applications simultaneously, without requiring changes to the programs. Contact Intel Corp., Personal Computer Enhancement Operation, Mail Stop TOD-07, 5200 Northeast Elam Young Parkway, Hillsboro, OR 97124-6497, (503) 629-7354.
Inquiry **558.**

Turbo Basic from Borland

Borland International announced Turbo Basic, a $99.95 programming environment for the IBM PC. The company claims the program compiles at 12,000 lines per minute to produce native executable (.EXE) code. The program also includes a memory-to-memory compiler, a full-screen editor, an internal linker and run-time library, and a Microcalc spreadsheet with source code.

Turbo Basic takes advantage of the interactive strength of the BASIC language and also uses the structured, modular approach of Pascal. Conditional control is provided by the block IF (including ELSEIF) and SELECT CASE statements. Turbo Basic also supports DO WHILE, DO UNTIL, LOOP WHILE, and LOOP UNTIL statements. Turbo Basic also offers true recursion, pull-down menus, and a multiwindow environment. It is written in assembly language and is compatible with IBM Advanced BASIC and Microsoft GW-BASIC, and EGA graphics are supported.

Turbo Basic provides 8087/80287 math coprocessor support, which generates in-line coprocessor instructions and calculates intermediate results to 80 bits of precision, according to Borland.

continued

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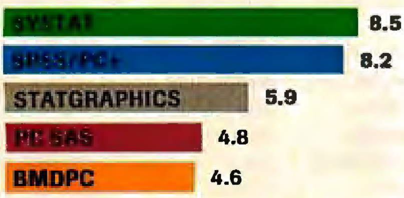

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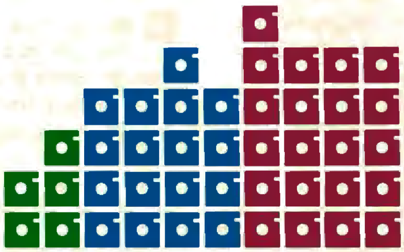

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The compiler, editor, and executable programs are fully integrated, and you can output program text to a window or to the full screen. You also have control over the placement, size, and color of windows in your programming environment.

You can develop programs larger than the traditional 64K-byte limit, with the $SEGMENT compiler directive. Borland reports that string data can occupy up to 64K bytes of RAM, and the program provides dynamic string memory management.

Contact Borland International, 4585 Scotts Valley Dr., Scotts Valley, CA 95066, (408) 438-8400.
Inquiry **559.**

80386 Chip Set

Chips and Technologies Inc. has developed the CS 8230 AT/386 CHIPSet, a seven-chip alternative to the Intel 80386 32-bit microprocessor family. The chip set, which operates at 16 MHz with zero wait states and supports from 1 to 16 megabytes of memory, consists of an 84-pin bus controller, an 84-pin page/interleave memory controller, two 68-pin address buffers, two 68-pin data buffers, and a 68-pin control signal buffer.

According to the firm, if the chip set is used in conjunction with the 82C206 Integrated Peripherals Controller, manufacturers can build 80386 AT-compatible systems that require fewer than 40 chips (not including memory) instead of the more than 200 ICs in a typical 80286-based IBM PC AT system. A Chips and Technologies-based system would have a motherboard that is 45 square inches compared to a typical 140-square-inch board. Also, the AT/386 CHIPSet system would consume 11 watts of power instead of the standard 45 watts.

Chips and Technologies also provides an AT/386 development kit that includes a system board with 2 megabytes of memory, AT-compatible BIOS from Phoenix Technologies, diagnostic software, data sheets, application notes, and schematics. The AT/386 CHIPSet is available in quantities of 100 for $196.40 per unit, and the development kit is priced at $2995 per unit. Contact Chips and Technologies Inc., 521 Cottonwood Dr., Milpitas, CA 95035, (408) 434-0600.
Inquiry **560.**

ProWrite lets you edit up to eight windows at once.

Microsoft Word for the Macintosh

Microsoft Word version 3.0 is a word processor that runs on a Macintosh with 512K bytes of RAM. The program is not copy-protected and sells for $395. It comes on an 800K-byte disk, but you can order it on two 400K disks.

Some of the features of the word processor include an 80,000-word spelling checker, customizable menus, and the ability to preview up to two pages of a document, manipulate columns, and use a keyboard interface instead of a mouse. For more details, see "Applications Only" by Ezra Shapiro on page 395.

Contact Microsoft Corp., P.O. Box 97017, Redmond, WA 98073-9717, (206) 882-8080.
Inquiry **561.**

Amiga Word Processor

ProWrite from New Horizons is a $124.95 word processor that offers proportionally spaced character fonts, sizes, styles, and colors.

Six pull-down menus give you a choice of hanging indent, justification, decimal or left tab settings, inclusion of IFF color graphics, and draft or standard print. Menu selections include Edit, with undo and cut and paste; Search, with find and change; and Character, which offers the font, size, style, and color choices for text.

ProWrite enables you to edit in up to eight windows at once. The Paragraph menu contains format commands, and the Document menu gives you control over headers, footers, and page numbers.

Contact New Horizons Software Inc., P.O. Box 43167, Austin, TX 78745, (512) 329-6215.
Inquiry **562.**

Group Document Review

ForComment works with your word-processing program and enables up to 16 people to review, make comments, or suggest revisions to text on a line-by-line basis. One person acts as the author, while the other 15 are reviewers. The program keeps an audit trail of the editorial process and collates all changes on one disk.

To run ForComment, you must read a word-processing document into the program. The original remains unchanged in a top window, and you enter comments and changes in a lower window. Each comment is labeled with the reviewer's initials, and a swapping function lets you give revisions a try before saving them.

ForComment works in local area networks as well as in stand-alone environments. It runs on IBM PCs and compatibles with 256K bytes of RAM. The program costs $195 for a single author or $995 for the network version.

Contact Broderbund Software Inc., 17 Paul Dr., San Rafael, CA 94903-2101, (415) 479-1700.
Inquiry **563.**

Controller Expands Hard Disk Storage

Konan's hard disk controller card, the KXP-230 Drive Maximizer, expands the storage capacity of hard disks for IBM PCs, XTs, and compatibles. The company reports that the half-slot controller increases the capacity of hard disks by compacting and compressing data. With the KXP-230, for example, a 20-megabyte drive can be increased to a total capacity of 32 megabytes.

Other features include an on-board BIOS ROM that lets you configure the card for any ST506/412-compatible disk drive. The controller provides disk caching and fragmentation control, automatically organizing clusters so that fewer seeks are required. Its error detection can correct up to 65,536 bit errors and recover complete clusters.

The controller is priced at $249 and requires a computer running DOS 3.0 or higher. Contact Konan Corp., 4720 South Ash Ave., Tempe, AZ 85282, (602) 345-1300.
Inquiry **564.**

continued

PC-Compatible Wang LapTop

Wang Laboratories introduced a laptop computer that includes a 10-megabyte hard disk and printer as standard features. The Wang LapTop Computer, which weighs slightly more than 14 pounds, does not come with a floppy-disk drive; 5¼- and 3½-inch floppy drives are optional. The company says that in addition to being able to run all software for Wang's desktop computers, the machine is compatible with the IBM PC XT.

Priced at $3530, the LapTop uses NEC's V30 processor with a clock speed of 8 MHz. Memory is 512K, expandable to 1 megabyte with a board ($695) the user can install. The LapTop's 80-character by 25-line, nonbacklit LCD uses Hitachi's supertwisted crystals and displays high-contrast dark blue characters on a yellow background. Its resolution is 640 by 200 pixels. The LCD is removable and can be replaced with a color monitor.

The LapTop's full-size keyboard has 92 keys, including 16 function keys. The Epson-compatible thermal-transfer printer outputs near-letter-quality text at 18 cps. The computer has an RS-232C serial port (a serial-to-parallel adapter is optional), an IBM CGA-compatible external-monitor connector, and a port for an optional numeric keypad ($95). Other options include internal, Hayes-compatible 1200-bps and 2400-bps modems, priced at $425 and $795, respectively.

The Wang LapTop also offers an SCSI port, through which up to six external devices can be daisy-chained.

The LapTop is bundled with MS-DOS 3.2. Additional software includes Wang Integrated Word Processing ($385), a 2110/VT-100 terminal-emulation package ($200), an asynchronous communications package ($100), and Wang Systems Networking ($400).

With a 5¼-inch floppy disk drive, the computer costs $3895; with a 3½-inch floppy disk drive, $4048. For more information, contact Wang Laboratories Inc., One Industrial Ave., Lowell, MA 01851, (617) 459-5000.
Inquiry **565.**

Wang's LapTop has a 10-megabyte hard disk.

PC-based Circuit Emulator

Beck-Tech's ROMICE, a PC-based circuit emulator, is designed for engineers who are developing firmware for embedded microcomputer systems. The emulator includes an add-in card for the IBM PC, XT, AT, and compatibles; an emulator package that provides real-time, in-circuit emulation of a ROM or EPROM up to 64K bytes in size; cables for connection to the development circuit board; and support software.

The hardware consists of a 7- by 4-inch plug-in circuit board and a 24-inch emulation cable with a connector for plugging into a JEDEC 28-pin socket. Adapters for 24-pin JEDEC sockets are also available. Maximum PC bus access time is 200 nanoseconds.

The control software is processor-independent and operates with 4-, 8-, 16-, and 32-bit systems, emulating any standard-size EPROM from 2716 to 27512. The program enables users to load, modify, edit, or patch hex-format files. Commands include support for checksum computation, moving memory contents, and page examination.

The system sells for $595 and is also compatible with all standard DOS assemblers and compilers. For more information, contact Beck-Tech Corp., 41 Tunnel Rd., Berkeley, CA 94705, (415) 548-4054.
Inquiry **566.**

Floppy Drive Holds 10 Megabytes

Konica Technology introduced a 10-megabyte, 5¼-inch floppy disk drive that uses standard floppy disks. According to Konica, the half-height KT-510 disk drive formats disks for 480 tracks per inch (tpi), enabling formatted storage capacities of 10.9 megabytes. The drive can also read data from disks previously formatted for either 360K bytes or 1.2 megabytes. Its data-transfer rate is 1.6 megabits per second.

An SCSI port is used to connect the KT-510 to the computer. Initial OEM shipments will begin this month, with quantity shipments to begin in April 1987. In large quantities, the drive will sell for $400. Complete subsystems, which the company says will be available in the second quarter of 1987, will retail for less than $1000. Contact Konica Technology Inc., 777 North Pastoria Ave., Sunnyvale, CA 94086-2918, (408) 773-9551.
Inquiry **567.**

Local Area Networks for Amiga

Ameristar Technologies has developed an Ethernet controller, a version of Sun Microsystems' Network File System (NFS), and an ARCNET controller for the Commodore Amiga. The 10-megabit-per-second Ethernet controller and NFS enable the Amiga to function as a graphics workstation on a network with Sun workstations, IBM PCs, DECs, and other computers running an implementation of NFS.

The Ethernet controller uses Advanced Micro Device's LANCE chip set and provides standard and thin Ethernet interfaces. The card is available in 86-pin side-mount ($749 in single quantities) or Zorro backplane ($699) versions, both of which are compatible with the Amiga's autoconfiguration architecture.

The ARCNET LAN controller operates at 2.5 megabits per second and supports up to 255 Amigas and IBM PCs in a token-ring network. The controller handles network reconfigurations automatically, allowing machines to be dynamically connected or disconnected from the network. This controller is also available in side-mount and Zorro backplane forms, which retail for $499 and $425, respectively, in single units. Contact Ameristar Technologies Inc., P.O. Box 415, Hauppauge, NY 11788, (516) 724-3344.
Inquiry **568.**

continued

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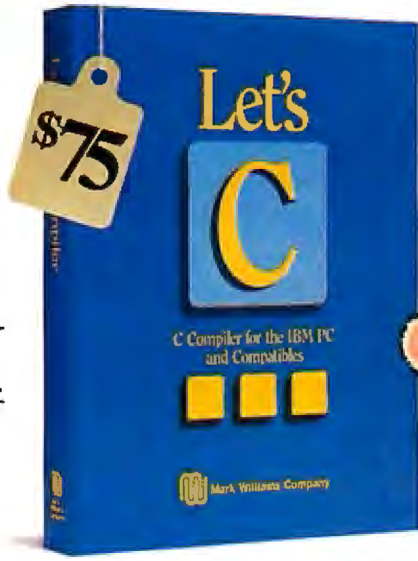

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Let's C Benchmark Done on an IBM-PC/XT, no 8087.
Program: Floating Point from BYTE, August, 1983.

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SYSTEMS

Datavue's Snap 1 + 1 Laptop

Datavue, manufacturer of portable computers, announced its first laptop, which in one configuration weighs only 5 pounds. The Snap 1 + 1 has a full-screen LCD that folds over an 83-key keyboard, two 3½-inch floppy disk drives, up to 640K bytes of RAM, and connectors for serial and parallel interfaces and RGB and composite monitors. In this configuration, the laptop weighs 10 pounds. The rear half of the unit, which contains the disk drives, can be separated from the front, which contains the keyboard, display, processor, and 512K bytes of memory. The front half can then be used as a full-function 5-pound IBM compatible running on a RAM disk.

Three 80-character by 25-line LCDs are available, all of which feature super-twisted birefringent crystals for high contrast. As an option, one of the disk drives can be replaced with a 20-megabyte hard disk. A half-size expansion slot and optional internal 300/1200-bps modem are also available.

With two floppies, 640K bytes of memory, and a blue-colored LCD, the Snap 1 + 1 costs $2095. The company claims it will be shipping in the first quarter of 1987. For more information, contact Datavue Corp., One Meca Way, Norcross, GA 30093-2919, (404) 564-5668.
Inquiry 569.

The Snap 1 + 1, a PC-compatible laptop from Datavue.

AST's Premium/286

AST Research introduced the Premium/286 series of IBM PC AT-compatible computers that run on an 80286 processor with selectable speeds of 6, 8, and 10 MHz. Available with 512K bytes or 1 megabyte of RAM, the computers are equipped with a 1.2-megabyte floppy disk drive, a multimode enhanced graphics adapter that supports four display standards, a floppy/hard disk controller, and an optional 20-, 40-, or 70-megabyte hard disk drive. Monochrome and enhanced color graphics monitors are an option.

Two of the computers' seven expansion slots are capable of running without wait states at any of the machines' three speeds. These slots add a third connector to the standard two-connector 16-bit AT bus, which provides direct access to the 80286 and maintains compatibility with AT slots.

MS-DOS 3.1 and GW-BASIC are bundled with the machines. Prices range from $1995 for a model with 512K of RAM and a single floppy disk drive to $3995 for a model with 1 megabyte of RAM and a 70-megabyte hard disk. Contact AST Research Inc., 2121 Alton Ave., Irvine, CA 92714.
Inquiry 570.

80386-based Multibus Single Boards

Intel announced four Multibus single-board computers based on its 16-MHz 80386 microprocessor. The iSBC 386/21, 386/22, 386/24, and 386/28 offer 1, 2, 4, and 8 megabytes of 32-bit memory, respectively. All can be expanded to 16 megabytes through add-on modules. The company says that the increased memory gives the microprocessor access to memory through a 64K-byte zero-wait-state cache, eliminating the need to go through the system bus.

The boards use a dual bus structure: a 32-bit-wide bus for data transfers between the microprocessor, cache, and dual-ported memory; and a 16-bit bus for transfers over the Multibus or iSBX bus. All of the boards are supported by iRMX 286, XENIX, and UNIX System V operating systems, as well as proprietary operating systems for the 8086 or 80286. The memory-expansion modules are available with 1, 2, 4, or 8 megabytes of RAM.

Prices are set at $4800 for the 386/21, $5970 for the 386/22, $8310 for the 386/24, and $12,990 for the 386/28. Contact Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052-8065, (503) 640-7399.
Inquiry 571.

CompuTitan AT Compatible

American Mitac's CompuTitan is an IBM PC AT-compatible computer based on an 80286 processor running at 6 or 8 MHz. The $1695 system comes with one 1.2-megabyte floppy disk drive and 640K bytes of RAM. The standard configuration includes eight expansion slots, a battery-backed real-time clock/calendar, a socket for an 80287 math coprocessor, a keyboard controller, and a 192-watt power supply. The system uses the Phoenix BIOS and is bundled with MS-DOS 3.2 and GW-BASIC.

Hard disk drives with storage capacities of 20, 30, or 40 megabytes are available as options. For more information, contact American Mitac Corp., 3385 Viso Court, Santa Clara, CA 95054, (408) 988-0258.
Inquiry 572.

Kimtron's PC Workstation

Kimtron, maker of IBM PC-compatible terminals, has announced a diskless PC workstation for IBM PCs and ATs. Called the Satellite, the workstation is based on NEC's V40 microprocessor running at a selectable speed of 5 or 8 MHz. The motherboard has 256K bytes of RAM (expandable to 640K), a battery-backed real-time clock, a socket for a math coprocessor, and two full-size PC-compatible slots. Also provided are a serial and a parallel port, as well as circuitry that supports Hercules monochrome graphics and IBM color graphics.

Priced at $995, the machine is equipped with the company's K-Net local area network board. It comes with a 12-inch monochrome monitor and an AT-style keyboard. For more information, contact Kimtron Corp., 1705 Junction Court, Building 160, San Jose, CA 95112, (408) 436-6550.
Inquiry 573.

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Inquiry 426

PERIPHERALS

SCSI-based Storage Units Stack Up

Western Digital announced a set of stackable storage devices based on the SCSI port for IBM PCs and compatibles. Called VersaStak, the set includes a 225-watt base unit ($395); a 70-megabyte hard disk ($2995) with an access time of 30 milliseconds; a 140-megabyte hard disk ($3995) with an access time of 25 milliseconds; and a 60-megabyte tape drive ($1395). Future options will include a CD-ROM drive and a write-once optical drive.

Other future options for the VersaStak should allow the system to function as a standalone network file server. These options include 80286- and 80386-based processor modules and a variety of network interface modules. For more information, contact Western Digital, 2445 McCabe Way, Irvine, CA 92714, (714) 863-0102.
Inquiry **574.**

Add Memory and More to Amiga

MicroBotics is offering the StarBoard2 memory-expansion unit for the Commodore Amiga. The base unit is equipped with a half megabyte of RAM on a main board socketed for an additional half megabyte of memory. You can upgrade the board by installing additional 150-ns RAM chips. With the Upper Deck, a board with sockets for 1 megabyte of RAM, you can expand the unit to 2 megabytes.

An optional multifunction module provides four additional features: a battery-backed clock/calendar; support logic for parity-checked memory, which requires that you install additional parity memory (four 256K-bit chips for each megabyte); a socket for a 68881 math coprocessor; and a write-protectable Memory Disk, which allows you to allocate memory as a RAM disk that can retain data after a warm system reboot.

The StarBoard 2 is powered by the Amiga and automatically configures when running under AmigaDOS 1.2. Additional peripherals can be connected to the unit, which sells for $495 with 512K. The Upper Deck with 0K RAM costs $99.95; the multifunction module costs $99.95. For more information, contact MicroBotics Inc., P.O. Box 855115, Richardson, TX 75085, (214) 437-5330.
Inquiry **575.**

Portable Power Protector

The Modem/Power/Static Pac from Electronics Specialists is a power-protection unit designed for use with portable computers. The unit provides broadband AC power filtering, extended-range spike suppression, modem RF filtering, modem spike suppression, and a static discharge plate.

The $184.95 unit plugs into a conventional 3-prong outlet and uses a CEE-22 universal portable computer power connector. It connects to modems via a standard RJ-11 jack and comes with a 6-foot power cord. For more information, contact Electronic Specialists Inc., 171 South Main St., Natick, MA 01760, (800) 225-4876; in Massachusetts, (617) 655-1532.
Inquiry **576.**

Video Digitizer for Mac

The MacViz Video Digitizer for the Macintosh digitizes a frame of video data from an NTSC RS-170 video source in $\frac{1}{30}$ second. The unit can display a digitized 512- by 512-pixel image on the Macintosh screen every $\frac{6}{10}$ second. It creates a 1-bit gray-scale digitized representation in a hardware circuit; thus the digitized images have no software-generated dither patterns and gray-scale steps, the company claims.

MacViz images are compatible with MacPaint files. The unit comes alone or as part of the MacViz DTP (Desktop Publishing) System, which includes the following components: the MacViz Video Digitizer, MacViz software, a black-and-white CCTV video camera, a video lens, and a lighted copy stand.

The digitizer alone sells for $595, and the complete system costs $1295. For more information, contact Microvision Co., 38 Montvale Ave., Stoneham, MA 02180, (617) 438-5520.
Inquiry **577.**

Personal Logic Analyzer

The Personal Logic Analyzer from PrimeLine performs state, timing, and signature analysis. The unit has a 10-MHz clock rate that yields up to 100-nanosecond resolution. It offers 16 channels for data input with 256 bits per channel for acquisition memory and a reference memory of 256 bits per channel. Other features include 15-ns glitch detection; triggers using words; three-function display of state, timing, and signature; data acquisition in three modes (single, repeat, and compare); multiple display modes; and a variable-delay trigger function.

The unit (Model PLA-3300) operates on a built-in rechargeable nicad battery, from a conventional AC power source, or from an external DC source. It sells for $1995, which includes an input probe. For more information, contact PrimeLine, P.O. Box 670, San Fernando, CA 91341-0670, (800) 525-5554; in California, (818) 764-5400.
Inquiry **578.**

JDL's Color Printer/Plotters

JDL has introduced a series of color printers/plotters designed for engineering and architectural applications. The series provides 14-color plotting and text printing on A- through C-size paper and vellum in both engineering and architectural formats.

The 850 EWS, which sells for $2495, offers a plot speed of 24 inches per second (ips) at a resolution of 90 by 90 dots per inch (dpi) or 12 ips at 180 by 180 dpi. The printer accepts media up to 18 inches wide. In the print mode, the 850 EWS provides five fonts, including the IBM graphics character set. Its draft-quality print rate is 360 characters per second; its near-letter-quality rate, 144 cps. The printer emulates the Diablo 630, IBM color graphics printer, and Epson printers. A serial or parallel port is available, and optional ROM cards provide additional fonts and emulations.

The 850 EWS/GL ($3495) has all the features of the 850 EWS, incorporates an internal card for HP-GL compatibility, and comes with serial and parallel ports as standard. The 850 EWS with GL Processor Controller offers the same features as the 850 EWS and has an external controller that provides HP-GL compatibility and vector file conversion. The controller offers additional graphics features such as scaling, rotation, and reduction. This model sells for $3495 to $3895, depending on the amount of memory. For more information, contact JDL Inc., 2801 Townsgate Rd., Suite 104, Westlake Village, CA 91361, (805) 495-3451.
Inquiry **579.**

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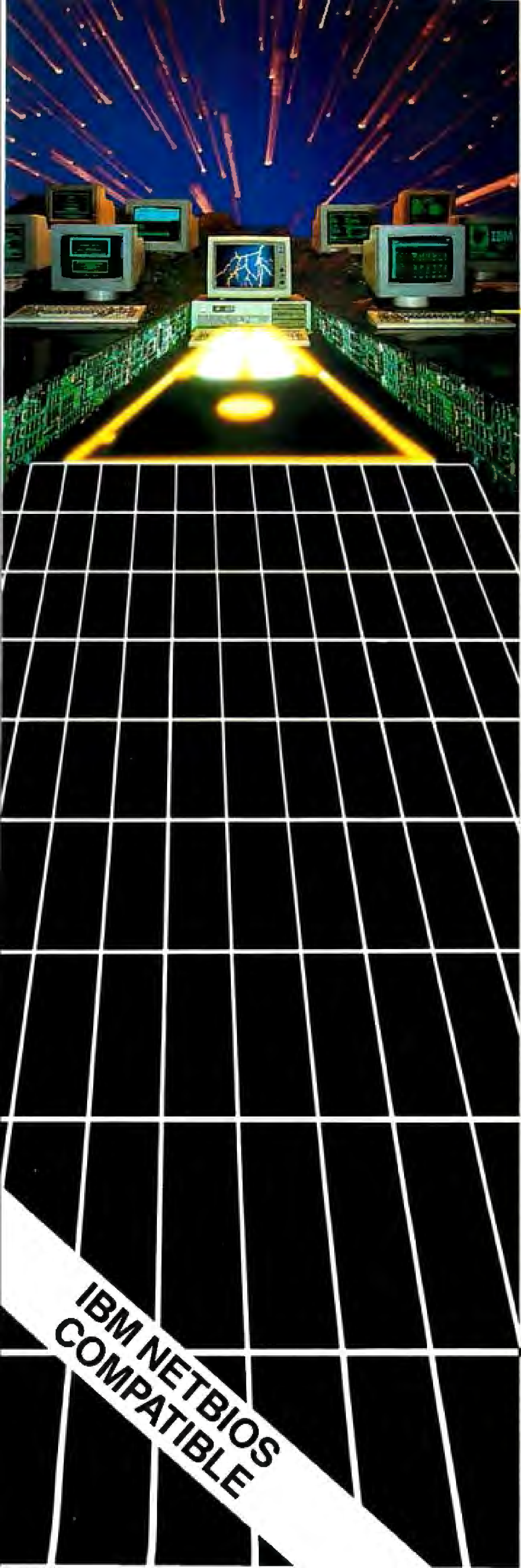

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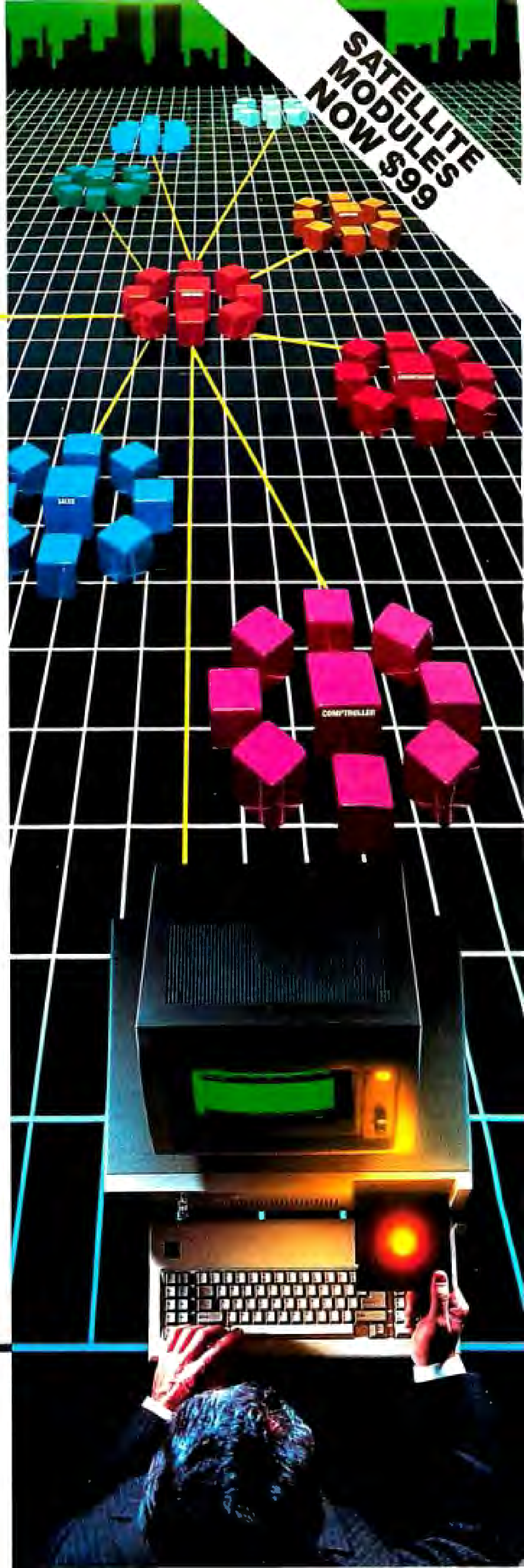

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ADD-INS

Card Converts PC to AT

The MotherCard 5.0, an 80286-based board, provides an IBM PC with full hardware and software compatibility with the IBM PC AT, including support for future protected-mode DOS, the company claims. In addition to an 8- or 10-MHz 80286 microprocessor, the $995 board comes with 640K bytes of conventional memory and 320K of EMS memory (expandable to 16 megabytes), a real-time clock, and a socket for an 80287 (5-, 8-, or 10-MHz) coprocessor. While running in the 80286 mode, you can switch back to the PC's 8088 by typing a DOS-level command.

The board also includes a VLSI PC-to-AT bus converter, an AT-compatible reconfigurable BIOS, a hardware reset button, EMS drivers, and RAM disk, disk cache, print-spooling, and diagnostic software. The reconfigurable BIOS, stored in battery-backed memory, contains all the extended features of the IBM PC AT BIOS, the company says. The board's BIOS can be reconfigured at any time by loading the desired BIOS upgrade with the SETUP program.

The board plugs into a full-length expansion slot. Installation requires that you remove the 8088 from the PC's motherboard and plug it into a socket on the MotherCard. For more information, contact SOTA Technology Inc., 657 North Pastoria Blvd., Sunnyvale, CA 94086, (408) 245-3366.
Inquiry **580.**

Slotbuster for Apple IIs

The Slotbuster II multifunction card for Apple II computers offers a variety of expansion options on a single plug-in board. The basic card, which costs $149.95, comes with an 8K-byte buffer and a utilities disk. The board is sold with one or more of the following options: a parallel printer port ($19.95), a serial printer port ($14.95), a modem port ($29.95), a port for the BSR X-10 home control unit ($29.95), and a speech synthesizer ($39.95). Additional options include 32K and 64K buffers, software for blind users, and a variety of cables.

The company says the board fits in any slot except slot 3 without affecting other slots. It works in the Apple II, II+, IIe, and IIGS. For more information, contact RC Systems Inc., 121 West Winesap Rd., Bothell, WA 98012, (206) 672-6909.
Inquiry **581.**

Higher Resolution for Desktop Publishing

Designed for desktop publishing with IBM PCs, XTs, ATs, and compatibles, the ConoVision 2800 board combines a high-resolution monochrome graphics adapter with an optional raster image processor that doubles the resolution of laser printers. The adapter provides a resolution of up to 2880 by 1024 pixels and can display two pages with typefaces readable to 6 points, the company claims.

The board includes 512K bytes of video RAM and hardware for scrolling, pan, and zoom. Screen drivers enable software that runs under Microsoft Windows to run on the board, which can access the company's library of typefaces and offers a mode that lets you run Hercules-compatible software.

The optional raster image processor increases the resolution of laser printers based on the Canon LPB-CX engine (including the HP LaserJet) to 600 by 300 dots per inch. The processor can produce formatted pages and 2880- by 1024-pixel screen prints in 8 seconds.

Priced at $1325 ($1985 with the image processor), the board works with 20-inch, 100-MHz monitors and 15-inch, 50-MHz monitors. Contact Conographic Corp., 17841 Fitch, Irvine, CA 92714, (714) 474-1188.
Inquiry **582.**

DSP Uses TI's 32020 Chip

The DSP-16 digital signal processor plugs into a single slot in an IBM PC, XT, AT, or compatible. Based on Texas Instruments' TMS32020 digital signal processor, the board includes all components necessary for audio-frequency data acquisition and processing.

In addition to the TMS32020, which provides a throughput of 5 million instructions per second, the board has a 512K-byte data buffer and two 16-bit channels of input/output conversion at a maximum sample rate of 50 kHz. The sample rate is programmable from 5 kHz to 50 kHz. The data buffer can store up to 21 seconds of audio at maximum bandwidth or 3½ minutes at minimum bandwidth. The analog subsystem includes input buffering, antialiasing filters, output filters, and I/O sample and holds.

The company supplies interfaces to seven languages with source code. Also bundled with the board are six sample applications for using it, for example, as a storage oscilloscope and waveform synthesizer, a digital/audio delay line with feedback, an audio loop editor, and a TMS32020 Program Development System. The board costs $2495. Contact Ariel Corp., 110 Greene St., Suite 404, New York, NY 10012, (212) 925-4155.
Inquiry **583.**

Multifunction Modem Card

The Practical Multifunction 1200 is an IBM PC-compatible multifunction card with a 1200-bps modem. The full-length card can hold up to 512K bytes of RAM and has two serial ports, a parallel port, and a battery-backed clock/calendar. Its Hayes-compatible modem offers auto-dial and auto-answer capabilities, pulse or Touch-Tone dialing, automatic adaptive equalization, and two phone jacks.

Software bundled with the board includes two communications programs, Pop-Up Deskset Plus, and RAM disk, print-spooling, and other utilities. With 0K bytes of RAM, the card sells for $395. For more information, contact Practical Peripherals, 31245 La Baya Dr., Westlake Village, CA 91362, (800) 641-0814; in California, (818) 991-8200.
Inquiry **584.**

Add Four Slots to a PC

The Addcard slot-expansion board plugs into the fifth slot of an IBM PC or compatible and provides four additional expansion slots inside the system unit. Priced at $79, the board can hold PC-compatible half-length expansion boards, including memory and accelerator boards, graphics adapters, hard or floppy disk controllers, modems, and others.

According to the company, the board is fully compatible with the IBM PC. For more information, contact Merak Industries, 8704 Edna Dr., Warren, MI 48093, (800) 231-4310, ext. 768.
Inquiry **585.**

continued

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True BASIC 2.0 Lets You Program with Modules

True BASIC announced version 2.0 of its programming language True BASIC. The new version will support graphics display cards, including IBM's Enhanced Graphics Adapter and the Hercules Graphics Card Plus, according to the company. It also has faster execution speeds, improved 8087/80287 support, scripts for automatic entry of commands stored on disk, and improved disk and screen I/O, the company reports.

True BASIC version 2.0 gives you the capability to program with modules, a feature usually found in languages like Modula-2 and Ada. You can share public data across modules without the need for parameter passing. The use of modules offers you public versus private routines, data hiding and sharing, and module initialization. You can store modules in True BASIC libraries and workspaces. Version 2.0 has dynamic array capability, enabling you to redimension static and dynamic arrays while still retaining data.

The programming language runs on IBM PCs, the Macintosh, and the Amiga. True BASIC reports that a version for the Atari ST is in the works.

True BASIC version 2.0 costs $149. Contact True BASIC Inc., 39 South Main St., Hanover, NH 03755, (603) 643-3882.
Inquiry **586.**

Pascal Programming

Execution Pascal offers a high-level-language programming environment, visible programming, and direct tracing. Tracing is automatic, and the program displays the data, control, and procedure flow. Working on a virtual Pascal machine, you don't have to translate, compile, or interpret. It includes all the standard Pascal constructs and some extended constructs.

Execution Pascal displays the Pascal program on the screen, flashing each line of text as the line is executed. The program traces and displays the results on the screen.

The program runs on IBM PCs and compatibles with 256K bytes of RAM and MS-DOS or PC-DOS 2.0 or higher and sells for $29.95, plus $5 for shipping and handling. For more information, contact Dir-Exec Software Inc., 6305 Contention Court, Bethesda, MD 208017, (301) 454-7935.
Inquiry **587.**

BASIC to Pascal Converter

BAS_PAS is a source-code translation system that converts BASIC programs into Pascal. Gotoless Conversion, the manufacturer, reports that the software was originally developed to translate IBM BASICA; however, any BASIC similar to BASICA can be translated by BAS_PAS by changing the statement delimiter and/or the remark starter.

The program transforms your BASIC statement to native Pascal code, if an equivalent Pascal statement exists. If it doesn't exist, the program will translate the statement into a procedure call in Pascal. Statements that have no meaning in Pascal, such as DELETE and EDIT, are turned into comment lines in the converted program.

The program generates Turbo Pascal, ANSI-standard Pascal, or Professional Pascal.

From the option menu, you have a choice of BASIC or Pascal, indentation size, tab size, and maximum target source line length.

BAS_PAS runs on IBM PCs and compatibles with 256K bytes of RAM and PC-DOS or MS-DOS 3.0 or higher. The program sells for $85. Contact Gotoless Conversion, P.O Box 50068, Denton, TX 76206, (214) 221-0383.
Inquiry **588.**

Opal

The Software Factory announced Opal, an interpretive batch executive language that enables you to prototype program functions and user interfaces. With Opal, you don't have to recompile the program every time you make a change.

The program is DOS-compatible and offers screen and menu definition, flow of control, calls, "do" groups, numeric calculation, string manipulation, and disk, file, directory, and system functions.

Opal runs on IBM PCs and compatibles and costs $169. Contact The Software Factory Inc., 15301 Dallas Parkway, Suite 750, LB 44, Dallas, TX 75248, (214) 490-0835.
Inquiry **589.**

Modula-2 Compiler for 8086 IBM PCs

Farbware announced a Modula-2 compiler that produces object files compatible with the PC-DOS and MS-DOS link utility programs. The program is a native code compiler, code generator, and run-time package that, according to Farbware, implements the full Modula-2 language, as defined by Niklaus Wirth.

The source code for all definition and implementation modules is included, as well as a UNIX-like make utility. The source code is written in 8086 and supports any IBM-compatible assembler, Farbware reports. Some low-level PC-DOS interface routines are included and are written in 8086. The make utility compiles, links, and executes several test programs.

The compiler is not copy-protected. It costs $89.95. Contact Farbware, 1329 Gregory, Wilmette, IL 60091, (312) 251-5310.
Inquiry **590.**

Design, Organize, and Capture Screens on the IBM PC

Screen Master from Genesis Data Systems has announced Screen Master, Screen Diemon, Magikey, and Drun modules, which give you the ability to design and manipulate screens.

The Screen Master module enables you to design screens and menus and save them on disk. You can also save parts of screens separately as objects.

The Screen Diemon (pronounced "demon") is a screen organizer that lets you arrange screens and objects in any order and control their display with pauses, GOTOs, GOSUBs, branches, and other embedded commands. You can also create demos, tutorials, and prototypes with Screen Diemon.

The Magikey module is a memory-resident program that enables you to capture screens from other programs. You can use the screens in Screen Diemon to create demos and tutorials and replace them in the program you captured them from.

Drun is a run-time module for distributing Screen Diemon projects to other systems.

Screen Master runs on IBM PCs and compatibles with at least 256K bytes of RAM and MS-DOS or PC-DOS 2.0 or higher. It sells for $99.95. Contact Genesis Data Systems Inc., 5403 Jonestown Rd., Harrisburg, PA 17112, (717) 652-1200.
Inquiry **591.**

continued

SOFTWARE • SCIENTIFIC AND ENGINEERING

Three-Dimensional CAD for $349

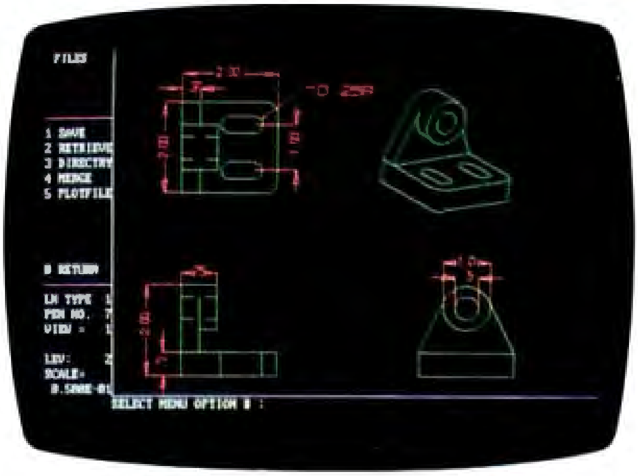
CADPlus Systems announced 3DCAD, a $349 three-dimensional computer-aided-design program with a menu-driven interface that lets you use the mouse or keyboard as input devices. You can construct two- or three-dimensional wireframe geometry in three-dimensional space, or on an arbitrary plane, called the working plane, which you define.

You can modify, save, and combine 3-D models with other models. The program uses a universal file-exchange format, which enables you to interface other engineering programs such as numerical control and finite-element programs.

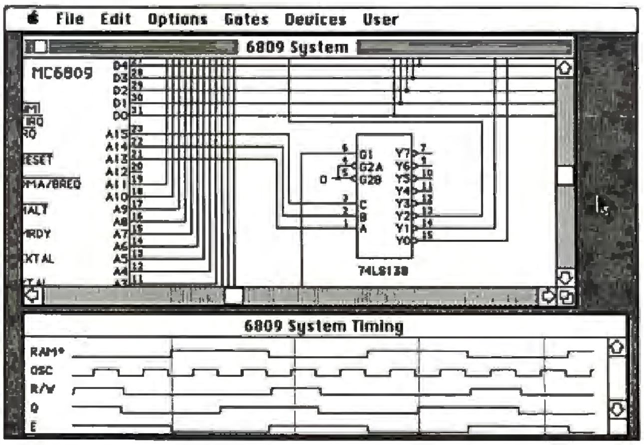
The program includes seven standard views plus user-defined rotations, intersections of geometry, or cutting sections with the working plane.

An IBM PC, XT, AT, or compatible with at least 256K bytes of RAM is required, along with MS-DOS or PC-DOS 2.0 or higher and dual floppy disk drives or one floppy and one hard disk drive. The Color Graphics Adapter, Enhanced Graphics Adapter, and Hercules Graphics Card are supported, and you can use Hewlett-Packard, Houston Instrument, or IBM pen plotters, as well as IBM or Epson dot-matrix printers. The program also supports up to 512K bytes of RAM, a math coprocessor, and Microsoft or other mouses.

For more information, contact CADPlus Systems, P.O. Box 90056, Indianapolis, IN 46290, (317) 844-7127.
Inquiry **592.**



3DCAD for IBM PCs and compatibles.



LogicWorks lets you test and design Macintosh circuitry.

Design and Test Circuits on the Mac

LogicWorks is a $159.95 program that enables you to design and test computer circuitry on the Macintosh. The program presents a circuit on-screen, and you make connection, input, and device parameter changes. A menu of standard symbols for logic devices is included, and you can also create your own. The mouse controls the functions, and you only use the keyboard to place a device or signal name on the diagram.

You can simulate circuit operation with LogicWorks, testing for design errors before they are wired into hardware. You can also see the effects of changing device parameters, and you can display them on a simulated output device or in the form of a timing diagram that graphs signal changes over time.

For more information, contact Capilano Computing Systems Ltd., P.O. Box 86971, North Vancouver, British Columbia, Canada V7L 4P6, (604) 669-6343.
Inquiry **593.**

Graphics and Statistical Analysis

PlotIT analyzes data and processes the results into a report-ready format. You can also use PlotIT to produce over 300 graphs, including three-dimensional, pie, bar, scatter, and histogram charts, according to Gracon Services.

The statistical and graphics program costs $550 and runs on IBM PC ATs, XTs, and compatibles. It requires MS-DOS or PC-DOS 3.1 or higher, 640K bytes of RAM, and a hard disk drive. For more information, contact Gracon Services Inc., 4632 Okemos Rd., Okemos, MI 48864, (517) 349-4900.
Inquiry **594.**

Measure from Lotus

Collect data from measurement instruments with Measure and send it to Lotus 1-2-3 for analysis, display, and storage. The program works as a single program with 1-2-3, according to Lotus, as it uses the same user interface and macro environment.

The price of $495 includes support for RS-232C and IEEE-488 communications buses, as well as for selected data acquisition boards.

Measure runs on IBM PCs, XTs, ATs, and compatibles with Lotus 1-2-3 version 2.0 or higher. It requires 512K bytes of RAM, MS-DOS or PC-DOS 2.0 or higher, and a hard disk.

For more information, contact Lotus Development Corp., 55 Cambridge Parkway, Cambridge, MA 02142, (617) 577-8500.
Inquiry **595.**

AutoCAD 2.5 for Apollo Workstations

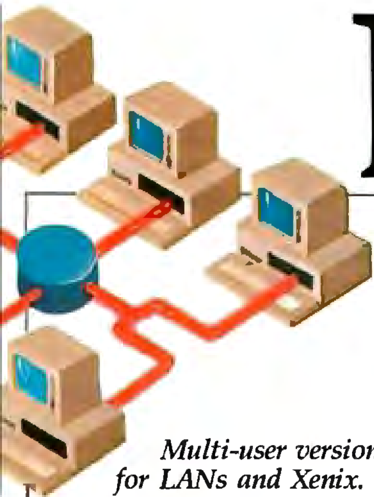
Apollo announced a version of AutoCAD for its Domain workstations. The program sells for $2750.

If you currently run Apollo's personal computer version of AutoCAD, Apollo reports that you can use its Personal Computer Interconnect to run AutoCAD on the Domain workstation.

For more information, contact Apollo Computer Inc., 330 Billerica Rd., Chelmsford, MA 01824, (617) 256-6600.
Inquiry **596.**

continued

Btrieve®



The Programmer's Choice.

Whether you're a programming pro or just beginning, there's one thing to remember when developing applications: Btrieve.

The Btrieve file manager is an alternative to all those DBMSs that promise ease of use—but deliver something far different. Like languages that take weeks to master. Performance that fizzles instead of sizzles. Programs that won't network. Of course you can write applications with these "revolutionary" packages. But someday you'll wish you hadn't.

If you know a programming language, you already have what it takes to build better applications. All you need is Btrieve.

Btrieve is the programmer's choice for file management. But you don't have to be a professional programmer to use it. With Bt ieve loaded in your PC, your programs can use simple subroutine calls to retrieve, store and update records.

Multi-user versions for LANs and Xenix. *When your applications need to network, Btrieve's multi-user versions connect you to the industry's most popular LANs: IBM PC Network, Novell Advanced Netware, or any DOS 3 network. Btrieve is also available for Xenix and multitasking operating systems such as MultiLink Advanced, Microsoft Windows and IBM Topview.*

Help is just a phone call away. *Need technical support? You've got it! Btrieve users receive 30 days of unlimited phone support at no charge. This "Direct Connect" policy is renewable for a full year at low cost. And try SoftCraft's free bulletin board for technical tips, seven days a week.*

Thorough documentation, easy implementation. *Getting started with Btrieve is easy: the manual is packed with step-by-step instructions and examples of every Btrieve function in BASIC, Pascal, COBOL and C.*

Btrieve has built-in security features and the ability to handle four billion byte files. ***And there are no royalties on Btrieve applications.***

B-tree based for high performance. *Performance is all-important, especially as your database grows. That's why Btrieve implements the b-tree file structure—the most efficient data access method known. With Btrieve your applications run fast.*

Database queries, report writing. *Add Xtrieve™ to your Btrieve applications for a fully-relational DBMS. Xtrieve's menu-driven interface lets you look up information easily—without programming. Add our report writer option to produce custom reports and forms.*

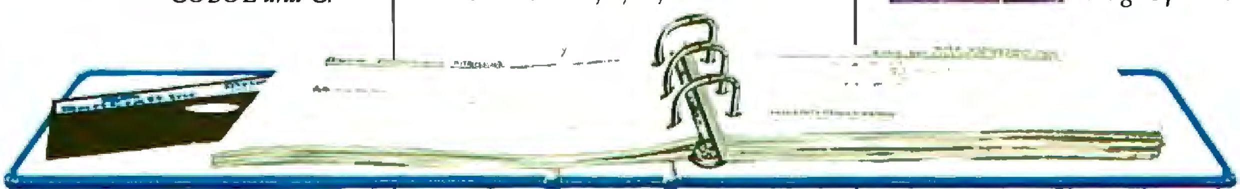
Interfaces to C, BASIC, Pascal, COBOL. *Don't waste time learning a proprietary language! With Btrieve you can use the language you know best—and immediately begin programming the right way. Over 15 language interfaces are available.*

Fault tolerant. *Btrieve insures against database disasters. Two levels of fault tolerance guarantee data integrity during accidents or power failures—no extra programming required.*

SoftCraft

P.O. Box 9802 #917
Austin, Texas 78766
(512) 346-8380 Telex 358 200

Suggested retail prices: Btrieve, $245; multi-user Btrieve, $595; Xtrieve, $245; multi-user Xtrieve, $595 (for report generation, add $145 single-user and $345 multi-user). Available from SoftCraft and selected distributors. Requires PC-DOS or MS-DOS2.X, 3.X, Xenix. Btrieve is a registered trademark and Xtrieve is a trademark of SoftCraft Inc.



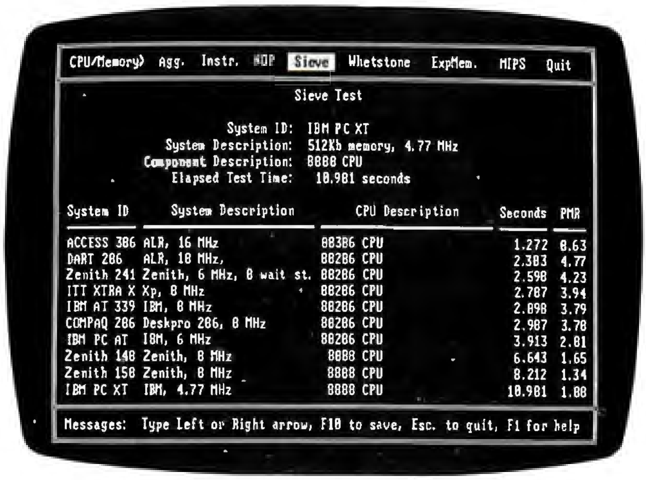
SOFTWARE • BUSINESS AND OTHER

A Measurement Tool for IBM PCs and Compatibles

Power Meter measures overall system performance using spreadsheet, database, word-processing, and program development simulations. With the tests provided, you can evaluate and compare CPUs, disk drives, and video displays on more than one system and get results in single-instance and ratio format. You can also use your own application software with Power Meter.

Pull-down menus, a database, and 10 utility functions are included. You also have the capability to generate reports, sort records, and use the help facility.

Power Meter costs $89.95 without copy protection and $49.95 copy-protected. For more information, contact The Database Group Inc., 75 South Milpitas Blvd., Suite 205, Milpitas, CA 95035, (408) 262-7766.
Inquiry **597.**



Evaluate and compare hardware with Power Meter.

Transfer Files on the Amiga

DOS-2-DOS transfers MS-DOS file types to and from AmigaDOS. It supports 3½-inch and 5¼-inch disks. The program also formats 3½-inch and 5¼-inch disks, converts ASCII-file characters, and provides WordStar compatibility.

DOS-2-DOS detects duplicate filenames and provides you with query/replace options and TYPE and DELETE commands. Full directory path names with wild cards in filenames are supported, and the program enables you to select MS-DOS and Amiga-DOS subdirectories. The program displays a sorted directory listing, and you can rename files where filename restrictions occur. The program remains resident to permit AmigaDOS disk swapping.

The disk-to-disk file-transfer program costs $55. For more information, contact Central Coast Software, 268 Bowie Dr., Los Osos, CA 93402, (805) 528-4906.
Inquiry **598.**

Sales Analysis

Sales Analysis from Computer Associates International is an addition to the EasyBusiness Systems accounting family. The decision support tool enables salespeople to plan, forecast, recognize trends, and analyze key market segments. You can use Sales Analysis alone or combine it with modules in the EasyBusiness series. Sales Analysis can retrieve information from other modules to produce statistics, detail, and summary reports. If you run Sales Analysis with the EasyPlus Windowing System, you don't have to reenter information to transfer data from one module to another.

Sales Analysis can report your accumulated sales transactions for any period of time, the accumulation limited only by disk space, according to Computer Associates.

The program costs $395 and runs on IBM PCs and compatibles with one floppy and one hard disk drive, 128K bytes of RAM, and MS-DOS or PC-DOS 2.0 or higher. You also need a printer that can print at least 132 characters per line. With the EasyPlus Windowing System, you'll need at least 256K bytes of RAM, although the manufacturer recommends 512K.

For more information, contact Computer Associates International Inc., 2195 Fortune Dr., San Jose, CA 95131, (408) 942-1727.
Inquiry **599.**

Spreadsheet for the Atari ST

PowerPlan ST has a 65,536- by 65,536-cell spreadsheet, a built-in calculator, an on-line notepad, and integrated graphics. You can display the information from the spreadsheet in pie, bar, and line charts, using the graphic capabilities.

The GEM-based program can use up to seven windows, which can simultaneously display parts of the spreadsheet or graphic displays of the data.

PowerPlan ST works with monochrome or color monitors and sells for $79.95. For more information, contact Abacus Software, P.O Box 7211, Grand Rapids, MI 49510, (616) 241-5510.
Inquiry **600.**

Atari ST Desktop Accessory

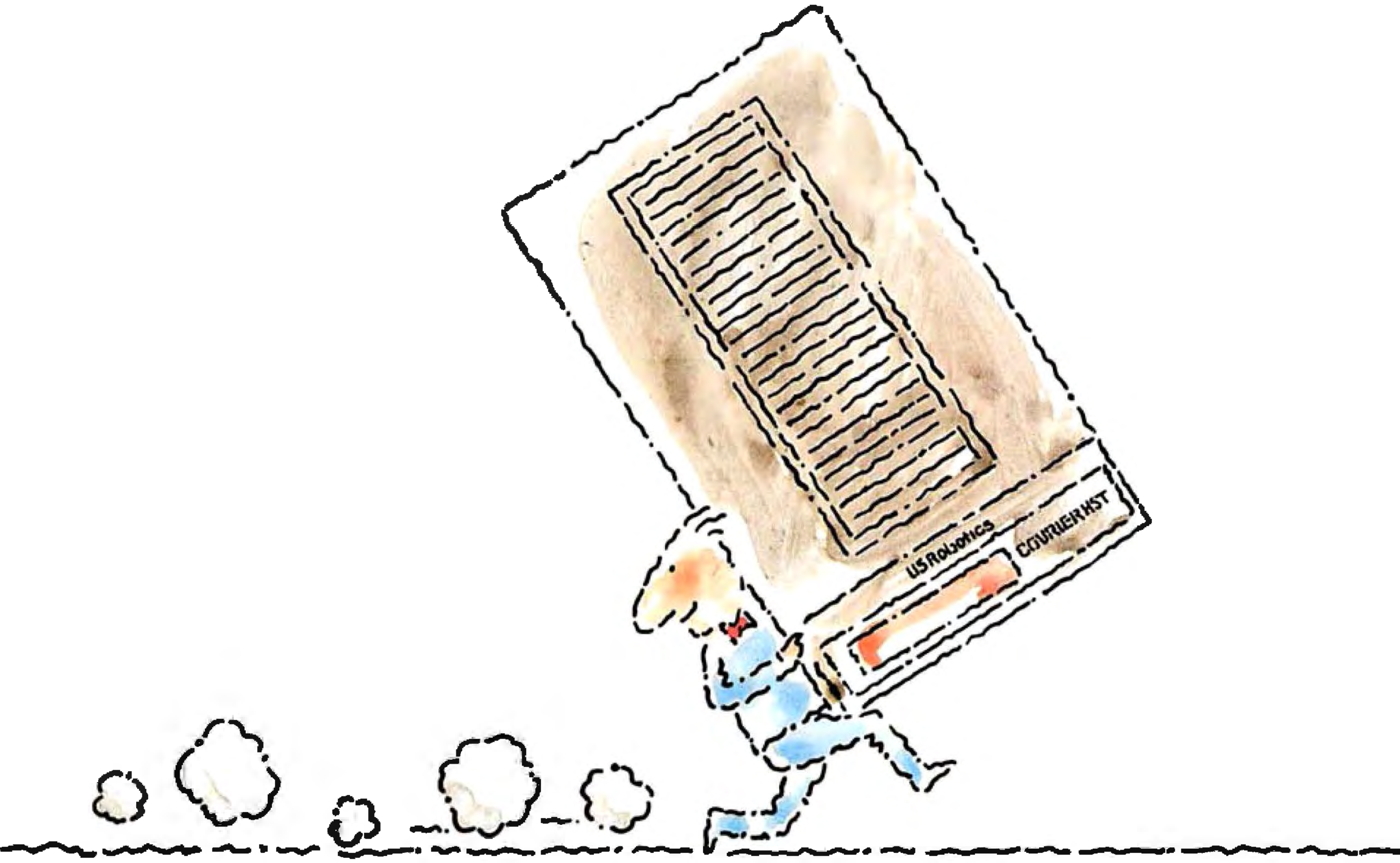
Fast is a desktop accessory that sells for $49.95 and is accessible from within any GEM program, according to Migraph. Included is ST DOS, which lets you perform the most common DOS commands. An ST editor has search, replace, block editing, and other editing features. Its card file is a database set up as an address book that you can configure. A calculator, calendar, ASCII table, and clock are also included in Fast.

The program operates in low, medium, and high resolution, and you can change many of its parameters to suit your needs.

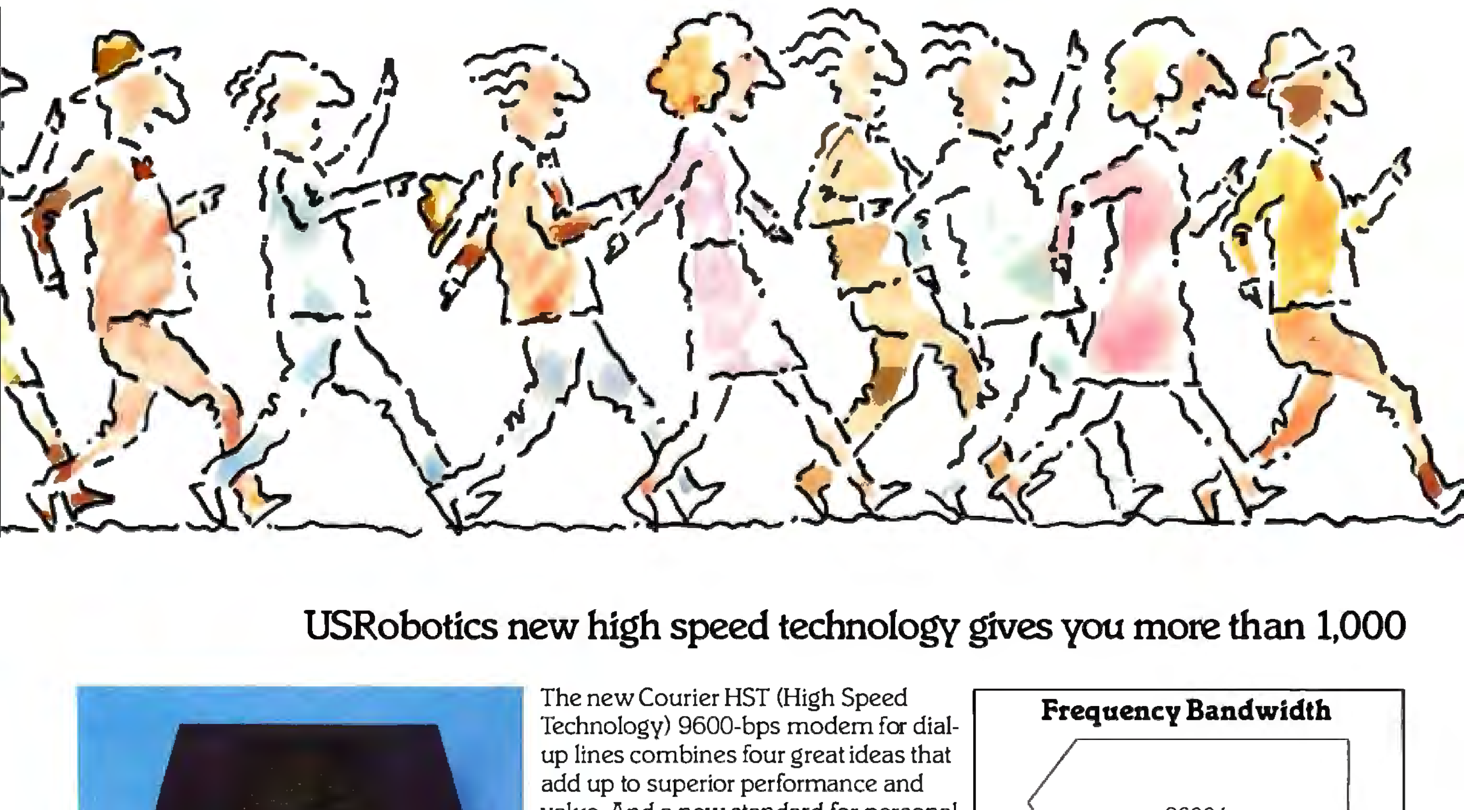
For more information, contact Migraph Inc., 720 South 333rd St., Suite 201, Federal Way, WA 98003, (206) 838-4677.
Inquiry **601.**

WHERE DO NEW PRODUCT ITEMS COME FROM?
The new products listed in this section of BYTE are chosen from the thousands of press releases, letters, and telephone calls we receive each month from manufacturers, distributors, designers, and readers. The basic criteria for selection for publication are: (a) does a product match our readers' interests? and (b) is it new or is it simply a reintroduction of an old item? Because of the volume of submissions we must sort through every month, the items we publish are based on vendors' statements and are not individually verified. If you want your product to be considered for publication (at no charge), send full information about it, including its price and an address and telephone number where a reader can get further information, to New Products Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

Get the new USRobotics Courier HST™ 9600-bps modem...



Then watch the rest of the world play catch-up.

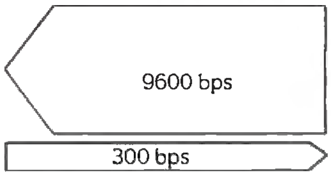


USRobotics new high speed technology gives you more than 1,000

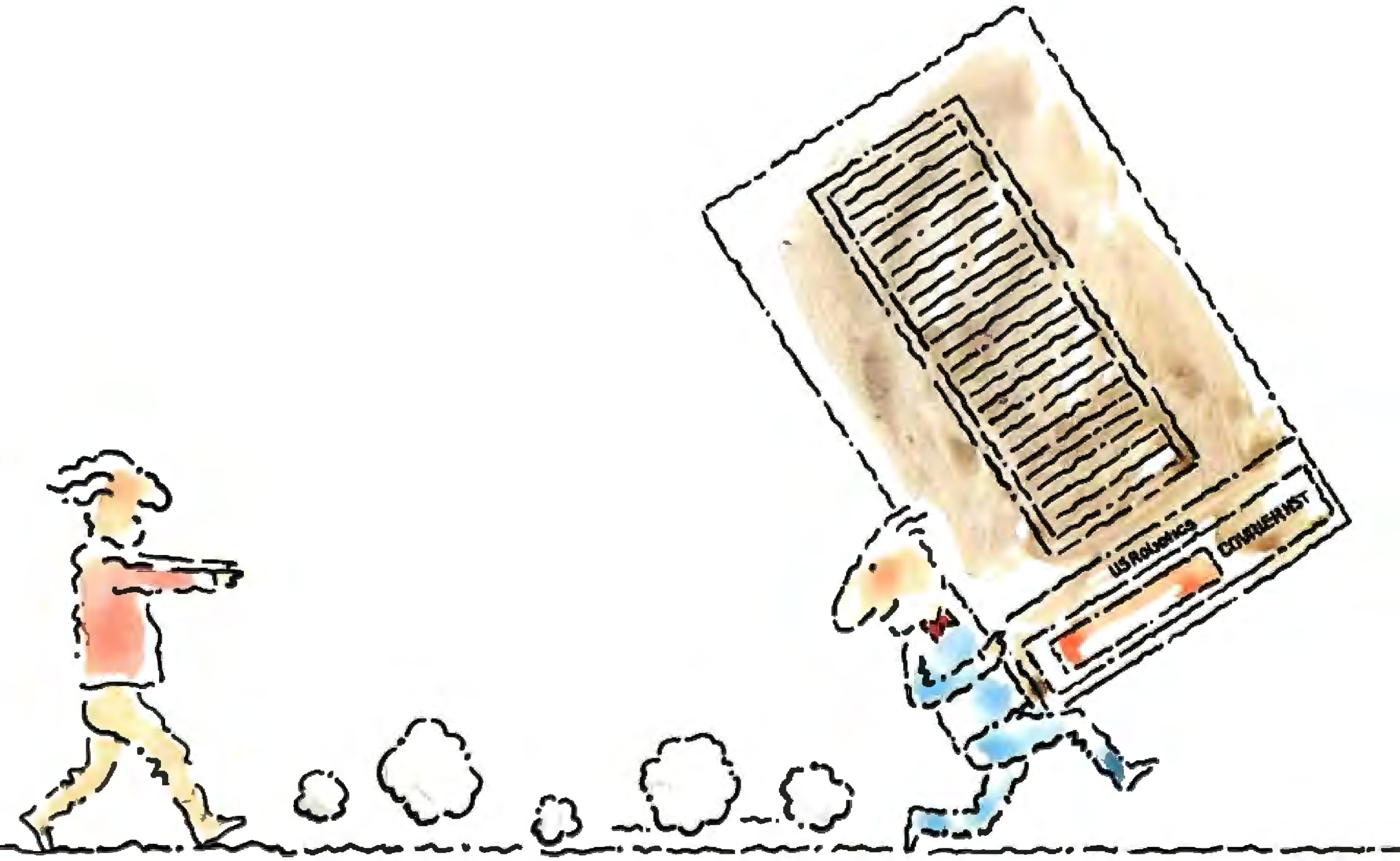
The new Courier HST (High Speed Technology) 9600-bps modem for dial-up lines combines four great ideas that add up to superior performance and value. And a new standard for personal computer data communications.

Courier HST provides simultaneous two-way communication (full-duplex) by dividing the phone line into high speed (9600-bps) and low speed (300-bps) channels—automatically assigning the high speed channel direction. This

Frequency Bandwidth



Courier HST divides the frequency bandwidth of a dial-up phone channel into non-overlapping high-speed and low-speed carriers.



characters/second on more dial-up phone lines. For less than $1,000.

asymmetrical solution avoids the problems of echo-cancelling technology or inefficient half-duplex schemes.

The most powerful data signalling technique—Trellis Coded Modulation—lets Courier HST achieve maximum speed over a much wider range of phone line conditions than 9,600-bps modems using other technology. Independent tests prove it.

A unique error- and flow-control method allows Courier HST to send up to 1,100 data characters a second over local or long distance phone connections...error-free. That's far better performance than the competition.

Courier HST gives you incredible power in a modem that's as familiar as any 2400- and 1200-bps modem. Same features, same commands and, in most cases, the same software. In fact, Courier HST automatically falls back to 2400, 1200 and 300 bps, connecting you with nearly all modems.

High speed. High accuracy. High value. And a two-year parts and service warranty.

The new high speed standard.

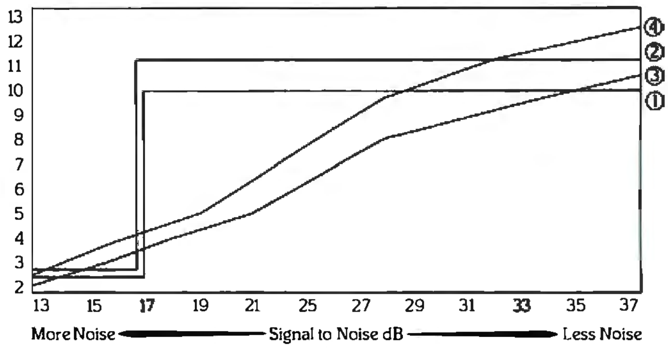
Get the USRobotics Courier HST, priced under $1,000. While the rest of the world plays catch-up, you'll already own the new standard in 9600-bps modems.

Stay ahead of the crowd for only $995.

For just a little more than you'd normally pay for a conventional 2400-bps modem, you can own the state-of-the-art. And... *you maintain the ability to communicate with almost any other modem type or speed on the market.* The new Courier HST offers you all the features you'd want in lower-speed modems as well. So why hesitate? Call us for our free brochure about Courier HST technology and advantages. And stay ahead of the crowd.

ASCII Characters	Words (5 Ch./ word)	Courier HST at 1100 cps	2400-bps Modem at 240 cps	1200-bps Modem at 120 cps
25,000	5,000	23 sec.	1 min. 44 sec.	2 min. 28 sec.
125,000	25,000	1 min. 54 sec.	8 min. 40 sec.	17 min. 22 sec.
5,000,000	1,000,000	1 hr., 15 min. 45 sec.	5 hr. 47 min. 13 sec.	11 hr. 34 min. 26 sec.
31,680,000	6,336,000	8 hours	36 hr. 40 min.	73 hr. 20 min.

Courier HST can pay for itself in just 8 hours. A 1200-bps modem takes over 65 hours longer to send the same data. At an average long-distance telephone rate of slightly more than $15 an hour (25 cents a minute), the savings equal Courier HST's $995 purchase price.



① Courier HST average bit/sec. rate in thousands.
② Courier HST average character/sec. rate in hundreds.
③ Half-duplex "Multi-carrier" average bit/sec. rate in thousands.
④ Half-duplex "Multi-carrier" average character/sec. rate in hundreds.

Courier HST transmits 1,100 characters/second at 9600-bps over much noisier phone lines than more expensive modems that use a half-duplex, "multi-carrier" modulation technique.

Call 1-800-DIAL-USR. In Illinois (312) 982-5001 or send in this coupon.

Get your FREE 8-page brochure explaining the new Courier HST and today's new high speed technology. Fill out and mail today.

Name ______________________

Title ______________________

Company ______________________

Address ______________________

City ______________________

State ______________ Zip ________

Business Phone ______________________

1/87 BY-96001

Also, to help us more accurately anticipate your needs, please answer the following questions.

1. What will be the primary use(s) for your modem?
(Please circle all that apply.)
A. File transfer between computers.
B. Electronic mail.
C. Access public database services (e.g. CompuServe).
D. Communicate between data terminal and mainframe or mini computer.
E. Operate Bulletin Board System.
F. Other (Specify) ______________
2. Please tell us the brand name and model of the microcomputer or data terminal with which you will use a modem:
____
3. Please tell us the name and version number, if known, of the telecommunications software you will use with a modem:
____
4. Circle any of the following products you currently own or use.
A. Modems for standard voice grade lines data rate: ________ brand: ________
B. Modems for leased or dedicated lines data rate: ________ brand: ________
C. Short haul, limited distance modems brand: ______________
D. Rackmounted modems (brand): ______________
E. Synchronous modems for connection to IBM system (brand): ______________
F. Multiplexers (brand): ______________
G. Local area network (brand): ______________
5. Who in your organization is responsible for data communications equipment purchase decisions, if other than yourself?
Name ______________ Title ______________
6. Would you also like more information on:
Courier 2400e ________ Courier 2400 ________
Rackmount 30 Modular Modem System ________
IBM PC Plug-In Modems ________

USRobotics™
The Intelligent Choice in Data Communications
8100 McCormick Blvd., Skokie, Illinois 60076.

EVENTS AND CLUBS

January 1987

EVENTS

Inside the IBM PC XT, AT, Orange County, CA, and Houston, TX. Northeastern University, State-of-the-Art Engineering, New England Regional Technology Center, 370 Common St., Dedham, MA 02026, (800) 521-5260; in Massachusetts, (800) 842-4900 or (617) 329-8775. *January*

1987 International Winter Consumer Electronics Show, Las Vegas, NV. Consumer Electronics Shows, 2001 Eye St. NW, Washington, DC 20006, (202) 457-8700. *January 8–11*

Interfacing Sensors with the IBM PC, Madison, WI. E. K. Greenwald, Department of Engineering Professional Development, University of Wisconsin-Madison, 432 North Lake St., Madison, WI 53706, (608) 262-0573. *January 12–14*

Information Systems Security (INFOSEC), Los Angeles, CA. UCLA Extension, P.O. Box 24901, Los Angeles, CA 90024, (213) 825-3344. *January 12–16*

PC FAB Expo '87, Orlando, FL. PMS Industries, 1790 Hembree Rd., Alpharetta, GA 30201, (404) 475-1818. *January 13–15*

Multi '87, San Diego, CA. The Society for Computer Simulation, P.O. Box 17900, San Diego, CA 92117, (619) 277-3888. *January 14–16*

InstrumentAsia 87, Singapore. Sponsored by the Instrumentation and Control Society. Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, (201) 652-7070. *January 14–17*

PTC '87: Pacific Telecommunications Users: A Spectrum of Requirements, Honolulu, HI. Pacific Telecommunications Council, 1110 University Ave., Suite 308, Honolulu, HI 96826, (808) 941-3789. *January 18–21*

Computer Graphics: A Comprehensive Introduction, Washington, DC. Yolande Amundson, Manager Education Services, 5800 Hannum Ave., P.O. Box 3614, Culver City, CA 90231, (800) 421-8166; in Canada, (800) 267-7014. *January 20–23*

Winter 1987 USENIX Technical Conference, Washington, DC. USENIX Association, Conference Office, 16951 Pacific Coast Highway, P.O. Box 385, Sunset Beach, CA 90742, (213) 592-3243. *January 21–23*

Computer Animation Using Video Techniques, New York, NY. Gideon Nettler, 80-40 Lefferts Blvd., Kew Gardens, NY 11415, (718) 849-6313 or 441-4054. *January 22*

Mathematical Modeling and Digital Computer Simulation of Engineering and Scientific Systems, Los Angeles, CA. UCLA Extension, P.O. Box 24901, Los Angeles, CA 90024, (213) 825-3344. *January 26–30*

Advanced Semiconductor Equipment Exposition & Technical Conference, Santa Clara, CA. ASEE'87, Cartlidge & Associates Inc., 1101 South Winchester Blvd., Suite M259, San Jose, CA 95128, (408) 554-6644. *January 27–29*

Computer Graphics New York '87, New York, NY. Exhibition Marketing & Management Inc., 8300 Greensboro Dr., Suite 690, McLean, VA 22102, (703) 893-4545. *January 28–30*

Conference on Desktop Communications, San Francisco, CA. The Seybold Group Inc., 20695 Western Ave., Torrance, CA 90501, (213) 320-9151 or (408) 297-0888. *January 28–31*

Computers & Reading/Learning Difficulties, San Francisco, CA. Educational Computer Conferences, Dept. N, 1070 Crows Nest Way, Richmond, CA 94803, (415) 222-1249. *January 29–31*

Sixth Annual Alabama Council for Computer Education Convention, Mobile, AL. Dr. Rick Daughenbaugh, College of Education, University of South Alabama, Mobile, AL 36688, (205) 460-6201. *January 29–31*

If you send notice of your organization's public activities at least four months in advance, we will publish them as space permits. Please send them to BYTE (Events and Clubs), One Phoenix Mill Lane, Peterborough, NH 03458.

CLUBS

AI Today, Artificial Intelligence Research Laboratories, 104 Frame Rd., Elkview, WV 25071, (304) 965-5548.

AMuseNews, New York Amiga Users Group, 151 First Ave., Box 182, New York, NY 10003, (212) 460-8067.

N.Y.U. Medical Center BBS, James A. Mihalcik, M.D., 300 East 39th St., New York, NY 10016. News for medical scientists. BBS: (212) 889-7022.

IBM PC User Group Österreich e.V., Postfach 40, A-1225 Wien, Austria. Also interested in interaction with other groups worldwide.

Heinz Dinter on Desktop Publishing, P.O. Box 558250, Miami, FL 33155, (305) 274-7440.

Systems Librarian and Automation Review, 27921 Lindvog Rd. NE, Kingston, WA 98346, (206) 297-2634.

Where It's Att, **First Attache/2001 User Group newsletter**, 1827 Haight St., Suite 16, San Francisco, CA 94117-2791. Newsletter on disk.

J-BUG ST, Jackintosh Boston Users Group newsletter, The Boston Computer Society, One Center Plaza, Boston, MA 02108. For Atari ST users.

Nevada Programmer's SIG, 4530 Meadows Lane, Las Vegas, NV 89107, (702) 870-1534.

Dover Commodore User's Club, P.O. Box 1313, Dover, DE 19901.

Connecticut IBM PC Users Club, John McGinley, P.O. Box 291, New Canaan, CT 06840-0291, (203) 762-0229.

Association of Small Computer Users, P.O. Box 14151, Atlanta, GA 30324. For IBM System 34/36/38 and PCs.

Atari Computer Club of the Palm Beaches, Jim Woodward, 605 Southwest First Court, Boynton Beach, FL 33435.

RainForest BBS, P.O. Box 841422, Pembroke Pines, FL 33084, (305) 434-4927. ■


COMPUTER INNOVATIONS
C86 PLUS
C COMPILER
C86 PLUS REFERENCE MANUAL
SUPREMACY.

SUBSTANTIATED.

SUPREMACY

It's a bold claim. A claim we're prepared to stake our reputation on. And at Computer Innovations, we've always taken our reputation very seriously.

It's no industry secret that the competitive C Compilers are at the end of their optimization cycle — they're just about as good as they are going to get. C86PLUS begins where everybody else has left off. It's an entirely new technology based on artificial intelligence and advanced compiler design techniques. Designed with the serious programmer in mind, C86PLUS provides the ultimate development environment, matching unparalleled execution speed with a host of productivity features.

FAST EXECUTION

- 20% faster than Microsoft C, version 4.0
- 70% faster than existing C86, version 2.3
  (timings based on the classic sieve benchmark)

ANSI C COMPILER FEATURES

- Register variables
- Structure assignment
- Function prototypes
- New type modifiers
  - -near
  - -far
  - -signed
  - -const
  - -volatile
- Long double 80 bit floating-point
- Enumerator data types (enums)
- Extended preprocessor capabilities

FULL CONTROL OVER COMPILATION ENVIRONMENT

- Small, Medium, and Large memory models
- 8086/80186 and 80286 code generation options
- In-line 8087/80287 floating point
- 8087/80287 auto detect emulator
- Source level debugger support
- Wild-card compilation
- Make utility
- ROMable code
- Linkable with macro assembler output
- Intel-standard OMF object files
- Optional assembly language output
- Warning level control

EXTENSIVE FUNCTION LIBRARIES FOR INCREASED PRODUCTIVITY

- Over 250 library functions
- Full ANSI C library
- Functional equivalents to most UNIX System V libraries
- Shared file and network support
- Low-level machine access functions
- IBM ROM BIOS support routines
- Fully compiled small, medium and large model libraries
- C library source code
- Run-time start-up source code
- Source code librarian
- Object code librarian

MICROSOFT COMPATIBILITY

If you're a current Microsoft user, we invite you to consider this simple point. C86PLUS will recompile most applications developed using MS-C without changes to your source code. You'll find that your application runs much faster.

PROVEN EXPERIENCE

In 1981, Computer Innovations and its founder, George Eberhardt, revolutionized the DOS programming world with the introduction of the first C Compiler for the PC called C86. Today, C86 boasts a satisfied and loyal user base of over 20,000 programmers worldwide. C86PLUS represents an extension of this expertise and reputation. It's backed with more than a decade of intensive research and development.

PROVEN SUPPORT

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ASK BYTE

Conducted by Steve Ciarcia

IBM Typewriter Interfaces
Dear Steve,

I have one of the original IBM Selectric mag card machines. It is still functioning and putting out beautiful letter-quality print. Do you know of an interface that would allow me to use it with my IBM PC as a printer?

Marley Kittleman
Greenville, MS

Ron's Electronics (N5009 Sunset Vista, Onalaska, WI 54650) sells and installs computer interfaces for IBM typewriters. Their telephone number is (608) 783-5341. Have the model number of your unit available when you call.—Steve

Game Library on a Disk
Dear Steve,

I have several Infocom games, and I am wondering if you know of a way to put more than one game on a disk. I could then use a menu to call up the game I wanted to play. This would be a lot easier on my pocketbook than buying several disks. Of course, my question does not pertain to Infocom games only; it would be nice to keep games from several companies on a single disk.

Feliberto Escobar III
Robstown, TX

Infocom's game programs save all game data to disk under a single filename. This normally precludes saving more than one game to a given disk. To accomplish your goal, you must ensure that each game is saved to disk under a different filename. This will involve changes in the way each program functions.

Your first step will be to eliminate copy protection used by the programs; for this purpose, contact Computist, P.O. Box 110846, Tacoma, WA 98411. Their publications, called The Book of Softkeys, Volumes 1 and 2, *give instructions for removing the protection from numerous popular programs, including many of the Infocom games. Once you've gotten the program onto a standard, nonprotected disk, you can alter it to suit your needs. While it is not illegal to copy and modify legitimately obtained commercial software for your own personal use, it is illegal and unethical for you to sell, give away, or otherwise distribute such software. Refer to the software licensing agreement of each package for specific details.*

Don Lancaster, in Enhancing Your Apple II and IIe, Volumes 1 and 2, *(Howard W. Sams, 1984), gives instructions for the "tearing" method of disassembling memory-resident programs and creating source code. You can utilize his methods for determining how the programs function and then make the changes you desire. Another book by the same author might also prove useful:* Assembly Cookbook for the Apple II-IIe, *(Howard W. Sams, 1984).*

Keep in mind that what you want to do may be more trouble than it's worth. The process, however, can be very educational, and the value of what you learn could easily make the effort worthwhile. —Steve

Applesoft Compilers
Dear Steve,

After programming in Applesoft BASIC for several years, I have become frustrated by its lack of speed. As a result, I have been searching for a high-quality inexpensive Applesoft compiler. Unfortunately, all of the ones I have looked at are either too expensive or no longer available. Do you happen to know of any users groups that might have such a program, or even better, a compiler that's in the public domain? Otherwise, I wonder if you could recommend a commercially available Applesoft compiler?

J. M. Maing
Honolulu, HI

At one time there were several compilers for Applesoft available from commercial software houses, but there seem to be very few left. Microsoft's TASC compiler has been recommended as a good one. It is currently being advertised by a number of mail-order firms for about $100.

The August 1986 issue of Nibble *magazine contains a very favorable review of a product called Micol BASIC (Micol Systems, 9 Lynch Rd., Toronto, Ontario, Canada M2J 2V6, (800) 268-1121), which consists of an editor/compiler/run-time system capable of compiling existing Applesoft programs. It will also compile program text written in a more modern, structured form using the system editor. At its advertised price of $49.95, the Micol system seems to be a bargain, especially in light of the good review.*

Another possibility that you might consider is the use of a product called Macrosoft, a compiler available from Nibble *(MicroSPARC Inc., 45 Winthrop Street, Concord, MA 01742, (617) 371-1660). Although it doesn't compile Applesoft, it does accept a BASIC-like source file and compile it to 6502 machine code using the* Nibble *assembler. Current price is about $50 without the assembler, $100 with.*—Steve

XT Questions
Dear Steve,

I have two questions regarding IBM PC XT operation.

First, how can I determine the presence or absence of an 8087 coprocessor?

Also, I have a Hercules Graphics Card in my PC XT. It can display both text and graphics simultaneously. Are they kept in different areas of display RAM and displayed by some switching method, or are text and graphics in the same memory area so that the display is simply bit-mapped?

If the answer is the latter case, then how is the character generator on the board distinguishing between graphics pixels and characters?

Zafar Mansoor
San Jose, CA

A method of testing for an 8087 or 80287 in assembly language programs

continued

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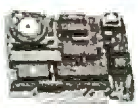

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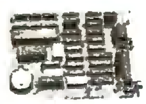

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y 225

was given in the September 1985 issue of Dr. Dobb's Journal *in Ray Duncan's "16-Bit Software Toolbox" column. Briefly, the procedure involves forcing a reset of the 8087 with the* finit *command and checking the 8087 control word value. If it is 03FF hexadecimal or if the upper byte is 3 in the 80287, then the coprocessor is present.*

Most, if not all, high-level language compilers that use the 8087 produce executable programs that perform this test automatically at start-up. If the language you are using does not perform this test, you will need to either write the above code into an assembly language subroutine for your program to call, or write an assembly program to execute as part of the loading procedure for your program.

Text on the graphics screen with the Hercules Graphics Card is apparently done about the same way it is with the IBM Color Graphics Adapter. That is, the characters are bit-mapped into the graphics screen buffer by the video controller's character generator.

When in text mode, a character and its attribute use two bytes in the text screen buffer and can be read as two data bytes by programs, so actual characters can be read off the screen. In graphics mode, however, you can read only pixel data (on or off), making it very difficult or impossible to read characters by value. That is, you can copy a character to another location pixel by pixel, but if you can determine the value at all (e.g., is it a V or a T?) it is only with a great deal of difficulty.

The screen buffer addresses for the Hercules card (in segment:offset notation) are

Text screen—B000:0000 to B000:0FFF (4K)
Graphics page 0—B000:0000 to B000:7FFF (32K)
Graphics page 1—B800:0000 to B800:7FFF (32K), where all values are in hexadecimal.

When the card is in graphics mode, all text and graphics data are mapped into screen 0 and simultaneously displayed by default. You can switch the screen display to page 1 by setting bit 7 of the display mode control to 1.

This allows the programmer to write applications that display one picture while a second one is being built on the other page (out of sight) and to swap pages to change the display when the second picture is complete. This is often a good animation technique.—Steve

Inside 1-2-3

Dear Steve,

I am a systems analyst/design engineer with a company specializing in health care management software. Our applications are heavily database-oriented. We have a minicomputer-based version of our system and a microcomputer-based version.

All our microcomputer users (using IBM PCs or compatibles) have clamored for an interface to Lotus 1-2-3. I called Lotus and the operator told me that I wanted "Technical Marketing." I was connected to that department but no one was there. I decided to write instead.

I wrote and asked for their policies on such interfacing and for guidelines of any sort for vendors interested in developing interfaces to 1-2-3.

I never got a reply. I posted a query to USENET on the off chance someone out there could help. Not even a murmur. I really don't want to have to pick worksheets apart with some low-level bit-twiddler. Do you know of a published guide to 1-2-3 file structure? I am desperate enough to investigate DIF for-

continued

Inquiry 418

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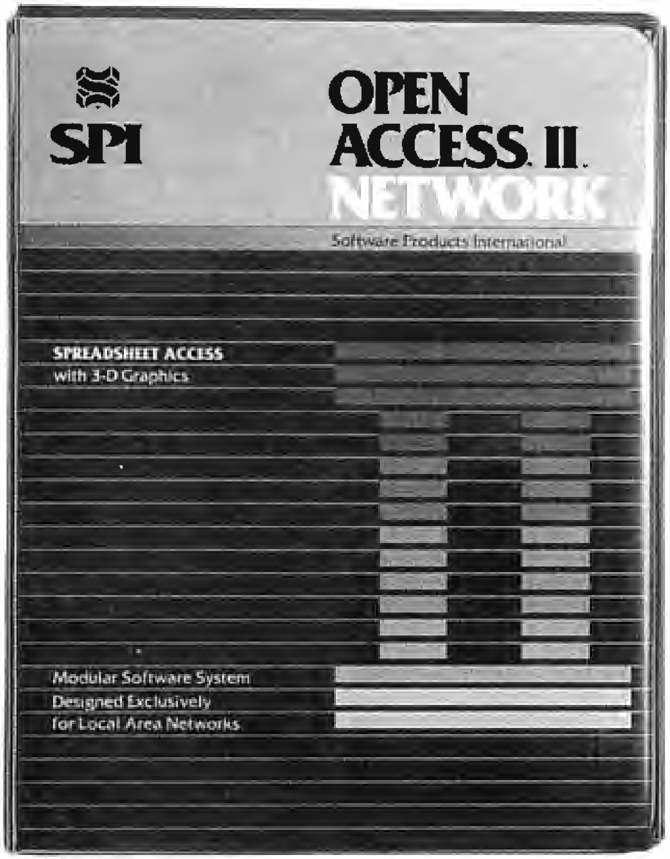

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mat as a possible solution, but I really would like to build 1-2-3 worksheets directly.

Brendan F. Hemingway
New Haven, CT

You're in luck! There's a book covering just what you need. Ask your local bookstore for File Formats for Popular PC Software: A Programmer's Reference *by Jeff Walden (John Wiley and Sons, 1986).*

This gives a byte-by-byte breakdown of what goes into making up a 1-2-3 spreadsheet file for releases 1A and 2. It also includes several other program file formats, including SuperCalc and Symphony. It's even got the dope on DIF!

Lotus used to publish a book that gave their file formats, and I'm surprised they didn't tell you about it. It explains things a little better than Jeff Walden's book, so it's worth a shot. Try calling Lotus back and asking for the worksheet file format book they put out in 1984. If they still claim no knowledge, try writing to:

Lotus Development Corporation
Worksheet File Format
161 First Street
Cambridge, MA 02142
(617) 492-7171

The above is the address you were supposed to use to report bugs in the book, so there may be someone there that knows how to obtain a copy.

Actually, depending on what you want to do, it may not be necessary for you to build a spreadsheet file directly. Lotus 1-2-3 release 1A can import data, and 1-2-3 release 2 can do a much better job. If your program can produce a straight ASCII file, you might be able to distribute a set of 1-2-3 macros to do the job. That would keep open the option of importing the same file into dBASE III or whatever other programs your customers may be using without your having to cook up a unique file format for each one.

Take a look at the File Import Text and File Import Numbers commands in release 1A and 2, as well as the Data Parse command in release 2. The requirements on the ASCII input file aren't too stringent and it's bound to be a lot easier than encoding the data as a spreadsheet file.
—Steve

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One-Size-Fits-All Computer?

Dear Steve,

In light of the NEC V20 and V30 chips and the rumored NEC chip (that may well run everything from Z80 to 80386 software) plus the announced Atari-to-IBM compatibility box, I wonder if you have any plans for a single computer that would run both the SB180/Z-System and MS-DOS?

Also, it would be wonderful to be able to put any disk of any format in a drive (of the correct size, of course) and just use it; by having the system decide which format to use, we would not be bound by any one manufacturer's dictates, successes, or failures.

Ian A. Park
Highlands, NJ

I presently have no plans for a combination Z-System/MS-DOS computer.

Although total compatibility is a nice idea, it's not very probable, given the large number of hardware and software manufacturers. Things are improving, though: Software products like Uniform and Media Master both allow many CP/M, Z-System, and MS-DOS machines to read, write, and format disks from other machines. Here's where you can get these products:

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MicroSolutions
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DeKalb, IL 60115
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—Steve

The Speed of Light

Dear Steve,

I use the Home Run computer to turn on lights when the computer detects movement in the appropriate area of the house. It takes about 2 seconds for the light to go on once the sensor switches. Is there any way to speed that up? I am halfway down the stairs before the stairway light comes on. I think descending into darkness is kind of exciting, but my wife. . .

Bruce Winter
Rochester, MN

You don't indicate whether you're using direct control or a BSR-type method, but from the time period you describe, I suspect that you have some version of BSR-type controller. If this is the case, much of the time is being lost in the data transmission to the lamp control and you can do little to speed that up.

My approach to this problem would be to reposition the sensors to allow them to trigger earlier. If this is a problem because of false triggering, then multiple sensors and the requirement of two closures to activate the light might be a solution.—Steve

Serial ADC

Dear Steve,

I would like to know if you are aware of any books or articles dealing with analog-to-digital converter (ADC) circuits that interface via an RS-232C port. Most of what I have run across seems to assume that access to the computer bus is available. Since I am at the neophyte level when it comes to hardware, I am reluctant to hook anything to my NEC laptop or my Sanyo desktop by way of the internals. They both have an RS-232C port that seems handy and—if the ADC board is well protected—less risky.

My dream board would interface via an RS-232C port and have several DAC outputs and several ADC input channels.

David Fischer
Ann Arbor, MI

There have been many articles describing A/D conversion with serial interfacing. Two such articles are

"DAC/UART Interface Circuits Aid Serial Data Processing" by Wes Freeman, EDN Magazine, *February 3, 1983, pages 133-143.*

"Analog-to-Digital Conversion" by Robert F. Tinker, TERC Newsletter, *Fall 1981.*
—Steve

Finding DAAs

Dear Steve:

In your "Build the Touch-Tone Interactive Message System" article in the March 1985 BYTE, you mention that registered data-access arrangements (DAAs) are available from various sources, including the phone company.

Since you describe only the CH1810 from Cermetek, I'd very much appreciate knowing the names and addresses of other manufacturers who also sell DAAs.

Jim Groff
Morgan Hill, CA

In addition to Cermetek and the local telephone company, you can purchase DAAs from the following companies:

Glasgal Communications Inc.
207 Washington Street
Northvale, NJ 07647
(201) 768-8082
(714) 662-0252/6, Los Angeles office
(415) 838-7550, San Francisco office

Racal-Milgo
1601 North Harrison Pkwy.
Sunrise, FL 33323
(305) 475-1601

Racal-Vadic
1525 McCarthy Blvd.
Milpitas, CA 95035
(408) 946-2227

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734
(602) 746-1111

A phone call to any modem manufacturer should give additional leads to manufacturers of DAAs. All major standalone modems contain this circuitry.
—Steve

Digital Sound Synthesis

Dear Steve,

I am a musician and I am interested in the possibility of building a synthesizer to interface with my Leading Edge PC. Have you ever printed an article on building such a project? If you haven't, could you clue me in to somewhere I could find information about digital sound synthesis?

continued

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I have been unable to find any helpful information on the subject. It really irks me to have a powerful computer with 640K bytes of of memory and not be able to use it for my music.

Paul Edson
Fairfax, VA

There hasn't been a Circuit Cellar project that deals with your question. However, the June 1986 issue of BYTE *dealt with this subject in some detail.*

There are various ways to connect a computer to musical instruments (e.g., synthesizers). One of the fastest-growing methods is the MIDI (musical instrument digital interface), which was described in that issue. If you want to build your own synthesizer and interface a microcomputer to it, you might consult the three books listed below:

Musical Applications of Microprocessors, 2nd edition, *Hal Chamberlin (Hayden Book Co., 1985).*

Computer Music: Synthesis, Composition, and Performance, *Charles Dodge and Thomas A. Jerse (Schirmer Books, 1985).*

Foundations of Computer Music, *Curtis Roads and John Strawn (Oxford University Press, 1985).*
—Steve

Electronics 101

Dear Steve,

I would like to learn how to build computers such as your SB180, but I have no electronics training. What books could I get about building computers and circuit boards?

Also, how do you interface the Term-Mite to the SB180?

Mark DeCoste
Columbus AFB, MS

A good source of information on general construction practices for electronics, along with a wealth of other reference information on electronics, is the ARRL Handbook for the Radio Amateur. *This resource is available from the American Radio Relay League, Newington, CT 06111. Good home-study electronics courses are also available from McGraw-Hill and Heathkit.*

You interface the Term-Mite to the SB180 by connecting the serial interfaces of the two boards with a cable described in the manuals of both. You must also set the communication parameters of the boards to the same value. Finally, to make the system fully functional you must connect a keyboard and a video monitor to the Term-Mite board.—Steve ■

NUMERICAL RECIPES: THE ART OF SCIENTIFIC COMPUTING
William H. Press, Brian P. Flannery, Saul A. Teukolsky, and William T. Vetterling
Cambridge University Press
New York: 1986
ISBN 0-521-30811-9
818 pages, $39.50

65816/65802 ASSEMBLY LANGUAGE PROGRAMMING
Michael Fischer
Osborne/McGraw-Hill
Berkeley, CA: 1986
ISBN 007-881235-6
684 pages, $19.95

PROGRAMMING THE 65816 INCLUDING THE 6502, 65C02, AND 65802
David Eyes and Ron Lichty
Prentice Hall Press
New York: 1986
ISBN 0-89303-789-3
607 pages, $22.95

80386/80286 ASSEMBLY LANGUAGE PROGRAMMING
William H. Murray III and Chris H. Pappas
Osborne/McGraw-Hill
Berkeley, CA: 1986
ISBN 007-881217-8
548 pages, $19.95

Numerical Recipes: The Art of Scientific Computing

Reviewed by Joseph Alper and Mark Bridger

Anyone who relies on scientific computing has, at one time or another, needed mathematical procedures commonly called "numerical methods." These procedures range from finding the inverse of a matrix to solving a set of first-order differential equations or integrating some complicated function not found in standard integral tables. Although some of the books on numerical analysis provide listings of sample programs to carry out these procedures, programmers often choose to write their own routines or use one of the commercially available packages of subroutines.

Organization

Both practices have their pitfalls. Unless you are an expert in numerical analysis, the subroutines you write tend to have various shortcomings. They may be inefficient, consuming a great deal more computer time than is necessary. They may be inaccurate because of limitations in the (finite) precision of the machine or deficiencies in the algorithms. The subroutines can even fail completely, and for a variety of reasons. They may not take into account those special cases for which the general method does not work, or they may be unstable—for example, two sets of input data that differ in a seemingly insignificant way can give rise to radically different "solutions."

Numerical Recipes by William H. Press et al. explores these difficulties. For each mathematical problem treated in the book, such as the solution of ordinary differential equations, the authors present the various numerical methods that have been developed to solve these problems. They explain these methods in enough detail so that you can understand both how and why the methods work and learn how to choose which method to use for a particular problem. In addition, the authors give their own evaluations and advice concerning the merits of various competing methods. They then provide both the FORTRAN and Pascal code for each of the subroutines discussed. Thus, although the routines listed in the book can be copied and used as "black boxes," the authors have provided the information for intelligent choice as well as possible modification.

Scope

Numerical Recipes is remarkably complete. In almost 700 pages of text it covers linear algebraic equations, interpolation and extrapolation, integration of functions, evaluation of functions, special functions, random numbers, sorting, root finding, extrema of functions, eigensystems, Fourier transform methods, statistical analysis and modeling of data, and ordinary and partial differential equations. It contains many more routines than many commercial mathematics packages and so provides the user with a great deal of flexibility for handling a variety of problems. The emphasis is clearly on techniques used in the physical sciences and mathematics.

Because the methods and programs in this book are designed

continued

ILLUSTRATION BY TOM CENTOLA

to be used at the research level, the book is not elementary. To understand it, you should be familiar with linear algebra and intermediate or preferably advanced calculus. You'll also need a working knowledge of either FORTRAN or Pascal. In addition, although the authors assume no previous familiarity with the methods they discuss, you'll find that a background knowledge of numerical analysis and its applications will enable you to read the book as it was meant to be read.

The authors' aim is to get you to understand and appreciate the "recipes" as much as they obviously do. Their comments and advice about the merits and demerits of the various methods are of particular value to the nonexpert who often must decide between competing numerical algorithms. Their sense of humor, which surfaces sporadically and unpredictably throughout the text, is refreshing in a subject regarded by outsiders as a necessary but tedious interruption of their primary concerns. Even if you don't have a particular problem in mind, it's enjoyable to browse through the book until your attention is caught by some topic you'd heard about but never had the opportunity to read up on: Gaussian quadrature, perhaps? Chebyshev approximation? or maybe fast Fourier transforms?

Some Opinions

We particularly liked the chapter on ordinary differential equations. The emphasis on systems as opposed to single equations was especially useful, and the algorithms were very cleanly implemented and explained. Although they devote a section to predictor corrector methods, the authors "predict" that these methods have had their day and that Runge-Kutta (for convenience) or Bulirsch-Stoer (for precision) methods will dominate in the future.

On the other hand, we felt that the material on spline interpolation was a bit incomplete—especially in view of the importance of splines and Bézier curves in computer graphics.

The only general complaint we have concerns the lack of a detailed discussion of the use of FORTRAN double-precision numbers to increase accuracy. Problems caused by round-off error are covered in the introductory chapter and in the discussion of the individual subroutines where these errors can arise. However, double precision is used in only a few of the routines, and little or no explanation is given about why it appears in those and not in others. For scientists who use double precision in all their programs just to be safe, some general guidelines for deciding when double precision is necessary would be useful.

Supplementary Books and Disks

As a means of making the book even more useful, all of the subroutines listed in the book are available both in FORTRAN and in Pascal on 5¼-inch double-sided, double-density floppy disks ($19.95 each). They operate on DOS 2.0/3.0 on the IBM PC, XT, AT, and compatible machines. In addition, the authors have written two example books (one version in FORTRAN and the other in Pascal, each $18.95) that contain a short driver program for each of the subroutines listed in the text. Among these examples are programs that use the random-number-generator subroutines to evaluate pi (by comparing the area of a square to that of its inscribed circle) and a program that solves the differential equation whose solutions are the Bessel functions and compares the numerical solutions found thereby with the values of the Bessel functions calculated using an explicit routine from another section in the book. These example programs are also available on disks in both FORTRAN and Pascal versions.

Note that the FORTRAN routines are intended for FORTRAN 77 implementation and will work "as is" with the Microsoft FORTRAN 77 or IBM Professional FORTRAN compilers (MS-DOS). The Pascal is "plain vanilla" and will work "as is" with

continued

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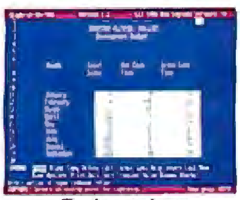

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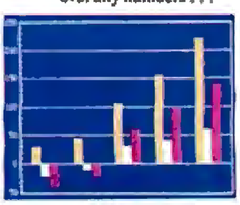

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Turbo Pascal. The routines are also available for the UCSD p-System, for the Macintosh (Pascal), and on tape, for the DEC VAX.

These supplements to the text are quite useful for anyone who plans to use even a few of the subroutines. The example book makes it clear how to incorporate the subroutines into your own application program. We have tested a few of these examples, and they work very well indeed.

In Sum

The authors are generous in their scholarship. They have gleaned material from scores of texts as well as a number of recent papers, which are included in the references at the end of each section. While no text can compete in timeliness with the current periodical literature, *Numerical Recipes* is an excellent introduction to contemporary numerical methods.

Joseph Alper is a professor of chemistry at the University of Massachusetts (Boston, MA 02125). Mark Bridger is an associate professor of mathematics at Northeastern University (Boston, MA 02115).

65816/65802 Assembly Language Programming
and
Programming the 65816 Including the 6502, 65C02, and 65802

Reviewed by Jesse D. Sheinwald

When the Western Design Center in Mesa, Arizona, developed the 16-bit version of the 6502, the 65816, and its brother, the 65802, it was to take advantage of certain strengths. Both the 65816 and the 65802 processors have the same enhanced instruction set, additional addressing mode capabilities, and code compatibility with the 6502 and 65C02. The difference between the 65816 and the 65802 is the address bus; the 65802 has a 16-bit address bus that allows it to address 64K bytes of memory, and the 65816 has a 24-bit bus that enables it to address 16 megabytes of memory.

But since their introduction, there has been much speculation and little hard information. These two books, *65816/65802 Assembly Language Programming* by Michael Fischer and *Programming the 65816 Including the 6502, 65C02, and 65802* by David Eyes and Ron Lichty, rectify this situation and may well become standard texts for learning how to use and program these chips.

These books appear at a propitious time. Apple Computer recently introduced the Apple IIGS, the first commercial microcomputer with the 65816. (See Product Preview: "The Apple IIGS" by Gregg Williams and Richard Grehan, October 1986 BYTE.) In addition, there is the increased availability of enhancement boards that either contain a 65816/65802 or have provisions for the 65816/65802 for use in the older Apple IIs. For the adventurous, the microprocessor can be removed from any 6502-based machine and replaced with the pin-compatible 65802.

While the authors of both books did their program development work with hardware-enhanced Apple IIe machines, these books should not be construed as exclusively Apple-oriented. With the exception of several example programs that use Apple monitor calls, the information in these books can be used on any machine that uses or will use a 65xx or 658xx series microprocessor.

An Academic Text

An academic text by Michael Fischer, *65816/65802 Assembly Language Programming* functions like a reference encyclopedia,

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containing five discernible categories. The chapter on assemblers is outstanding—perhaps the best that I have seen in any book on assembly language. Although the discussion is tailored to assemblers for the Apple II series and the 65xx and 658xx families of microprocessors, the basic information is applicable to any microprocessor.

The book delves into the features of the new and basic architecture, addressing modes, and mnemonic instructions of the 658xx series of microprocessors. As a direct descendant of the 6502, the architecture of the 65816/65802 is similar. The major differences are that the registers have been expanded to 16 bits, an additional data bank and program bank register exists, a dual accumulator was added, and the status byte is enhanced. There is a new emulation (or "E") bit in the status byte. The intent of the emulation of the 65816/65802 is to ensure backward compatibility with the considerable body of software that has been written for the 6502. Unfortunately, Fischer glosses over the powers and ramifications of using the 65816/65802 in emulation mode. For a detailed understanding of the use of 6502 emulation mode, the reader would have to refer to the relevant sections in the Eyes and Lichty book.

One of the major stumbling blocks in learning 6502 assembly language (as well as one of the features that gives the chip its power) is the abundance of addressing modes available to the programmer. With eight new addressing modes, the 65816/65802 does not make the addressing problem any easier. Fischer explains the use of these new addressing modes within the context of the op codes of the microprocessor. The examples are thorough, but the illustrations used to describe these modes are not; I found the explanations and graphics expressed better in the Eyes and Lichty book. Addressing is often complex enough that even experienced programmers need to review things when they start working with an addressing mode that they are not accustomed to using.

The obligatory listing of all the mnemonics that make up the microprocessor is included. To the experienced 6502 programmer, most of these op codes will be old friends; however, there are 36 new ones that give the 65816/65802 additional powers. Each op code is listed with a description of what it does, how it is used (often with an illustrative segment of code), and what flags (if any) it will set upon execution. Where relevant, a table of all permitted addressing modes that can be used with a given op code is provided. The tables also give the format for all possible addressing modes, the hexadecimal version of each op code, the number of machine cycles used by each op code in both 8-bit and 16-bit formats, and the number of bytes of memory each op code and address will use.

Discussions of program development include small functional modules of 65816/65802 code: arithmetic operations, loops, character-coded data, code conversion, sorting, and subroutines. Fischer describes programming techniques that are glossed over in less sophisticated books, such as defining and writing position-independent code and using interrupts. By design, the 65816/65802 excels in both these applications.

Fischer also concentrates on the value of structured programming. Given an assembly language program of any complexity, the author shows that structure pays off in ease of design, debugging, documentation, and maintenance. The idea of structuring your code may be common in Pascal or C, but few assembly language books give it much importance. The author also advocates doing a flowchart of your program before writing any code, suggesting that it should not be considered a lost art. Debugging techniques for assembly language programs are also included.

Extensive appendixes consist mostly of the manufacturer's specifications sheets for the 65816/65802 and 65C02 micropro-

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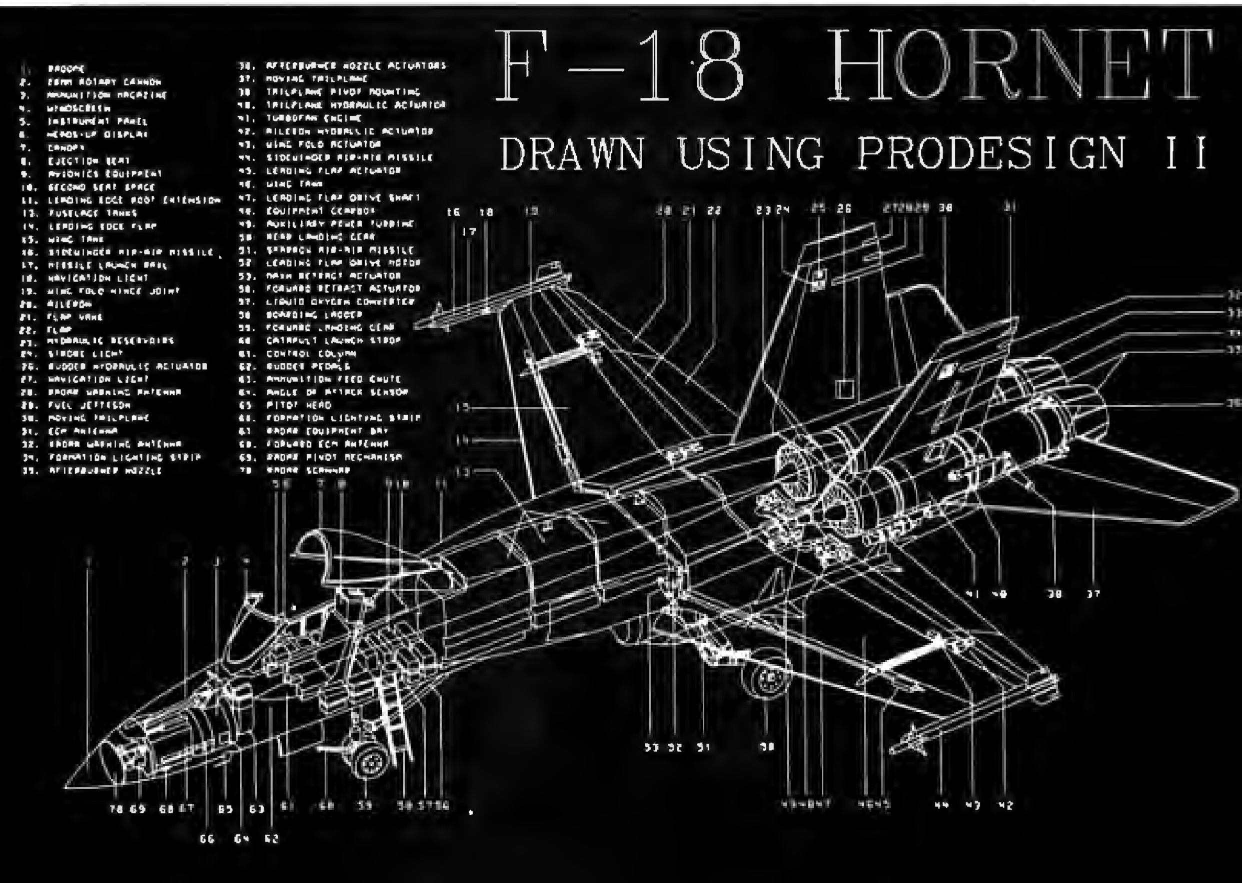

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cessors and most of their support chips. This information will interest the hardware designer, but the software designer can also gain some insight by skimming through a microprocessor's data sheet. Comparative charts of instructions and address modes for the 658xx/65xx family and the 68xx/68xxx family of microprocessors are included. Historically, these two families have a common ancestor in the 6800, and much of the knowledge and skills gained with one family is useful with the other.

While this book served a good purpose, the Eyes and Lichty review that follows provides a solid comparison because it is different both in style and purpose.

An Introductory and Explanatory Book

David Eyes and Ron Lichty have written a substantial book on assembly language programming for the 658xx/65xx family. While the technical content of *Programming the 65816 Including the 6502, 65C02, and 65802* is almost identical to that of Fischer's book, I will focus on the principal differences between the two approaches.

First, the foreword of this book was written by the designer of the 65C02, 65802, and 65816 chips, William D. Mensch Jr., the founder of the Western Design Center in Mesa, Arizona. In the foreword, he acknowledges that coauthor Eyes originally suggested the 6502/65C02 emulation capabilities for the 65816/65802. Mensch also mentions an upcoming chip called the 65832. This next-generation processor will have 32-bit floating-point operations and will be plug-compatible with the 65816 and software-compatible with the 65C02 and 65816. Although author Fischer also mentions this chip in his book, he erroneously refers to the 65832 as a coprocessor for the 65816.

Two chapters review the architecture and instructions of the 6502/65C02 microprocessors. This enables the experienced 6502/65C02 programmer to get a new footing into the world of the 65802/65816 and gives the novice programmer a feel for the history and lineage of the new 16-bit chips. In addition, for code-comparison purposes, several example listings that are given first in 6502/65C02 code are followed by the identical problem executed in 65816 code. These examples illustrate the additional power and efficiency of the newer microprocessor over the old in terms of reduced number of machine cycles and reduced amount of memory usage needed for the execution of similar types of programs.

In addition to the information on the standard 65C02, *Programming the 65816* has a separate appendix that covers the R65C02, which is the version of the 65C02 manufactured by Rockwell International Corporation in Newport Beach, California. The R65C02 has several additional op codes that set reset bits and branch on a set or reset bit. The code for these additional instructions controls completely different functions in the 658xx series. If these instructions are used, code written for the R65C02 is unusable and not upwardly compatible with the 65816/65802.

The Comparison

Since both books refer to the Western Design Center's notes on the 65816/65802, their technical content is similar. Both cover the same basic material: addressing, op codes, interrupts, and so on. But Eyes and Lichty tend to be less didactic, and some of their descriptions and explanations are clearer and more satisfying. (On the other hand, the encyclopedic nature of Fischer's book makes looking up a particular example or a specific instruction and its permitted addressing modes both faster and easier.)

The books differ considerably in the programming examples they offer. While both have sample segments of code for study and application, the Eyes and Lichty book has some interesting

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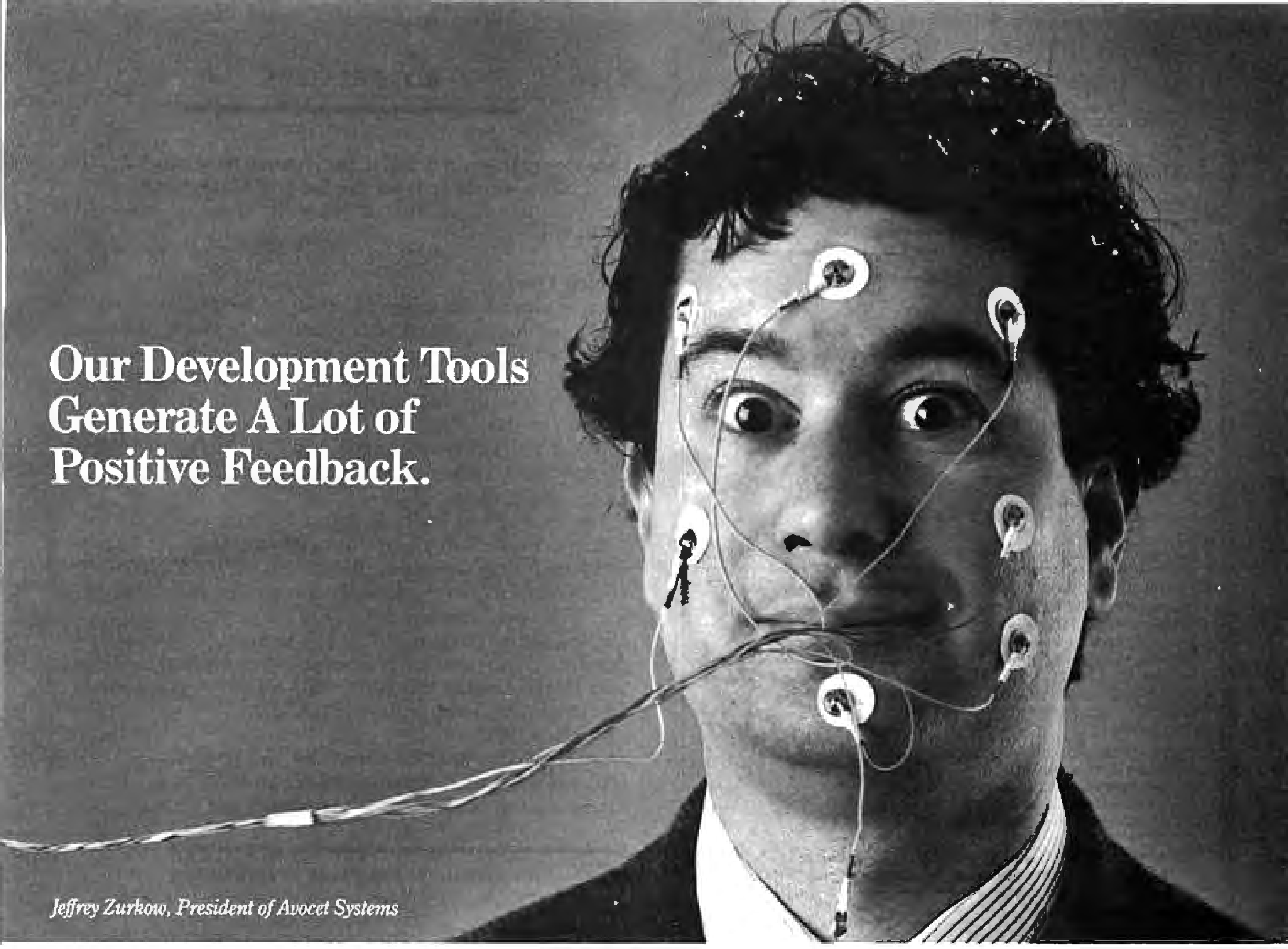

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code for programs of actual utility. Among these programs are the 65816 assembly code for the Sieve of Eratosthenes benchmark and one of the first 65816 utility programs available, DEBUG16.

Which One?

Because experienced programmers enjoy the insights into programming that individual authors are able to give to the same theme, both books are appropriate for basic coverage of the chips. But while they cover the same family of microprocessors, they are philosophically and pedantically different. Fischer's book is the more staid of the two. He calmly goes through each instruction and address mode and then builds up to coding examples. The book is destined to become a standard reference for the 65802/65816.

The Eyes and Lichty book covers the same technical information as Fischer's in a looser, more informal style. Do not misunderstand; *Programming the 65816 Including the 6502, 65C02, and 65802* is thorough and nothing is glossed over or trivialized. This book is the one that will be the introductory/explanatory text for the 65816/65802. It will introduce beginning programmers to this new series of microprocessors, and it will be used by the existing legions of 6502/65C02 programmers to bridge into the world of the 65816/65802.

Jesse D. Sheinwald (3965 Arthur Ave. N, Seaford, NY 11783) is a freelance writer and engineer who uses computers for the design and analysis of microwave circuits and systems.

80386/80286 Assembly Language Programming

Reviewed by John D. Unger

Appearances can be deceiving. From the title of the book, I expected William H. Murray III and Chris H. Pappas's *80386/80286 Assembly Language Programming* to be an advanced text about the two newest microprocessors from Intel. I was surprised when the introduction stated that the book was a primer designed to teach assembly language to someone with no previous experience. The authors state that their only assumption is that the reader know a high-level language such as BASIC or Pascal.

But the book progresses along at a fast pace that would be tough reading for a beginner. On the other hand, *80386/80286 Assembly Language Programming* contains a lot of elementary information, and an experienced programmer would benefit most from the final third of the book, where the authors discuss more advanced topics and programming techniques centered on the expanded instruction sets of the 80286 and 80386 microprocessors and their companion coprocessor chips.

Errors and Misstatements

After some introductory material and 131 pages of describing the complete 80286/80386 and 80287/80387 instruction sets, the book proceeds to teach assembly language programming through a series of progressively more complex example programs. Each of these programs is introduced in a step-by-step manner, and the assembly language source code programs are dissected and carefully explained.

However, these sections of *80386/80286 Assembly Language Programming* suffer from the presence of errors and misstatements that can confuse neophyte assembly language programmers and make experienced ones gnash their teeth. For example, the program listed in the book as figure 5-5 on page 210 is supposed to demonstrate multiple-precision addition using direct addressing. But instead it appears to be an error-ridden

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BOOK REVIEWS

version of the program listed correctly on page 212, which shows multiple-precision addition using both a table and indexed addressing. Also, the last statement in the flowchart on page 213 that describes this source code says to move the contents of the AX register into the variable MSBANS. However, the source code listing on the facing page clearly shows the correct statement: MOV MSBANS,DX to move the contents of the DX register into MSBANS.

When discussing the use of the BIOS interrupts to control the CRT screen on page 253, the assembly language listing and the supporting text both state that the DX register should be loaded with the lower right-hand row and column coordinates located on the screen by MOVing the hexadecimal value 2479 into it. This should be the decimal number 2479 or the hexadecimal number 184F.

Instruction Sets Explained

The book's strong point is in the way it presents the extended instruction set of the 80286 and 80386 processors. Murray and Pappas give example programs that gradually progress from 8088/8086 concepts into the 32-bit capability of the 80386. This approach allows the reader to see how the newest Intel processors expand on the instruction sets of their predecessors.

The final 100 pages of the book were the most useful ones for me. These two chapters describe some of the more advanced programming techniques, including special string-handling operands, and how to use the 80287 and 80387 coprocessors for calculations involving real numbers. The authors' discussion of the coprocessors is perhaps the best chapter in the book. I felt that they were truly in their element in covering this subject. They give examples of how to use the built-in trig functions of the 80387 and show how to develop a program that calculates and plots a sine wave on the screen using high-resolution monochrome graphics.

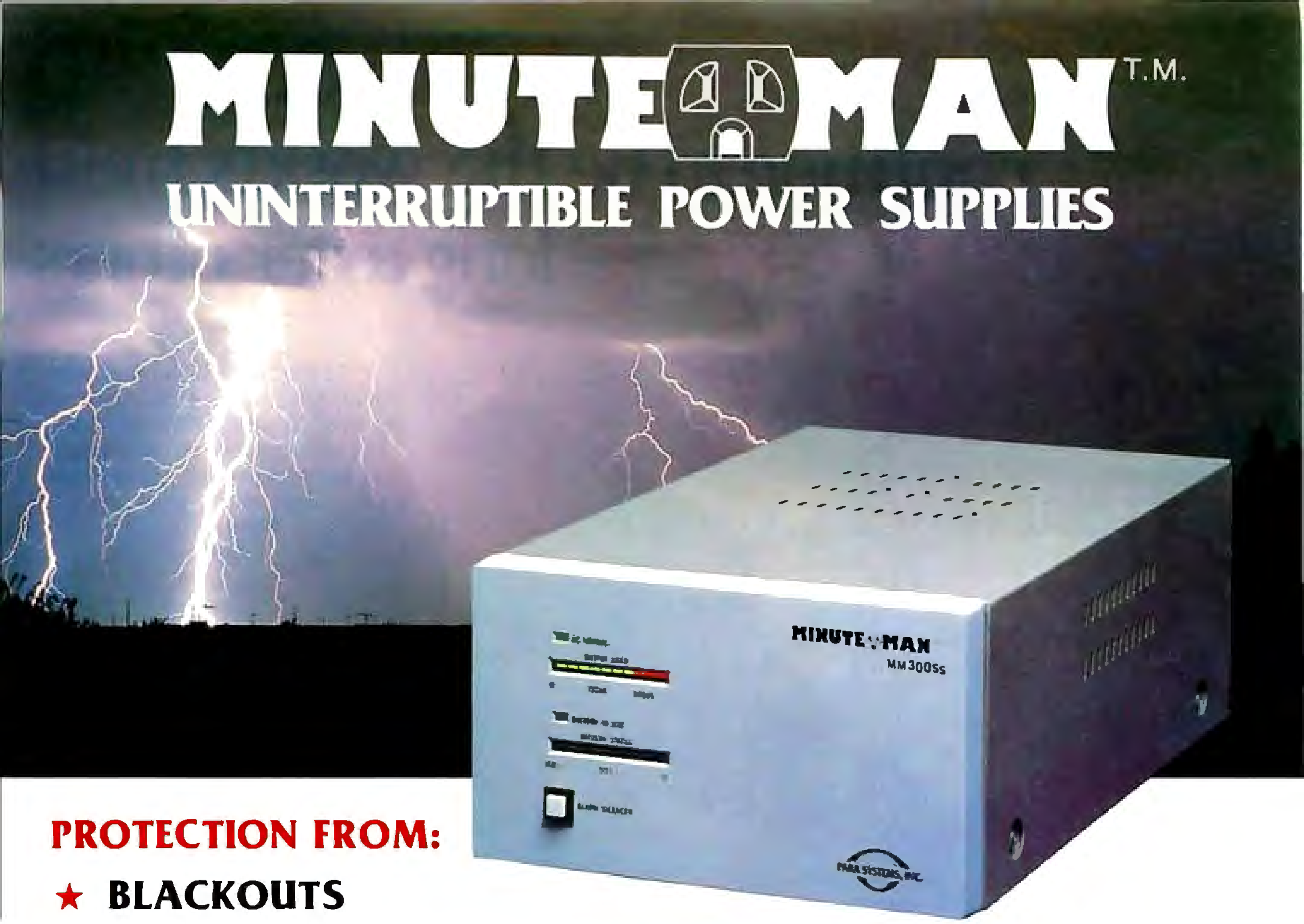
Source Code Listings

The program listings in the book are extremely useful because they are in the form of complete, ready-to-run source code and can be copied directly from the book, assembled, linked, and run by the reader. Other books on this general subject frequently use source code fragments or, in the case of assembly language, separate procedures as examples and do not include all the "overhead" or setup statements. Included with *80386/80286 Assembly Language Programming* is an order form for a disk containing the source code of all the listings in the book. Because only the source code is included on the disk, you will need one of the assemblers recommended by the authors to create executable programs—the IBM macro assembler, Microsoft's MASM assembler, or Speedware's Turbo Editasm. A helpful section in the appendix compares the three assemblers and shows how to use them.

Not Enough Soon Enough

Murray and Pappas's *80386/80286 Assembly Language Programming* includes a wide spectrum of subject matter and levels of ability ranging from a description of how to add two binary numbers to graphing the output of a program that creates and plots a square wave by summing the terms of a Fourier series. The book tries to cover too much ground in too short a time and with too few pages. However, the advanced sections of the book provide clear and useful examples of assembly language code and demonstrate the powerful features of the 80286/80386 processors and 80287/80387 coprocessors. ■

John D. Unger (P.O. Box 95, Hamilton, VA 22068) is a geophysicist who uses computers to study the stucture of the earth's crust in earthquake-prone regions of the Eastern U.S.



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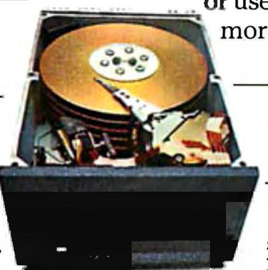

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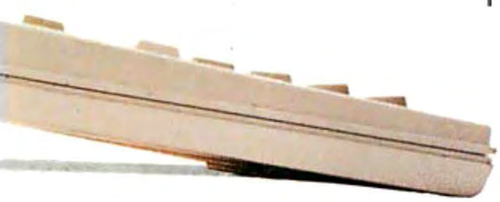

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Features

STEVE CIARCIA KICKS OFF this month's features with the conclusion of his GT180 color graphics board project, looking at the software that drives the graphics system. The first part of the article consists of an overview of the Hitachi HD63484 ACRTC registers and commands. Then Steve introduces a high-level software tool—Borland International's Modula-2 with special SB180/GT180 graphics extensions. Turbo Modula-2 is a complete development environment, similar in use to Turbo Pascal.

Writing listing programs in common languages such as BASIC is very tedious and repetitive because when you are ready to store the lists, you find that you have to write a whole new sequence of programs for every little database. Christopher D. S. Moss's "Intelligent Databases" offers an alternative in logical-language databases, which yield program efficiency while using a minimum of memory.

Next, Gregg Williams introduces us to the *relaxation method*, a numeric technique that will come in handy to scientists and engineers whose work involves solving such matters as systems of simultaneous equations, framework problems, and beam-deflection problems.

Our January Programming Project, "Look It Up Faster with Hashing," offers an explanation of a hashing function and its uses. Jon C. Snader provides a number of code examples to illustrate the implementation of such a function.

This month's 68000 feature is devoted to RegionMaker. Howard Katz takes a look at this Macintosh program for building a region from a graphics screen image.

If you count clock cycles and shuffle code to boost program performance, you'll be interested in Byron Sheppard's Programming Insight. "High-Performance Software Analysis on the IBM PC" describes a high-resolution timer that will allow you to examine single instructions and accurately analyze your favorite speed-up techniques.

In his Programming Insight "Dynamic Memory Allocation," Antonio Fernandes discusses linked lists and the basic concepts you need to work with dynamic structures in Apple II Pascal.

"Testing Intrinsic Random-Number Generators," another Programming Insight, takes as its subject a survey of the statistical characteristics and adequacy of several random-number generators on microcomputers. The results, say the authors, show that all RND functions are not created equal.

Finally, Wilfred J. Hansen, a system designer at Carnegie-Mellon University, explains how the university recently took on the task of displaying typographic-quality text on the IBM RT PC.

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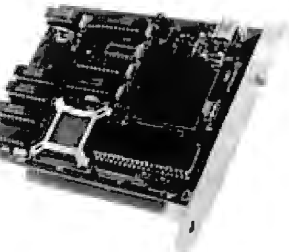

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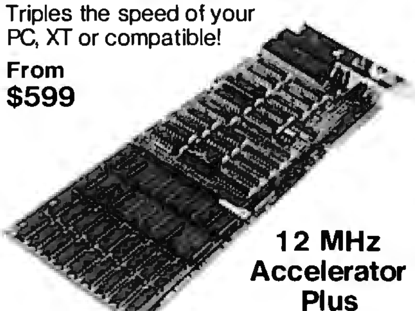

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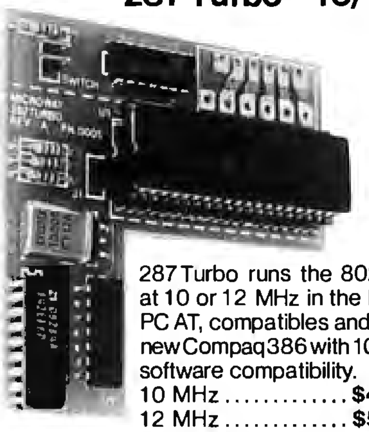

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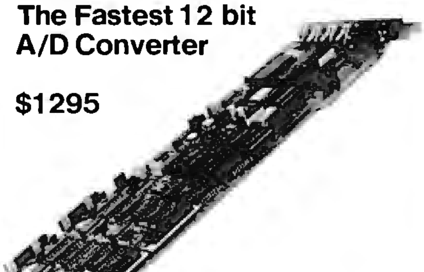

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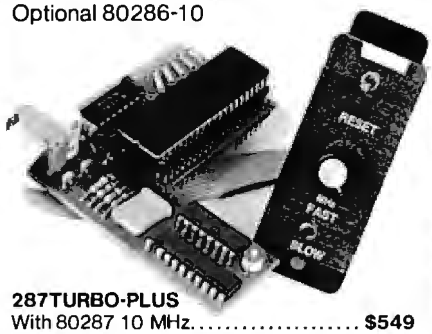

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Steve Ciarcia

Part 3: Software

Build the GT180 Color Graphics Board

A look at the software that drives the graphics system

During the last two months, we investigated the GT180's graphics hardware design, CRT basics, and the roles of key chips: the ACRTC, GMIC, GVAC, and palette D/A converter. This month, we'll look at the software that drives the graphics system. We'll start with an overview of the ACRTC registers and commands and then introduce a high-level software tool—Borland's Modula-2 with SB180/GT180 graphics extensions.

Programming the ACRTC

The ACRTC is an extremely complex device, containing three separate 16-bit processors, more than 200 bytes of registers, and 38 high-level commands. The on-chip CPUs perform separate tasks: timing control, display control, and drawing. Each CPU includes specialized registers optimized for its specific task.

In typical operation, the timing control registers establish the basic CRT timing. Once you initialize them, you rarely change them. The contents of the display control registers specify the frame-buffer scanning method, including hardware split screen and window. You will periodically reprogram these registers to move or resize splits and windows. Drawing commands and parameters issued to the ACRTC create an image on the screen.

A complete discussion of each of the more than 200 ACRTC registers is beyond the scope of this article. (This information is contained in the *Hitachi HD63484 User Manual*.) Instead, we'll highlight the main command and control registers.

Like other chips that contain a large number of registers, the ACRTC adopts an indirect addressing mechanism that reduces the number of address lines required to specify an individual register. The ACRTC uses only one address line, RS (register select), instead of eight address lines to access the more than 200 bytes of registers on-chip. Accessing a particular ACRTC register is a two-step process. First, write the register address of interest into the address register (RS=low). Then, read from or write to the selected register (RS=high).

Reading the status register returns the overall state of the ACRTC. Information returned includes whether a command has completed or a command error has occurred. Also, to support the clipping and hitting functions, an area-detection flag is provided. This is set when a drawing operation attempts to enter (hit) or leave (clip) a programmer-defined area on the screen. Another bit in the status register indicates when an optional light pen has been activated. (The GT180 uses this bit as a flag that indicates when vertical sync is occurring.) Finally, 4 bits reflect the state of the separate read and write first-in/first-out registers that communicate with the ACRTC drawing processor.

To speed drawing operations, separate 16-byte read and write FIFOs buffer communication to and from the ACRTC drawing processor. As mentioned above, the status register allows you to determine the FIFO's state. For the read FIFO, the status register shows whether the FIFO is full or not empty. For the write FIFO, the status register shows whether the FIFO is empty or not full. While the drawing processor is a 16-bit CPU (and the ACRTC has a 16-bit data bus), the SB180 interface is 8 bits wide. Consequently, commands, parameters, and data are transferred in high byte–low byte order.

Command Control Register

The lower 8 bits of the command control register correspond exactly to the 8 bits in the status register and are used to enable or disable each status bit from generating an interrupt to the CPU. For instance, as an alternative to polling, you could program the system so that the FIFO's state generates an interrupt, invoking the CPU to read or write the appropriate FIFO.

Besides polling and interrupt-driven transfer, the ACRTC can also request direct memory access transfer. This is ideal for high-speed reading and writing of the frame buffer. In response to a data-transfer command, the ACRTC will automatically invoke DMA to move the data between the frame buffer and main memory. You can program the type of DMA request as either burst or cycle steal (correspondingly, you must program the HD64180 DMA controller to be level- or edge-sensitive).

You specify the number of colors the ACRTC supports by programming the number of bits per dot as either 1 (monochrome), 2 (4 colors), 4 (16 colors), 8 (256 colors), or 16 (64K colors). In the GT180, 4 bits per dot is specified.

Finally, 2 bits allow you to abort or pause ACRTC command processing. An abort stops command processing, clears the FIFOs, and reinitializes the status register. A pause simply stops command processing without affecting the FIFOs or status register. Paused commands can be restarted later.

Operation Mode Register

The operation mode register determines the ACRTC's overall operation mode and

continued

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The ACRTC alternates frame-buffer accesses between display and drawing operations. Thus, the GT180 can perform drawing operations at any time.

must be initialized before enabling the display.

Both display and drawing operations contend for access to the frame buffer. In some older designs, the display operation required full-time, top-priority access to the frame buffer to meet CRT timing constraints. The resulting approaches for drawing were either draw at any time, overriding display accesses, or draw only during retrace when the CRT is blanked. Neither of these is very productive. In the first one, the conflicting display/draw operation causes the well-known screen "flash" effect; the second one results in slow drawing since retrace time is only about 25 percent of total display time.

The ACRTC has the ability to alternate frame-buffer accesses between display and drawing operations using a technique called interleaving (see the text box below). Thus, the GT180 can perform drawing operations at any time (during display and retrace) without screen flash occurring. When the ACRTC uses interleaving, however, twice as many bits must be pulled from the frame buffer each cycle to keep up with the display timing of the CRT. Calculation shows that to meet the constraints of the CRT and use interleaved mode requires pulling 64 bits from the frame buffer each display cycle. Thus, we program the ACRTC graphics address increment mode (within the operation mode register) as 4, meaning four 16-bit words, or 64 bits.

The dynamic RAMs used for the frame buffer need to be refreshed periodically. The ACRTC includes an on-chip DRAM refresh scheme that does the job. Once enabled, the DRAMs are automatically refreshed during horizontal retrace when the CRT is blanked. Some of you might suggest that the periodic scanning of the frame buffer for CRT display eliminates the need for specifically refreshing the DRAMs. This is fine if the frame buffer contains only one screen. In the case of the GT180, however, the frame buffer can hold multiple screens, fonts, icons, etc. Since only a portion of the frame buffer is being displayed at one time, we need to use the ACRTC refresh feature to preserve the contents of the undisplayed portion of the frame buffer.

Display Control Register

This register lets you enable, disable, or blank each of the ACRTC's four logical screen areas: the base, upper and lower split screens, and the window. Only the base screen must be defined (it can only be enabled or blanked, not disabled).

Timing Control Registers

Thirty bytes of timing control registers configure the on-chip timing control CPU to generate the appropriate CRT timing—particularly HSYNC and VSYNC frequency and pulse width. These depend on the specifications of the CRT being used and must be appropriately initialized before ACRTC display or drawing can occur. Also, the timing control registers hold configuration information for the split screens and window (see figure 1).

Display Control RAM

Forty-eight bytes of registers referred to as the display control RAM configure the on-chip display control CPU to modify the frame-buffer display address generation to account for the split screens and window (see figure 2). The split screens and window are specified in terms of physical frame-buffer addresses.

Drawing

Of the three on-chip CPUs (timing, display, and drawing), the drawing processor is most like a conventional CPU. Besides containing some registers, the drawing processor executes a sequence of user commands that correspond to a program on a conventional CPU. The drawing processor is programmed via FIFOs, providing the same high-performance benefits as a pipeline on a conventional CPU.

Register-Access Commands

Since communication with the drawing processor is via FIFO, the drawing processor provides a special set of commands to allow the programmer to access the drawing registers. Two distinct sets of drawing registers are used: the drawing parameter registers and the pattern RAM. These registers modify and control the way in which a drawing command is executed (see figure 3). Items programmed by the drawing parameter registers include colors, patterns, clipping area definition, modify mode, and other parameters.

Data-Transfer Commands

These commands allow high-speed reading, writing, clearing, and modifying of the frame buffer. This is especially useful for applications with digitizers or scanners, devices that construct an image as an actual bit map rather than as a sequence of drawing commands. Also, you can implement your own drawing commands using these data-transfer commands as basic building blocks.

Drawing Commands

These commands cause the ACRTC to automatically draw a number of common figures (like lines, circles, arcs, and rectangles) and to perform operations like filling and painting. The commands provide absolute and relative address versions. Absolute versions specify an address (like the endpoints of a line) as *x,y* displacements from an "origin" whose location in the frame buffer is set with the ORG command. Relative versions specify addresses as an *x,y* displacement from a "current pointer" location. You can change the current pointer location with

Interleaved Access Mode

The ACRTC's interleaved design for screen access provides considerable advantages over a noninterleaved access method. In the latter, drawing can occur only during retrace time minus the time for DRAM refresh. Since display time accounts for 68 percent of the total time available, and DRAM refresh occurs 7 percent of the time, drawing time is about 18 percent for a noninterleaved design.

An interleaved design permits display and drawing operations to alternate, increasing drawing time by 34 percent (half the display time of a noninterleaved system). This gives a total drawing time of 52 percent—nearly three times faster than a noninterleaved display.

In fact, for computer-bound (not bus-bound) instruction sequences, the relative improvement of interleaved mode will be higher than a factor of 3. This is due to the effect of idle drawing cycles—drawing cycles that the ACRTC can't use because it is performing an internal computation. In noninterleaved mode all idle drawing cycles are wasted, while in interleaved mode some idle cycles will overlap with timeshared display cycles, reducing the effective waste.

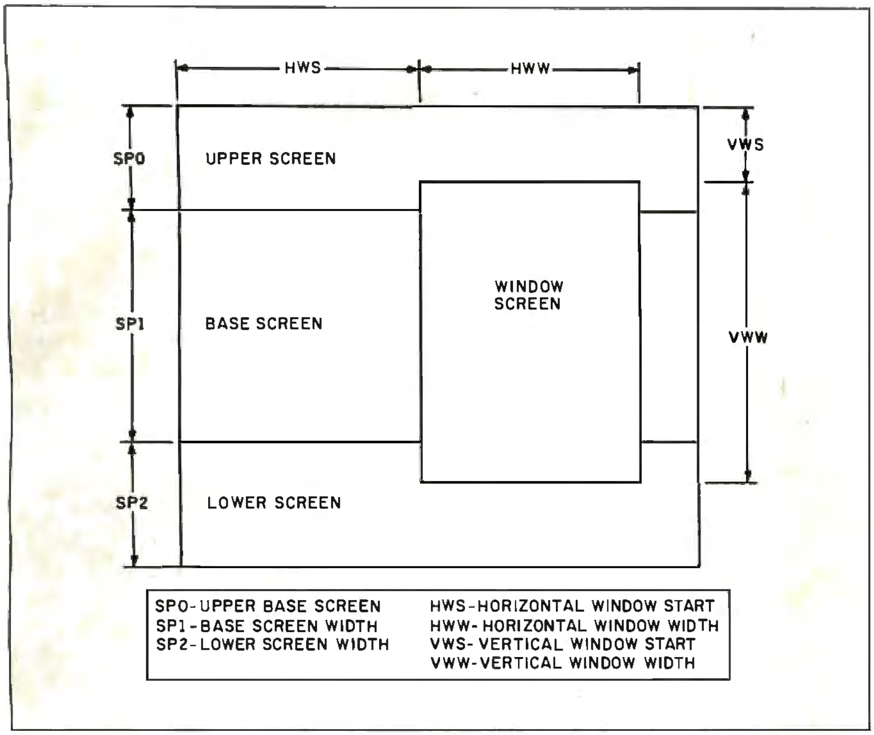

Figure 1: *Besides establishing basic CRT timing, the timing control registers partition the screen into the upper, base, lower, and window portions. The upper, lower, and base screens are all background screens that are overlapped by the foreground window. The vertical specifications (SP0, SP1, SP2, VWS, and VWW) are in units of rasters, while horizontal specifications (HWS, HWW) are in units of display cycles. Usually, only the base (covering the entire CRT screen) need be defined.*

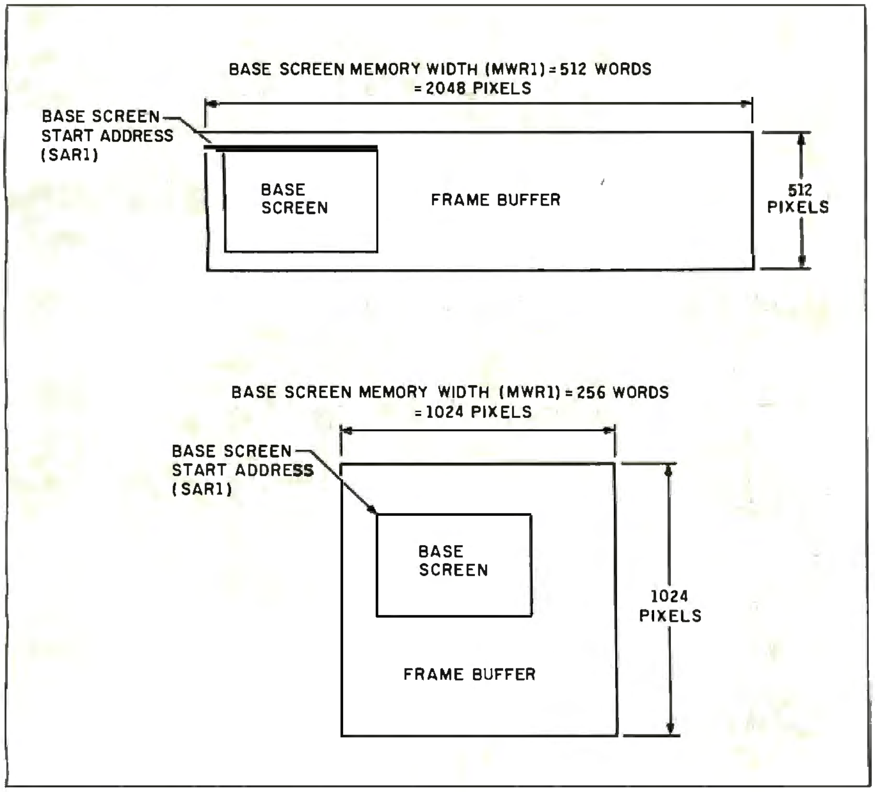

Figure 2: *The display control RAM's registers associate each CRT screen partition (upper, base, lower, and window) with a physical location in the frame buffer. In these examples, a 640 by 480 base screen is mapped into the frame buffer using two different memory-width values. (The memory-width parameter tells the ACRTC how many pixels in the x direction are associated with a single raster.) The number of pixels is equal to the memory width times 4, since the standard GT180 defines 4 bits per pixel and memory width is in units of words. The start address associates the top left corner of the screen with a particular pixel in the frame buffer. By changing the start address, the contents of the screen can appear to scroll smoothly in the horizontal and/or vertical direction.*

a MOVE command or as a result of a previous drawing command (see figure 4).

High-Level-Language Graphics

By using detailed knowledge of ACRTC registers and commands, you can write an assembly language program to initialize the ACRTC and draw some figures. However, for more complex applications, many programmers prefer to use a high-level language, preferably with graphics extensions available.

When I considered which popular, high-performance, low-cost language to choose, Borland International's Turbo Pascal emerged as the best possibility. In contacting Borland, I made two fortuitous discoveries. First, an 8-bit version of a new language, Turbo Modula-2, was almost ready and looking for a beta test site. Second, key people at Borland, including R&D engineer Mike Weisert, the compiler writers, and even Philippe Kahn himself, had an interest in exploring the limits of this new hardware and software technology. Above all, Philippe wanted

continued

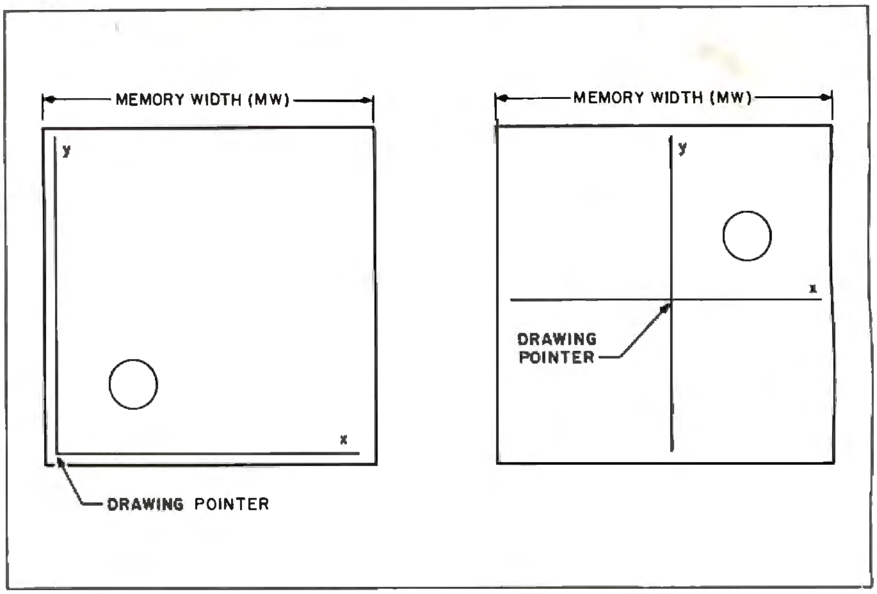

Figure 3: *The ACRTC's graphics-drawing commands (in this example,* MOVE *and* CIRCLE*) use a logical x,y coordinated pixel map independent of a pixel's physical frame-buffer address. The ACRTC uses the drawing pointer to make the translation from x,y coordinates to physical address. The drawing pointer specifies a screen (upper, base, lower, or window), a frame-buffer physical word address, and a dot offset within the word. Given the specified screen's MW and the physical address in the frame buffer associated with coordinates (0,0), the ACRTC can automatically translate an x,y address to a frame-buffer address. The two examples here show the origin in the bottom left corner and the origin in the center of the screen.*

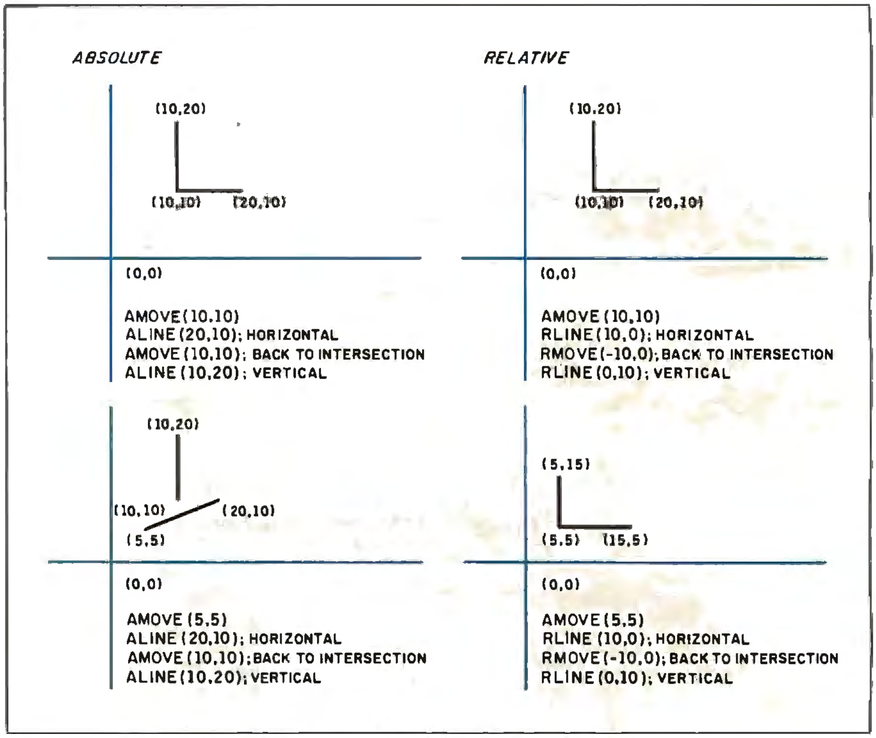

Figure 4: *Absolute-addressing drawing commands specify a displacement from the origin, while relative-addressing commands specify offsets from the current pointer (CP). The CP is set directly by the* MOVE *command and indirectly as the result of other drawing commands (for instance, it is set to the endpoint of a drawn line). These examples illustrate the virtue of using the relative mode. The intention is to draw the same figure at a different location by changing the first* AMOVE *command. Notice how the absolute version requires every instruction's coordinates to be changed, while the relative version works correctly.*

8-bit users to know that he had not abandoned them.

Modula-2 bears a very strong resemblance to Pascal. This is not a coincidence, since both were authored by Niklaus Wirth. Modula-2's primary difference (and improvement) is its inclusion of powerful facilities to allow modular program development. Modula-2 is closely aligned with the concept of structured programming, in which an application is dissected into functional modules. In fact, the details of the implementation of a particular module can be hidden or encapsulated—you need only know the interface definition in order to use the module. Furthermore, you can fix or change individual modules without having to recompile the entire application.

Turbo Modula-2 closely follows the standard defined in Wirth's *Programming in Modula-2*. Extensions are provided to handle I/O, string and exception handling, and other low-level system functions.

Turbo Modula-2 is a complete development environment, including integrated compiler, linker, editor, library manager, and more. It is quite similar in use to Turbo Pascal, including its menu-driven interface and WordStar-compatible editor.

For those of you unfamiliar with Turbo Pascal, you're in for a treat with Turbo Modula-2. Transitions in the edit-compile-run sequence are quick and easy. When a compile error is encountered, not only can you automatically enter the editor with the cursor positioned at the error point, but the compile automatically continues after you edit the flawed statement! Though a compiler, Turbo Modula-2 allows the free-flowing interactive style of programming normally associated with interpretive languages.

To boost performance and ease of use further, Borland has added special features to the SB180/SB180FX version of Modula-2 above and beyond those of the standard Z80 CP/M version. These include the use of new HD64180 op codes (like INO, OUTO to access on-chip I/O and MLT to speed up multiply routines). Also, the package uses the DU: (drive, user number) scheme for naming files (this worked so well, it was retrofitted to the CP/M version as well). However, the most important feature specific to the SB180 version is its ability to handle programs larger than 64K bytes. Whenever a module is called, Modula-2 reprograms the HD64180 memory management unit as required to access modules located in extended memory.

Turbo Graphix Tools

With Modula-2 in hand, Borland's next step was to create a series of tools (modules and procedures) that provide a simple, high-level interface to the raw power of the ACRTC. Modules are provided at different levels of abstraction. The various procedure modules are layered; higher-level modules use lower-level modules as primitive building blocks.

There are three layers of modules. The bottom layer provides simplified access to the most basic hardware resources contained in the ACRTC and the palette D/A converter. The next layer maps the ACRTC instruction set to Modula-2 procedures. In most cases, the ACRTC instruction format is directly mapped. In others, some preprocessing is done so that the instructions are more straightforward to use. The highest layer provides some enhanced graphics services like loading bit-map images and handling bit-mapped text.

Using these lower layers, you can write your graphics application as one or more higher layers. Examples might include routines to draw a specific image (like a bar or pie chart), a paint or draw program, or a multiwindow visual interface.

Toolbox Modules

Like the ACRTC registers, it is a bit much to try to explain all the Graphix Toolbox modules here. Instead, I'll briefly describe some of the more significant procedures.

ACRTC Module

Procedures within the ACRTC module initialize a myriad of ACRTC registers and set up a default palette. Typically, you should compile this module and include it in your system START alias to initialize the graphics system automatically when the Z-System is booted. The module defines key graphics parameters, including

The GT180 can use up to a 32-MHz crystal for greater than 780 by 520 resolution.

CRT timing and resolution. Thus, by changing the contents of ACRTC (and in some cases the timing crystal), you can accommodate different monitors. Assorted initialization files for a 25-megahertz crystal are included with the Graphix Toolbox. (The GT180 board can use up to a 32-MHz crystal for greater than 780 by 520 resolution.)

REGISTERS Module

These routines access the ACRTC FIFO, control registers, drawing parameter registers, and the pattern RAM. The FIFO is accessed constantly to issue commands and transfer bit maps. The ACRTC control registers, like those contained in the display and timing processors, can be directly accessed for special-purpose routines. The drawing parameter registers

continued

Listing 1: *A simple bar-chart program.*

```
MODULE bar;
FROM ACRTC IMPORT Xres, Yres;
FROM Graphics IMPORT aMove,rMove,rLine,rFilledRec,Pattern;
FROM Registers IMPORT ReadParamReg,WriteParamReg,ParamReg,WritePatRAM;
FROM Fonts IMPORT FONT, LoadFont;
FROM BitTexts IMPORT graphic,GotoRC;
FROM Patterns IMPORT SelectPattern, PatternName;

PROCEDURE labelaxis;
TYPE
   month = ARRAY [0..8] OF CHAR;
VAR
  months: ARRAY [0..11] OF month;
  curfont: FONT;
  i: CARDINAL;
BEGIN
  months [0]:='January ';
  months [1]:='February';
  months [2]:=' March   ';
  months [3]:=' April   ';
  months [4]:='  May    ';
  months [5]:=' June    ';
  (* load a font *)
  IF LoadFont (curfont,'M:14X8.FNT',Xres+16*8,0,0FFFFH,0) THEN END;
  GotoRC (3,20);
  WRITE (graphic,'XYZ Company Sales - 1st Half 1986');
  GotoRC (7,0);
  WRITELN(graphic,'Sales'); WRITE(graphic,'$000s');
  GotoRC (33,10);
  FOR i:=0 TO 5 DO
  WRITE (graphic,months[i],'  ');
  END;
  GotoRC (0,0);
END labelaxis;
```

continued

```
PROCEDURE drawaxis;
BEGIN
  WriteParamReg (ColReg0,0H); WriteParamReg (ColReg1,0FFFFH);
  SelectPattern(Empty);  (* black & white - solid pattern *)
  aMove(60,30);
  rFilledRec (2,360);  (* Y axis *)
  aMove(60,30);
  rFilledRec (490,2);  (* X axis *)
  SelectPattern(Arrow);  (* arrowhead *)
  aMove (53,390);
  Pattern(16,11,0);    (* arrowhead y axis);
  aMove (550,39);
  Pattern(16,11,6);    (* arrowhead x axis);
  aMove (85,33);
  WriteParamReg(ColReg1,0FFFFH);  (* setup color for drawbar *)
END drawaxis;

PROCEDURE drawbar (color:CARDINAL; Pat: PatternName; datavalue: INTEGER);
VAR
  cpx,cpy: CARDINAL;
BEGIN
  SelectPattern(Pat); (* dollar sign pattern *)
  color := color*4096 + color*256 + color*16 + color; (* bar color *)
  WriteParamReg(ColReg0,color);
  ReadParamReg (CurPtr1,cpx); ReadParamReg(CurPtr2,cpy); (* save CP *)
  rFilledRec (45,datavalue); (* draw the bar *)
  rMove (-12,4);
  WRITE (graphic,datavalue); (* label bar value *)
  aMove(cpx,cpy);  (* restore CP *)
  rMove (80,0); (* position for next bar *)
END drawbar;

BEGIN
  SelectPattern(Solid);  (* dollar sign pattern *)
  labelaxis;
  drawaxis;
  drawbar(10,CrossHatch,208);  drawbar(12,Arrow,110);  drawbar(8,Hand,220);
  drawbar(9,Triangle,240); drawbar(3,Hatch,296); drawbar(2,HalfTone,318);
END bar.
```

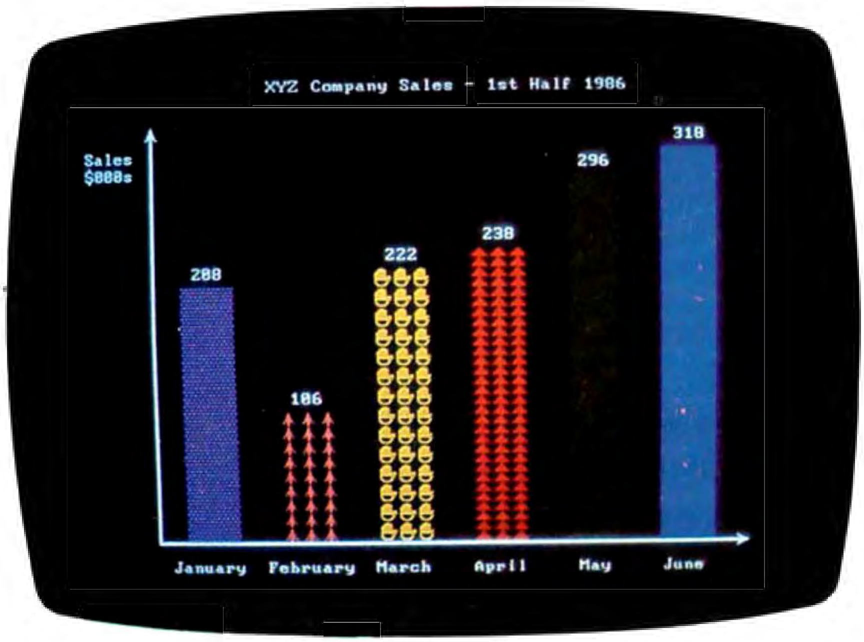

Photo 1: *This display is generated by the program shown in listing 1.*

and pattern RAM affect the basic operation of figure-drawing commands and should be set appropriately before a drawing command is issued.

PALETTE Module

These routines are used to access the BT450 palette D/A converter. Single colors or the entire palette can be read or written, either immediately or at the next vertical retrace. Since changing the color of an object is simply a matter of changing the corresponding palette entry, you can produce interesting effects like "flowing" water by dynamically reloading the palette.

GRAPHICS Module

This module contains all the ACRTC figure-drawing commands. Each command has a separate version for absolute and relative addressing, and they all use logical pixel *x,y* addressing; you don't have to translate to a physical address in the frame buffer.

Besides simply mapping directly to the

associated ACRTC command, some procedures perform useful error checking and pre/postprocessing. For example, the ACRTC on-chip PAINT command cannot handle overly complex figures, while the Turbo Graphix Toolbox PAINT command can.

Two parameters apply to specific commands. When drawing circles, ellipses, and arcs, you set the circular motion parameter to indicate the drawing direction as clockwise or counterclockwise. For the pattern and graphic copy commands, which move rectangular blocks of pixels, the CPScan parameter defines the scan direction during the block transfer. This allows you to slant or rotate an object during the transfer.

GRAPHMODES Module

Figure drawing is subject to various modes, which include operation, color, area, and edge modes. Like the drawing parameter registers and pattern RAM, you need to set up the drawing modes prior to issuing most commands. In simple applications, once you initialize the modes, you rarely need to modify them.

DATATRANSFER Module

Besides drawing figures, the other primary way to create a display is by moving bit-map images between host main memory and the frame buffer. (Since the frame buffer holds more memory than can be displayed on one screen, you can also "draw" pictures by moving them around within the frame buffer.) This module implements the ACRTC data-transfer commands designed for this purpose. Unlike the figure-drawing commands, the data-transfer commands use physical, instead of logical *x,y,* frame-buffer addresses.

The basic functions (read, write, clear, copy, and modify) are available, with or without DMA and "on the fly" masking and logical operations. The DMA option is used for large bit-map transfers (for example, loading an entire screen image), while the non-DMA versions are best for handling the transfer of a single word. A complete screen (640 by 480) DMA transfer between SB180 RAM and the frame buffer takes only a fraction of a second.

BITTEXT Module

One important requirement is to handle bit-mapped alphanumerics. Sometimes a word is worth a thousand pictures. The BITTEXT module makes writing text on the graphics screen as easy as writing it to a terminal.

FONTS Module

In conjunction with BITTEXT, the FONTS module lets you select multiple disk-based fonts. The fonts are loaded into an undisplayed area of the frame buffer. Font size and color are programmable, and you can add your own fonts as well.

PATTERNS Module

The ACRTC pattern RAM stores patterns (up to 16 by 16 dots), which are useful in two ways. First, all the figure-drawing commands refer to the pattern RAM when drawing. As each dot is drawn, pattern-RAM pointers are updated to point to the next dot in the pattern. This allows effects like dashed lines and tiling. Essentially, the "pen" can become a multidot pattern instead of just a single dot. Second, the pattern command simply moves the contents of the pattern RAM into the frame buffer, with optional rotation and slanting. This is useful for commonly used patterns like characters, cursors, and arrowheads.

BITMAPS Module

BITMAPS contains routines that let you transfer large bit-map images between the frame buffer and disk (floppy, hard, or RAM). Of course, it is quite possible to convert other machines' bit maps (like the Macintosh, Amiga, and Atari 520ST) for use on the GT180.

SCREENS Module

SCREENS eases the interface to the ACRTC display controller that manages the ACRTC split screens and window. It is easy to specify the screen's size and position as well as the display address of the contents. These routines can be used as the basis for a window manager, pull-down menus, status lines, and other visual interface techniques.

Using the Turbo Graphix Toolbox

The best way to get up to speed is to run through an application example. Let's use Modula-2 and the Turbo Graphix Toolbox to build a simple bar-chart program (see listing 1). The program accepts data values, legends, and bar color information and constructs a bar chart on the graphics screen. In this simplified example, the data values and legends are hard-wired into the program to keep the focus on the graphics routines. Obviously, your own chart program could adopt much more sophisticated data capture and scaling routines.

Since we are writing a program rather than a group of procedures, we don't need a definition module. After telling the compiler the name of the main module (bar), we use a series of FROM statements to specify which modules we are planning to use. IMPORT is used in conjunction with FROM to load specific functions and procedures from each module. We'll use a variety of Turbo Graphix Tools to complete the chart: text, patterns, filled rectangles, and others.

High-performance graphics hardware now available will let the SB180 and 8-bit software evolve to include graphics applications.

First, the labelaxis routine uses the bit-mapped text modules to label the graph, axis, and bar representing each month. Note the use of a disk-based font and the similarity of the bit-mapped text routines to the conventional terminal text routines. For instance, GotoRC locates the cursor at the correct line on the screen (depending on font size). Also, I extended the conventional WRITE ('text') statement—which prints text on the terminal—with the WRITE (graphic,'text') function that prints text on the graphics screen.

Next, the drawaxis routine draws the *x* and *y* axes. I used filled rectangles to make thick (three pixels wide) lines. This is easier than drawing three lines next to each other, which would achieve the same effect. However, unlike multiple lines, the filled rectangle approach works only for thick lines parallel to the *x* or *y* axis. The arrows at the end of each axis are a nice touch obtained by selecting the arrowhead pattern (with selectpattern) and then drawing it with the pattern command. Note how the same arrow pattern is used for both axes by changing the scan direction parameter of the pattern command.

Finally, each bar is drawn by calling drawbar with a data value and a color. Besides solid colors, you could use selectpattern to spruce up each bar with an illustrative pattern (see photo 1).

In Conclusion

As a stand-alone computer, the SB180/SB180FX, like most 8-bit systems, has traditionally been limited to alphanumerics. When 8-bit systems were introduced, a good graphics subsystem cost thousands of dollars, often more than the computer itself. Now that high-performance, low-cost graphics hardware is available, the SB180 and 8-bit software can evolve to include graphics applications. Using Modula-2 and the Graphix Tools, you can write software to tailor the SB180/GT180 for a variety of different graphics applications.

continued

Finally, a project as big as the GT180 could have been accomplished only with the help of many people. Foremost among them, I would like to personally thank Philippe Kahn of Borland International. His unwavering support for this project and 8-bit users in general demonstrates that he is a man of his word.

Experimenters

As with the the majority of Circuit Cellar projects, I encourage you to build them. To aid you in that endeavor, the Circuit Cellar BBS, (203) 871-1988, has been set up as an interchange for communication among builders and as a source for the various free software routines that complement these projects. With regard to the GT180, assorted graphics utilities are available for downloading.

Also, if you have been a supporter of the SB180 and are now interested in knowing more about the SB180FX, contact me and I'll send you a schematic and spec sheet. Finally, even though the SB180FX is not a BYTE project, I will offer support to BYTE readers who wish to build it. The object code of the monitor boot ROMs for the SB180FX and the original SB180 are posted on my BBS, and the BIOS will be sent in exchange for a picture of your handiwork. As with all the software supplied in this manner, it is completely free but limited to noncommercial personal use.

Circuit Cellar Feedback

This month's feedback begins on page 58.

Next Month

Next month's project features an infrared remote controller. ■

Special thanks to Tom Cantrell, Ken Davidson, and Mike Weisert for their contributions to this project.

Editor's Note: Steve often refers to previous Circuit Cellar articles. Most of these past articles are available in book form from BYTE Books, McGraw-Hill Book Company, P.O. Box 400, Hightstown, NJ 08250.

Ciarcia's Circuit Cellar, Volume I covers articles in BYTE from September 1977 through November 1978. *Volume II* covers December 1978 through June 1980. *Volume III* covers July 1980 through December 1981. *Volume IV* covers January 1982 through June 1983. *Volume V* covers July 1983 through December 1984.

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(203) 871-6170
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1. GT180 graphics board: RGBI version less palette D/A converter. Comes with demo disk and user's manual.
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   board with Modula-2 and GT180 Graphix Toolbox $449
2. GT180 graphics board: RGBI and analog version with palette D/A converter. Comes with demo disk and user's manual.
   board alone $449
   board with Modula-2 and GT180 Graphix Toolbox $499
3. Borland International's Turbo Modula-2 and GT180 Graphix Toolbox software for the SB180 and SB180FX computers, optimized for the 64180 processor. Supplied on 5¼-inch DS/DD SB180 format disks with 552-page manual.
   SB180 Modula-2 alone $69
   SB180 Modula-2 with Graphix Toolbox alone $89
4. SB180FX 5.75- by 8-inch single-board computer, accommodates 512K bytes of memory, two serial ports, three parallel ports, parallel printer port, floppy disk controller, SCSI controller, ROM monitor, 6-MHz 64180. Comes with ZRDOS, ZCPR3, hard disk BIOS, and user's manuals. Populated with 256K-byte memory, less 53C80 SCSI controller chip.
   SB180FX board alone $409
   SB180FX board with software $499
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   9.216-MHz 64180 processor upgrade (SB180FX only) $50

GMIC, GVAC, ACRTC, and palette D/A converter chip sets are available for experimenters who wish to hand-assemble the GT180. Call for price and availability information. Borland's Turbo Modula-2 is also available for most CP/M Z80 machines. Contact Echelon Inc., 885 North San Antonio Rd., Los Altos, CA 94022, (415) 948-3820. The SB180FX is hardware- and software-compatible with the SB180.

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There is an on-line Circuit Cellar bulletin board system that supports past and present projects. You are invited to call and exchange ideas and comments with other Circuit Cellar supporters. The 300/1200/2400-bps BBS is on-line 24 hours a day at (203) 871-1988.

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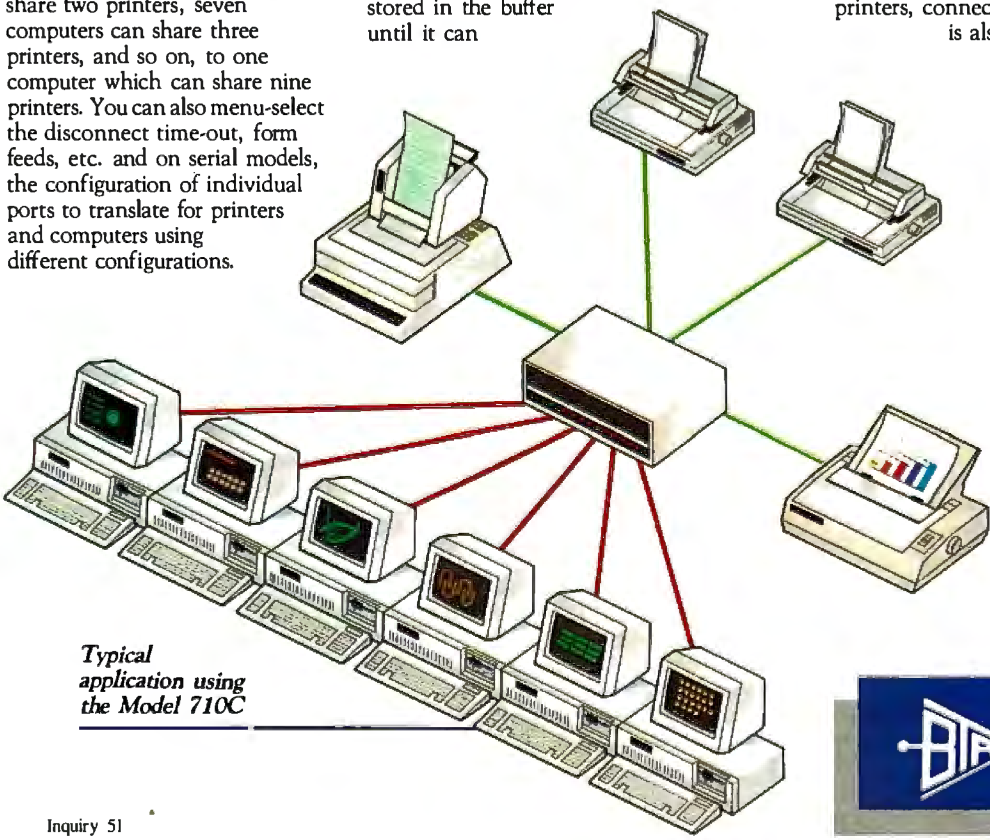

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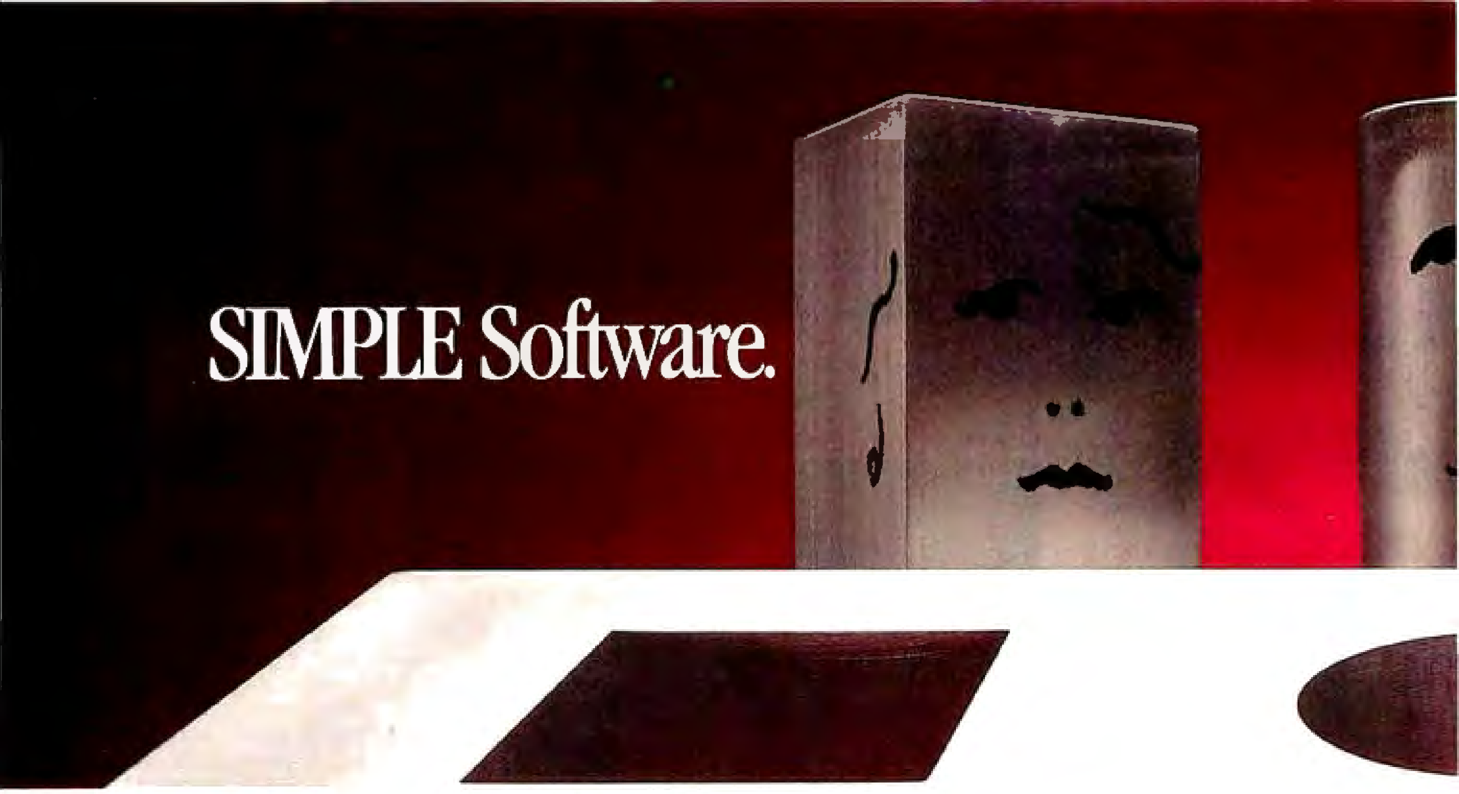
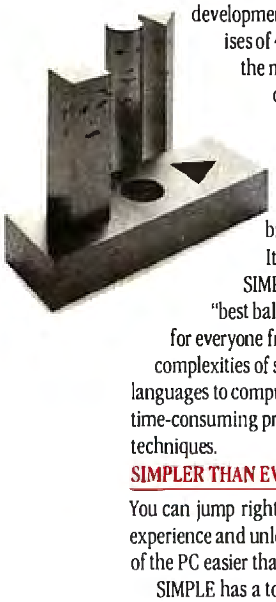


The 3-in-1 applications development



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2. It's a Relational Database Manager.

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SIMPLE's relational joins are easy to construct and the most efficient to process. Rather than a physical view, you get a logical view without the need to create an additional physical file at any time. Joins are accomplished dynamically at time of processing and support one-to-many and many-to-many relationships.

With SIMPLE, database management becomes more than just a question of "how many" files or "how many" fields, but a question of "how much more" you can do, and "how easily" you can do it.

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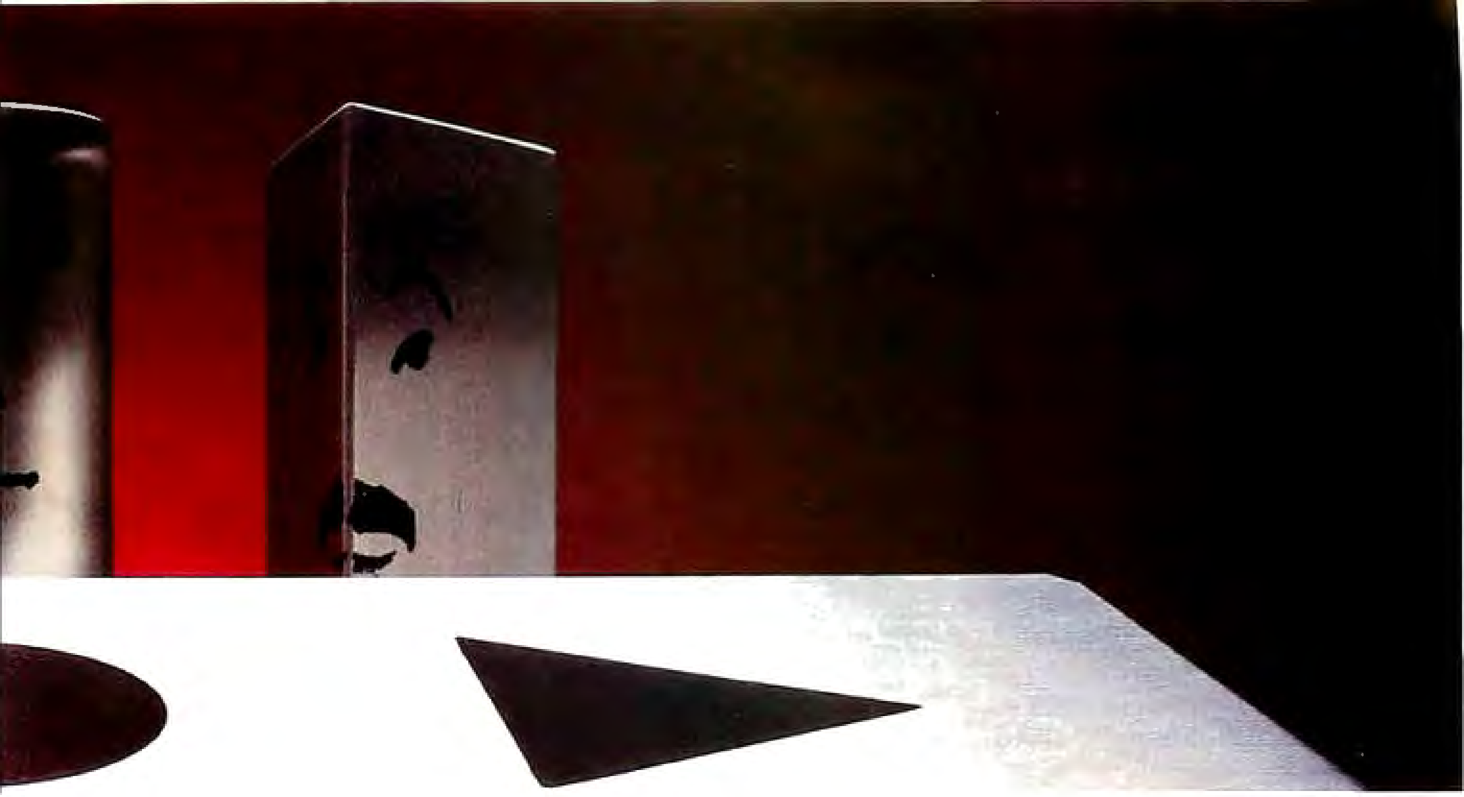
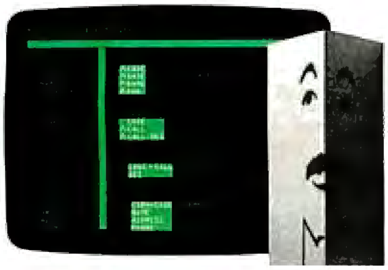
In the Design Worksheet, you simply paint or draw an example of the input screen or report you want. The Design screen may be painted exactly the way you want it using SIMPLE's built-in editor.



tool for every Tom, Dick and Harriett.



For Example, Company Managers like Tom, Head of Customer Support for a Chain of Retail Outlets, easily develop customized applications. SIMPLE lets Tom develop a Branch Reporting System which reports information from support service calls. Tom wants a system which validates certain information and provides a customer history to improve the branch's support capabilities. With SIMPLE's Specify Worksheet on screen, Tom simply joins data from four different files and establishes their relationship. This enables the user to pull-up call classifications, also verify if the caller has been called on before.

For Example, Information Center Staff Members like Dick, who works for a major Computer Hardware Manufacturer, develop new microcomputer applications systems with SIMPLE. Dick is working with the Director of Marketing on a lead-tracking system. Today, they're reviewing the data entry screens developed with SIMPLE. Dick sits down to review the main data entry screen which shows the prospect demographic information, the media source and date from which the lead was generated, and the fulfillment literature to be sent.

For Example, System Analysts/Programmers like Harriett easily prototype design changes, interacting directly with department heads. Harriett has completed the prototyping with the help of SIMPLE of some previously requested changes in a large Insurance Company's Mainframe Payables System. She has built a test database with data imported from the mainframe and is going to review a check-ledger report in the Controller's office on her portable computer. Harriett shows the Controller exactly how the new system gives a report of all checks issued.

The full-screen editor offers a wide range of capabilities to aid you—including the ability to delete or insert a character or an entire line, move or copy blocks of information, lasso text or variables to move around the screen and window to other worksheets in one or two keystrokes.

Your design worksheet invokes powerful specification macros that provide your application user with a richness of features and functionality that you demand from a development tool. Pop-up a window and browse through another file, interrupt data entry to perform another program, provide context-sensitive help, and perform conditional processing based on the user's input.

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Christopher D. S. Moss

Intelligent Databases

Logical-language databases yield program efficiency with minimum memory space

One of the simplest uses of a computer is keeping lists such as telephone directories, recipes, indexes of books and periodicals, and so on. Yet writing these programs in common languages such as BASIC is very tedious and repetitive because when you are ready to store the lists, you find that you have to write a whole new sequence of programs for every little database. You must write programs to implement such file functions as entering data, storing computation results, retrieving information from files, finding an item according to some criterion, listing out the entries in a predetermined order, and altering or deleting file entries.

The problem is that a BASIC program has to know about the shape of every new database, and you end up writing most of the program again because each database has its own special requirements; that is, the diet database has to know about units, the book index must distinguish the difference between titles and dates, and so on.

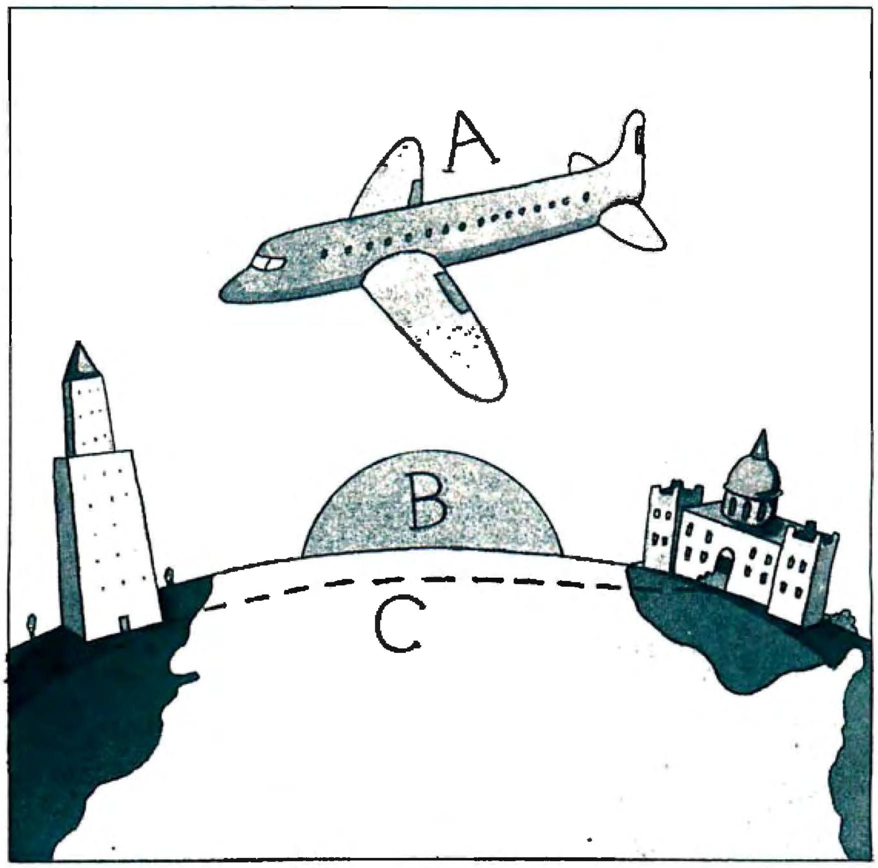
The obvious alternative to writing programs is to use a database system or a file-handling system. Either of these can deal with the tasks described above, but you may not be happy with the way your database handles some features (data entry, for instance). If you're lucky, the system will have facilities for changing some of these features (though it is usually more work that way), but database systems don't ordinarily deal well with the special functions associated with each database.

Often, a programming language that is something like BASIC is associated with the database. For instance, dBASE II has its own language, with conditionals and arithmetic and so on. Database programming can be a little tedious (witness the aids now being offered that claim to speed up the programming process), but that is not the major drawback with these systems when applied to complex databases.

The main problem with most such databases is that they have a hard-and-fast dividing line between the ideas of "data" and "program." The difficulty is that data is kept in one file and procedures in another. You must know whether a particular relation is represented as data or program (i.e., explicitly or implicitly). Also, the language used to describe data is usually entirely different from that used for the program.

What is the effect of this? Suppose that you want to construct a table of flight distances between the world's major air-

continued



Christopher D. S. Moss holds a doctorate in computing science from Imperial College, London, where he works in the Department of Computing. He can be contacted at the Department of Computing, Imperial College, London SW7 2BZ, U.K.

ILLUSTRATION BY CATHARINE BENNETT

ports. This table can be represented in a BASIC program by a two-dimensional array (see table 1), but this layout is not suitable for a database. In a database you would represent the data as pairs of names, as shown in table 2.

Suddenly you see the size of the whole project. Not only are the same names written again and again, but the total number of entries required is vast. (Do you list Houston to San Francisco as well as vice versa?) If you include 100 airports, you need (100 × 99) / 2 = 4950 entries) and that is a substantial amount of data entry as well as a large file (possibly 250K bytes excluding indexes).

There is a better way to do this. If you know the latitude and longitude of each city, you can easily calculate the approximate distance between any two of them by using a little spherical trigonometry. If the longitude and latitude of the two points are (x_1, y_1) and (x_2, y_2) and the radius of the earth is represented by R, then the distance (D_{12}) can be expressed as follows:

$$D_{12} = R \times \text{arc cos } (\sin y_1 \sin y_2 + \cos y_1 \cos y_2 \cos (x_2 - x_1)).$$

The only data you need to store is the latitude and longitude of the 100 cities, which might take about 4K bytes of space. What you need, therefore, is something that looks exactly like a database but simply uses the formula to calculate distances. This database can be thought of as having entries of the following form:

Chicago Houston 965

But the entries are there only "implicitly." The database actually contains the latitudes and longitudes and the formula used to calculate distance. If you think it is time-consuming to do the calculation repeatedly, remember that it is also time-consuming to access a large file. In practice you might easily keep 4K bytes of this type of data in main memory, but not 250K bytes.

Prolog

Prolog is a language designed to handle words and lists. It is a "relational" language, although it is richer than most relational databases. Based on fundamental ideas of logic, Prolog has been simplified to the point where schoolchildren can use it. It is also the language the Japanese chose to form the kernel of their "fifth-generation" computer project.

The hypothetical database described below uses the form of the Prolog language known as microProlog. The shell called simple provides a friendly top-level environment. (A product of Programming Logic Systems, 31 Crescent Dr., Milford, CT 06460, microProlog is available for CP/M- and MS-DOS-compatible micros as well as for the Commodore 64 and other home computers.)

The Timetable Database

To introduce Prolog I will use an airline timetable, but the same principles apply to a subway or bus timetable or any other scheduled activity. In the process of demonstrating how to get information into and out of a Prolog database, I'll also illustrate the power of general rules in a database.

The basic unit of an airline timetable is the flight of one aircraft. To start this database I'll use the information in table 3. To start microProlog, type prolog load simple at the A> prompt. (Input is shown in a bolder typeface.)

```
A>prolog load simple
microProlog Version 4.0
(c) LPA Assoc
41240 bytes free
&&.
```

The prompt &. signifies that the system is awaiting input. There are two ampersands because the program has already obeyed the first command to load the simple shell. The first task is to enter a few names and numbers. We'll use the accept command, to which we add the name of the relation we are entering, which we'll call flight.

```
&.accept flight
flight.(PA51 London New-York (Sat
  10.00) (Sat 13.45))
flight.(PA51 New-York Houston (Sat
  16.40) (Sat 19.30))
flight.(PA52 Houston New-York (Sun
  12.35) (Sun 16.45))
flight.(PA52 New-York London (Sun
  19.00) (Mon 06.40))
flight.(BA193 London New-York (Mon
  10.30) (Mon 09.20))
flight.(BA192 New-York London (Tue
  09.30) (Tue 18.10))
flight.end
```

Parentheses are used extensively in microProlog to mark where items begin and end. In this case the outer parentheses indicate the beginning and end of each record, and the inner parentheses mark the individual items in the record (the day and time, respectively).

Each word is a separate item, and a hyphen rather than quotes or parentheses is used to indicate that New-York is one word. This is a matter of choice. The system prints flight. to remind you that you are inputting to this relation, and you type end (without parentheses) when you have

continued

Table 1: *Flight distances represented as a two-dimensional data array.*

	Chi	Hou	Lon	Mex	NY	SF
Chicago	0	965	3946	1710	730	1866
Houston	965	0	4858	751	1451	1645
London	3946	4858	0	5540	3451	5360
Mexico City	1710	751	5540	0	2101	1930
New York	730	1451	3451	2101	0	2586
San Francisco	1866	1645	5360	1930	2586	0

Table 2: *Flight distances organized for use in a database system.*

Chicago	Houston	965
Chicago	London	3946
Chicago	Mexico City	1710
San Francisco	New York	2586
. . .etc.		

Table 3: *Airline timetable data.*

Flight number	Starting point	Destination	Departure time	Arrival time
PA51	London	New York	Sat 10:00	Sat 13:45
PA51	New York	Houston	Sat 16:40	Sat 19:30
PA52	Houston	New York	Sun 12:35	Sun 16:45
PA52	New York	London	Sun 19:00	Mon 06:40
BA193	London	New York	Mon 10:30	Mon 09:20
BA192	New York	London	Tue 09:30	Tue 18:10

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	Execution Time	Code Size	Compile/ Link Time
Dhrystone Benchmark			
Manx Aztec C86 3.3	34 secs	5,760	93 secs
Microsoft C 3.0	34 secs	7,146	119 secs
Optimized C86 2.20J	53 secs	11,009	172 secs
Mark Williams 2.0	56 secs	12,980	113 secs
Lattice 2.14	89 secs	20,404	117 secs

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Library Source Code -c	Mixed memory models -c
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All Prolog systems have ways of saving their databases in files and restoring them.

entered enough. If you cannot get the whole record on one line, you can continue on the next, and the system will remind you how many levels of parentheses remain to be closed.

The simplest query into this database is a check to see if a particular record is there. This query is called is. You invoke this query by typing

```
&.is(flight (BA193 London New-York
   (Mon 10.30) (Mon 09.20)))
YES
&.is(flight(PA52 New-York London
   (Sun 19.00) (Sun 06.40)))
NO
&.
```

Notice here that the name of the relation (flight) is indicated before the first item and that all the items are enclosed in parentheses. This is the standard way of representing a relation in Prolog. In the query three sets of parentheses are used: one surrounds the is query, another the arguments of the relation, and a third the lists that make up the individual items. This may look forbidding, but it rarely gets more complicated than this in a microProlog program.

Why did the second query fail? Even though there is a flight on Sunday at 19.00, there is no flight on Sunday at 06.40 (the 06.40 flight leaves on Monday). Notice that matching is done at all levels of nesting.

It is not very useful just to confirm what you already know. You need to get information out, and for this purpose you use the which command, with variables standing for anything you don't know. A variable is written as an underscore followed by a word (e.g., _X or _var). (This is now standard in microProlog and accepted by CProlog and other versions.)

Suppose you want to know the time and flight number of a plane from London to New York. You type:

```
&.which (_X_Y: flight (_X London
   New-York _Y _Z))
PA51 (Sat 10)
BA193 (Mon 10.3)
No (more) answers
&.
```

The which command has two parts separated by a colon. The first part is an answer template, _X _Y. The second part is a query, flight (_X London New-York _Y _Z). Note that the answer template does not have to include all possible information (you did not ask for the arrival time to be printed out). But the query has to include the same number of items as the original data. You also have to enter the times as floating-point numbers so that not all the decimal places are printed out.

Besides variables, the answer template can contain any words needed for clarity. For instance:

```
&. which(Flight _X leaves on _Day
   at _Time:
   flight(_X London New-York
      (_Day _Time) _Arr))
Flight PA51 leaves on Sat at 10
Flight BA193 leaves on Mon at 10.3
No (more) answers
&.
```

In the case above, two of the variables (_Day and _Time) in the query were placed inside inner parentheses, whereas in the first query the variable Y corresponded to the entire item enclosed in parentheses. This shows how you can "split open" a complex item. In general, a variable can match any item enclosed in parentheses such as a list or an individual item. Queries in Prolog are very flexible because they can have more than one answer and you can specify different parts of the answer.

For instance, suppose you want to know the arrival time of any flight to New York on Saturday. The following query will do the job:

```
&.which(_X from _Y: flight(_Z
   _Y New-York _Dep (Sat _X)))
13.45 from London
No (more) answers
&.
```

If you want to know only arrivals after a certain time, you can add other conditions to the first query, using the same variable names to keep track of the information.

```
&.which (_X from _Y: flight(_F
   _Y New-York _Dep (_Day
   _X)) and 16 LESS _X)
16.45 from Houston
No (more) answers
&.
```

To find the times of all flights that do not start in New York, you can use this query:

```
&.which(_X from _Y to _Z:
   flight(_F _Y _Z _X _arr) and
   not(_Y EQ New-York))
(Sat 10) from London to New-York
(Sun 12.35) from Houston to New-York
(Mon 10.3) from London to New-York
No (more) answers
&.
```

The predicates LESS and EQ (equal) are two examples of the many built-in predicates in Prolog. I will not attempt to give a full list because your local Prolog implementation may be different. Any predicates such as these that have exactly two arguments can be written as expressions.

In both of the previous two queries it is important that the variables receive a value before the test is made because Prolog evaluates several queries linked by and in order from left to right. If you attempt to evaluate 16 LESS _X before _X has a value, Prolog will report a control error.

In this instance, Prolog is more user-friendly than Pascal: If you make a test before assigning to a variable in Pascal, the result will be more or less random. In the second example, if Y does not have a value, not will fail (because EQ succeeds, by setting _Y to New-York), and the query will fail, leaving you confused.

The connectors and and not are two of the fundamental elements of Prolog and behave like the elementary logic circuits of the same names, from which computers are built. You can also use the logical or connector, but it is not as common (most of its uses are dealt with by other means, as you'll see).

Any number of conditions can be strung together. For instance, if you wanted to find all flights from New York on Saturday after 4 p.m. except those going to Miami, you could make the following query:

```
&.which(_X to _Y: flight(_F New-
   York _Y (Sat _X) _A) and 16
   LESS _X and not(_Y EQ
   Miami)))
16.4 to Houston
No (more) answers
&.
```

Changing and Storing the Database

The primary database in Prolog is kept in RAM. All Prolog systems have ways of saving their databases in files and restoring them. Some also have ways of efficiently accessing databases stored on disk.

Let's look at some of the commands available for storing databases in the microProlog system. You can list a particular relation by typing LIST followed by

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the relation name, or you can type ALL for all current relations.

You can save the current workspace on disk by using the SAVE command in conjunction with a filename that is not the same as any relation. Because in microProlog uppercase and lowercase letters are distinctly different, it is all right to use the same name as a relation but in uppercase letters, for example, SAVE FLIGHT.

If you want to start a new database, you can delete all current relations by typing KILL ALL and reload another program saved on the disk with LOAD [*filename*]. Sequential and random access input/output are also available as aids to programming the database.

To edit a program, microProlog has several types of editors, depending on the size of the system. The simplest is a line editor similar to Microsoft BASIC, and the most elaborate is that found in the Macintosh version of Prolog.

If you look at the file of a microProlog program, you'll discover that the syntax is different from that presented in this article. It has an "internal" syntax similar to LISP. Don't worry, the simple front end takes care of the differences. It is possible to program in the internal syntax and even to invent your own internal syntax if one of those provided does not suit you.

Incorporating Rules into the Database

So far I have not incorporated any rules into the airline database. Rules can be used for such purposes as conducting an interactive dialogue and showing dependence. But here I will consider only rules that extend the database and allow users to capture "regularities" in the data.

It's easy to pick out regularities in airline schedules. Most flights have several stopovers, and departure and arrival times are repeated when each leg of a journey is described. For most airlines, the basic schedule is a daily one, with the same flight numbers used every day. But there are exceptions to these regularities. Often flights do not run on certain days of the week, and public holidays play havoc with the schedules.

If you are constructing a personal database for scheduling, it is worth recording a certain amount of detail—for example, the dates of public holidays—so that your database does not produce misleading information. Prolog rules form a highly convenient method of passing such information in a compact form. In constructing your database, you may need to layer it to distinguish the rules that are convenient for querying the database from those that are used for storing the data. (This is a methodological distinction, not a requirement of Prolog.)

First, you must store each stopover point separately and be able to bring together the starting point and destination when needed. The data must be organized as shown in table 4. The final column gives the direction the plane is traveling in so you don't have to cope with the complexities of local time zones, changes of day, etc., when deciding if PA51 goes from London to Houston or vice versa. Notice that the Concorde (flight BA193) arrives in New York earlier than it departs London (local time).

In table 4, "missing data" is represented by a dash (–) (this could be any other convenient symbol). Also, because you have to represent flights that run beyond midnight, some times (such as that for PA52) are greater than 24 hours.

We will now write a rule, similar to the original rule, that will construct a table from this new layout (ignoring at this point the question of flight frequency). This rule can be simply stated as shown in figure 1.

The rule can be easily understood in terms of the queries we have already considered. We interpret the three conditions after the if function as a query into the database. The conclusion, the flies expression, written at the beginning, corresponds to the answer template. But this time the conclusion forms a new relation that can be treated exactly like the database entries that composed it originally. It is, in fact, an "implicit" relation, behaving in this case somewhat like a "relational join" in database terminology.

continued

Table 4: *The normalized Prolog database.*

	Flight No.	City	Arrival	Departure	Order
&.accept calls					
	(PA51	London	—	(daily 10:00)	1)
calls.	(PA51	New-York	(daily 14:22)	(daily 16:40)	2)
calls.	(PA51	Houston	(daily 19:30)	(daily 20:30)	3)
calls.	(PA51	Mexico-City	(daily 22:35)	—	4)
calls.	(BA193	London	—	(daily 10:30)	1)
calls.	(BA193	New-York	(daily 09:20)	(M-Th 10:20)	2)
calls.	(BA193	Washington	(Tu Th 11:15)	—	3)
calls.	(BA193	Miami	(Mo We 11:50)	—	3)
calls.	(PA52	Mexico-City	—	(daily 09:00)	1)
calls.	(PA52	Houston	(daily 11:05)	(daily 12:35)	2)
calls.	(PA52	New-York	(daily 16:45)	(daily 19:00)	3)
calls.	(PA52	London	(daily 30:40)	—	4)
calls.	(BA192	New-York	—	(daily 09:30)	1)
calls.	(BA192	London	(daily 18:10)	—	2)
calls.end					
&.					

```
flies(__Flightnumber __From __To __Dep __Arr) if
calls(__Flightnumber __From __Arr1 __Dep __Stop1) and
calls(__Flightnumber __To __Arr __Dep2 __Stop2) and
__Stop1 LESS __Stop2 and
```

Figure 1: *The rule for constructing a new timetable.*

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To add a rule to the database, we use the add command, surrounding the whole clause with parentheses, as shown in figure 2.

You can make queries of the new relation identical to those for any other relation, such as: &.which(__F to __Dest: flies(__F New-York __Dest __D __A)).

So far, we have not made allowance for the different days of the week. Most airlines have their own codes for showing days of the week. Any of these could be used. Notice that in table 4 a single flight does not always follow the same route on each day of the week. For instance, after stopping in New York, the Concorde goes to Washington on Tuesdays and Thursdays and to Miami on Mondays and Wednesdays. The meaning of the codes can be expressed as database rules, as shown in figure 3.

```
&.add(flies(__Flightnumber __From __To __Dep __Arr) if
  calls(__Flightnumber __From __Arr1 __Dep __Stop1) and
  calls(__Flightnumber __To __Arr __Dep2 __Stop2) and
  __Stop1 LESS __Stop2)
```

Figure 2: *Adding a new rule to the database.*

```
days(__X __Y) if day(__X __Y)
days(daily __X) if day(__Y __X)
days(M-TH __X) if day(MoWe __X)
days(M-TH __X) if day(TuTH __X)

day(MoWe    Monday)
day(TuTH    Tuesday)
day(MoWe    Wednesday)
day(TuTH    Thursday)
day(Fr -    Friday)
day(Wend    Saturday)
day(Wend    Sunday)
```

Figure 3: *Database rule for expressing days of the week.*

```
.&which(__Day: flies(__F London Washington (__FreqD __TimeD)
  (__FreqA __TimeA)) and days(__FreqD __Day) and
  days(__FreqA __Day))
Tuesday
Thursday
No (more) answers
&.
```

Figure 4: *Using the* days *relation to check the Concorde schedule from London to Washington.*

```
flight(__Flight __From __To (__Day __TimeD) (__Day TimeA)) if
flies(__Flight __From __To (__FreqD __Time)) (__FreqA __TimeA) and
days(__FreqD __Day) and days(__FreqA __Day) and __TimeA LESS 24

flight(__Flight __From __To (__Day __TimeD) (__Next __ TimeAr)) if
flies(__Flight __From __To (__FreqD __Time) (__FreqA __TimeA)) and
days(__FreqD __Day) and days(__FreqA . . . ) and 24 LE __TimeA and
next(__Day __Next) and __TimeAr = (__TimeA-24)

next(Monday       Tuesday)
next(Tuesday      Wednesday)
next(Wednesday    Thursday)
next(Thursday     Friday)
next(Friday       Saturday)
next(Saturday     Sunday)
next(Sunday       Monday)
```

Figure 5: *Rules for determining days of the week.*

This example shows how easily tables can be nested and made to include other tables. The first rule of days says that all instances of day are also days. In fact, the use of the second relation day is strictly unnecessary. You can make the conditions of a rule refer to the rule itself (recursion), but then you have to be careful that you don't introduce circularities. For instance, if you check which days correspond to "daily," the program in figure 3 will generate every day of the week exactly once. If, however, you include the rule days(daily __X) if days(__Y __X), you would get an infinite number of results!

Prolog uses the rules it has to generate more answers without checking to see whether it has already produced the same answer. In general, it is wise to avoid recursive definitions in database situations.

Let us use the days relation (see figure 4) to ask which days of the week the Concorde flies from London to Washington. Trace through the execution of this query. The relation __FreqD is bound to daily and __FreqA is bound to TuTH. Thus the first call to days will generate seven solutions for __Day, but only two of them are acceptable to the second call.

Prolog deals with the goals from left to right, solving all the subgoals of a goal before going to the next goal. If the program fails at any point, it returns to a previously solved goal and tries to find another solution.

One important part of the timetable has been neglected so far. Flights often start on one day and finish on the next, especially those going from west to east. To allow for this, we have continued the 24-hour clock into the next day where necessary, and we must now convert these times to normalized day times of day.

The complete program for a flight now has two separate cases (shown in figure 5). The use of several rules instead of an or or if. . .then. . .else construct (as demonstrated in figure 5) is one feature of the Prolog style that separates it from other languages. Conventional programming constructs are available in Prolog, but they do not necessarily lead to clearer programs (though sometimes they are

continued

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Prolog is highly interactive, but strategy still depends on the programmer.

desired for efficiency). Try recoding flight to see what I mean. Remember that you cannot "change" the value of a variable. You will have to introduce new ones. Another way to improve efficiency (so that flies is not evaluated twice) is to introduce a subsidiary relation.

Connecting Flights

It should now be easy to see how to handle connecting flights in this database. You need to find two flights that go via an intermediate point so that there is sufficient time to change planes but not too long a stopover. A program that does this is given in figure 6. Again, you must allow for two cases in reasonable because it is always possible to make the change over midnight (across a Day boundary). Notice that the relation flight is used to work out the exact days of the week so that frequency of different flights is taken into account. When you are dealing with relations, you can assume that all possible answers are returned.

The relation ok depends only on the time difference, but it could easily be extended to deal with different airports, airlines, etc. If the time differences are not exact hours, you must take more care with the subtraction because minutes have been expressed as hundredths of hours.

Evaluating Prolog Queries

In many of the examples, I have used the which command to generate all the solutions to a query. This is normally the appropriate method for a database, and I have been careful to ensure that the programs are finite.

However, Prolog does not operate in the normal style of databases. The common database technique for finding all connecting flights is to take all the solutions to the first leg and all the solutions to the second leg and find the "join" of these two sets. Since there are probably thousands of flights in a week, this is an expensive operation.

Prolog does it differently by attempting to find one solution first to each subgoal, proceeding strictly from left to right. If it fails, it backtracks and attempts to find another way through. In most databases, where only a small fraction of even the first subgoal meets the criteria, this leads to substantial saving of program run time.

But there is another factor. At each stage, Prolog keeps the most general solution. In figure 5, it will not settle on the day of the week until it reaches the days predicate. Thus when Prolog does backtrack, it usually doesn't have far to go. These two features make it much more efficient than many comparable strategies.

This does not mean that there is no skill involved in ordering the subgoals sensibly within a procedure. Prolog is a programming language and the strategy is left to the programmer. But because it is a highly interactive language, it is possible to test out your ideas immediately, and after a little practice most people have little trouble predicting where the inefficiencies lie. Ironically, people with a strong mathematical or logical background and programmers who immediately look for the familiar assignment statement often have the most trouble with Prolog.

The left-to-right strategy is very successful on sequential-logic machines, in part because it leads to an efficient stack-based memory management strategy. On parallel-architecture machines other strategies may be far more successful.

```
schedule( (_Flight change at _Int for _Flight2) _From _To
_Depart _Arrive) if flight(_Flight _From _Int _Depart
_IntArr) and flight(_Flight2 _Int _To _IntDep _Arrive) and
reasonable(_IntArr _IntDep _Int)

reasonable( (_Day _TimeA) (_Day _TimeD) _Port) if _Diff =
(_TimeD - _TimeA) and ok(_Diff)

reasonable( (_Day _TimeA) (_Next _TimeD) _Port) if next(_Day
_Next) and _Diff = (_TimeD - _TimeA + 24) and ok(_Diff)

ok(_Wait) if 1.0 LESS _Wait and _Wait LESS 4.0
```

Figure 6: *Program used to determine stopover times between connecting flights.*

```
Here is the "flies" predicate written in the "Edinburgh" style.

flies(Flight, From, To, [Day1,Dep], [Day2,Arr]) :-
calls(Flight, From, -, [Day1,Dep], D1), calls(Flight, To,
[Day2,Arr], -, D2), D1 < D2.

And here is the "flies" predicate written in the "Waterloo" style.

flies(Flight, From, To, Day1.Dep.[ ], Day2.Arr.[ ]) <-
calls(Flight, From, no. Day1.Dep.[ ], D1) & calls(Flight, To,
Day2.Arr.[ ], no. D2) & D1 < D2.
```

Figure 7: *A comparison of the Edinburgh and Waterloo syntaxes using the* flies *predicate.*

Other Versions of Prolog

Like all popular languages, Prolog is acquiring many different dialects. I know of over thirty systems. In some ways the different versions are less dissimilar than is the case with other languages because they all possess a common evaluation mechanism and underlying semantics even though their syntaxes can be very different.

The two most popular forms are the "Edinburgh" syntax and the "Waterloo" syntax. The Edinburgh syntax was originally written for the Digital Equipment Corporation PDP-10, but it is now available on Digital's VAX computers and many other machines. The Waterloo syntax was originally written for IBM mainframes. (See figure 7.)

Prolog variables are written with capitals, though an underscore or asterisk prefix may be allowed. Constants must start with lowercase letters unless they are enclosed in single quotation marks. List notation is distinguished from a function or relation call, whereas in microProlog only lists are used. Commas abound and serve several functions, especially in the Edinburgh syntax.

Moves are underway in the U.K. to standardize the different dialects of Prolog and bridge the gaps before they become a serious handicap to the development of software. The process is not helped by the unclear meaning of the more "impure" Prolog features, which I have intentionally avoided here. ■

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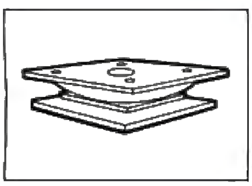

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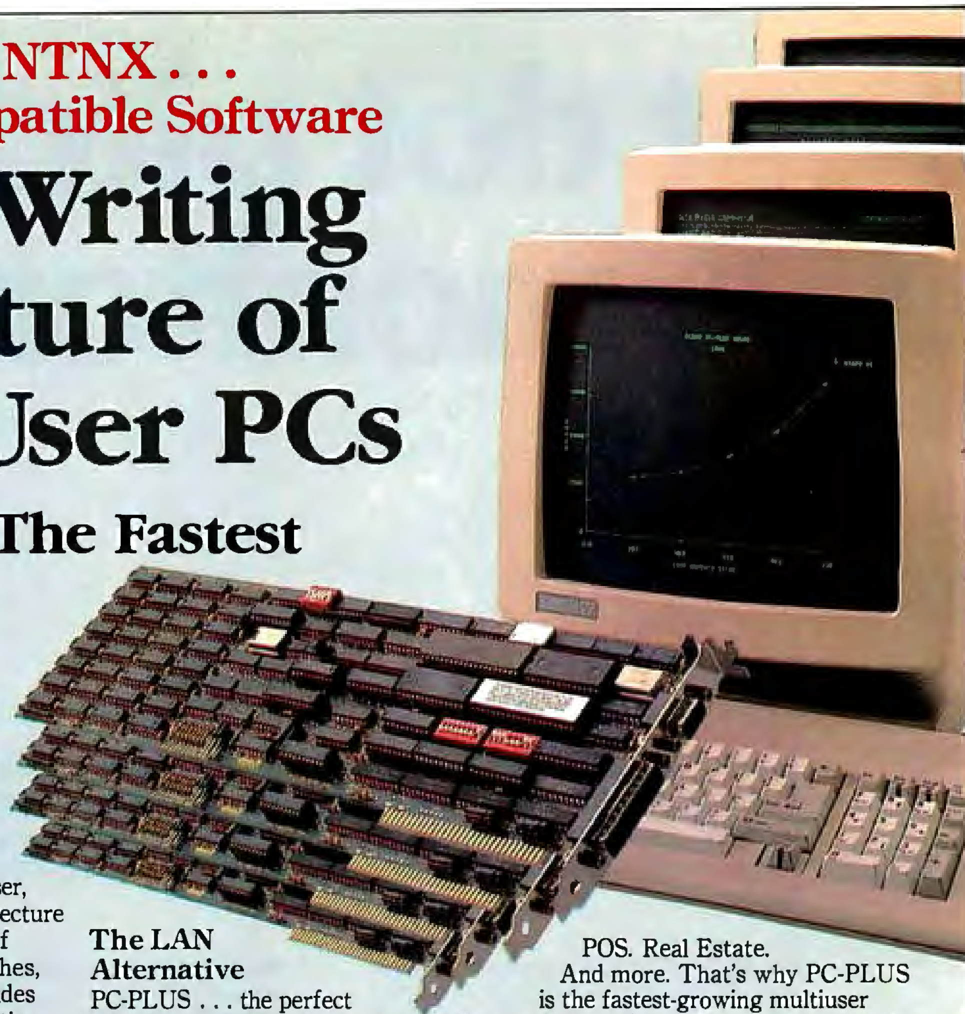

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Gregg Williams

An Introduction to Relaxation Methods

An unusual numeric technique for solving physics problems

Computers help many of us in our work, but no two groups benefit more from their use than scientists and engineers. Both professions deal with the endless manipulation of numbers, and computers have given them the ability to manipulate more numbers with greater accuracy. In particular, both groups deal frequently with situations governed by ordinary and partial differential equations. These equations are often difficult to solve algebraically, but when a specific answer (instead of a general solution) is sufficient, computers can usually deliver it with any practical degree of accuracy.

A numeric technique called the *relaxation method* is not well known, but it is very useful in solving such matters as systems of simultaneous equations, framework problems (where you find the equilibrium position of a flexible framework given certain forces at each joint), and beam-deflection problems. In this article, I will concentrate on the method's most interesting use, the solution of two-dimensional systems that can be described by Poisson's equation:

$$\frac{\delta^2 w}{\delta x^2} + \frac{\delta^2 w}{\delta y^2} + W(x,y) = 0.$$

I will focus on a special case, Laplace's equation, where the condition $W(x,y)=0$ gives the equation

$$\frac{\delta^2 w}{\delta x^2} + \frac{\delta^2 w}{\delta y^2} = 0.$$

This partial differential equation describes the behavior of many two-dimensional systems, like the distribution of electric potential in a region of constant resistivity or the distribution of stress in a cylinder being twisted. The simplest and most intuitive application of the relaxation method is in determining the internal temperatures of a homogeneous solid presented with given fixed temperatures on its surfaces.

An Intuitive Explanation

In the context of heat traveling through a homogeneous cross section, it is simple to describe the relaxation method intuitively. (See "Formal Derivation of the Relaxation Equation" on page 112.) First, superimpose a square grid on the cross section and note the (unchanging) temperatures at its edges. It is intuitively plausible that the center node in figure 1a is stable (points of the cross sections will be referred to as *nodes* and their corresponding array entries as *elements*): Its value, 13, is the average of its adjacent nodes. This can be stated as an equation in two ways:

$$w_0 = \tfrac{1}{4} (w_1 + w_2 + w_3 + w_4)$$

continued

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ILLUSTRATION BY KYLE SKRINAK

or

error $F_0 = \frac{1}{4}(w_1 + w_2 + w_3 + w_4) - w_0$.

In the case of figure 1a, the error is 0. The center node in figure 1b, however, is given by

$F_0 = \frac{1}{4}(17 + 10 + 9 + 16) - 12 = 1$

and it is plausible that the error should indicate the magnitude and direction of the needed correction. If we think of the error as "tension" in the system, the relaxation method is one that causes nodes to iteratively "relax" toward equilibrium. To help match the literature, we should change the preceding error equation to

$F_0 = (w_1 + w_2 + w_3 + w_4) - 4w_0$

or

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0,$$

where F_0 is the error, Σw_n is the sum of w_1 through w_4, and the nodes are labeled as in figure 1a.

The preceding equation is for situations governed by Laplace's equation. The corresponding equation for situations governed by Poisson's equation, where each node w_i has an inherent value W_i, is

$$F_0 = \sum_{n=1}^{4} w_n - 4w_i + h^2W_i,$$

where h is the distance between two adjacent nodes (also called the *unit grid size*).

Formal Derivation of the Relaxation Algorithm

The relaxation method for solving

$$\frac{\partial^2 w}{\partial x^2} : \frac{\partial^2 w}{\partial y^2} + W(x,y) = 0$$

is based on approximating the two partial derivations by combinations of the terms w_0 through w_4. Start by approximating the ordinary derivative dw/dx. The function w at a point x near x_0 is given by the Taylor's series expansion:

$$w = w_0 + \left(\frac{dw}{dx}\right)_0 (x - x_0)$$
$$\frac{1}{2!}\left(\frac{d^2w}{dx^2}\right)_0 (x - x_0)^2$$
$$+ \frac{1}{3!}\left(\frac{d^3w}{dx^3}\right)_0 (x - x_0)^3$$
$$+ \frac{1}{4!}\left(\frac{}{dx^4}\right)_0 (x - x_0)^4 + \ldots$$

By substituting the values $w_1 = x + h$ and $w_1 = x - h$ into this, we get

$$w = w_0 + h\left(\frac{dw}{dx}\right)_0 + \frac{h^2}{2}\left(\frac{d^2w}{dx^2}\right)_0$$
$$+ \frac{h^3}{6}\left(\frac{d^3w}{dx^3}\right)_0 + \frac{h^4}{24}\left(\frac{d^4w}{dx^4}\right)_0 + \ldots$$

and

$$w_3 = w_0 - h\left(\frac{dw}{dx}\right)_0 + \frac{h^2}{2}\left(\frac{d^2w}{dx^2}\right)_0$$
$$- \frac{}{6}\left(\frac{}{dx^3}\right)_0 + \frac{h^4}{24}\left(\frac{}{dx^4}\right)_0 - \ldots$$

Adding these together, we get

$$w_1 + w_3 = 2w_0 + h^2\left(\frac{d^2w}{dx^2}\right)_0 + O(h^4),$$

where $O(h^4)$ is a term that includes the fourth, sixth, and higher order terms; for a suitably chosen h, this term is small enough to ignore. Rearranging the equation, we get

$$h^2\left(\frac{d^2w}{dx^2}\right)_0 = w_1 + w_3 - 2w_0.$$

When we transfer this approximation to two dimensions, we get the two equations

$$h^2\left(\frac{\partial^2 w}{\partial x^2}\right)_0 = w_1 + w_3 - 2w_0$$

and

$$h^2\left(\frac{\partial^2 w}{\partial y^2}\right)_0 = w_2 + w_4 - 2w_0$$

(the ds change to ∂s because the ordinary differential terms become partial differential terms). These are called finite difference equations because they approximate a derivative by the difference of nearby points.

Multiplying the original Poisson's equation by h^2 and substituting the two difference equations into it, we get

$$(w_1 + w_3 - 2w_0) + (w_2 + w_4 - 2w_0) + h^2W_0 = 0$$

or

$$\sum_{n=1}^{4} w_n - 4w_0\, h^2W_0 = 0,$$

which has an error of $O(h^4)$. If node 0 does not have its true value, we define the error function F_0 as

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0 + h^2W_0.$$

In the simpler Laplace's equation, where $W(x,y) = 0$, this becomes

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0.$$

The Relaxation Algorithm

Let us say we have a two-dimensional array NODE (I,J), whose elements represent the temperatures of the cross section. If the array has MROWS rows and MCOLS columns, the edge elements (all elements in rows 1 and MROWS and columns 1 and MCOLS) represent the unchanging boundary temperatures, and all the rest represent the internal nodes that we are working on. Let us also define an array of the same size, RESID(I,J), that has the value 0 for boundary nodes and the error function F_0 for all internal nodes. From the above equation and figure 1, it's apparent that if we change the temperature of an internal node by 1 degree (i.e., increase NODE(I,J) by 1), its error function (in RESID(I,J)) goes down by 4 and the error functions of all adjacent internal nodes each increase by 1; the RESID values of edge nodes remain at 0 because their temperatures are fixed. Pictorially, we represent this set of relationships as in figure 2; the values inside the circles are the changes to the RESID array, and the +1 outside the center node represents the change to the corresponding NODE element.

With that in mind, the relaxation program goes as follows:

1. Define the NODE array.
2. Calculate the RESID array from the equation for F_0 and the NODE array.
3. See if the computations are finished and repeat as long as they are not:
   a. Find the element with the greatest RESID value,
   b. "Relax" that element to 0.
4. Print the answer (the NODE array).

One important detail not specified by the preceding algorithm is the determination of when the computations are finished. In most numerical analysis algorithms, we halt the computation for N decimal places of accuracy when the absolute value of the error function becomes smaller than $5 \times 10^{-(N+1)}$. We do that for each interior element in the NODE array (i.e., we wait until the absolute values of all the RESID elements are less than $5 \times 10^{-(N+1)}$), but we also monitor the sum of all the RESID elements until its absolute value is less than a given quantity. If the errors are on both sides of 0, they will add to a number near 0; if they are not, we will get a larger positive or negative number that indicates that we need to do additional relaxation to "fine-tune" the system. For our purposes, we will look for the sum of all RESID elements to be less than 10^{-N}.

In summary, the relaxation algorithm is finished when

$$\text{RESID(I,J)} < 5 \times 10^{-(N+1)}$$

for all interior elements of NODE and $\sum_I \sum_J \text{RESID(I,J)} < 10^{-N}$.

An Example

With two Applesoft BASIC programs, we can experiment with relaxation problems. [Editor's note: *The two programs plus a help file are available on disk, in print, and on BIX under the names RELX1.BAS, RELX2.BAS, and RELXH.TXT. See the insert card after page 424. Listings are also available on BYTEnet. See page 4.*] We will start with the 5 by 5 NODE array shown in table 1a (which also shows the RESID-error array associated with it). When I started the RELAXN program, I specified one decimal place of accuracy. This means that the program will not finish until all RESID elements are between −0.05 and 0.05, and the sum of all the RESID elements is between −0.1 and 0.1. I have written the program so that the printouts of NODE and RESID round and display to one more decimal place of accuracy than is specified; in this case, all numbers will be shown rounded to the nearest hundredth, but their true values are the same values, rounded to the nearest tenth.

Looking at RESID, we see that the largest error is 40, at element (3,4). To reduce this to 0, we must add 10 to NODE(3,4), which means that RESID (3,4) becomes 40 +(−4 × 10), or 0, and that RESID(2,4) and RESID(3,3) are increased by 10 each. The other two neighboring nodes, RESID(3,5) and RESID(4,4), do not change because they are boundary nodes. The resulting NODE and RESID arrays are shown in table 1b.

After 10 iterations, the NODE values look closer to being correct, and the RESID values are smaller and more evenly spread through the interior nodes (see table 1c). The program stops after 53 relaxations (see table 1d); the largest-magnitude RESID is 0.0176 (a value that is printed out at the end, even though it is rounded in the RESID array to 0.02), and the sum of the RESID array is 0.0864. In general, the RESID sum criterion is fulfilled long after the largest-magnitude criterion has been fulfilled. Here, the algorithm could have stopped when the largest-magnitude RESID value was 0.05. Because it went on to 0.0176, I am more comfortable that the NODE values are correct to one decimal place, as specified. (The NODE values in table 1d must be rounded to one decimal place.)

Block Relaxation

At the beginning of a relaxation solution, RESID values often gather in one area. When this happens, the unmodified relaxation algorithm can take hundreds of steps to distribute them across the array. Also, it turns out that the relaxations of adjacent nodes cancel each other out, making this point-by-point relaxation very inefficient. It is possible to create relaxation templates that specify the net effect of a unit change to a rectangular array of nodes instead of a single node. If we combine the results of relaxing three nodes in a straight line, we get the relaxation template of figure 3a. The dotted oval marked +1 around the three nodes indicates that the NODE value of these three nodes should be increased by +1 each; the values in each circle are the amounts to be added to each RESID element. Figure 3b shows a larger example, that of 3 by 4 block relaxation.

Figure 3c shows the generalization of block relaxation to an m by n block. (The 1 by n block is an exception to the algorithm below; its construction can be inferred from figure 3a.) To find the template for a given block, we must

1. Draw a dotted oval around the block and label it +1. Each node inside the dotted oval should have 1 added to its NODE element.
2. Draw all the neighboring nodes that are outside the block; this should be two nodes each for the four corner nodes and one node each for the nodes on the edge of the block. Label each outside node with a 1. These nodes will have their RESID elements increased by that amount.
3. For each edge node that has one neighboring node outside the block, place a −1 in that circle. For each corner node that has two neighboring nodes outside the block, place a −2 in that circle. For each interior node that has all its neighbors inside the block, place a 0 in that circle. These nodes will have their RESID elements increased by −1, −2, and 0, respectively.

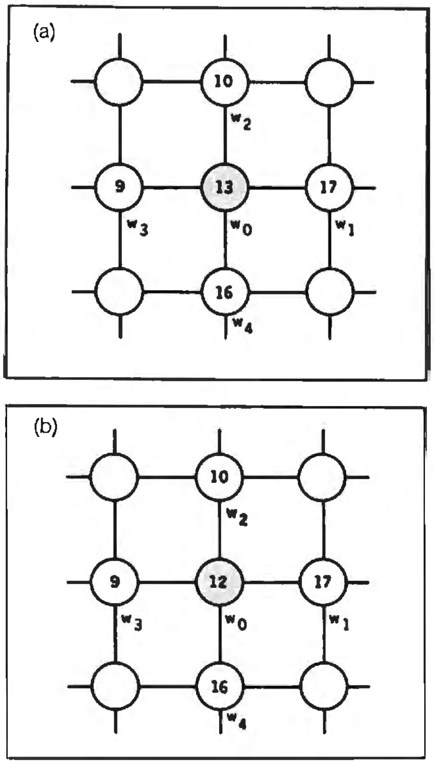

Figure 1: *An intuitive analysis of node interrelationships. With a little arithmetic, we can see that node w_0 in figure 1a (red) is correct because its value is the average of its four neighbors. Node w_0 in figure 1b is not correct because it is less than the average of its neighbors.*

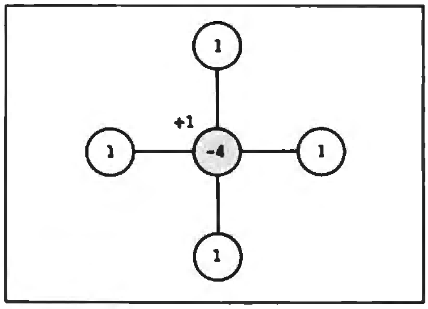

Figure 2: *The basic node relaxation template, which is read as follows: When the node value of the center (red) node is increased by 1, its error value is decreased by 4 and the error values of its neighbors are each increased by 1. See the text for further details.*

Doing point relaxations of an m by n block changes $5mn$ array values. Doing a block relaxation of the same block changes $mn+4(m+n-1)$ array values. If you look at the template of figure 3c, you will realize that an m by n block relaxation takes $2m+2n$ units out of its edges

continued

Table 1: *An example of the relaxation method. Table 1a shows the beginning NODE array and the RESID array calculated from it. The cross section of the solid being modeled is a rectangle with a corner cut off. In this example, the inactive elements are marked by a −1 in the NODE array. The relaxation will be carried out to one decimal place of accuracy. The red element, element (3,4), is the first to be relaxed because its RESID value has the largest absolute value in the RESID array. Table 1b shows the NODE and RESID arrays after relaxing element (3,4). To decrease the RESID of 40 to 0, increase the NODE value from 0 to 10. The RESID values of elements (3,4) and its neighbors (red) change according to the template of figure 2, except that elements (3,5) and (4,4) (blue) do not change because they are border elements. Table 1c shows the arrays after 10 iterations. Table 1d shows the arrays for the solved cross section, which occurs after 53 point relaxations. The NODE values should be rounded to one decimal place. The sum of the RESID elements is 0.0864 and the largest-magnitude value is 0.0176; these are less than the maximum error values for one decimal place of accuracy, 0.1 and 0.05, respectively. (The 0.0864 and 0.0176 values do not show up in the RESID array as shown because its elements have been rounded to two decimal places.)*

(a) NODE array is:

−10	−10	−10	−10	−10
10	0	0	0	10
10	0	0	0	10
10	0	0	30	−1
−10	−10	−10	−1	−1

RESID array is:

0	0	0	0	0
0	0	−10	0	0
0	10	0	40	0
0	0	20	0	0
0	0	0	0	0

(b) NODE array is:

−10	−10	−10	−10	−10
10	0	0	0	10
10	0	0	10	10
10	0	0	30	−1
−10	−10	−10	−1	−1

RESID array is:

0	0	0	0	0
0	0	−10	10	0
0	10	10	0	0
0	0	20	0	0
0	0	0	0	0

(c) NODE array is:

−10.00	−10.00	−10.00	−10.00	−10.00
10.00	0.00	0.00	2.50	10.00
10.00	4.37	5.37	11.56	10.00
10.00	2.11	6.46	30.00	−1.00
−10.00	−10.00	−10.00	−1.00	−1.00

RESID array is:

0.00	0.00	0.00	0.00	0.00
0.00	4.37	−2.13	1.56	0.00
0.00	0.00	0.93	1.62	0.00
0.00	2.40	1.62	0.00	0.00
0.00	0.00	0.00	0.00	0.00

(d) NODE array is:

−10.00	−10.00	−10.00	−10.00	−10.00
10.00	1.33	0.18	3.13	10.00
10.00	5.18	6.26	12.35	10.00
10.00	3.13	7.34	30.00	−1.00
−10.00	−10.00	−10.00	−1.00	−1.00

RESID array is:

0.00	0.00	0.00	0.00	0.00
0.00	0.02	0.01	0.02	0.00
0.00	0.00	0.02	0.00	0.00
0.00	0.02	0.01	0.00	0.00
0.00	0.00	0.00	0.00	0.00

and transfers them to the layer of nodes surrounding it.

How should we use a block relaxation template? By what number should we relax each node in the block to get the best effect overall? One approach is to relax the block so that the sum of the errors in that block becomes 0. Suppose the sum of all the RESID elements in the block (call this the *RESID sum*) is S. Each unit of block relaxation reduces that sum by $(2m+2n)$ units. Thus, if we relax the system by $S/(2m+2n)$ units, the RESID sum for that block will be 0.

Often, the beginning RESID array shows a heavy concentration of errors either around the edges of the array or in the center. One of two operations, *blocking in* or *blocking out*, can distribute the error more over the entire array and at the same time zero out the RESID sum of a block of the array, thereby facilitating the overall solution. Blocking in consists of doing block relaxations over increasingly smaller, concentric blocks—for example, block relaxations over a 6 by 8 block, then the 4 by 6 block in its center, then the 2 by 4 block in its center. Blocking out is the reverse process and, strangely enough, both processes end in identical results.

Table 2 shows an example of blocking in. Table 2a shows the NODE and RESID values for a 7 by 5 array. The largest block we can work on, in this case, is the entire interior of the array, from element (2,2) to element (6,4). In table 2a, the RESID sum of the cross section is −118, and there is a pretty heavy ring of negative values around its edge. After doing two block relaxations by the above algorithm (with results accurate to one decimal place), the first with the block from (3,3) to (5,3) and the second with the block from (2,2) to (6,4), we get the results shown in table 2b. It is easy to see that individual RESID values are, in general, less extreme than they are in table 2a. What is not so obvious, though, is that the RESID sum of both blocks is exactly 0 (the larger block actually adds to 0.3 because of roundoff errors in the printing of the RESID array).

Solving the NODE array of table 2a

continued

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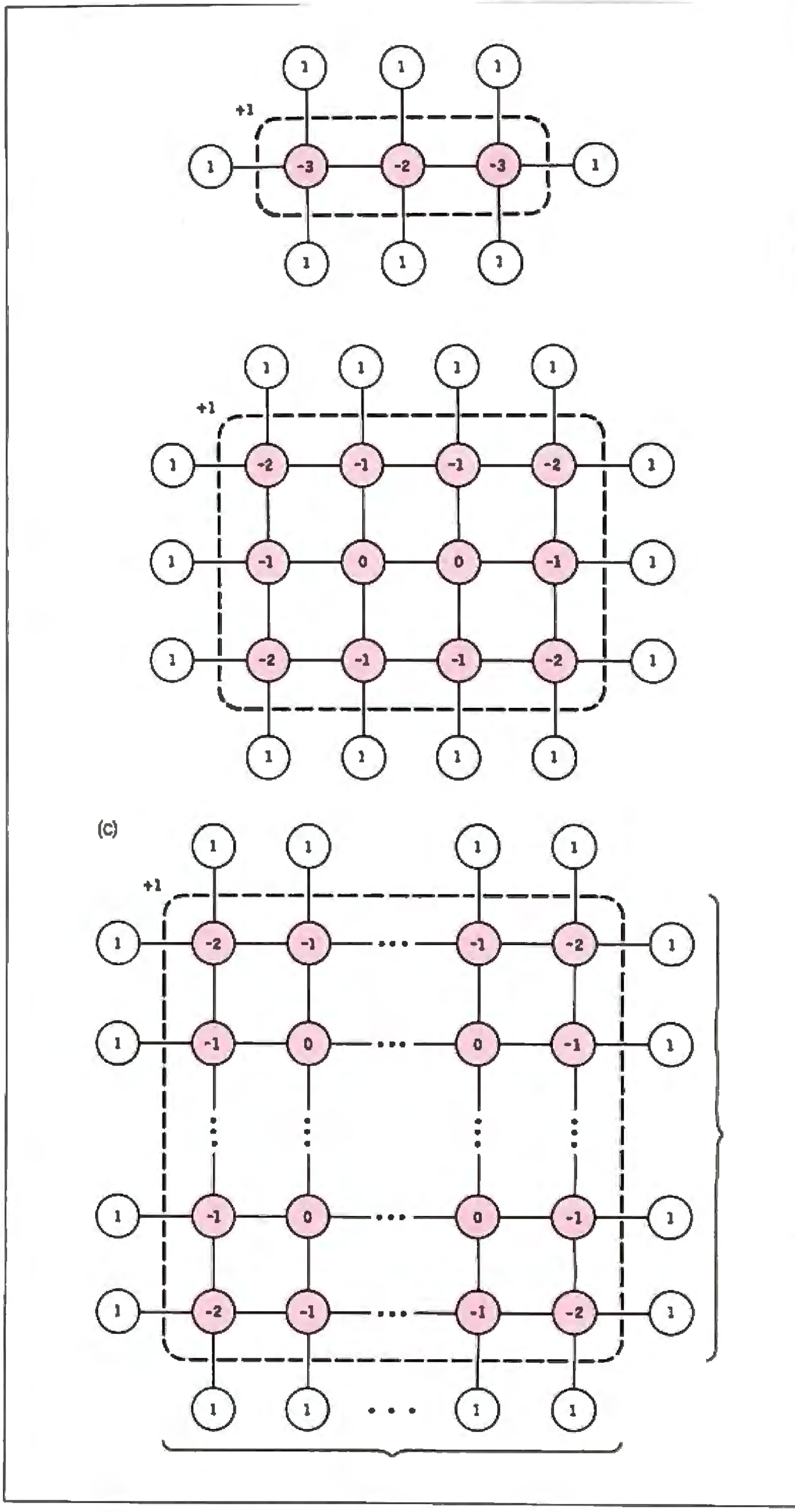

Figure 3: *An example of block relaxation. By relaxing a block of nodes at once, we can eliminate redundant computations and greatly facilitate the solution of the cross section. The three figures show the templates for 1 by 3, 3 by 4, and m by n blocks. In all cases, each red node has its NODE value increased by 1, and all nodes have their RESID values changed by the amount shown inside the circles. See the text for the details on constructing an m by n block template.*

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2201 Lively Boulevard, Elk Grove Village, IL 60007, Phone: 312/364-1180 TLX: 280-803 both with and without blocking out gives us some measure of its utility. Without block relaxation, this array is solved to one decimal place in 196 point relaxations (or 980 changes to arrays); with block relaxation, it is solved in two block relaxations and 153 point iterations (or 823 changes to arrays). The difference here is modest, but it increases with the size of the block.

Moving to a Finer Grid

When we get the results of a cross-section problem, how do we know how accurate it is? Just because we have taken a problem out to three decimal places does not mean that it is accurate to that amount. One indicator of accuracy is the finite difference equation on which the relaxation algorithm is based (see the text box "Formal Derivation of the Relaxation Algorithm" on page 112). The Taylor's series expansions of

$$\frac{\partial^2 w}{\partial x^2} \text{ and } \frac{\partial^2 w}{\partial y^2}$$

each have error terms of $O(h^4)$, where h is the unit grid size. This means the total error is no greater than Kh^4 for some (unknown) K and all h smaller than a given h_0. This is known in mathematics as the "big-oh" notation; for a more complete explanation, see *The Art of Computer Programming, Volume 1: Fundamental Algorithms*, 2nd ed., by Donald E. Knuth (Addison-Wesley, 1975, page 104). In simpler terms, this means that we can achieve a given desired accuracy with a sufficiently small h. Although this does not tell us as much as we would like to know, it does say that the accuracy, whatever it is, improves to the fourth power of the change in h; if we halve the grid size, our results will be 2^4, or 16, times more accurate.

We can begin to gauge the accuracy of our results by halving our grid size and solving the same cross section. Given a desired grid size for a cross section, you should solve a coarser grid, transfer the answers to every other node in the finer cross section, interpolate unknown values from known ones, and solve the finer cross section; if you solve the finer grid from scratch, the solution will take more time. For example, I solved a 5 by 5 array in 60 iterations, expanded it, and solved the resulting 9 by 9 array in 126 iterations. The same 9 by 9 array, solved by itself, took 1242 iterations.

The easiest method of solving a cross section goes like this: First, solve the cross section at the desired grid size and accuracy; then keep halving the grid size and solving until the corresponding node values no longer change between one grid and its next smaller counterpart; then take all the node values of the next-to-last grid as being correct to the desired accuracy.

Although the method just described will definitely produce accurate results, it may be impractical to solve that many grids: Remember, each finer grid has four times the number of nodes of its predecessor. Given the solutions of a cross section and the next two cross sections resulting from half- and quarter-size grids, we can estimate the true value of a node and, from that, the approximate error in the most accurate guess. Let the three values of a given node be called w_c, w_m, and w_f (c, m, and f stand for "coarse," "medium," and "fine"), and let w_t be the (unknown) true value. If we assume that the ratio of errors between any two consecutive grid sizes is the same, which is reasonable given that the error is $O(h^4)$, we can estimate w_t (call this estimate w_e) from the equation

$$\frac{w_c - w_e}{w_m - w_e} = \frac{w_m - w_e}{w_f - w_e}.$$

Solving this for w_e, we get

$$w_e = \frac{w_c w_f - w_m^2}{w_c + w_f - 2w_m}.$$

If we take w_e as a good approximation of w_t, we can assume that the error from the finest net, w_f, is *approximately* equal to $(w_f - w_e)/w_e$.

For example, let us suppose that the values (to one decimal place) of a given node are 64.1, 55.5, and 53.9 for cross sections solved with grid sizes that are 0.5, 0.25, and 0.125, respectively. Then the value of w_e is

$$w_e = \frac{(64.1)(53.9) - (55.5)^2}{64.1 + 53.9 - (2)(55.5)}$$
$$= \frac{374.74}{7.0} = 53.534$$

$= 53.5$ (rounded to one decimal place).

The error is approximately

continued

Table 2: *An example of blocking out. Table 2a shows the NODE and RESID arrays for a 7 by 5 cross section; note the large values in the red ring. After blocking out the block from (3,3) to (5,3), then the block from (2,2) to (6,4) (see table 1b), the sum of the RESID values in both blocks is 0, and the RESID values are more evenly distributed than they were before the blocking out. Compare the red values in tables 2a and 2b.*

(a) NODE array is:

−10	−10	−10	−10	30
10	14	19	26	30
10	14	19	26	30
10	14	19	26	30
10	14	19	26	30
10	14	19	26	30
−10	0	10	20	30

RESID array is:

0	0	0	0	0
0				0
0	1			0
0				0
0				0
0				0
0	0	0	0	0

(b) NODE array is:

−10.00	−10.00	−10.00	−10.00	30.00
10.00	6.63	11.63	18.63	30.00
10.00	6.63	12.38	18.63	30.00
10.00	6.63	12.38	18.63	30.00
10.00	6.63	12.38	18.63	30.00
10.00	6.63	11.63	18.63	30.00
−10.00	0.00	10.00	20.00	30.00

RESID array is:

0.00				0.00
0.00				0.00
0.00		−0.25		0.00
0.00		0.50		0.00
0.00		−0.25		0.00
0.00				0.00
0.00				0.00

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$$\frac{53.9 - 53.5}{53.5} = 0.0075.$$

We can say, then, that the answer of 53.5 is probably correct to within 1 percent.

Curved Boundaries

Cross sections with curved boundaries present a problem when using the relaxation method. One solution is to use a fine enough grid so that the boundary is "close enough" (whatever that means subjectively) to the grid nodes. However, this informal solution is probably not good enough when values close to the surface are important. For such situations, we can use a modified node template.

Start with the node diagram of figure 4a, which shows a node that is closer to the boundary than the grid size h. Suppose that the node normally at node 1 is outside the cross section and that the arm connecting nodes 0 and 1 intersects the boundary at w_B at a distance of ξh, where $0 < \xi < 1$. (This figure and the corresponding templates can be rotated to take care of situations where the boundary truncates one of the other arms.)

By doing a Taylor's expansion of w in powers of $(x - x_0)$ and substituting $(x_0 + \xi h)$ for w_1 and $(x_0 - h)$ for w_3, we get an approximation of $\partial^2 w/\partial x^2$ that gives us the template of figure 4b for node 0 and that of figure 4c for node 3; nodes 2 and 4 are affected only if any neighbor nodes are less than h units away. (For the derivations of these templates, see page 65 of *Relaxation Methods* by D. N. de G. Allen, McGraw-Hill, 1954.) You will get maximal accuracy by using these templates at the appropriate nodes, but they are somewhat less precise than the standard template of figure 2; the equation leading to the former has an error term of $O(h^3)$, while that of the latter (as discussed before) has an error term of $O(h^4)$.

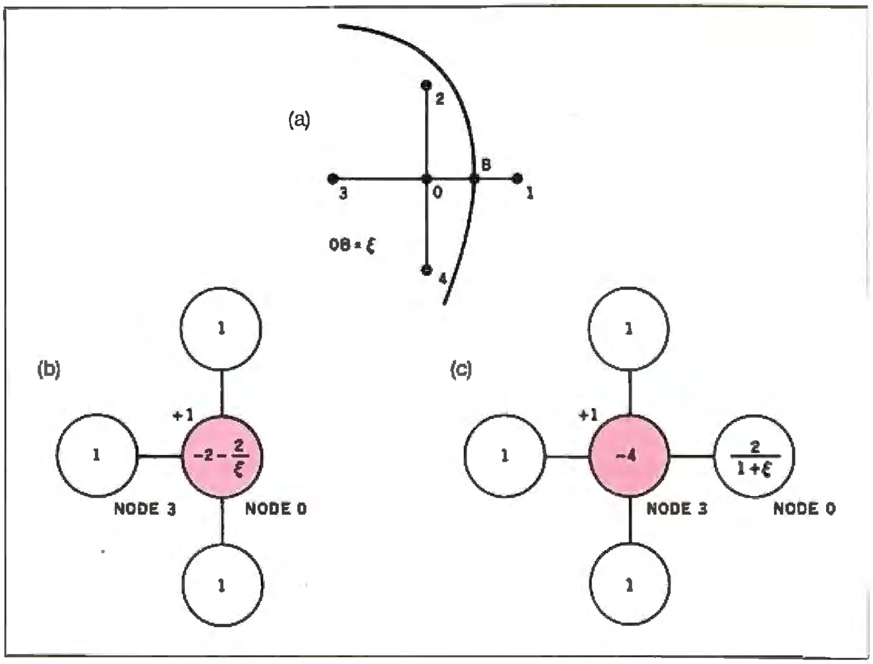

Figure 4: *An example of dealing with a curved boundary. When the boundary of a cross section comes between the node points on the superimposed grid (4a), we must use modified templates for node 0 (4b) and node 3 (4c).*

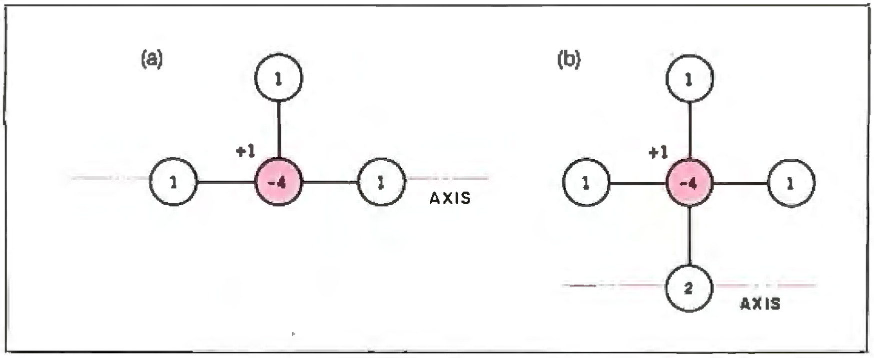

Figure 5: *Symmetry in one dimension. When you relax only the unique half of a symmetrical cross section, the relaxation template changes for a node on the axis of symmetry (5a) or one node away from the axis (5b).*

Symmetry

Often, a cross section is symmetrical about one or two axes. When this is the case, you can modify the relaxation templates for nodes near or on the line of symmetry and work on only half or one-quarter of the number of nodes you normally would. For cross sections with one axis of symmetry, use the template in figure 5a for nodes on the axis and figure 5b for nodes one node away from the axis. For cross sections with two (perpendicular) axes of symmetry, use the templates in figures 6a through 6c in the appropriate situations (remember that the node being relaxed is the one marked +1); for nodes that have all neighbor nodes along only one axis, use the templates of figures 5a and 5b. If you visualize the unshown reflected nodes, you will see why certain neighbor nodes have values of 2. All templates in figures 5 and 6 can be reflected or rotated to fit certain configurations.

Graded Grids

In some cases, you will be interested in the results within a certain rectangular subset of a cross section, and you will want more precision there than you will be able to calculate for the entire cross section. It is possible to create a grid that changes from a mesh size of h to one of $h/2$, as shown in figure 7. To change from the coarse grid (squares) to the fine grid (darkened circles), we must go through a transition layer of nodes (triangles). Different nodes will have different formulas for computing F_0 and different relaxation templates.

If the system under study is based on Poisson's equation, then different nodes have different formulas. The error for square nodes is calculated by

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0 + h^2 W_0.$$

The error for the circle nodes is

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0 + h^2 W_0/4.$$

Finally, the error for the triangle nodes is

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0 + h^2 W_0/2.$$

If the system under study is based on

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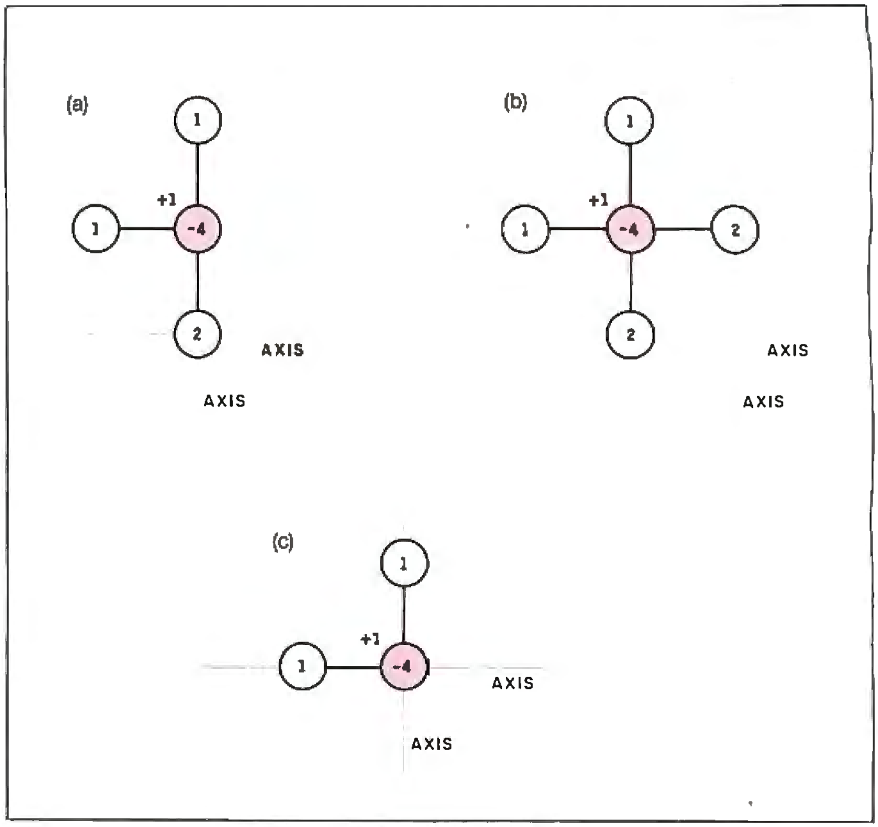

Figure 6: *Symmetry in two dimensions. Figures 6a through 6c show the relaxation templates for nodes on or near both axes of symmetry. For nodes near only one axis, use the templates of figures 5a and 5b. All templates can be reflected or rotated to achieve a desired node configuration.*

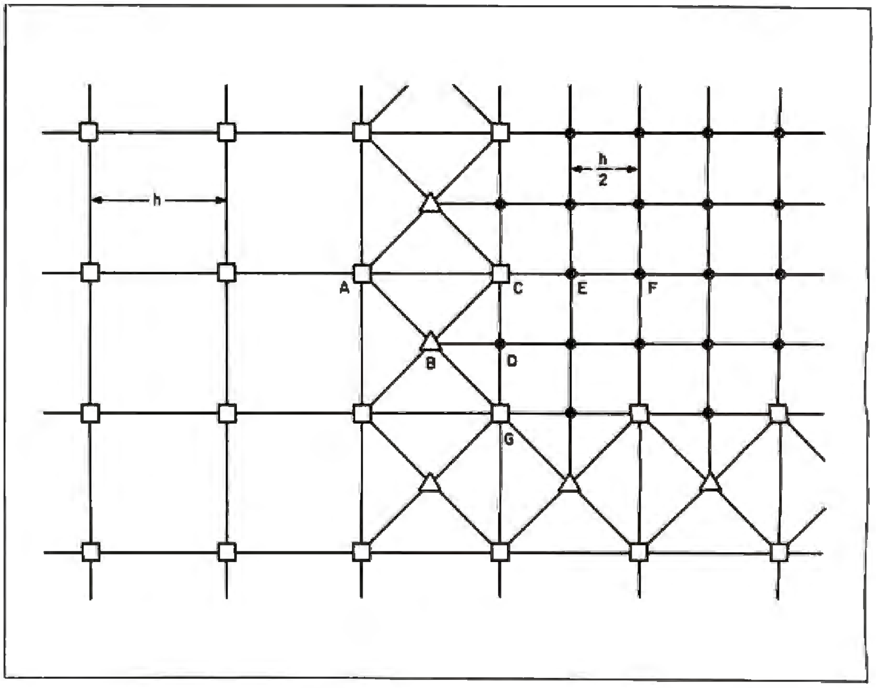

Figure 7: *An example of using a graded grid. You can switch from a coarse grid (squares) to a finer grid (dark circles) by using a transition layer of nodes (triangles). In this way, you can get more precise answers in an area of interest without having to use the finer grid for the entire cross section. See figure 8 for the relaxation templates of the nodes marked A through G.*

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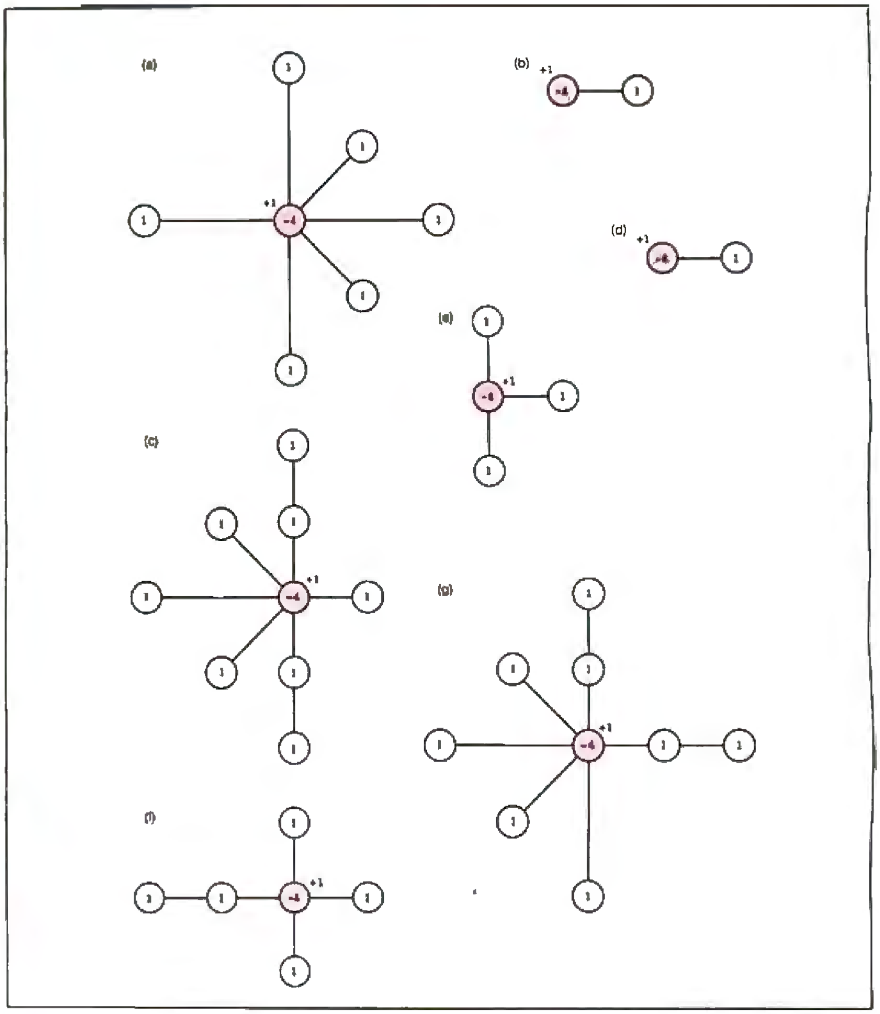

Figure 8: *Relaxation templates for special nodes in figure 7. Figures 8a through 8g are the templates for the nodes labeled A through G, respectively, in figure 7. Most of the other square and circle nodes are relaxed according to the normal template.*

Laplace's equation, then $W_0 = 0$ at all points, and the preceding three formulas reduce to

$$F_0 = \sum_{n=1}^{4} w_n - 4w_0.$$

In figure 7, the letters A through G label nodes that need special treatment when being relaxed. Figures 8a through 8g show the respective relaxation patterns for those nodes. For information on the derivation of these equations and templates, see page 69 of D. N. de G. Allen's book mentioned previously.

Commentary

According to Allen, the relaxation method was first used in 1935 by Sir Richard Southwell at Oxford University. It is a numeric technique that was invented before electronic computers. As a matter of fact, Allen's book uses the word "computer" in its original meaning as a person who computes: For example, Allen states that a certain point "is a matter for the personal inclination of the individual computer." The relaxation method is often shown as an integer-only algorithm; the main departure from the classical approach in this article is the adaptation of the algorithm to use floating-point arithmetic, a process that a BASIC program performs more easily than integer arithmetic. (Some books describe a similar algorithm for the numerical solution of partial differential equations under the name "finite-difference method.")

The relaxation method is attractive because it is simultaneously simple, intuitive, and powerful. Unlike many numeric techniques that must be followed explicitly, this method can suffer from being applied blindly. In this respect, it is not so much an algorithm as a set of guidelines that should be applied intelligently to a problem. I hope you find it as interesting and useful as I have. ■


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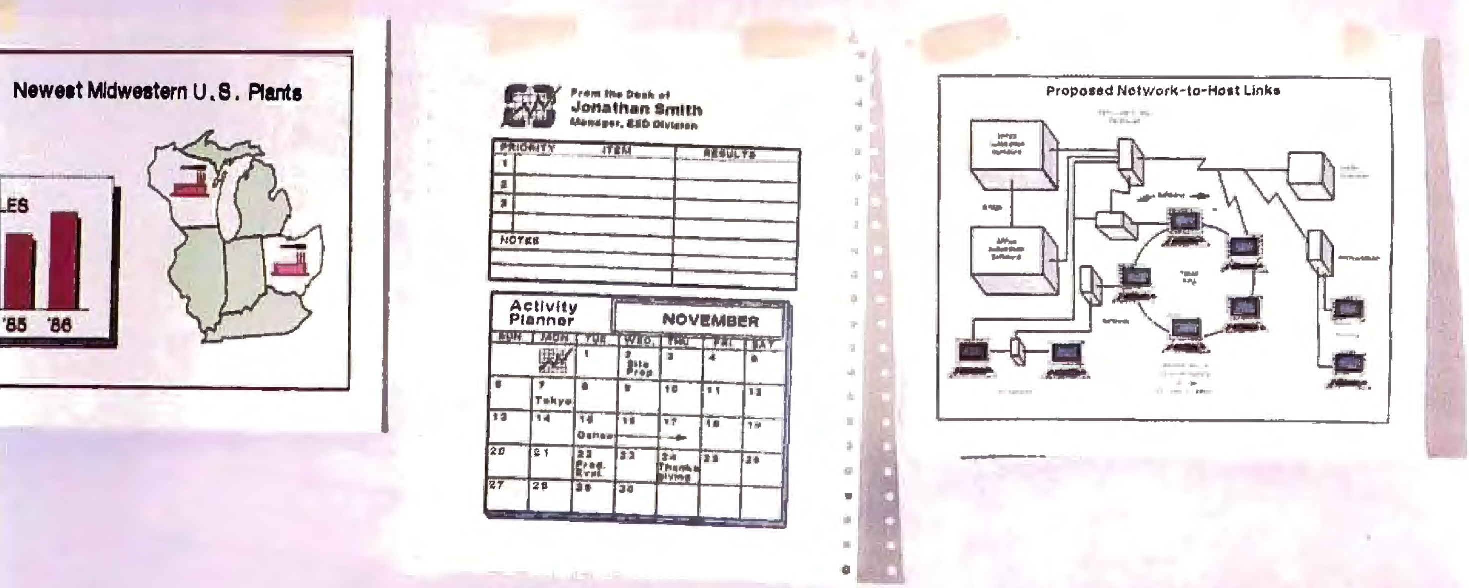
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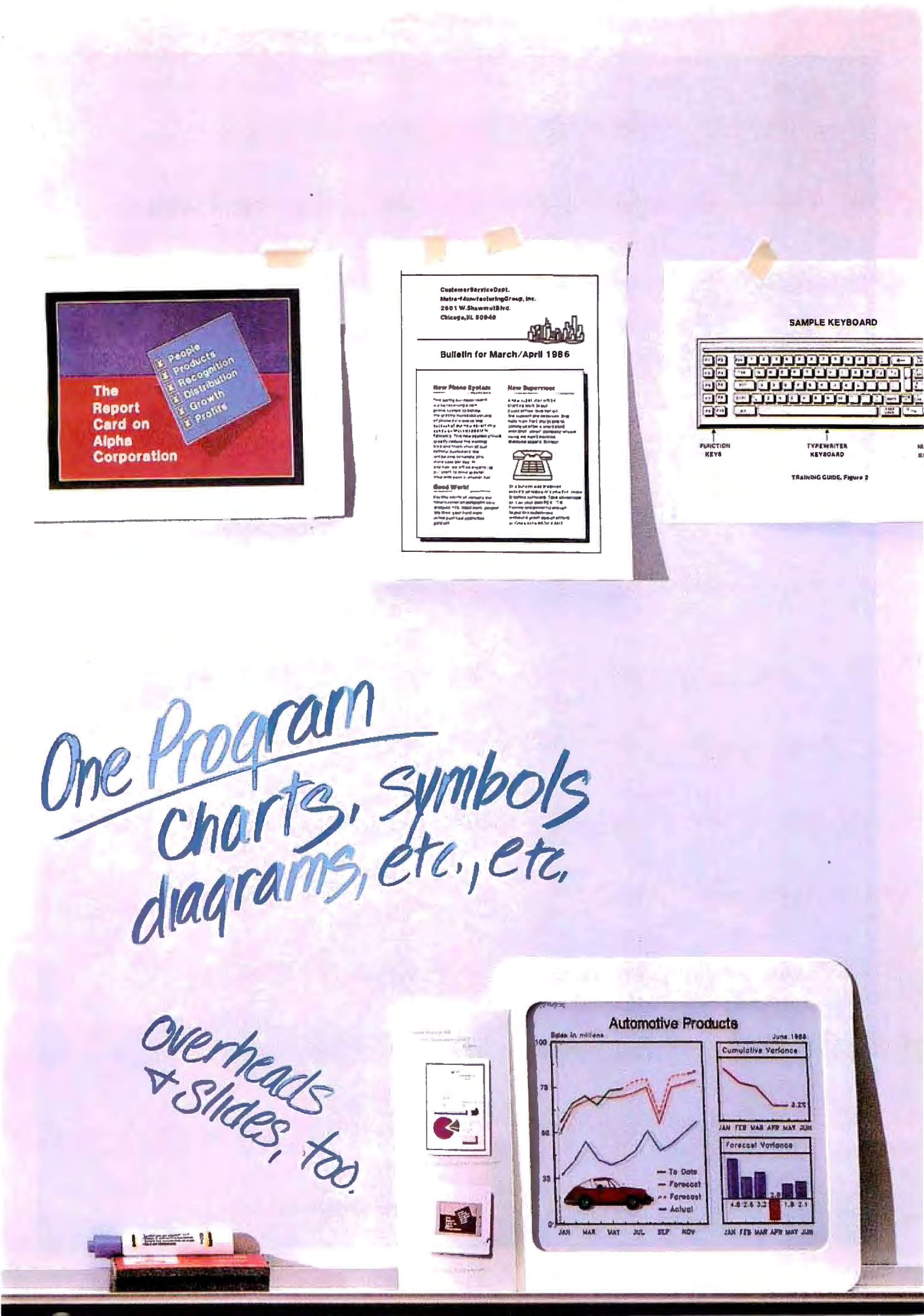

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Jon C. Snader

Look It Up Faster with Hashing

A potpourri of code fragments showing basic hashing functions

Many applications in programming require you to store and retrieve information in tabular form. One method that minimizes the number of comparisons needed to find an item is the binary search (see "A Faster Binary Search" by Dr. L. E. Larson, March 1983 BYTE). Unfortunately, the binary search suffers from two defects that limit its application. First, it requires that the table it is searching be in sorted order. Second, because of the first requirement, it is difficult to add items to the table. Quite frequently, the addition of a new item into an unsorted table is required. For example, the symbol table lookup routine in an assembler or compiler must determine if a given symbol is already present and then provide for its addition to the symbol table if it isn't.

Table lookup methods classified as *hashing schemes*, or *hash-table techniques*, not only meet the two objections above but are usually faster than the binary search. Although several hashing schemes are known and in use, they divide into two subclasses known as *chaining* techniques and *open-addressing* techniques. I will examine each type in turn, give some examples, and compare their strengths and weaknesses. For those who want to delve more deeply into the subject, I will indicate the results of some recent research in this area and provide some references.

At its most basic level, our problem is to find the entry in a table that contains the name (or symbol or account number, etc.) we are looking for. This name is called the *key*, and the part of each table entry that contains the key is called the *key field*.

In general, the table entry contains other data associated with the name in the key field, but for simplicity we will ignore the associated data. We are interested only in finding a name in the table or adding the name to the table if it's not already there.

The Hashing Function

The central idea behind all hashing schemes is the direct calculation of a table entry from a key. We define a function, called the *hashing* function, that associates each key with an entry (or index) in the table where we search for a matching name in the key field. Empirical and theoretical results suggest that the division method is the most successful for calculating the value of the hashing function from the key.

In the division method, the key—thought of as an unsigned integer—is divided by the table size. The remainder is the value of the hashing function. That is, $h(\text{KEY}) = \text{KEY} \bmod M$, where M is the table size. The table size is important here. Excellent results are obtained if M is a prime number, but very poor results are obtained if it is a power of 2. Therefore, the table size should be prime, or at least odd.

Listings 1 through 4 show the implementation of the above hashing scheme in various languages. At first glance they appear to differ considerably, but they all calculate the same value for a given key.

Once the key has been transformed into an entry number by the hashing function, we check the key field in that entry. If the name in the key field matches KEY, we have found the proper entry and we exit the lookup routine with a "found." If the key field of the table is empty, we enter KEY into the key field and exit the routine with a "not found."

All hashing schemes have these steps in common. They differ in what they do if the key field of the entry is not empty and does not match KEY. In this case, a *collision* is said to occur. Since the hashing function can provide at most M values (0, 1, . . . , $M-1$), such collisions are inevitable.

Collision Resolution by Chaining

One successful method of collision resolution is the chaining technique, in which each entry of the table is treated as the first link of a chain of entries, all having keys that hash to the same value. This is accomplished by dividing the table into two parts—a primary table consisting of M entries and a secondary or "overflow" table to hold keys that collide with an entry in the primary table. To chain together entries whose keys hash to the same value, an extra field is added to each entry. This field, called the *chain pointer*, points to the next entry in the table that has the same hash value associated with its key. The chaining together of entries is illustrated in figure 1. To find an entry in the table, KEY is hashed to find the head of the chain, and the chain is followed until a match is found or a null chain pointer, indicating a "not found" condition, is encountered. The algorithm below (where TAB is the search table) implements this scheme in an efficient manner:

1. Set INDEX = h(KEY).
2. If TAB[INDEX] is empty, set TAB[INDEX] = KEY, and exit "not found" with the number of the newly created entry in INDEX.
3. If TAB[INDEX] = KEY, exit "found" with the entry number in INDEX.
4. If CHAIN[INDEX] < > null, set

continued

Jon C. Snader (Department of Mathematics, University of South Florida, Tampa, FL 33620) has a Ph.D. in mathematics from the University of Illinois. He has been involved with computers for 20 years and is interested in numerical analysis and compiler design.

INDEX = CHAIN[INDEX]; go to step 3.
5. Set OVFLO = OVFLO + 1 (update the pointer to the next available overflow entry). If OVFLO > TAB size, then abort with table overflow.
6. Set TAB[OVFLO] = KEY, set CHAIN[INDEX] = OVFLO, set INDEX = OVFLO, and exit "not found" with the number of the newly created entry in INDEX.

Listings 5 and 6 show implementations of this algorithm in BASIC and Pascal. Figure 2 shows the table after several items have been entered.

The chains are usually short, and because only entries with the right hash value are examined, this algorithm is very fast. The number of attempts we examine to find the desired entry—called *probes*—depends on how full the table is. The load factor, L, for a table is defined by $L = N/M$, where M is the (primary) table size and N is the number of occupied entries. For the chaining method, N can be larger than M, so that L might be larger than 1.

Listing 1: *A BASIC subroutine that implements the hashing function using the division method. The* CVI *function tells BASIC to treat the 2-byte substrings of* NA$ *as integers.*

```
50 '~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
55 '                                                                       ~
60 'Subroutine to hash a four-character string                             ~
65 '                                                                       ~
70 'Enter with the string to be hashed in NA$                              ~
75 '                                                                       ~
80 'On exit the hash value is in H                                         ~
85 '                                                                       ~
90 '~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
95 '
100 H = (CVI(MID$(NA$,1,2)) XOR CVI(MID$(NA$,3,2)))
    MOD 61
110 RETURN
```

Listing 2: *A Pascal function implementing the hashing function. The variable record construct is used to refer to* KEY *as both character and integer data. Although this function seems more complicated than the one in listing 1, most of the source code is compiler directive and generates no run-time code.*

```
Function h( KEY: string4 ): integer;
   Type
      KEY_types = (char_KEY, integer_KEY);
      KEY_overlay = record
         case KEY_types of
            char_KEY:     ( KEY_in_characters:
                              string4 );
            integer_KEY: ( dummy: byte; {takes up
                             room for string size}
                             integer_KEY_1: integer;
                             {first 2 bytes of KEY}
                             integer_KEY_2: integer;
                             {last 2 bytes of KEY}
                           );
      end;

   Var
      KEY_record: KEY_overlay;
   begin {hash}
   with KEY_record do
      begin
         KEY_in_characters := '    '; {clean out
                in case KEY < 4 chars}
         KEY_in_characters := KEY;
         h := ( integer_KEY_1 xor integer_KEY_2 )
                mod number_TAB_entries;
      end;
   end; {hash}
```

The expected number of probes to find an item in the table, A_s (i.e., the average number of probes over a large number of tables), is given approximately by $A_s = 1 + L/2$. Thus, with a load factor of 0.9, the expected number of probes to find an item is 1.45. Even for $L = 2$, which means there are $2M$ entries in the table, the expected number of probes is only 2. If the entry we are searching for is not in the table, the expected number of probes, A_u, is given approximately by $A_u = e^{-L} + L$.

While the chaining method is fast, it requires more memory. First, each entry must have an additional field for the chain pointer. Next, because many of the entries will be placed in the overflow table, it is likely that several entries in the primary table are unoccupied. On small systems, this is a problem due to limited memory. The other type of collision-resolution scheme I will discuss is called the open-addressing method because the table can be addressed freely rather than through a linked list. Open addressing is more efficient in its use of memory but at a slight degradation in speed.

Collision Resolution by Open Addressing

I will examine two open-addressing methods: *linear probing* and *double hashing.*

In linear probing, if a collision occurs, the rest of the table is searched sequentially, in a circular fashion, until either the correct entry is found or an empty entry is found. In the latter case, the new KEY is entered into the empty entry and the routine exits with a "not found." Thus, if KEY hashes to 4 (i.e., h(KEY) = 4), the sequence of entries searched is 4, 5, . . . , $M-1$, 0, 1, 2, 3.

A few remarks about linear probing are in order. First, there is no wasted space. No chain pointers are required, and, unlike the chaining method, every entry in the table is available for use. Second, the algorithm itself is very simple; it consists essentially of the hash value calculation and a linear search. Third, whereas the chaining method examines only entries with the proper hash value, linear probing, as the table fills up, spends the bulk of its time examining entries with a hash value different from KEY. This characteristic, which is shared by all open-addressing methods, causes an increase in the number of probes necessary to find the proper entry or an empty entry. As with chaining, the expected number of probes depends on the loading factor, L, and is different for successful and unsuccessful searches. For linear probing we have

$A_s = (1 + 1 / (1-L)) / 2$ and
$A_u = (1 + 1 / (1-L)^2) / 2$.

continued

Listing 3: *A FORTRAN subroutine implementing the hashing function. The FORTRAN* EQUIVALENCE *statement is used to refer to* KEY *as both character and integer data. The* EOR *function performs an exclusive-OR on its input.*

```
C   ***************************************************
C   *                                                 *
C   * A SUBROUTINE TO CALCULATE A HASH VALUE BETWEEN  *
C   * 0 AND 60                                        *
C   *                                                 *
C   *                                                 *
C   * INPUT:   KEY - FOUR BYTES OF CHARACTER DATA TO BE *
C   *                HASHED                           *
C   *                                                 *
C   *                                                 *
C   * OUTPUT:  INDEX - AN INTEGER VALUE BETWEEN 0 AND 60 *
C   *                                                 *
C   ***************************************************
C
        SUBROUTINE HASH(KEY,INDEX)
        CHARACTER KEY*4,WKEY*4
        INTEGER*2 INDEX,IKEY(2),EOR
        EQUIVALENCE (WKEY,IKEY)
        WKEY=KEY
        IKEY(1)=EOR(IKEY(1),IKEY(2))
        INDEX=MOD(IKEY(1),61)
        RETURN
        END
```

Listing 4: *The hashing function implemented as 8086/8088 assembly language code. The first two bytes of* KEY *are exclusive-ORed with the last two bytes, and the result is divided by the table size. The remainder from this division is returned in the accumulator.*

```
;----------------------------------------------
;HASH—Procedure to hash a four-byte string
;
;       Input:  AX := first two bytes of string
;               BX := second two bytes of string
;
;       Output: AL := hash value (0-60)
;
;       Registers destroyed:    AX,BX
;----------------------------------------------
;
TAB_sz  equ     61              ;define table size
hash    proc    near
        push    dx              ;save DX
        xor     ax,bx           ;combine into 16 bits
        xor     dx,dx           ;clear DX-dividend in
                                ; DX AX
        mov     bx,TAB_sz       ;table size to BX
        div     bx              ;divide-remainder is in
                                ; DX
        mov     ax,dx           ;remainder to AX
        pop     dx              ;restore DX
        ret
hash    endp
```

If $L = 0.5$, then $A_s = 1.5$ and $A_u = 2.5$. Notice that these values compare favorably with those for chaining. As L approaches 1, however, these values become very big, reflecting the large number of extra entries that must be examined. Certainly when the maximum load factor is 0.5 or less, linear probing is very competitive with chaining and, in general, it performs well if $L \leq 0.75$.

The poor performance of linear prob-

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The open-addressing with double-hashing scheme virtually eliminates clustering.

ing as the table fills up is due to the phenomenon of *clustering*, the tendency for several entries to clump together in consecutive entries of the table. For example, if 5 entries in a 10-entry table are nonempty (N=5, M=10), it is far better that entries 0, 2, 4, 6, and 8 be occupied than that entries 0, 1, 2, 3, and 4 be occupied. In the first situation, a successful search takes only one probe and an unsuccessful search at most two; in the second situation, a successful search can take up to five probes (an item that hashes to 0 is stored in 4) and an unsuccessful search can take up to six probes. Naturally, this situation is aggravated in larger tables, where the clumps can be longer.

The open-addressing with double-hashing scheme virtually eliminates clustering. This method is like linear probing, except that instead of searching entries h(KEY), h(KEY) + 1, h(KEY) + 2, . . . , we search entries h(KEY), h(KEY) + j, h(KEY) + 2j, h(KEY) + 3j, . . . , for some j. If j were the same for each KEY, this method would be no better than linear probing since clusters of records j entries apart would form. Instead, j is made to depend upon KEY in such a way that the clustering of items is eliminated and that the sequence h(KEY), h(KEY) + j, h(KEY) + 2j, . . . , will eventually cover the entire (circular) table.

continued

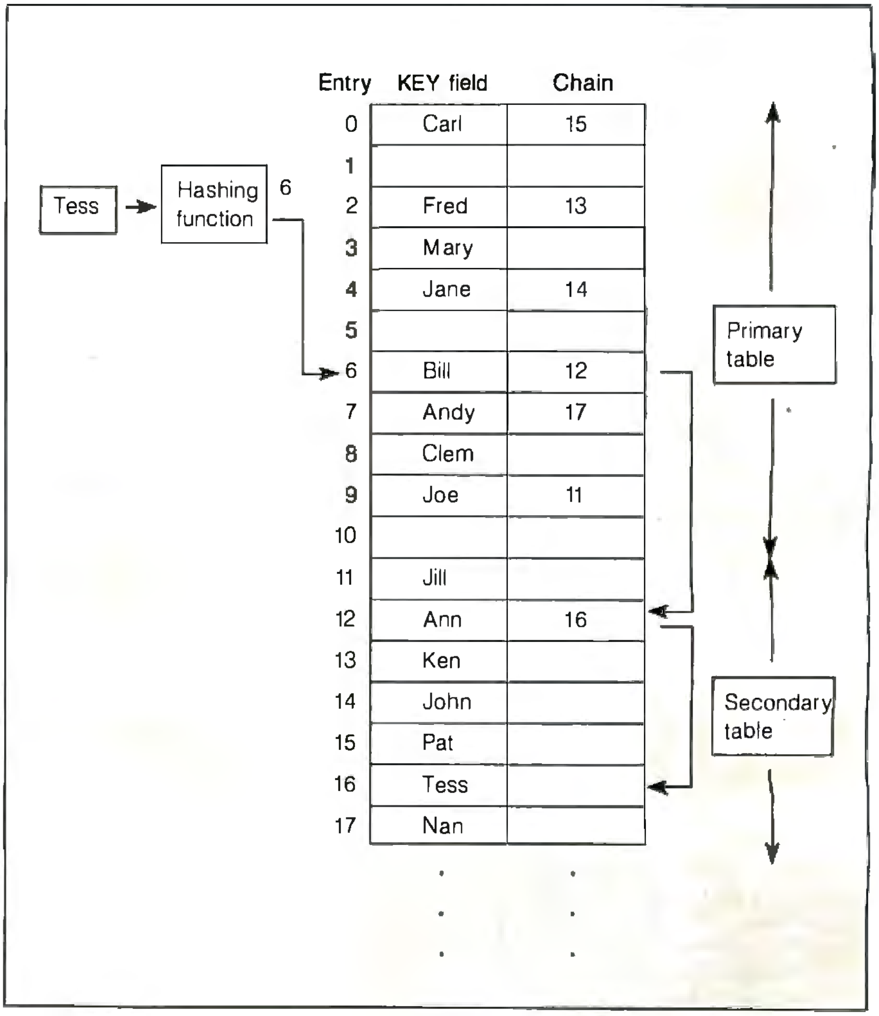

Figure 1: *The* KEY *Tess is being searched for. The hashing function gives a value of 6 for Tess, but the sixth entry of the table contains Bill. The chain field entry contains 12, telling the search routine that the next entry with a hash value of 6 is the twelfth entry. The twelfth entry is not Tess either, but it points to the sixteenth entry—the desired entry. In this example, M = 11, entries 0 through 10 are the primary table, and the secondary table begins at entry 11 with Jill.*

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Entry	KEY field	Chain	
0	Carl	15	
1		<null>	
2	Fred	13	
3	Mary	18	
4	Jane	14	
5		<null>	Primary table
6	Bill	12	
7	Andy	17	
8	Clem	<null>	
9	Joe	11	
10	Jean	<null>	
11	Jill	<null>	
12	Ann	16	
13	Ken	<null>	
14	John	<null>	Secondary table
15	Pat	<null>	
16	Tess	<null>	
17	Nan	<null>	
18	Tony	<null>	
19		<null>	

Figure 2: *This figure shows the table* TAB *after several names have been entered. In this example, M = 11, N = 17, and the primary table occupies entries 0 through 10. The secondary table begins at entry 11. Note that the longest chain (beginning with Bill) is three entries long. The average number of probes in a successful search is 1.53, and the loading factor, L, is 1.55.*

Listing 5: *A BASIC subroutine implementing the chained hashing method.*

```
100 'Routine to do a table lookup using chained hashing
110 '
120 'TB = table of names to be entered/looked up.
130 'CH = table of chain pointers
140 'IX = index to entry of TB where the name was
 entered or found
150 'OV = pointer to the last entry used in the overflow
 table
160 'FD = flag reporting result of search: 0=not found,
 1=found
170 'K$ = holds the current KEY being searched for
180 'MT = maximum total table size (primary and
 secondary)
190 '
200 FD = 0  'initialize result of search to "not found"
210 GOSUB 1000 'go hash the key in K$; the result is
 returned in IX
220 '
230 'examine first entry with correct hash value
240 '
250 IF TB(IX) = "" THEN TB(IX) = K$: RETURN 'it's empty
 - enter KEY and return
260 IF TB(IX) = K$ THEN FD = 1: RETURN  'found it - say
 so and return
270 '
280 'the first entry had some name other than KEY in it
 - step down the chain
290 '
```

continued

While there are several ways to choose j, the following method produces excellent results. First, choose a set of twin primes, that is, two prime numbers that differ by two. Examples of twin primes are 59 and 61, 269 and 271, 521 and 523, and 1019 and 1021. To implement open addressing with double hashing, the table size is chosen to be the larger of the twin primes. The smaller of the twin primes is used to calculate the increment j in much the same way as the larger prime is used to calculate the hash value. That is,

$$j = (\text{KEY mod } P') + 1$$

where P' is the smaller prime.

If P and P' are two primes and $P = P' + 2$, then the following algorithm implements open addressing with double hashing. The algorithm assumes that TAB is a table of P entries ($M=P$), numbered 0, 1, . . . , P–1. The number of active entries in TAB, N, is initialized to zero.

1. Set INDEX = KEY mod P.
2. If TAB[INDEX] = KEY, then exit "found" with the entry in INDEX.
3. If TAB[INDEX] is empty, go to step 8.
4. Set J = (KEY mod P') + 1.
5. Set INDEX = INDEX + J. If INDEX >= P, then set INDEX = INDEX – P (make the table circular).
6. If TAB[INDEX] is empty, go to step 8.
7. If TAB[INDEX] = KEY, then exit "found" with the entry in INDEX; otherwise, go to step 5.
8. If N = P – 1, then TAB is full, so abort with a "table overflow" condition. Otherwise, set N = N + 1 and set TAB[INDEX] = KEY. Exit "not found" with the number of the newly created entry in INDEX.

Listing 7 shows an implementation of this algorithm in Pascal.

We have approximations for the expected number of probes. With the method of calculating j given above, these are

$$A_s = -(ln(1-L)) / L \text{ and}$$
$$A_u = 1 / (1-L)$$

Thus, when the table is half full (L= 0.5), A_s = 1.4 and A_u = 2.

Extensions and Further Reading

I have barely touched upon the many and diverse hashing schemes that have been proposed and implemented. Among the three schemes discussed, there are many variations, each addressing some weakness of the parent method.

For example, Donald Knuth (reference 1) discusses a chaining algorithm by F. A. Williams in which no secondary table is

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```
300 IF CH(IX) <> 0 THEN IX = CH(IX): GOTO 260 'step down
 the chain
310 '
320 'We found the end of the chain,  so enter the key
 and return with FD = 0
330 '
340 OV = OV + 1  'advance to next empty overflow entry
350 IF OV > MT THEN GOTO 2000 'goto the error routine
 and never return
360 TB(OV) = K$      'enter KEY
370 CH(IX) = OV      'and add the new entry to the end of
 the chain
380 IX = OV          'set IX to tell the caller where we
 entered it
390 '
400 RETURN
```

Listing 6: *A Pascal implementation of a search routine using chained hashing. A slight modification of the algorithm takes advantage of Pascal's heap management facilities to save memory. Instead of primary and secondary tables, a table* (node) *M entries long of pointers is used. Each actual table entry is allocated as needed by the Pascal* New *procedure. The entries of* node *then point to the head of each chain. This eliminates the necessity of having a large secondary table available and—for large* TAB *entries—minimizes the space wasted by unused primary table entries. The* Dispose *procedure can be used to make this routine delete entries.*

```
Program Search_With_Chaining;

   Const
     max_TAB_entry = 60;          {last TAB entry number}
     number_TAB_entries = 61;  {the number of entries in
                                 TAB}

   Type
     tab_pointer = ^tab_entry;   {define a pointer to
                                    tab_entry (below)}
     string4 = string[4];
     tab_entry = record           {define an entry of TAB}
        KEY_field: string4;       {holds KEY for this entry}
        CHAIN: tab_pointer;       {pointer to next entry
                                    with same hash value}
     end;

   Var
     found: boolean;          {set true by Search if KEY is
                                found}
     index: tab_pointer;      {pointer to the current TAB
                                entry being examined}
     KEY: string4;   {name to be found or entered}
     i: integer;   {for FOR loop use}
     node: array[ 0 .. max_TAB_entry ] of tab_pointer;
                                       {heads for each chain}

   Procedure Search( KEY: string4 );

     Function h( KEY: string4 ): integer;
        Type
          KEY_types = (char_KEY, integer_KEY);
          KEY_overlay = record
             case KEY_types of
                char_KEY:     ( KEY_in_characters:
                                 string4 );
                integer_KEY: ( dummy: byte; {takes up
```

continued

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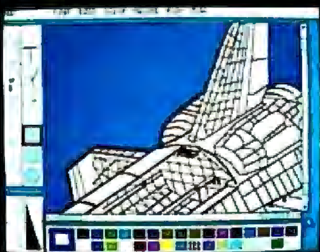
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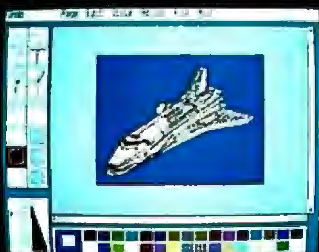
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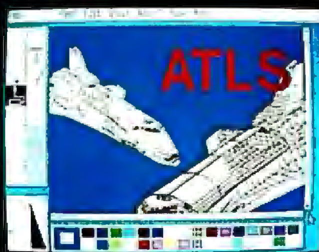

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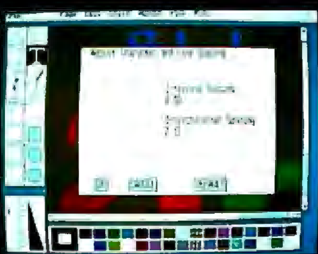
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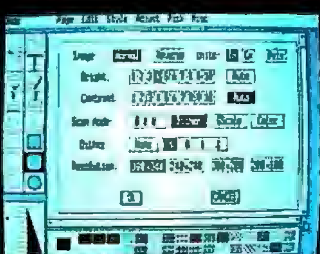
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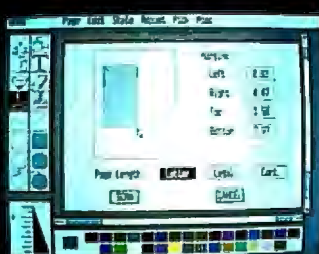
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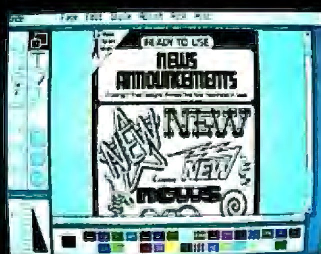

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```
                                room for string size}
                                integer_KEY_1: integer;
                                  {first 2 bytes of KEY}
                                integer_KEY_2: integer;
                                  {last 2 bytes of KEY}
                               );
      end;

   Var
      KEY_record: KEY_overlay;
   begin {hash}
   with KEY_record do
      begin
         KEY_in_characters := '    '; {clean out in
                                    case KEY < 4 chars}
         KEY_in_characters := KEY;
         h := ( integer_KEY_1 xor integer_KEY_2 )
                                 mod number_TAB_entries;
      end;
   end; {hash}
Var
   hash: integer;       {holds the hash value of the
                         current KEY}
   last_index: tab_pointer; {points to the last
                             entry examined}

Begin {Search}
   found := false;
   hash := h( KEY ); {go hash KEY}
   index := node[ hash ];
   if index = nil then {this is the first KEY with
                        this hash value}
      begin
         new( index );  {create an entry for it}
         node[ hash ] :=  index; {and set node to
                                  point to it}
         index^.CHAIN := nil; {mark this entry as
                               the end of the chain}
         index^.KEY_field :=  KEY; {enter KEY into
                                    TAB entry}
      end
   else {there are entries with this hash value -
         search them}
      begin
         while ( index <> nil ) and not found  do
             begin
                if index^.KEY_field = KEY then
                                         {found it}
                   found := true
                else {point to next entry with this
                      hash value}
                   begin
                      last_index  := index; {point
                                 to the LAST entry}
                      index := index^.CHAIN;
                   end;
             end;
          if not found then {create a new entry}
             begin
                new( last_index^.chain );
                index := last_index^.chain; {and
                        point to it with index}
                index^.CHAIN := nil; {mark this
                          entry as end of chain}
                index^.KEY_field := KEY; {enter KEY
                                   into TAB entry}
             end;
      end;
   end; {Search}
Begin {Search_With_Chaining}
```

continued

Since an item will be looked up several times after it is entered, it makes sense to spend time on the item's insertion.

used. Although there is a slight degradation in speed due to the occasional coalescing of the individual chains, the substantial savings in memory makes this an attractive algorithm. In fact, Knuth recommends Williams's algorithm over the direct chaining method described above.

Two variants of open addressing with double hashing, also discussed by Knuth, are worth mentioning. In the first, the time-consuming (especially for 8-bit processors) division in the calculation of the increment j is avoided by substituting

$$j = 1 + h(\text{KEY}) = 1 + (\text{KEY mod } M)$$

for $j = (\text{KEY mod } P') + 1$.

This also eliminates the need for twin primes. Although a little more clustering takes place with this method, this is usually compensated for by the elimination of the division.

Since an item will be looked up several times after it is entered, it makes sense to spend some time on the insertion so that subsequent lookups will be easier. This idea is used in an algorithm by Richard P. Brent. In Brent's algorithm, the extra work done in entering an item in the table limits the average number of probes to find an item in the table (A_s) to less than 2.5, even as the table fills up.

Another interesting class of hashing algorithms, which is still the subject of active research, is the set of so-called perfect hashing algorithms. In these methods, the table entries must be fixed and known in advance, but the hashing function is chosen in such a way that no collisions take place. Thus, an entry is located by a single calculation. Naturally, these perfect hashing functions are difficult to find; practical methods limit the maximum table size to about 40 entries. The papers by Cichelli (reference 2) and Jaeschke (reference 3) describe two such methods.

The numbers quoted above for A_s and A_u are the expected or average number of

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```
    for i:=0 to max_TAB_entry do node[i]:=nil; {set
                                   nodes to point nowhere}

         {User Code Goes Here}

End. {Search_With_Chaining}
```

Listing 7: *A Pascal implementation of a search routine using double hashing.*

```
Program Search_With_Double_Hashing;

  Const
    max_TAB_entry = 60;          {last TAB entry}
    number_TAB_entries = 61;     {number of entries in
                                  TAB}
    empty = '    ';              {what an empty entry
                                  looks like}
    p_prime = 59;                {first twin prime-used to
                                  calculate increment}
    p = 61;                      {second twin prime-used
                                  to hash KEY}

  Type
    string4 = string[4];

  Var
    found: boolean;              {set true by search if
                                  KEY is found}
    index: integer;              {pointer to the TAB entry
                                  being examined}
    KEY: string4;                {name to found or
                                  entered}
    i: integer;                  {for FOR loop use}
    n: integer;                  {number of entries
                                  currently in TAB}
    TAB: array[ 0 .. max_TAB_entry ] of string4;

  Procedure Search( KEY: string4 );

    Function h( KEY: string4; modulus: integer ):
            integer;

      Type
        KEY_types = (char_KEY, integer_KEY);
        KEY_overlay = record
          case  KEY_types of
            char_KEY:     ( KEY_in_characters:
                              string4);
            integer_KEY:  ( dummy: byte; {takes
                             up room for string size}
                             integer_KEY_1: integer;
                                    {first 2 bytes}
                             integer_KEY_2: integer;
                                   {last 2 bytes} );
        end;

      Var
        KEY_record: KEY_overlay;

      begin {h}
        with KEY_record do
          begin
            KEY_in_characters := '    '; {in case
                                     KEY < 4 chars}
            KEY_in_characters := KEY;
            h := ( integer_KEY_1 xor
```

continued

```
                        integer_KEY_2 ) mod modulus;
          end;
      end; {h}
   Procedure add_KEY_to_TAB;
      begin {add_KEY_to_TAB}
         n := n + 1;  {one more entry in TAB}
         if n > max_TAB_entry then {table is full}
            begin
               writeln('      ***Fatal Error***');
               writeln('Table overflow in table
                     TAB');
               writeln('       program aborted');
               halt; {stop with a fatal error}
            end
         else {there's still room, so add another
               entry}
            TAB[ index ] := KEY;
      end; {add_KEY_to_TAB}

   Var
      j: integer;                {increment for current
                                  KEY}

   begin {search}
      found := false;
      index := h( KEY, p );  {go hash KEY}
      if TAB[ index ] = KEY then {found it}
         found := true
      else {we have to do some more looking}
         begin
            if TAB[ index ] = empty then {it's not
                                  there - enter it}
               add_KEY_to_TAB
            else
               begin
                  j := h( KEY, p_prime ) + 1;
                        {calculate the increment}
                  repeat
                     index := index + j; {step index
                                   to next entry}
                     if index > max_TAB_entry then
                              {off the end of TAB}
                        index := index -
                         number_TAB_entries; {make
                                       circular}
                     if TAB[ index ] = KEY then {we
                                       found it}
                        found := true;   {so say so}
                  until ( TAB[ index ] = empty ) or
                                       found;
                  if not found then {we need to enter
                                  KEY}
                     add_KEY_to_TAB;  {so do so}
               end;
         end;
   end; {search}

Begin {Search_With_Double_Hashing}
   n := 0;  {no entries in TAB yet}
   for i := 0 to max_TAB_entry do TAB[ i ] := empty;
                             {all entries available}


    {User Code Goes Here}


End. {Search_With_Double_Hashing}
```

probes to find an entry or determine its absence. In the worst case, we could have $A_s = N$ and $A_u = N + 1$. This corresponds to the case in which each KEY hashes to the same value. While this is a theoretical possibility, I feel intuitively that it is not very likely. A **comforting** paper by Gonnet (reference 4) shows that this intuition is correct. He proves that the expected length of the longest probe sequence in the common hashing methods grows very slowly and is nowhere near the worst-case value.

The best general reference on hashing is Donald Knuth's book (reference 1). This encyclopedic work contains a wealth of both theoretical and practical material. Several methods are given as step-by-step algorithms; for instance, the above algorithm for open addressing with double hashing is taken from Knuth with only minor modification.

An excellent and very readable introduction to hashing can be found in Morris's famous and influential survey article (reference 5). In addition, Morris gives an implementation in FORTRAN of the chaining method and another type of open-addressing scheme, called random probing, that laid the basis for the double-hashing method.

Finally, the survey article by Knott (reference 6) contains an interesting history of hashing in which edge-notched cards appear as a precursor to the hashing idea. Knott's paper is somewhat demanding mathematically, but it is worth looking at for its exhaustive bibliography, which is current to about 1974.

[Editor's note: *You can find two alternate ways of doing file indexing in Bruce Webster's "A Simple File-Indexing Scheme" (June 1986 BYTE) and Stephen C. Perry's "Keyed File Access in BASIC" (September 1986)*.] ■

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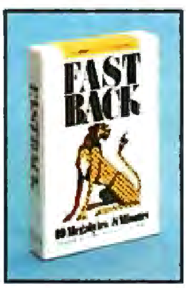

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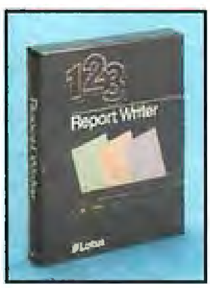

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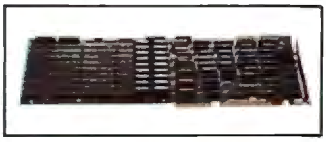

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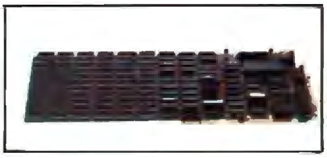

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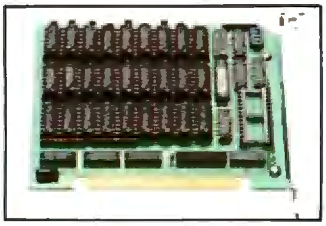

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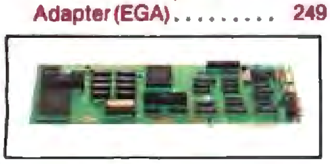

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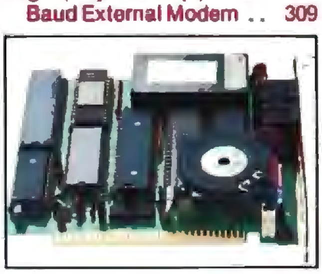

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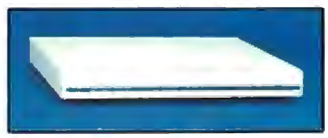

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Howard Katz

RegionMaker

A Macintosh program for building a region from a graphics screen image

Regions are data structures of fundamental importance to the Macintosh user interface and are primarily used by the Window Manager section of the Macintosh ROM. You can save these regions on disk as Macintosh resources, which you can then import and use in other applications.

The purpose of the RegionMaker program is to build a Macintosh region from an arbitrary graphics image on the screen. I wrote the RegionMaker program for the Macintosh using Apple's MDS Assembly-Language Development System.

To build the region data structure, the program uses a contour-tracing algorithm that traverses the boundary of the image, determining which pixels constitute its edge. While the concept of regions is specific to the Macintosh, the traversal algorithm is of more general utility and should be transportable without much difficulty to other 68000 machines. I'll discuss regions and several other QuickDraw concepts in some detail, then the contour-tracing algorithm. Finally, I'll discuss the program. [Editor's note: *The source code for RegionMaker is available on disk, in print, and on BIX; see the insert card following page 424. The listing is also available on BYTEnet; see page 4.*]

QuickDraw

The Macintosh ROM contains over 500 procedures and functions (documented in Apple's *Inside Macintosh*) that programmers can call on when writing applications. Most of these routines support the well-known Macintosh user interface; its features include such objects as windows, menus, dialog boxes, and alerts. The balance of the ROM routines implement the more traditional operating system functions, such as file operations, device management, and low-level input/output, as well as the Macintosh-specific operations of the Memory Manager, segment loader, and sound driver, among others.

The routines in ROM are conceptually grouped into units known as managers. For example, the Menu Manager handles all activities relating to the creation, display, and selection of menu items at the top of the screen. The largest of the managers in ROM is QuickDraw with 145 procedures and functions that primarily support the creation and manipulation of graphics images on the Macintosh screen.

QuickDraw knows about such objects as points, lines, rectangles, and ovals; routines in ROM let you create, manipulate, and display these objects in a variety of ways. A simple example of a QuickDraw drawing command is LineTo. In Pascal, the call

```
LineTo(20,100);
```

for example, draws a line from the current position of the pen to the new point whose *(x,y)* location is (20,100). The Line command is similar but indicates a relative draw; the two parameters indicate the change in *x* and *y* of the line segment to be drawn, again starting from the current pen position. I've used Pascal notation here because *Inside Macintosh* uses that language for documenting the ROM routines. For the sake of simplicity, I've also omitted a discussion of such Macintosh entities as ports, local and global coordinates, pen sizes, and patterns.

Rectangles are important in the QuickDraw environment. A rectangle is defined in memory by a data structure consisting of four integers that specify the coordinates of its top left and bottom right corners. In Pascal, the ROM call

```
SetRect(Rect, 20, 20, 100, 100);
```

assigns the coordinates (20,20) and (100,100) to the opposing vertices of the variable Rect.

In assembly language, you can use the above ROM call to define the size of the rectangle, or you can directly assign the coordinates using the Define Constant directive. You can create the same rectangle simply by typing

```
Rect   DC.W   20, 20, 100, 100
```

Note that both techniques serve only to define the size of the rectangle as a set of integers in memory—they do not display it. This distinction between routines that internally manipulate the parameters describing a QuickDraw object and routines that actually display the object is important.

Several shape-drawing routines are available for drawing the rectangle on the screen. FrameRect(Rect) is an example of a frame-drawing command: It draws a hollow outline around the boundary of the rectangle. PaintRect(Rect) draws the rectangle and fills in every pixel inside its border. Similar shape-drawing operations exist for the other QuickDraw objects mentioned above. Rectangles and these other shapes can also be erased, filled with a specified pattern, and inverted.

Regions

QuickDraw has 18 calls that deal with a data structure known as a region. Regions let you deal with an arbitrary collection of points as a cohesive unit. The Window Manager uses regions primarily to keep

continued

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track of screen areas that will require redrawing when previously hidden windows are brought to the foreground.

In the least rigorous sense, a region is simply a collection of pixels in the bit plane. QuickDraw shape-drawing commands analogous to those described above are available for drawing regions. Figure 1a shows the results of a FrameRgn call, while figure 1b shows the same region drawn using PaintRgn.

Regions can be quite complex. The region in figure 1 has a hollow interior—points within that interior space, while enclosed by the region, are not part of it. If this region were to be painted over an existing image on the screen, pixels from the underlying object would remain visible within the hollow interior of the region. Note that this particular region has two boundaries, one on the outside of the shape and one on the inside. A region can even consist of two or more areas that are unconnected.

Regions with disjoint areas and regions with holes are built from simpler ones using several QuickDraw calls that essentially permit logical operations on pairs of regions. The call UnionRgn takes two existing regions and produces a third region with pixels that are the sum of the pixels in the first two. SectRgn produces the graphics equivalent of a logical intersection—a region with pixels common to both source regions. DiffRgn takes two regions and produces a third with pixels that lie within the first but not the second. UnionRgn produces a region consisting of two or more disjoint areas, while DiffRgn produces a region with one or more holes.

While the shape-drawing commands that draw regions are similar to those for the simpler shapes described above, you handle their creation in a radically different fashion. Rectangles and ovals are described by clearly defined, static data structures whose component values you can assign or examine directly. The data structure describing a region is of variable length, and you cannot create regions or manipulate them in such an explicit fashion. You create regions dynamically through an indirect process that builds a region definition.

To create regions, you bracket a series of calls to Line, LineTo, or any of the QuickDraw frame-drawing commands between the two calls OpenRgn and CloseRgn. The only requirement is that the series of calls must form one or more closed loops. For example, the sequence of ROM calls in listing 1 creates and then draws a region in the shape of an isosceles triangle.

You refer to regions by handles; the variable MyRegion in listing 1 is of type RgnHandle. Handles are a feature of the Macintosh Memory Manager and are used throughout the Macintosh programming environment (see *Inside Macintosh* for details). A handle is a doubly indirect pointer to the block of memory that contains the region data structure and is simply a way of referencing the region data. You can treat it much as any other variable.

The most important conclusion you can draw from the description of how QuickDraw creates regions is that the shape to be drawn is essentially defined by the code that specifies the lengths and directions of the line segments that bound it. The description of a region is hard-wired into the code of the application program that creates it. However, my objective in writing this program was to allow for the creation of a region from an arbitrary, preexisting shape that was created elsewhere by a program such as MacPaint or MacDraw. Once the object has been imported with the Scrapbook desk accessory, all that remains is to find some method of determining which pixels lie on its boundary by traversing it. This traversal, or movement along the edge of the object, can then be translated into a series of *x* and *y* increments that serve as the parameters for input to the QuickDraw Line command. A discussion of a suitable algorithm follows.

A Contour-Tracing Algorithm

I adopted the contour-tracing algorithm in this program from one that Theo Pavlidis discusses in *Algorithms for Graphics and Image Processing* (Computer Science Press, 1982). A pseudocode description of the algorithm is in listing 2. My algorithm is functionally identical to the one Pavlidis proposed. I have made several minor changes in notation, but these do not affect the algorithm's performance.

A single pixel in the image plane touches at most eight neighboring pixels. Figure 2a shows these eight neighbors, numbered clockwise 0 through 7, with the 0-neighbor lying directly above the central pixel. Pixels that share a common side with the central pixel are called d- or direct neighbors. In figure 2a, d-neighbors of the central pixel are numbered 0, 2, 4, and 6. Neighbors that touch the central pixel only at one of its four corners are called i- or indirect neighbors; these pixels are numbered 1, 3, 5, and 7. This numbering scheme identifies each of the pixel's eight neighbors; it also describes the direction of any neighboring pixel from the central pixel. For example, the pixel to the right of the central pixel is the 2-neighbor of the central pixel, or lies in the 2-direction from that pixel. Two of the minor changes I mentioned concern this numbering scheme: Pavlidis refers to the northern neighbor as the 2-neighbor and

continued

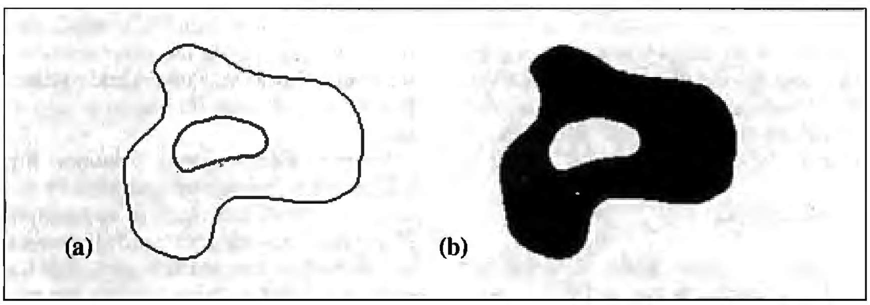
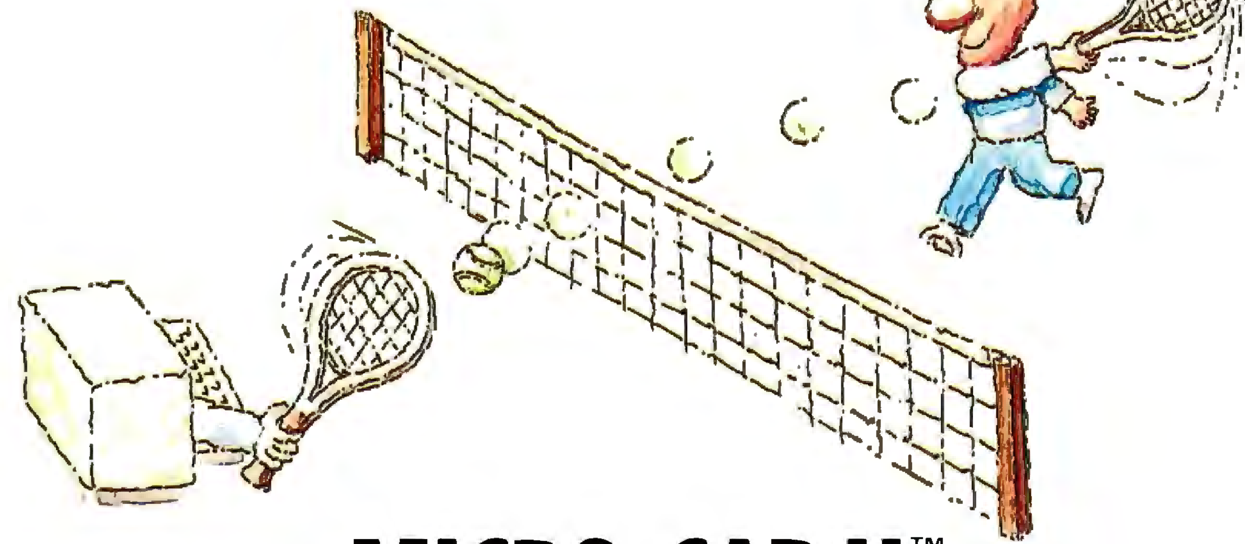


Figure 1: *A region drawn with the* FrameRgn *command is shown in (a). Note that the region has two edges. The same region drawn using* PaintRgn *is shown in (b). The hole is not part of the region.*

Listing 1: *A short sequence of QuickDraw ROM calls that create and display a triangular region. Note the origin (0,0) on the Mac screen is in the upper left corner. Also, the parameters to the line-drawing routine are relative screen coordinates, while those to the MoveTo routine are absolute screen coordinates.*

```
MyRegion := NewRgn;    { allocate initial space for the region }
MoveTo(200,200);       { position the pen                      }
OpenRgn;               { start the region definition           }
    Line(-60,60);      { draw down and to the left             }
    Line(120,0);       { draw the base of the triangle         }
    Line(-60,-60);     { return to the starting position       }
CloseRgn(MyRegion);    { finish the region definition          }
DrawRgn(MyRegion);     { and draw it                           }
```



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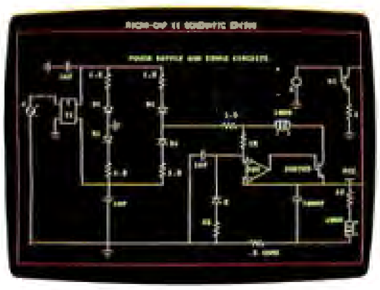

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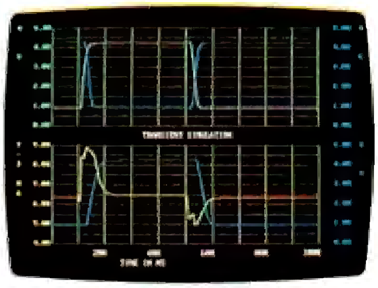

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numbers his pixels counterclockwise. This is a matter of personal preference.

Pavlidis's algorithm produces an i-contour of the object being traversed. This means that the contour forms a closed path whose pixels need abut only at their corners and not necessarily along their sides.

The contouring algorithm attempts to walk around the perimeter of the object starting at some pixel known to lie on the object's contour. The problem is to determine which pixel to examine next. Since each pixel has eight neighboring pixels, the algorithm for determining the search order should be very efficient.

The contouring algorithm assumes that you have given it a starting pixel known to lie on the left edge of the object. In the RegionMaker program, you do this by pointing the cursor at the left edge of the object and clicking the mouse button. The program then uses the algorithm shown in listing 2 to follow the object's perimeter.

In general terms, this search procedure starts by considering the 0-direction as the direction of traversal S and examines the three pixels in the (S−1), S, and (S + 1) directions from the initial pixel. If the algorithm does not find one of these pixels to be set, it will increment the search direction by three and reenter the loop for examining the (S−1), S, and (S+1) neighbors of the pixel. The direction is incremented by three to avoid redundantly checking a pixel that was examined the first time the procedure executed. The above sequence of three increments and a rotation of three repeats at most three times. After three repetitions, the algorithm will have checked the state of all eight pixels surrounding the current pixel. If none of the surrounding pixels is set, then none of the surrounding pixels lies on the i-contour of the object, and the traverse fails to produce a contour.

Listing 2: *Pseudocode of the contour-tracing algorithm used to trace the contours of objects pasted onto the RegionMaker screen from the Scrapbook. The RegionMaker program then creates a region from the traversal of these contours.*

```
Find a starting point A on the left edge of the object
Set the current point C to A
Set the search direction S to 0

REPEAT
  Tries = 0
  REPEAT
    Found = TRUE;
    IF the (S - 1) neighbor of C is set
      make it the current point
      S = S - 3
    ELSE
      IF the S neighbor of C is set
        make it the current point
      ELSE
        IF the (S + 1) neighbor of C is set
          make it the current point
        ELSE
          S = S + 3
          Tries = Tries + 1
          Found = FALSE
  UNTIL (Found = TRUE) OR (Tries = 3)
UNTIL (Found = FALSE) OR (C = A)
```

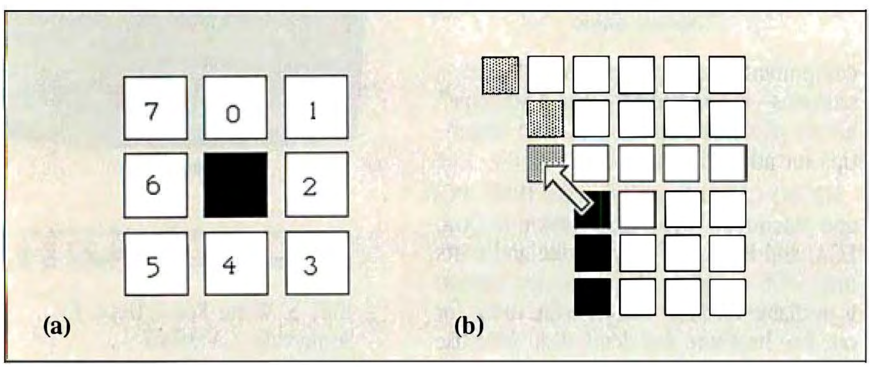

Figure 2: *The numbering scheme for pixels surrounding the current pixel is shown in (a). A portion of an edge contour is shown in (b). The arrow points from the current point to its 7-neighbor, which will be added to the contour on the next step. Note that the inflection point at the corner has been bypassed. Pixels that have been contoured are shown in black; pixels remaining to be contoured are shown in gray; pixels lying in the interior of the object and not on its edge are shown in white.*

If the algorithm finds a pixel that is on the contour of the object, this pixel becomes the current point. If the algorithm finds this pixel on an (S−1) attempt, the original search direction is decremented by two. If it encounters the pixel on an S or an (S+1) attempt, the direction is left unchanged.

The final step in completing the algorithm is to add a test for whether or not the traverse has returned to the starting position. If a closed loop does exist and the check for the starting point is left out, the algorithm will cycle endlessly. The algorithm will produce i-contours for holes within objects as well as for their exterior boundaries. You can easily verify that the sense of the traverse is reversed for a hole—contouring proceeds in a counterclockwise direction.

The technique used to determine whether a particular pixel on the screen is set or not is machine-specific. On the Macintosh, the QuickDraw function GetPixel returns a Boolean result that indicates whether the pixel at the specified location is turned on or off. A small overhead is paid for any call into the Macintosh ROM; this overhead becomes noticeable for repetitions of the GetPixel call when the object being traversed has a long contour (at a screen resolution of 342 by 512, a contour of several thousand pixels is not unusual for even a moderately small object). I chose to bypass the ROM routines and interrogate the screen memory directly using the 68000 instruction BTST, which tests the state of a particular bit and sets the zero flag accordingly. The program runs much faster; the penalty is a little extra bookkeeping to keep track of addresses and bit numbers within the current byte.

I'll close the discussion of the algorithm with a final comment on its correctness. By correctness, I mean the closeness of the match between the generated contour and the actual boundary of the original object. As I mentioned, the algorithm generates an i-contour, not a d-contour. The

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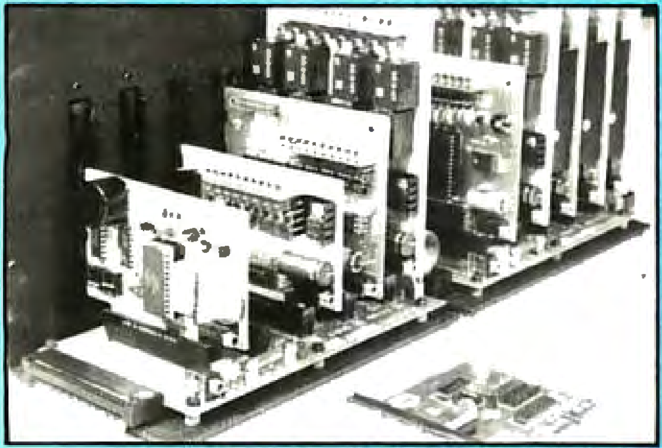

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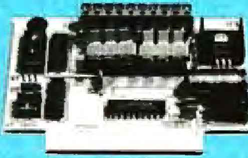

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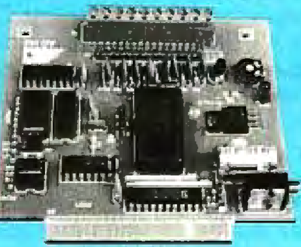

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Right-angle bends may not be faithfully reproduced since pixels on the contour can abut at corners.

fact that pixels on the contour are allowed to abut at their corners means that sharp, right-angled bends on the contours of the object might not be faithfully reproduced. The contour line segment that is generated at the corner will not pass directly through the pixel at the vertex of the corner. Instead, it will connect the two pixels adjacent to the vertex pixel. Figure 2b explains why this occurs. This is not a major problem. Interested readers might try their hands at producing a d-contouring algorithm.

The RegionMaker Program

The source listings for the RegionMaker program are in the files RgnMaker.ASM, Traverse.ASM, and SaveRgn.ASM. RgnMaker.ASM, the main module, draws the RegionMaker window, creates and manipulates the menus, pastes the Scrapbook image into the RegionMaker window, and handles a number of miscellaneous tasks. Traverse.ASM implements the contour-tracing algorithm, and SaveRgn.ASM creates a resource out of the region and writes it to disk.

You assemble these three modules separately, then link them with the MDS Linker. One final file, RgnMaker.R, provides the source code for the resource file that is input to Apple's RMaker (or Resource Maker) program. The resource file provides the basic templates that describe the windows, menus, dialog boxes, and alerts used in the program.

The program is a typical Macintosh application in that it draws heavily on the features of the Macintosh user interface, and much of the code in the program is dedicated to supporting those features. By contrast, the code in Traverse.ASM that handles the contouring accounts for less than 100 lines, or only about 10 percent of the total number of lines in the program.

Menus

The program has five menus. Three of these—the Apple, Edit, and File menus—are similar to those found in most Macintosh applications. The Apple menu corresponds to the format that Apple recommends in its user interface guidelines. It contains the standard "About . . . " dialog box, which gives credit to the author and provides a succinct description of how to run RegionMaker. It also supports whatever desk accessories are present in the System file.

The Edit menu's main use is to support copying and pasting of pictures from the Scrapbook desk accessory. Any picture in the Scrapbook can be pasted onto the RegionMaker window through the usual two-step copy-and-paste procedure. Selecting Copy copies the picture from the Scrapbook to the Clipboard. The Scrapbook does the copying, while RegionMaker handles pasting from the Clipboard to the screen. If you try to paste after closing the Scrapbook and no picture is on the Clipboard, the RegionMaker program will beep at you.

The File menu in RegionMaker contains only two items: Write Work Area to Disk and Quit. The meaning of Quit should be obvious; Write lets you save the region you've just built. The File menu format that Apple recommends has nine items in it, but most of the options in that menu are not applicable in this program and I've omitted them. This is generally considered poor practice, by the way: Apple's user interface guidelines in *Inside Macintosh* strongly recommend that all programs use standard Apple, Edit, and File menus to promote consistency across applications.

In addition to the standard menus, RegionMaker uses Traverse and Display menus. Traverse lets you select one of two contouring modes prior to running a traverse. When you select the Build Region mode, subsequent contouring actually creates a region from the object as it's traversed. When you select the Remove Pixels Only mode, a region is not created when the subsequent traverse is run. However, pixels on the contour of the object are erased as they are encountered. This provides immediate visual feedback on the traverse's progress. "Immediate" is the operative word here: The traverse of a 3000-pixel contour that examines over 7000 pixels takes less than three-quarters of a second. The Remove Pixels Only option was a useful tool during the early stages of writing this program because I had no other way of checking whether the contouring algorithm was working correctly.

The above statistics come right out of the program. Every time a traverse is completed, the number of pixels traversed and the number of pixels examined are written to the menu bar to the right of the Display menu.

The final three items in the Traverse menu are Copy Region to Work Area, Add Region to Work Area, and Subtract Region from Work Area. These menu selections deal with something I call the work area, although it might more properly be called the working region. The work area is initially just a separate copy of the first region created when you traverse an object. You can then run additional traverses on other objects in the RegionMaker window and add and subtract the regions created to the one in the work area to build more complex regions.

As you might suspect, Add Region to Work Area implements the QuickDraw UnionRgn call, while Subtract Region from Work Area implements DiffRgn. The first time you run a traverse, you initialize the work area with the newly created region by selecting Copy Region to Work Area. You can then go back and run additional traverses, adding and subtracting regions as you go.

Figure 3 is an example of a graphics object that requires multiple traverses. To create one region that reproduces the shapes of the three letters and their constituent parts, it is necessary to run eight separate traverses: three for the exterior boundaries, three for the interior boundaries, and two for the hole in the middle of the A.

The Display menu lets you display the region in the work area in several different ways. Erase Window should be obvious. Frame Region and Paint Region implement FrameRgn and PaintRgn, respectively. Invert Region calls the QuickDraw routine InvertRgn: Every white pixel in the region becomes black, and every black pixel becomes white. The last menu item in the Display menu is Display Region Size. This option writes the size of the region in the work area, in bytes, in the menu bar to the right of the Display menu.

Menu Manipulation

A good deal of the RegionMaker program concerns itself with varying the appearance and behavior of items in the menus at the top of the screen. A number of the routines in the Menu Manager section of ROM let you change the appearance of menu items during program execution. This includes the ability to enable or disable individual items or entire menus. An enabled menu item is selectable. That is, scrolling down the menu and releasing the mouse button over that item returns information to the program in the form of an event record. The program can inspect the event record to determine that the mouse was pressed. The program can then determine which menu item was selected and take appropriate action.

Certain selections might not be meaningful in all situations. This depends on context. In the RegionMaker program, for

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example, it makes no sense to invoke Copy Region to Work Area if a traverse has not yet been performed. Likewise, it makes no sense to select Paint Region if a region has not been copied to the work area. A disabled menu item appears dimmed, in a "ghosted" typeface. You can scroll up and down over a disabled item and the Menu Manager will take no action whatsoever. The Event Manager will not inform the program that a menu selection was made.

Once a region has been copied to the work area and all the menu items have been enabled, they remain enabled and selectable for the duration of the session. If you run a traverse to build a region and then switch to Remove Pixels Only mode, the program does not dispose of the region.

This raises one other point: The original picture that was pasted onto the Clipboard remains there for the duration of a session unless you return to the Scrapbook to get a new one. The picture can be repasted onto the screen (erasing what was there) at any time, either by selecting Paste from the Edit menu or by pressing Command-Shift-V. This is useful if you've made some catastrophic error along the way and want to start over again.

Cursors

Cursors are another user interface feature that can provide useful visual feedback. When the RegionMaker program launches, the initial cursor is Apple's customary "north-by-northwest" arrow. Once a picture has been pasted onto the screen, however, the standard arrow changes to a custom "traverse" cursor, a horizontal arrow that points to the right. The shape of the cursor suggests that you can now point to the right at the object you want to contour and press the mouse button to initiate a traverse.

Resources

Once you've created the region you want, the File menu selection Write Work Area to Disk lets you add the region to a new or existing file as a region resource. This term is of my own devising—unlike cursors and alerts, no standard resource type for regions exists in the Macintosh environment.

Resources are disk-based packets of information, many of which contain the basic templates that describe the size, location, and appearance of the objects used in the Macintosh user interface. A WIND resource, for example, describes the screen position and dimensions of a Macintosh window that is to be used by a particular program as well as the style of the window frame that surrounds it and its title. A CURS resource contains the 34 words of data that specify both the visual appearance of a Macintosh cursor and the point in the cursor image that is to be associated with the mouse's position. Resources can contain more than just this type of descriptive information. For example, a program's code is stored and retrieved from disk in the form of CODE resources.

The Resource Manager's facilities handle the storage and loading of resources from disk. The Resource Manager uses routines that are totally independent of those provided by the File Manager; indeed, the Resource Manager operates on resource files, a filing system that coexists with, but is distinct from, that used by the File Manager. Macintosh files consist of two parts or forks. File Manager operations access data in the data fork of a file, while the Resource Manager uses a file's resource fork for its disk-based storage.

Unlike File Manager operations, which need to specify the volume and filename of the file being operated on, Resource Manager operations refer implicitly to all open resource files. When a program launches, its own resource fork and that of the System file are automatically opened. Any search for resources that the program references automatically defaults to these two files. You can easily change these defaults.

The power and utility of the Resource Manager are evident in the ease with which programs can use its routines to access the resources they need. For example, the single call GetResource('CURS', 10) in RegionMaker searches the program's resource fork for the specified cursor resource, loads it into memory if it is found, and returns a handle to its location. The data for the cursor resource, along with the resources describing the program's windows, menus, dialog boxes, and alerts, was originally specified in the source file RegionMaker.R and compiled into the application's resource fork with the RMaker program.

The two parameters used by the GetResource call specify a resource type and a resource ID: These serve to identify the resource uniquely. In this particular case, a CURS resource is a standard Macintosh resource that is known to several routines in QuickDraw. However, programs can also define their own resources, the internal format of which is meaningful only to the particular program creating or using them. RegionMaker uses the AddResource call to create a region resource. AddResource takes a resource type, ID, and name as parameters, as well as a handle to the region data. The name parameter is optional.

Saving the Resource to Disk

The File menu selection Write Work Area to Disk invokes two dialogs. The first dialog gets the resource type, ID, and name of the region resource from the user and does some simple error checking on the validity of these parameters. The default resource type is REGN; you can change this to any four-letter sequence that you like.

The second dialog, SFPutFile, should be familiar to anyone who has used the Save or Save As File menu options found

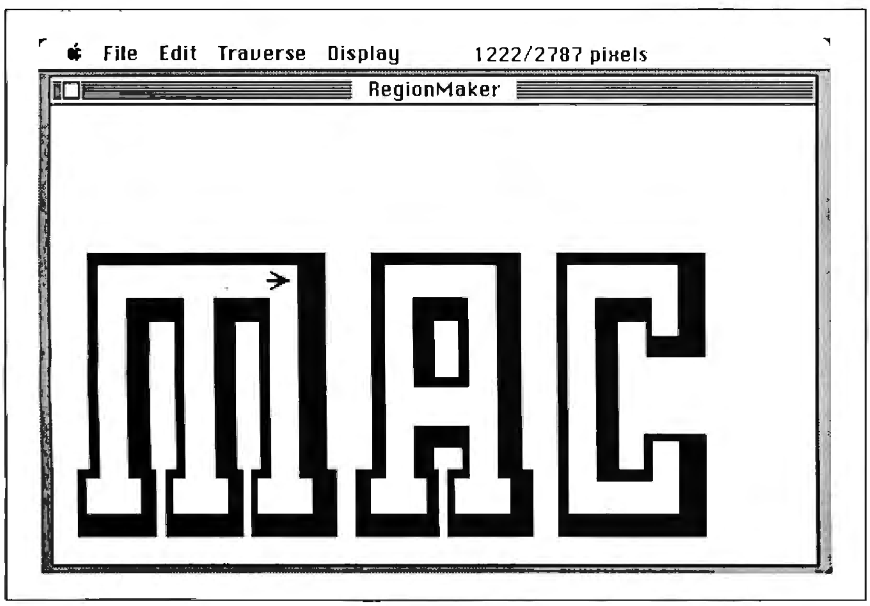

Figure 3: *The interior contour of the letter M has just been traversed. The traverse cursor points to the starting location of the traverse. The contour is 1222 pixels long, and 2787 points were examined during the traverse.*

continued

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in most Macintosh applications. It lets you enter the name of the file to which you want to save the resource and specify which disk the file is on. If the named resource file can be opened, it will be. If it can't be opened, it will be created. If it can't be created, the program reports an error.

When you're working with resources, these file-opening and -writing operations lie in the domain of the Resource Manager, not the File Manager. You open resource files with the call OpenResFile and create them with the call CreateResFile. You write the resource to the specified file with WriteResource.

Error Messages

Several error conditions can occur during RegionMaker's execution. Errors are generally reported in Macintosh programs by alerts, which are simply windows that appear on the screen with an informative message and an OK button that you can click once you have read the message. The seven error messages that RegionMaker displays are listed as string resources in the RgnMaker.R file.

The message "Couldn't Locate the Starting Point" indicates that the program could not locate a set pixel on its left-to-right scan after you pressed the mouse button to initiate a traverse. Instead of finding an object in its path, the scan ran up against the right side of the window. If you get this error message, you should reposition the mouse and try again.

"Couldn't Find a Closed Loop" announces that the algorithm has failed. This generally indicates that the exterior or interior boundary of the object being traversed does not form a closed path—the traverse failed to return to its starting position. This can happen in one of two ways: The algorithm failed to locate a next pixel on the contour from the current position, or the total number of pixels examined exceeded a preset maximum. I've set an arbitrary limit of 8000.

Several errors report that you entered invalid parameters during the dialog for specifying the resource type, ID, and name. The type, for example, must be exactly four characters long. The ID must lie in the range 0 to 32,767.

The message "That Resource Already Exists" indicates that the program detected a duplicate resource of the specified type and ID in the designated file. Change either the type or the ID to make it unique.

The last message, "Can't Add to Resource File," is a catchall indicating either that the Resource Manager was unable to create or write the resource or that the file the user selected to write to could not be opened or created.

Bug in ROM

You should be aware that a well-known bug in the 128K and 512K Macintosh ROMs can cause a dramatic crash if you attempt to build regions that are too complex. I've had this happen on several occasions. Figure 3 is a good example of this problem—I can run seven of the eight traverses required to produce one region from the objects, but the eighth attempt inevitably blows up my 512K Macintosh. The order of the traverses doesn't seem to matter. Apple says that the problem has been corrected with the new 128K ROMs in the Mac Plus.

RegionMaker might ultimately prove most useful as a desk accessory. At present, you must create the graphics images for contouring with other applications and then laboriously transfer them through the Scrapbook. With RegionMaker as a desk accessory, you would not have to do this, and you could do contouring right on top of the original application. The art of writing desk accessories, however, is fairly esoteric; until quite recently, I've had little experience in that area. It's on my list of several future projects. ■

Byron Sheppard

High-Performance Software Analysis on the IBM PC

Examine routine execution times with this high-resolution timer

Do you count clock cycles and shuffle code in order to boost program performance? Do you replace shift-by-*n* instructions with multiple shifts in an attempt to turbocharge your software? Or do you save values in unused registers rather than push them onto the stack? If you've done any of these, this article is for you. It describes a high-resolution timer capable of detecting speed differences down to a single bus cycle. This will allow you to examine single instructions and accurately analyze your favorite speed-up techniques. But be forewarned. The results may surprise you. Due to peculiarities of the 8088 microprocessor, many optimization attempts actually result in slower code!

Fortunately, the IBM PC includes all the hardware necessary to easily implement a high-resolution timer. I will discuss the design and implementation of such a timer, and then I'll demonstrate its use with examples illustrating optimization techniques on the 8088.

Background

DOS provides real-time clock functions through interrupt 21h (you can also use a BIOS interrupt 1Ah). Unfortunately, it only returns results down to 1/100 second. (Actually, since DOS monitors time by counting counter 0 interrupts, which occur every 55 milliseconds, the resolution provided by these services is closer to 1/20 second.) Inherent in these routines, however, is the ability to time events down to approximately 840 nanoseconds. The challenge is to get at this base-level resolution and manage it in a useful way.

The basic timing interval in the PC is approximately 210 ns. This interval is multiplied by four to generate a special signal occurring once every 840 ns. This signal drives counter 0 of the 8253 timer chip, which is initialized by BIOS to count 65,536 input pulses before generating a pulse of its own. Consequently, the output of counter 0 occurs once every 55 ms, forming the basis for the DOS time-of-day functions.

The method to achieving 840-ns resolution is obvious. By controlling when counter 0 begins to count and when it stops, as well as by reading the number of input ticks counted, you can create a very high resolution stopwatch. This stopwatch would be capable of timing any event lasting between 0 and 55 ms with a resolution exceeding 1 microsecond. Fortunately, this is quite simple to do.

The Routines

The routines shown in listing 1 consist of two procedures: timer__start and timer__stop. They are used like a regular stopwatch. Calling timer__start starts the watch, while a call to timer__stop stops it—automatically displaying the elapsed time rounded to the nearest microsecond. Incidentally, only the display is rounded; internal resolution is maintained at 840 ns.

The TIMER__START Procedure

The 8253 timer chip has several modes of operation. BIOS initializes counter 0 to operate in mode 3 with a count cycle of 65,536. Mode 3 produces a square wave. This waveform is fine for timing purposes, but the method used to generate it causes problems. The counter decrements by 2 for each half cycle, at which time it toggles the output to the opposite state, reloads, and starts over. This causes an ambiguity, since a count of 4, for example, will occur twice in any given cycle—once in the first half and again in the second half.

The solution is to change counter 0's mode of operation to mode 2. It will now decrement by 1. As a side effect, the output will change from a square wave to an active-low pulse. However, this is acceptable because the counter's basic period and interrupt function are unaffected (BIOS initializes the 8259 interrupt controller to be edge-sensitive).

Once counter 0 is loaded (i.e., the stopwatch is started) there will be approximately 55 ms before the first interrupt. Thus, there is plenty of time to obtain the BIOS time-of-day count applicable when the stopwatch was started. This count is required only because the routines were designed to time periods greater than one 55-ms cycle. Note, however, that the program ignores overflow from BIOS timer__low. This means that once every hour (on the hour, if you've set the time) these routines will be in error if they were in use at the time of the overflow. Since you should always take multiple readings, this shouldn't be a problem. If for some reason you require hour-long timing intervals *and* microsecond resolution (otherwise you'd be using BASIC's TIMER function, right?), then you should modify the routines to monitor the 32-bit time-of-day count maintained by BIOS.

Incidentally, I bypassed BIOS to get the timer__low word because BIOS enables interrupts. Certain (admittedly specific) situations require interrupts to be off during the timing interval. Note, however, that interrupts must be on in order to time events greater than 55 ms.

The TIMER__STOP Procedure

The timer__stop routine is equally straightforward. It reads the current count

continued

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Listing 1: *The source code for* Profiler_timer, *a high-resolution software timer.*

```
;TITLE: Profiler_timer
;DESCRIPTION: Fully compensated, high resolution
;timer.
;Internal timing resolution = 838 ns.
;CALLING SEQUENCE: call TIMER_START (FAR call)
;                  code to be timed
;                  call TIMER_STOP  (FAR call)
;OUTPUT: Display of elapsed time between the
;TIMER_START call and the TIMER_STOP call.
;REGISTERS CRASHED: none
;STACK REQUIREMENTS: 10 bytes
;CONDITION OF INTERRUPTS: TIMER_START = no change
;  TIMER_STOP  = variable, exit on
;SPECIAL NOTES: -Counter 0 is used and must not
;be modified in the interval between the two
;timer calls.
; -All DOS timekeeping functions will operate
;as normal.
; -Timing events > 54.925 milli-sec requires
;interrupts ON.
; -PROFILER_TIMER does not affect code under test.
; Data segment = word combinable as DATASEG
; Code segment = byte combinable as CODESEG
;---------------------------------------------
DATASEG SEGMENT WORD PUBLIC
timer_low       equ     ds:[006ch]
bios_dataseg    equ     0040h
timer_mode      equ     43h
timer0          equ     40h
count           dw      0       ;no. of interrupt ticks
                                ; (54.925 milli-sec)
count_micro     dw      0       ;calc. from interrupt ticks
count_milli     dw      0       ;calc. from interrupt ticks
timer_micro     dw      0       ;from 8253 countdown...
                                ;...also final value
timer_milli     dw      0       ;final value
timer_sec       dw      0       ;final value
max_count       dw      65535   ;65536 ticks in a full count
adjustm         dw      67      ;compensation factor
timer_convert   dw      8381    ;838.096 nsec per tick
count_convert   dw      54925   ;54.925 milli-sec per count
ten_thousand    dw      10000
five_thousand   dw      5000
thousand        dw      1000
ten             dw      10
message_sec     db      'Seconds: ','$'
message_milli   db      'Milli-seconds: ','$'
message_micro   db      'Micro-seconds: ','$'
ASCII_string    db      5 dup('d'),0dh,0ah,'$'
DATASEG ENDS
; *** print macro
print_string    macro   ;DOS function call to print string
        mov     ah,9    ;  pointed to by DS:DX
        int     21h
        endm

        public timer_start, timer_stop, bin_asc
CODESEG SEGMENT BYTE PUBLIC
        assume cs:codeseg, ds:dataseg
; ***timer_start routine
timer_start     proc far
        push    ax
        push    dx
        push    ds
        mov     dx,dataseg ;point to my own data segment
        mov     ds,dx
        mov     timer_micro,0
        mov     timer_milli,0
```

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```
        mov     timer_sec,0
;---- initialize counter 0 of 8253 timer ---
        mov     al,00110100B     ;ctr 0, LSB then MSB,
                                 ; mode 2, binary
        out     timer_mode,al    ;mode register for 8253
        sub     ax,ax            ;0 results in max count
        out     timer0,al        ;LSB first
        out     timer0,al        ;MSB next
;--- read current BIOS time-of-day ---
        mov     dx,bios_dataseg ;point to BIOS data segment
        mov     ds,dx
        mov     ax,timer_low     ;get count
        mov     dx,dataseg       ;point to my own data seg.
        mov     ds,dx
        mov     count,ax         ;save count
        pop     ds
        pop     dx
        pop     ax
        ret
timer_start     endp

; ***TIMER_STOP routine
timer_stop      proc    far
        push    ax
        push    bx
        push    dx
        push    ds               ;save user's DS
        mov     ax,dataseg       ;point to my own
        mov     ds,ax
; Elapsed time since TIMER_START consists of:
;   1) timer count intervals - 840 ns
;   2) interrupt ticks - 54 ms
;---- read counter 0 of 8253 timer ----
        mov     al,00h           ;latch counter for read
        cli                      ;interrupts off until
                                 ; BIOS tod is read
        out     timer_mode,al    ;8253 mode register
        in      al,timer0
        mov     dl,al
        in      al,timer0
        mov     dh,al    ;dx has 16 bit timer count
;--- calc the time due to 8253 counting ---
        mov     ax,max_count
        sub     ax,dx            ;timer count value
        mul     timer_convert    ;get in usable form
        div     ten_thousand     ;gives time in usec
        mov     timer_micro,ax   ;save usec, round nsec
        cmp     dx,five_thousand
        jb      cont             ;round down
        inc     timer_micro      ;round up
;--- get BIOS time due to interrupt ticks ----
cont:   mov     dx,bios_dataseg ;point to BIOS data segment
        mov     ds,dx
        mov     ax,timer_low
        mov     dx,dataseg       ;point to my own data seg.
        mov     ds,dx
        sti                      ;interrupts ok now
        sub     ax,count         ;now have # of 54 ms ticks
        mul     count_convert    ;get into usable form
        div     thousand
        mov     count_milli,ax   ;save milli-sec part
        mov     count_micro,dx   ;save micro-sec part
;---- check for jitter ----
        cmp     ax,0    ;check if elapsed time is "small"
        jne     jitter_ok ;if not don't worry about jitter
        mov     ax,adjustm
        cmp     timer_micro,ax   ;
        jae     jitter_ok         if no jitter then ok
        mov     timer_micro,ax   ; else "-ve time artifact"
                                 ;  so fix
; Combine timer and count values, put result in timer vars.
```

continued

```
jitter_ok:
        mov     ax,dx    ;get count_micro
        add     ax,timer_micro   ;sum micro fields
        cmp     ax,adjustm       ;check for underflow
        jae     compensate       ;  go ahead - safe
        dec     count_milli      ;  borrow
        add     ax,1000
compensate:
        sub     ax,adjustm       ;compensate for time delays
        mov     timer_micro,ax
        cmp     ax,1000          ;check for field overflow
        jb      fld_ok           ;timer_micro field ok
        sub     dx,dx            ;timer_micro too large
        div     thousand    ;so carry out into timer_milli
        mov     timer_milli,ax
        mov     timer_micro,dx
fld_ok: mov     ax,count_milli   ;sum milli fields
        add     timer_milli,ax
        cmp     timer_milli,1000 ;check as above
        jb      display
        sub     dx,dx
        mov     ax,timer_milli
        div     thousand
        mov     timer_sec,ax
        mov     timer_milli,dx
;------ Display results -----
display:
        lea     dx,message_sec   ;display seconds header
        print_string
        lea     bx,ASCII_string ;convert seconds in ASCII
        mov     ax,timer_sec
        call    bin_asc
        mov     dx,bx    ;bx points to converted ASCII string
        print_string             ;display seconds
        lea     dx,message_milli ;display milli-secs header
        print_string
        lea     bx,ASCII_string ;convert milli-secs in ASCII
        mov     ax,timer_milli
        call    bin_asc
        mov     dx,bx
        print_string             ;display milli-seconds
        lea     dx,message_micro ;display micro-secs header
        print_string
        lea     bx,ASCII_string ;convert micro-secs in ASCII
        mov     ax,timer_micro
        call    bin_asc
        mov     dx,bx
        print_string             ;display micro-seconds
        pop     ds               ;restore user's DS
        pop     dx
        pop     bx
        pop     ax
        ret
timer_stop      endp
;---------------------------------
; Binary to ASCII conversion routine
; Entry: BX = pointer to string buffer
;        AX = unsigned binary number
; Exit: BX = pointer to ASCII number
;---------------------------------
bin_asc proc near
        push    dx
        push    cx
        push    ax
        mov     cx,5             ;clear string buffer
clear_buf: mov  byte ptr [bx],30h
        inc     bx
        loop    clear_buf
convert: sub    dx,dx    ;clear upper half of dividend
        div     ten              ;(dx:ax)/10
        add     dx,30h           ;decimal digit to ASCII
```

continued

in the 8253 timer and the BIOS timer_low variable. It then computes and displays the elapsed time.

The program compensates for bias due to the timer routines. Notice that modifications in the code may require a different compensation factor. To calculate this factor, change the variable adjustm from 67 to 0 and then use the routines to time a zero-duration event:

```
call timer_start
call timer_stop
```

They will tell you that the zero-duration event took *x* microseconds. This amount represents the timer overhead that you should assign to adjustm.

Applications

The above routines were implemented in this manner to make them simple to use. For example, to time a point-plotting routine I had written, I created a test procedure with calls to the two timer routines as follows:

```
main_test proc far
          ;called from DOS
          mov     ax,xcoord
          mov     bx,ycoord
          call    timer_start
          call    pset
          call    timer_stop
          ;return to DOS
main_test endp
```

The elapsed time is displayed automatically. If the point-plotting speed is unacceptable, I can modify pset and easily retime its execution.

You can time program fragments just as easily. In order to compare the speed of various schemes mapping pixel coordinates to the required byte address, I timed the section of code that performed the mapping. I then used my editor's block-move feature to substitute other algorithms. When I had finished, I kept the fastest and threw away the rest. This is perhaps the area where high-resolution timers are most effective.

Experimenting with these timer routines can be very instructive. Few 8088 programmers really know how long various instructions take to execute. Published material can be misleading. Certain optimizing strategies actually result in slower code than nonoptimized versions. Consider, for example, the 8088 multiply (MUL) instruction.

MUL, the 8-bit register multiply, takes a minimum of 70 cycles to execute. This may be acceptable when multiplying 83 by 51, but not when multiplying by a fixed constant such as 15. In this case a multiply-

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```
        dec     bx
        mov     [bx],dl         ;save character
        or      ax,ax
        jnz     convert         ;finished?
        pop     ax
        pop     cx
        pop     dx
        ret
bin_asc endp
CODESEG ENDS
        end
```

by-15 subroutine implemented with shifts and adds could result in a significant speed improvement. Since this assumption is a common one, let's examine it.

Here is the multiply subroutine:

```
mult_by_15 proc near
  mov dx,ax   ;save the number
  mov cl,4
  sal   al,cl
  sub  ax,dx   ;ax = number * 15
  ret
mult_by_15 endp
```

Of course I'm cheating a little, since shifting by a count factor in CL requires [8 + (4 * CL)] = 24 cycles to execute. The special case of shifting by one only requires 2 cycles; therefore the multiply subroutine could be optimized by writing out four separate shift instructions as follows:

```
opt_mult15 proc near
      mov    dx,ax
      sal    al,1
      sal    al,1
      sal    al,1
      sal    al,1
      sub    ax,dx
      ret
opt_mult15 endp
```

We'll examine the following cases:

```
Case 1:
      call  timer_start
      mov  dl,15
      mul  dl
      call  timer_stop

Case 2:
      call  timer_start
      call  mult_by_15
      call  timer_stop

Case 3:
      call  timer_start
      call  opt_mult15
      call  timer_stop
```

Calculating the execution times by adding clock cycles results in the following:

Case 1 = 15 μsec, approx. 74 cycles
Case 2 = 14 μsec, approx. 68 cycles
Case 3 = 10 μsec, approx. 48 cycles

The actual results, however, are startling:

Case 1 = 14 μsec, MUL
Case 2 = 21 μsec, shift and add
Case 3 = 22 μsec, optimized shift and add

Clearly the MUL instruction is the fastest, performing as expected. The attempted improvements actually resulted in poorer performance. Incredibly, the most optimized version ran the slowest. Why? Because the 8088 CPU is severely bus-bound. Since most assembly language reference books are based on the 8086, this fact is often overlooked. This creates a severe distortion in performance expectations. Execution times listed must compensate for the 8088's byte-wide data bus. This translates into adding an extra four cycles for every word transfer, as well as recognizing that instruction fetch time is significant on the 8088. Thus a single shift instruction may very well execute in two cycles—or it may take four times as long. It depends on the preceding instructions.

The above shift and add subroutines may execute faster on an 8086, but not on an 8088. Improving over the MUL instruction requires in-line code. When the above subroutines are implemented as macros, the results change to

Case 1 = 14 μsec
Case 2 = 8 μsec
Case 3 = 10 μsec

Notice the large differences between in-line code and the subroutine implementation. These differences indicate a much larger overhead due to the CALL instruction than most people would expect. Compensating for the 8088's smaller data bus only partially accounts for the difference. In this case, the effect of nonlinear code on the instruction prefetch queue is subtly apparent. With in-line code, the multiply routines are entered with a full (or partially full) instruction queue. Thus, the first couple of instructions are drawn from the queue with no instruction fetch overhead. On the other hand, because the subroutine is a jump to a different area of memory, the bus interface unit has essentially wasted its time and is forced to dump the queue's contents. This results in the multiply routines being entered with an empty instruction queue. Consequently, the first instructions have a significant instruction fetch overhead. In fact, since this routine consists of extremely fast instructions, starting with an empty queue affects the entire routine. The queue never has time to catch up, and instruction fetch cycles are significant throughout.

Further analysis of the above examples indicates that the in-line version of case 2 results in a worthwhile speed gain. Notice, however, that the popular technique of writing out shift instructions for greater performance (case 3) is clearly inferior. Furthermore, the difference between case 2 and case 3 can be increased if register usage could be arranged so that CL already contains the required shift count, thus obviating a special MOV. This is consistent with my experience. While the repeated versions of instructions often appear to impose a significant performance penalty, the saving in op code fetches more than compensates. Regrettably, code optimized for the 8086 will consequently run slower on the 8088. It must be optimized differently.

Conclusion

The above examples suggest that 8088 programmers need to develop a unique feel for performance characteristics. The faster an instruction appears to execute, the greater will be the performance distortion. Notice that the MUL instruction performed as expected. This is because its execution is not dominated by data transfers nor op code fetch cycles. These types of instructions perform as fast as on an 8086. On the other hand, fast instructions like SHIFTs and MOVs drain the instruction queue, creating a substantial distortion error, often exceeding 100 percent. Branch instructions contain a hidden penalty in that they force the subsequent block of code to begin with an empty queue—often significant on the bus-bound 8088. These subtleties can result in optimized code underperforming its nonoptimized equivalent—a situation best detected with a high-resolution timer.

As always, achieving maximum performance requires a systems approach, but a high-resolution timer has proven to be an essential tool when analyzing high-performance software. Indeed, for those of you just finishing a clock-counting blitz, I have to ask:

How much time did you *really* save? ■

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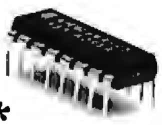

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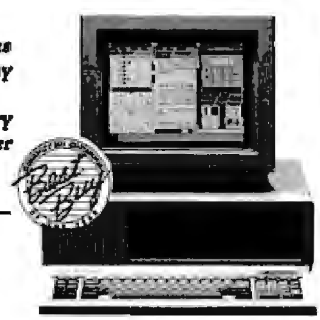

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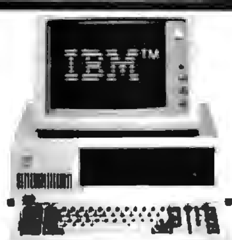

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Dynamic Memory Allocation

Dynamic data structures can expand and contract as needed

For many years, the built-in data types and structures used in high-level languages limited the way you could program. However, more recent languages allow you to express your programming creativity more fully.

Pascal gives you the flexibility you need to program according to the demands of the problem. For example, you can create data structures that expand until your *physical* memory is full. These *dynamic* structures offer an alternative to the more commonly used array structures.

The most popular dynamic data structures are trees, stacks, queues, and linked lists. I will discuss linked lists and the basic concepts you need to work with dynamic structures in Pascal (specifically, Apple II Pascal).

Static Memory

In Pascal, array structures and records provide excellent ways of manipulating related data and, if used together as an array of records, can provide the data structure necessary to handle, for example, inventory. However, the structure of the array of records structure is static and requires that you specify in the program code the maximum amount of memory that the structure will use (see listing 1). (I used the UCSD Pascal type string[*maximum*] instead of writing out packed array[1..*maximum*] of char.)

This structure defines the variable STOCK as an array of record type INFO. When you compile the program, you assume that there will never be more than 1000 coats in stock at any one time. If there are, the program will fail. You could probably change the array subscript and recompile the program. But if the program logic is centered on the array subscripts, you could face a massive rewrite. Another solution would be to use a different data structure.

Dynamic Memory

Dynamic memory is referenced as you need it during run time, not reserved ahead of time. It allows great flexibility during program execution because the data structure occupies only the memory it needs and no more. If you have two structures and you don't know which will need more memory, dynamic structures can expand and contract as needed to avoid overallocation.

Adding, deleting, and sorting elements in a dynamic data structure are easy and efficient. In figure 1 these three actions are performed on both an array and a linked list. Assume for the moment that each element in the linked list also has a pointer to the next element and that the last element points to a marker called NIL. Before you can add to the middle of the array (figure 1a), you must shift all the elements below that point to accommodate the new one while maintaining the order. If the array has many elements, this could take some time.

Deleting an element (figure 1c) generates just as much movement; you don't want an empty location in the middle of your array. If you sort the array conventionally (figure 1e), B and C must be physically moved from their respective locations. Again, this involves massive data movement.

However, to add to the linked list (figure 1b), you simply place the new element at the end of the list and set up your pointers. To delete an element (figure 1d) from the linked list, you simply bypass it, again with a pointer. This effectively removes the element from the list. Sorting (figure 1f) is also done with pointers. The only data movement involved is pointer movement; the elements themselves remain in their original locations.

Pointers

Pointers (specific memory addresses) provide the means for dynamic memory allocation. Most computer languages use pointers in one way or another. The compiler and the operating system use them to keep track of variables, etc. While most

continued

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Listing 1: *A data structure defining the variable* STOCK *as an array of the record type* INFO. *Notice the assumption that there will never be more than 1000 coats in stock at any one time.*

```
TYPE
  info=record
       COATS:integer;
       PRICE:real;
       KIND:string[7]
     end;
  inventory=array[1..1000] of info;
VAR
  STOCK:inventory;
```

high-level languages don't have the ability to manipulate pointers directly, Pascal does. However, the pointers must be of a predeclared type. The appropriate syntax is a ^ placed just before the type, whether it is a primitive type like integer or a record. The program reads the ^ as "pointer." For example, listing 2 contains a record type INFO and a declaration for INFOPOINT, which is a pointer to INFO.

The variable PERSON contains the pointer to (address of) the record type INFO. Note that you cannot write this value using WRITE or WRITELN or perform arithmetic operations on it. This declares one record; if you want *n* of these, you must predeclare *n* variables. To overcome this problem, some changes have to be made in data structure. Arrays of records are accessed by subscripts—for example, STOCK[1].field;. Without the array structure, you must define another field in the record to hold the pointer linking the records together. This field is a pointer to another record of type INFO, so it must be of type INFOPOINT. The final data structure looks like listing 3.

Notice that a reference to INFO is used before INFO is defined. This is the only time you can do this in Pascal. The INFOPOINT declaration must be made before the INFO declaration because INFOPOINT is the type of one of INFO's fields. If the declarations aren't in that order, you will get an error message during compilation.

Memory Management

Nowhere in these declarations do you set aside a certain amount of memory for the records. You obtain space for the previous record with the reserved word NEW—for example, NEW(PERSON);. When you call NEW at run time, you allocate memory locations for the record specified at the top of the *heap*, the area of memory occupied by the program, variables, etc. To deallocate the memory, a combination of the reserved words MARK and RELEASE is used; they will be described later.

At the other end of memory is the stack that builds down from high memory. The area between these two is the memory you can use (see figure 2). When memory is added to the system, the operating system pushes the stack back to higher memory. In most microcomputers, this lets you expand your system without changing the software.

Linked Lists

This record, the one with at least one field pointing to another record, is the basic building block in dynamic data structures and is called a *node*. Graphically, a node

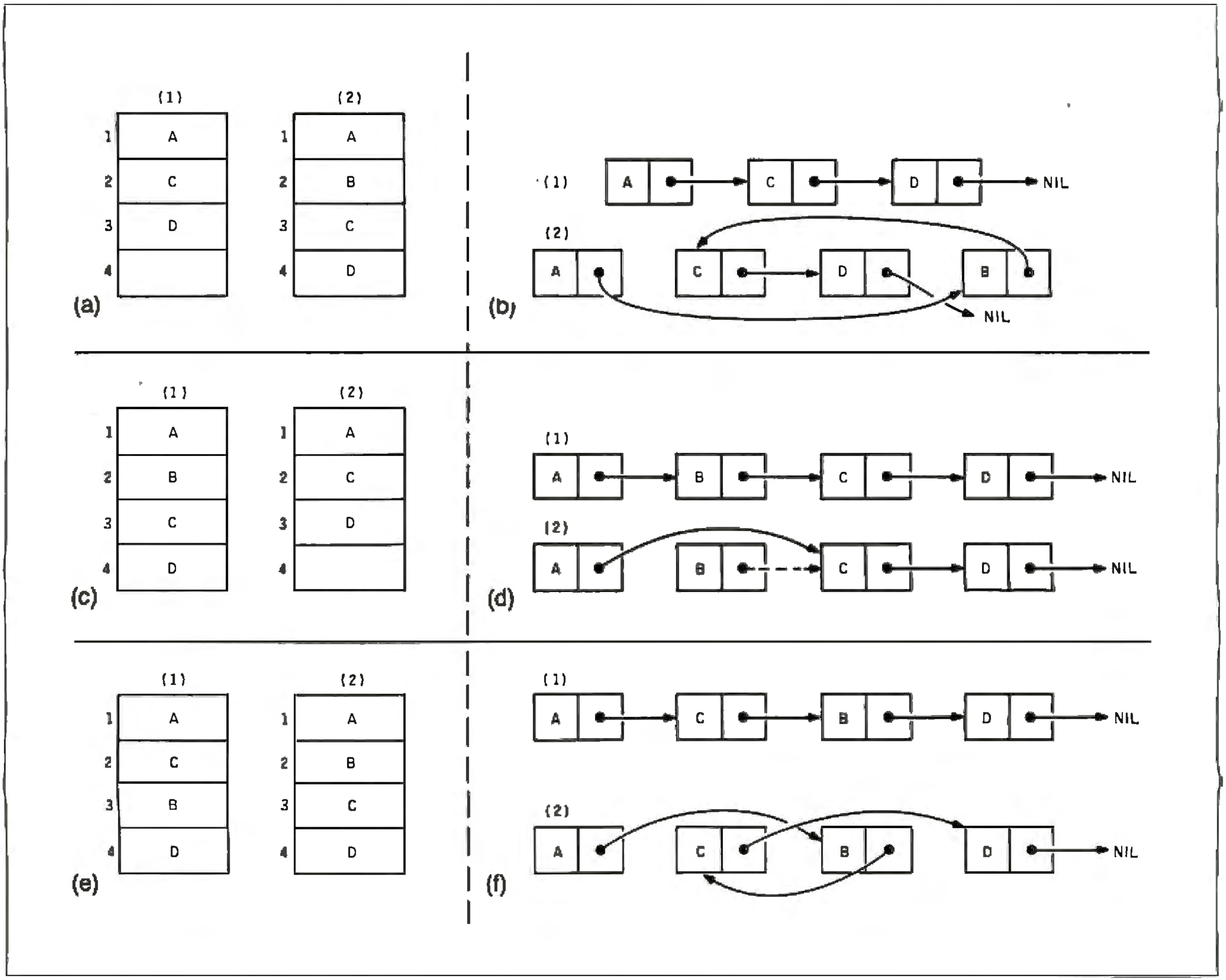


Figure 1: *Addition, deletion, and sorting performed on both an array and a linked list. (a) Addition operation performed on an array. (b) Addition operation performed on a linked list. (c) Deletion operation performed on an array. (d) Deletion operation performed on a linked list. (e) Sorting operation performed on an array. (f) Sorting operation performed on a linked list.*

is represented by the rectangle (the record) and the arrow (the pointer) as in figure 1.

How do you access the pointer to the next node, the link between the records? Since you are dealing with records, you use the same notation that you would for any record—but with an additional ^. For example, PERSON^.NAME accesses the node's NAME field, and PERSON^.LINK accesses the pointer. To summarize: PERSON contains the address of the record, PERSON^ is what's at that address, and PERSON ^.NAME is the value stored in the field NAME.

If two PERSON nodes are linked together and you want to get the NAME in the second node, you use PERSON^.LINK^.NAME. This refers to the value of NAME in the node pointed to by the LINK in the record addressed by PERSON. Thus, if you have a large series of nodes tied together by pointers and you want the NAME in the fourth node, you use PERSON^.LINK^.LINK^.LINK^.NAME. This becomes impractical, however, especially if you have to search through every node in the list. A better method is to have a pointer move along the nodes, examining their contents until it finds the appropriate node. The program LINKLIST.PAS maintains a linked list of strings in alphabetical order. [Editor's note: *The LINKLIST.PAS listing is available in Apple Pascal source code on disk, in print, and on BIX. See the insert card following page 424 for details.* The

continued

Listing 2: *A type declaration for record type* INFO *followed by a declaration for* INFOPOINT, *which is a type pointer to* INFO.

```
TYPE
  INFO=record
       NAME:string[10];
       ADDRESS:string[10]
     END;
  INFOPOINT=^INFO;
VAR
  PERSON:INFOPOINT;
```

Listing 3: *The final data structure. Notice the addition of the* LINK *field that holds a pointer that links the records together. It is a pointer to another record of type* INFO, *so it is also of type* INFOPOINT.

```
TYPE
  INFOPOINT=^INFO;
  INFO=record
       NAME:string[10];
       ADDRESS:string[10];
       LINK:infopoint
     END;
VAR
  PERSON:INFOPOINT;
```

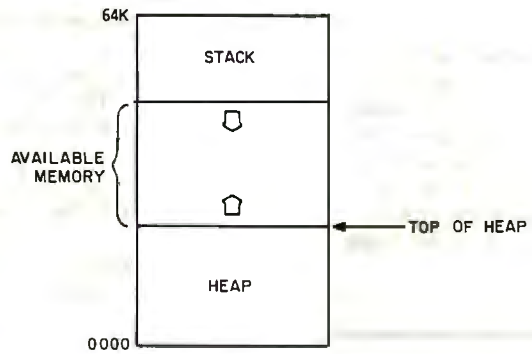
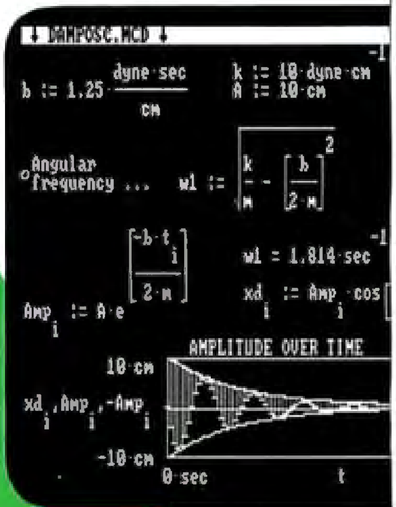


Figure 2: *Main areas of system memory.*

Listing 4: *The procedure* INITIALIZE, *which creates the first node in the linked list and sets up the heap pointer.*

```
PROCEDURE INITIALIZE(VAR LIST:LISTPOINT);
BEGIN
  NEW(LIST);
  LIST^.LINK:=NIL;
  MARK(HEAP)
END;
```

listing is also available on BYTEnet. See page 4.]

The procedure INITIALIZE (listing 4) creates the first node in the list using NEW, and then its pointer is set equal to NIL. The links must be defined; if they aren't, your pointer is meaningless. The NIL value provides us with a *plug* for unwanted links and an end-of-list indicator for which you can search (figure 3). Notice that there is no value for the field NAME. This first node is the head of the list and does not contain data. LIST contains the address of this node—that is, it points to this dummy node. I like to use a dummy node because it accommodates my search technique. Therefore, because LIST always points to it, you can pass it as a value parameter, and you can copy it. This lets you make such statements as CURRENT:= LIST, which means that CURRENT^.LINK points to the same thing as LIST^.LINK. When you equate CURRENT and LIST, both pointers contain the same address. However, the statement CURRENT^ :=LIST^ equates the data to which they point.

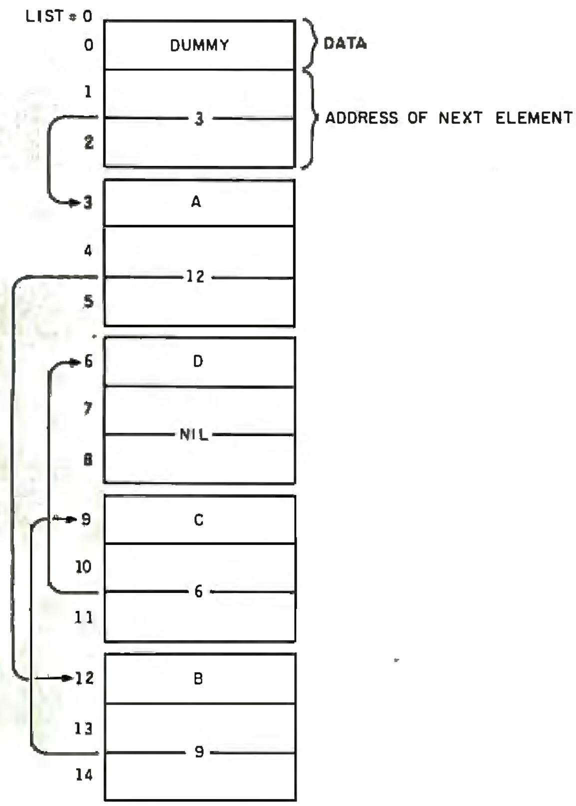


Figure 3: *This is the internal representation of an ordered linked list of characters. Each record takes 3 bytes: 1 for the data and 2 for an address between 0 and 64K bytes. In this example, the data was entered in the order* ADCB, *but notice how the linked list maintains the correct order. Begin with the dummy node. It points to and holds the address of the first element* A *at location* 3. *The* A *node in turn points to* B, *which is kept at* 12. *Going through the list in this manner, you get the feeling of the sequential nature of searches and retrieval. When elements are deleted, added, or sorted, some addresses change, but the data is never recopied.*

Listing 5: *The procedure* PREVIOUS, *which returns a pointer containing the address of the node prior to the target node or* NIL.

```
FUNCTION PREVIOUS(LIST:LISTPOINT; TARGET:ST1):LISTPOINT;
VAR
  CURRENT:LISTPOINT;
BEGIN
  CURRENT:=LIST;
  WHILE (CURRENT^.LINK^.NAME<TARGET) AND (CURRENT^.LINK<>NIL)
    DO BEGIN
      CURRENT:=CURRENT^.LINK
    END;
  PREVIOUS:=CURRENT
END;
```

You can move along the list by incrementing the pointer, but you must do it the right way. The following two seemingly equivalent statements represent the difference between effective and useless code:

Poor code:
LIST:=LIST^.LINK
Good code:
CURRENT:=CURRENT^.LINK

In both cases you move the list pointer along by storing the address of the next node in the variable that contains the address of the current node. However, in the first example, the original address of the list is lost. By creating an *auxiliary pointer*, CURRENT, you can move along the nodes as you wish, and when you want to return to the beginning, you just reequate the two variables.

There is an example of this process in the function PREVIOUS (listing 5). LIST points to the first node after INITIALIZE. CURRENT, the auxiliary pointer, is equated to LIST and then incremented to find the target. This procedure checks the name of the node ahead of it, so when the target is found, CURRENT is pointing to the previous node. The search terminates when it finds a NIL or encounters the target.

The procedure ADD (listing 6) calls NEW and manipulates the pointers so the new node is inserted after the mode selected by PREVIOUS. SUBTRACT (listing 7) modifies the pointer to the previous node, so it points two nodes down the list. However, when nodes are overstepped like this, their locations are lost to the software. You can recover them from the allocation with the reserved word DISPOSE. Unfortunately, this procedure isn't implemented in Apple Pascal, so whenever a node is overstepped, its memory is unusable from then on.

The last statement in the INITIALIZE procedure compensates partially for this. The MARK procedure marks the location of the top of the heap after it calls NEW. A call moves the pointer to the top into the variable HEAP.

When you want to empty the list, you can call the procedure KILL_LIST (listing 8). It contains a call to a procedure named RELEASE. RELEASE resets the heap pointer to the value determined by MARK, which in effect destroys the heap. I call MARK only after the first node has been placed on the heap so that when the heap is destroyed, a head node will always remain. If you remove the MARK and RELEASE procedures, the program soon runs out of memory as it processes more and more elements. It is extremely important that you be able to recover unused memory locations. An alternate, but much more complicated, method is to maintain a list of unused locations, so the software knows the location of every memory element and its state.

Program Goodies

I error-proofed the command entry with a set structure. If the entry is not in that set, the program waits until a proper one is entered. Also, I put a compiler command at the top that shuts off array-subscript range checking. This may speed up execution slightly.

The program accepts its entries from the keyboard, but you can easily modify it to read a data file instead (listing 9).

The Bad News

Dynamic memory allocation doesn't provide this added-on memory on all microcomputers. For example, the Apple Pascal designers (prior to version 1.2) permanently set the stack to start at 64K bytes and build down. This means that the extra 64K bytes in an Apple IIe will never be touched without some assembly language programming. Fortunately, Apple Pascal version 1.2 took care of this shortcoming. With the older version only about 36K bytes of memory were available for data.

Summary

The program LINKLIST.PAS should provide you with at least the basic building blocks for programs using abstract data types and structures. The procedures to do basic list operations are self-contained, so you can easily put them into your own programs. And with some imagination, you can turn the program's foundation into simple inventory management by adding a few fields to the record.

Dynamic memory allocation enables reservation systems to remain in operation as they expand simply by plugging in more RAM. The insertion or deletion of elements is much faster and more efficient because the data doesn't need to be moved around in memory. However, you pay a price for these advantages: an added overhead because the data access becomes sequential and the individual records become larger—you need room for the pointers. All in all, however, dynamic structures offer an excellent alternative to static memory. ■

Listing 6: *The procedure* ADD, *which adds a node to the linked list between two existing nodes.*

```
PROCEDURE ADD(VAR PREV:LISTPOINT);
VAR
  TEMP:LISTPOINT;
BEGIN
  TEMP:=PREV^.LINK;
  NEW(PREV^.LINK);
  PREV^.LINK^.NAME:=TARGET;
  PREV^.LINK^.LINK:=TEMP
END;
```

Listing 7: *The procedure* SUBTRACT, *which removes a node from between two other nodes.*

```
PROCEDURE (SUBTRACT(VAR PREV:LISTPOINT);
BEGIN
  PREV^.LINK:=PREV^.LINK^.LINK
END;
```

Listing 8: *The procedure* KILL_LIST *destroys the contents of the linked list.*

```
PROCEDURE KILL_LIST(LIST:LISTPOINT);
BEGIN
  RELEASE(HEAP);
  LIST^.LINK:=NIL;
  PAGE(OUTPUT);
  WRITELN('List is now empty.');
  SHOW_MEM
END;
```

Listing 9: *A procedure to read a data file into the linked list of the program LINKLIST.PAS.* READ_IN *assumes there is one name per line of the data file.*

```
PROCEDURE READ_IN(VAR LIST:LISTPOINT);
VAR
  LIST,NEXT:INFOPOINT;
  IN:TEXT;
BEGIN
  RESET(IN,'APPLE1:DATA.TEXT');
  NEW(NEXT);
  NEXT^.LINK:=NIL;
  LIST:=NEXT;
  WHILE NOT EOF
    DO BEGIN
      NEW(NEXT^.LINK);
      READLN(IN,NEXT^.NAME);
      NEXT^.LINK^.LINK:=NIL;
      NEXT:=NEXT^.LINK
    END;
  CLOSE(IN)
END;
```

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Testing Intrinsic Random-Number Generators

A survey shows that all RND functions are not *created equal*

We published the results of a survey in *Interfaces* on the statistical characteristics and adequacy of a number of random-number generators on microcomputers (see reference 1). This article recapitulates and updates our findings.

For our original survey, we selected nine of what, at that time, were commonly used microcomputers. Each of the machines we selected had an intrinsic random-number generator—that is, one which is already in memory and ready for use when the unit is activated. In some cases, different languages that run on a given microcomputer had their own intrinsic generators. This was true for the IBM PC and the Apple IIe. We tested the following: Apple IIe CP/M BASIC; Apple IIe intrinsic Applesoft BASIC; Apple IIe intrinsic Integer BASIC; Apple III Business BASIC; AT&T PC 6300 GW-BASIC; IBM PC BASIC; IBM PC extended BASIC; Hewlett-Packard's HP 86 intrinsic BASIC; Tandy's TRS-80 Model III intrinsic BASIC; and Texas Instruments' TI-99/4A intrinsic BASIC. In addition, we have tested the Apple Macintosh Microsoft BASIC random-number generator, and we have also generated streams of random numbers using Lotus 1-2-3 and Symphony on the IBM PC.

Cycle Size Considerations

Every random-number generator produces a series of random draws that eventually repeats, and the number of draws that can be made before repeating is the length of the "cycle" of a random-number generator. The problem of repeating a sequence in a given simulation experiment is avoided by having a cycle size that is so large the user will not use more than a small portion of the cycle.

While random-number generators on mainframe computers have cycle sizes in the millions, a testing of cycle sizes of microcomputer random-number generators shows that there are a number of instances of small cycles. The Apple IIe, for example, has three different cycles. These cycles are accessed by using the RND function with a negative argument value. The longest cycle on the IIe is one that is associated with (−1) as the argument of the RND function. This cycle has a length of 37,758. A second cycle, RND(−2), has a length of 32,366, and the third random-number cycle on the Apple IIe has a length of only 202 (RND(−4)).

The random-number generators of the Apple IIe are surprising in another way: They are preceded by leading tails of numbers that never repeat. The unexpected existence of leading tails explains the report (see reference 2) that some arguments of the Apple IIe random-number generator are associated with very long cycles. The Apple IIe generator had leading tails of lengths of 36,774 (RND(−4) cycle), 53,478 (RND(−2) cycle), and 81,412 (RND(−1) cycle). Using different values for the argument of the RND function causes entry into a tail at a position that generally does not use all of the tail. Unfortunately, there does not exist a mathematical rule upon which one could predict which cycle was being used given any particular value of the RND function. If this were true, then one could at least avoid the very short cycle, but since one cannot predict which arguments of the RND function lead to which cycles, the random-number generator of the Apple IIe is seriously flawed. The Integer BASIC random-number generator of the Apple IIe does not have leading tails, but it has only one cycle. This cycle has a length of 32,767, and, therefore, it is probably too short for use in serious simulation experiments.

Random numbers generated on the IBM PC have the following cycle properties: First, there are no leading tails of nonrepeating numbers. This is true for both BASIC and extended BASIC on the IBM PC. And second, there is one cycle with a length of 65,536; again, too short for simulation experiments. This does not preclude the ability of users to provide their own random-number generators, but constructing a statistically adequate generator that provides numbers quickly enough to be useful is a task that is far from being trivial.

Seeding Considerations

Although proper seeding procedure is critical when using a random-number generator, user's manuals are not entirely informative about appropriate procedures. Several important characteristics of the various seeding schemes should be understood by the user. Inexperienced users of random-number generators need to be aware of how automatic seeding works on most microcomputers. Furthermore, there are peculiarities of the seeding procedures on individual microcomputers that bear significantly on the use of those machines. Particularly, seeding on the Apple IIe and the IBM PC does not occur in the manner that you might expect.

All scientifically sound random-number generators operate using a procedure that produces a random number by transforming a number currently stored in memory (the base). The transformations are based

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upon modular arithmetic operations, and their result replaces the old base number every time a new number is generated. The continual changing of the base number guarantees a sequence of differing draws.

Seeding is the act of providing the procedure with its first base number. The inexperienced user of random-number generators should realize that seeding must always be done. Therefore, all microgenerators are designed to automatically seed if the user does not do so. For most generators, the same seed always is used for the initial draw, and as a result, the same sequence of draws will always appear. On the Apple IIe, this seeding actually takes place when the computer is turned on. All subsequent draws, even when made in different programs, are drawn in sequence (unless the user overrides with the user seeding procedure). On some machines, when using the BASIC language, seeding is described in the manual as being performed using the statement X = RND(A), where A is a negative number. On other machines, seeding is indicated using the statement RANDOMIZE A, where A is generally positive and may have other limits depending on the machine. Both of these procedures can be used on the IBM PC.

Generally, the appropriate seeding procedure is easy to use and is shown in the manuals. What is not discussed in the manuals is a peculiarity of seeding that can lead to an inadvertent use of equivalent seeds. For example, for two different seeds on the IBM PC, using A in one case and B in another, the same sequence of random draws is created whenever A and B are related as follows: $k \times B = 2 \times A$ where k is any integer (either positive or negative). Thus, for example, A values of 1, 2, 4, . . . , 64, 128, and so on, produce identical sequences. A different sequence is produced by A values of 3, 6, 12, . . . , 192, and so on. This seems very surprising until you understand the process by which the actual seed is produced from the A value. BASIC interprets the value of A into base 2 scientific notation, and the seed is the mantissa of that representation. Consequently, A and B have the same mantissa and therefore deliver the same seed. This will cause the identical sequence of random numbers to be produced.

Statistical Tests

Several statistical tests are available to examine the validity of random-number generators. Discussions of these tests can be found in references 3, 4, and 5.

When surveying random-number generators, depending on the test and the microcomputer, the time required for a given test on a given microcomputer was never less than 30 minutes, and in one case it was 100 hours. Required times were a result of our desire to run each test many times (usually 100). Because of this time requirement, the testing was limited to five common statistical tests, three to examine conformance to the uniform distribution and two to examine the assumption of independent draws.

The three tests used to examine uniformity were the categorical-uniformity test, the extreme-value test, and the bit-gap test. The categorical-uniformity test is probably the most commonly used test for random-number generators. It tests for the broadest set of possible deviations from uniformity and is easy to implement. All of the generators that were tested passed this test, which, as it was used, examines intervals of size .01, while in many studies outcomes with much lower probabilities are simulated. Generally, these events are simulated using one of the tails of the uniform distribution. For this reason, the extreme-value test was used to examine the lower tail of each generator by comparing the number of observed values less than .001 with the number expected based on the assumption of uniformity. The Apple IIe RND(−4) cycle failed this test; all the others passed.

The bit-gap test for uniformity is motivated by the use of so-called bit-meddling random-number generators. These generators are based on comparisons and rearrangements of bits. The resulting number is the random draw. The bit-gap test is based on the number of bits that come between the first bit (the most significant bit) of a draw and the next bit that equals it. Under the uniformity assumption, the gaps are distributed geometrically with parameter .5 (i.e., the probability of a zero-length gap is .5).

The test is performed by making a large number of draws, tallying the gap size for each draw, and then testing the resulting data for its conformity to the geometric distribution. The random-number generator of the IBM PC extended BASIC language failed this test, as did the RND(−4) cycle of the Apple IIe generator, while all other generators passed the test.

Another crucial characteristic that a random-number generator must have is apparent statistical independence of successive draws. Because draws from the generator are exactly determined by preceding draws, the effectiveness of this procedure in simulating independence is of considerable concern. Two tests that measure this independence include the two-way association and the three-way association tests. The two-way association test was used to examine the assumption of independent draws. It is similar to the categorical-uniformity test in that the unit interval was divided into equal-size categories (10 for this test). Draws from the generator then were made two at a time. The categorical value of each variate was computed, and counts were kept of occurrences of each ordered pair of categories. These observed counts were compared with counts expected on the basis of the assumption of independent draws. The RND(−2) and RND(−4) cycles of the Applesoft BASIC generator were the only failures on this test.

The three-way association test is the same as the two-way association test, except that three successive draws are taken and tallied instead of two. This test is used because many random-number generators can be explicitly arranged so as to minimize first-order correlation. This selection could cause higher-order associations to be worsened. All of the generators tested passed the three-way association test.

Operational Time

Since users of microcomputers for simulation work must be concerned about the

continued

Table 1: *Run time in seconds for a program that executes* X=RND(1) *10,000 times.*

Apple IIe	
CP/M BASIC	34
Applesoft BASIC	65
Integer BASIC	41
Apple III	182
AT&T PC 6300	12
IBM PC	36
HP 86	77
TRS-80 Model III	86
TI-99/4A	740
Macintosh	62

TABLE OF BENCHMARK RESULTS

This table shows the results of the processor/coprocessor speed tests using the April 1986 release of PC Magazine's 'PC Labs Benchmark Tests'. These are public domain programs, and are available on diskette from PC Magazine, or via the PC Magazine bulletin board. These results were obtained by us at PCSG, and are not yet official published PC Magazine figures.

The last line in the table, the Norton System Information Test, is not from PC Magazine, but is part of the popular 'Norton Utilities'. The version we used was 3.1, which is the latest version but may not give identical results to older versions.

	IBM PC	IBM AT	*BREAKTHRU 286*
Clock speed in MHz (IBM PC is 4.77)	4.77	6	8
Empty Loop	1	1.99	3.34
Integer add from memory	1	3.35	4.41
Integer multiply from memory	1	6.06	6.55
Floating point without coprocessor	1	3.33	4.42
Floating point w/8MHz coprocessor	n/a	n/a	1.82
Prime number test	1	1.95	2.85
Lotus 123 macro (640K)	1	2.64	3.69
Lotus 123 macro (256K)	1	1.77	3.54
Norton System Information Test	1	5.73	7.34

In every case but clock speed the numbers indicate how many times faster a test is performed than on a regular IBM PC.

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Few spreadsheet cells can contain random numbers.

time required to complete projects, the speeds of the various random-number generators were evaluated by making 10,000 assignments of a random number to the value of a variable (table 1). These results show that the Apple III and TRS-80 Model III are somewhat slower than most of the other generators, while the TI-99/4A is very slow. The AT&T PC 6300 and the IBM PC AT, in contrast, are very fast. These conclusions are reinforced by measuring the time required to make one iteration of each of the statistical tests that were run. The two-way test of serial association was the fastest test. This test could be run once every 6 seconds using the IBM PC AT, but only once every 230 seconds on the TI-99/4A. The three-way test of serial association was the slowest test, taking 58 seconds using the IBM PC AT. One run of this test took 660 seconds on the TRS-80 Model III, 1020 seconds on the Apple III, and 2640 seconds on the TI-99/4A. The TI-99/4A is so slow that it is difficult to recommend its use for simulation work.

Macintosh

After we conducted our original survey, we tested the Apple Macintosh using the Microsoft BASIC interpreter.

Tests of the Macintosh were unable to determine the length of the cycle of the random-number generator, although we know that its length is more than one-half million. It is a good guess that since Microsoft BASIC performs all arithmetic in double precision (14 significant digits), then the cycle of the random-number generator may well be very long. The cycle of random numbers that is produced did not have a "leading tail," such as in Applesoft BASIC, and there were no problems or idiosyncrasies observed with seeding the generator. Furthermore, the generator on the Macintosh passed all five of the statistical tests. One surprising result from using this generator was that it was not faster than that of the Apple IIe. This was surprising since the Macintosh with the 68000 microprocessor was considered to be two to five times faster than the IBM PC with the 8088 microprocessor. There is no sure explanation of these slower than anticipated times, but it is possible that the design of the Microsoft interpreter has not taken advantage of the speed of the 68000 microprocessor. It will be of interest to collect results for version 2.1 of Microsoft BASIC, which contains both a decimal version and a binary version.

Lotus 1-2-3 and Symphony

We have recently been examining the popular software packages Lotus 1-2-3 and Symphony. Experience with spreadsheets indicated that many simulation projects could be conveniently structured using this kind of application software. Unfortunately, popular spreadsheets such as VisiCalc and Multiplan do not provide an intrinsic random-number function. Since Lotus 1-2-3 and Symphony have become top-selling software packages and have expanded features including an intrinsic random-number function, we are studying these random generators and their possible use in simulation projects.

The Lotus 1-2-3 and Symphony random-number functions are called RAND (which does not have an argument). The random-number generator does not provide a seeding procedure. When the spreadsheet is initially loaded, the first random number generated is always the same. The seeding process is built in and the initial seed is fixed. Although the initial sequence of random numbers is fixed, the sequence will change with each recalculation performed by the spreadsheet. The new sequence of numbers is taken from the fixed sequence, starting at the point where the last sequence ended.

A serious limitation of the Lotus 1-2-3 and Symphony random-number generators is that even though the spreadsheet contains many rows and columns, only a few of these cells can contain random numbers. Using Lotus 1-2-3 on an IBM PC with 256K bytes, for example, no more than 5800 random numbers can be generated before memory is full. Using an IBM PC with 512K, no more than 15,400 random numbers can be generated. In a simulation project, many cells will contain values and formulas, and the size of the problem will be limited by memory, unless macros are written.

Using macros and recalculations allows the generation of an unlimited number of random numbers. This technique can be quite useful, but writing macros does require a higher level of programming skills than many users possess and eliminates the ease of use associated with spreadsheets.

Using the macro feature, the cycle length was tested and found to be greater than 1 million. The statistical tests used to evaluate random-number generators have now been completed, and the random-number generators of both Lotus 1-2-3 and Symphony passed all statistical tests.

Our experience in testing Lotus 1-2-3 and Symphony leads us to make the following observations:

- The use of macros and recalculations will allow the generation of a long sequence of random numbers.
- Some small simulation problems can be easily implemented on spreadsheets while most others may be extremely difficult.
- Simulation problems that use a large number of cells and many recalculations will be time-consuming.
- The programming skills that were required to implement the statistical tests using Lotus 1-2-3 and Symphony were possibly beyond those of average users. Furthermore, the tests were slow to run, even when using the IBM PC AT.
- Therefore, Lotus 1-2-3 and Symphony are fine for many things, but Monte Carlo simulation isn't one of them.

Summary

A number of random-number generators on microcomputers have been surveyed. Some of the random-number generators, particularly those of the Apple IIe, are flawed either for statistical reasons or because they have short cycles. The IBM PC is somewhat suspect, mainly because it has a cycle whose length is 65,536. A fully acceptable random-number generator should ideally have a cycle length in the millions. Some generators that can be supplied by users (see reference 6) have long cycles. Some random-number generators have acceptable cycles and statistical properties but are very slow (e.g., the TRS-80 Model III). The IBM PC has a flaw in the procedure for user seeding of the random-number generator that can lead to the use of equivalent seeds. ■

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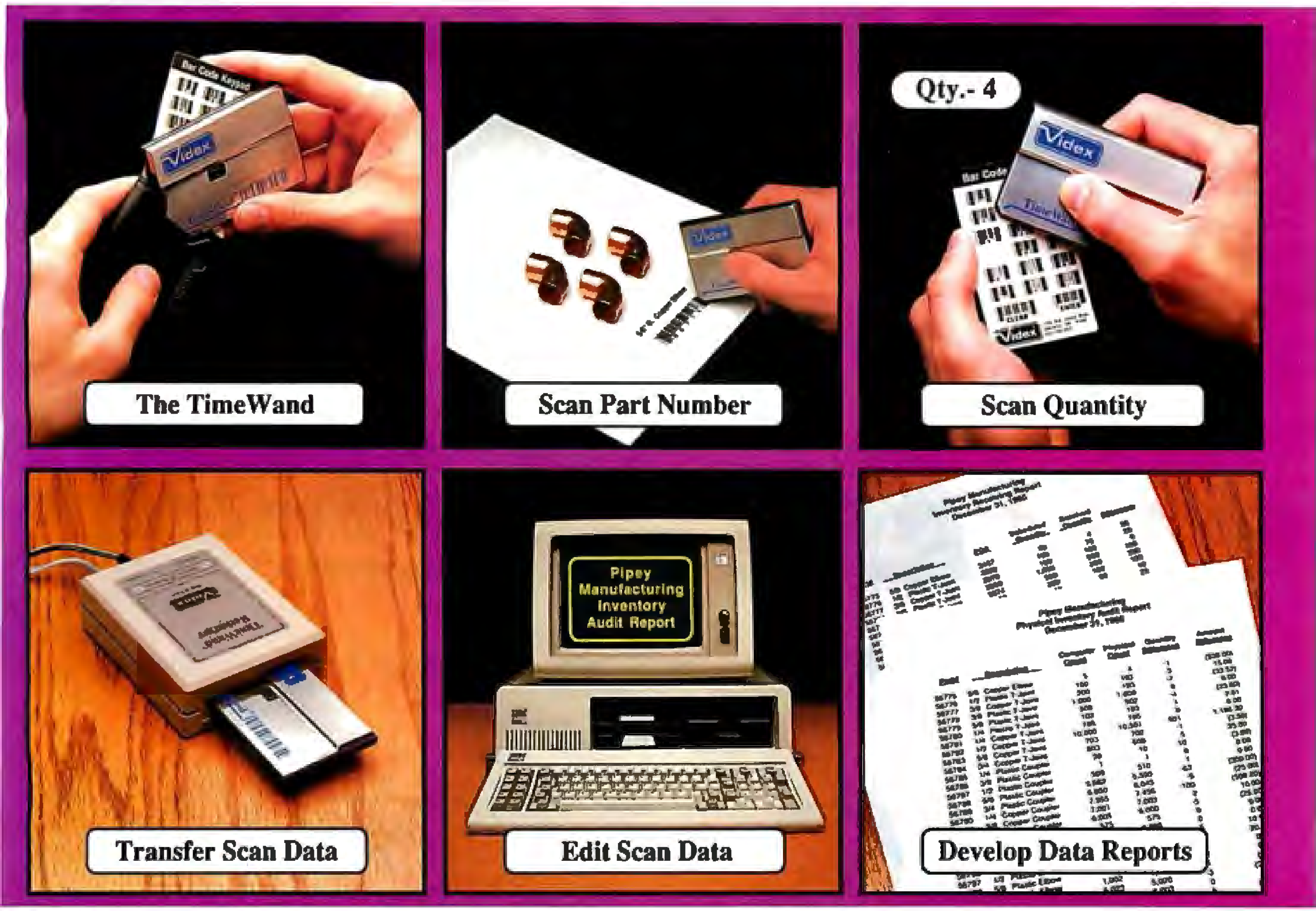

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Wilfred J. Hansen

Data Structures in a Bit-Mapped Text Editor

How Carnegie-Mellon University displays text on the IBM RT PC

In a bit-mapped graphics system like IBM's RT PC, text can be much more than a stream of ASCII characters. It can include, for example, differences in font, face code, size, justification, indentation, and subscripts or superscripts. However, these additions complicate how a character gets to the screen after you type it. In a less sophisticated system, the display device simply echoes keyboard input, but a modern workstation involves considerable software to store and display special text.

Recently, Carnegie-Mellon University took on the challenge of displaying text on advanced bit-mapped workstations for its Andrew system. Andrew is the software produced by the Information Technology Center, a joint project of IBM and Carnegie-Mellon. This software features a distributed file system designed so that anyone with an account can sit down at any of 5000 workstations to work with his or her files or communicate with other users.

The Andrew user-interface software includes a window manager, a subroutine package for dealing with text, an editor and a mail system that use the text package, and many other facilities.

Andrew is targeted to personal workstations that have a hard disk with 20 or more megabytes, at least 2 megabytes of RAM, a virtual memory management system, a speed of at least 1 million instructions per second, a network connection, a mouse, and a bit-mapped display with about 1 million pixels. For this, the IBM RT PC does nicely. The bit-mapped display is implemented with 1 bit of memory for each pixel on the screen. To draw an image, bits in the memory are turned to 1 or 0 to cause the screen to be black or white. To draw a character, the IBM RT PC copies a rectangular array of bits from a font file for each character. Having multiple font families, face codes, and sizes means having multiple font files, one for each combination. During its development, the Andrew system has had over 1000 different font files, although now that number has been reduced to 84.

continued

Wilfred J. Hansen is a system designer at Carnegie-Mellon's Information Technology Center, where he has worked on the Edittext text editor described here and its successor. His Ph.D. thesis project with Stanford University was the first hierarchical syntax-driven editor, and he has coauthored two texts with E. M. Reingold: Data Structures *(1981) and* Data Structures in Pascal *(1986), both published by Little, Brown. He can be reached at Carnegie-Mellon University, Information Technology Center, 4910 Forbes Ave., Pittsburgh, PA 15213.*

ILLUSTRATION BY RICHARD ALOISIO

The methods used by the Andrew system to store and display text make an interesting example of putting the IBM RT PC's power to work. Much of the software described below was originally written by James Gosling, who based it on his version of the EMACS editor. However, I have taken liberties with the names of routines and simplified many of the details, so they differ somewhat from the actual implementation. Moreover, an improved Andrew formatting system is being built, and it differs in many ways from what I describe here.

Documents

Documents are the heart of the Andrew text management system. A document is a stream of text that can be any size and can be changed dynamically. Documents are displayed for editing by the text editor, the shell command interpreter, the mail display system, and many other applications. Even the prompt line is a document, so a user can edit a search string with all normal editing commands. One application, the CMU-tutor lesson-writing system, even uses a (nondisplayed) document to store the results of compiling its lesson.

Conceptually, the program refers to the document as a stream of characters, with the first document numbered as 0 (figure 1). A program must first declare a variable to refer to a document:

```
struct document *doc;
```

This statement declares doc to be a pointer to a control block for a document; one element, length, is the number of characters in the document.

There are four principal operations on documents. First, NewDocument(initiallength) returns a pointer to a control block for a newly created document with capacity for initiallength characters. The document can get bigger than initiallength, so the exact value is not particularly important. Next, CharAt(doc, position) returns the character presently at location position in document doc. The operation will return nonsense if position is negative or as large or larger than the number of characters in the document. If doc has the contents shown in figure 2, CharAt(doc, 1) returns the value h. (For performance, CharAt is implemented as a macro in C.) InsertString(doc, position, string, length) inserts length characters from string into document doc. The insertion is such that the first inserted character will wind up in location position. The call InsertString(doc, 9, "talking," 8) will convert figure 1 to discuss a "talking raven." Finally, the call DeleteChars(doc, position, length) deletes length characters from doc, beginning with the character at location position. The call DeleteChars(doc, 22, 8) would result in "Why is a raven like a desk?"

With just these routines, you can implement all the operations on documents that are usually available in text editors. For example, consider the global replace operation. The system prompts the user to provide an old string and a new one. Then the editor replaces every instance of the old string in the text with the new one.

First, the find routine (listing 1) finds an instance of a string in a document and returns its location. Note that the outer while loop terminates when the length remaining in the document is shorter than the string str. The inner while loop terminates either when it finds the string, when i>=len, or when the ith character of the string does not equal the (pos+i)th character of the document.

Given the routine find, we can write the global replace algorithm (listing 2). In practice, the command processor calls it after the user supplies the old and new strings.

The document itself is implemented by brute force. The struct document control block points to a single array of characters large enough to store the document's text. As you can probably imagine, there are two problems with this scheme. The first is that each insertion might entail moving the rest of the document for each character inserted. However, leaving a gap in the middle of the text array at the location of

continued

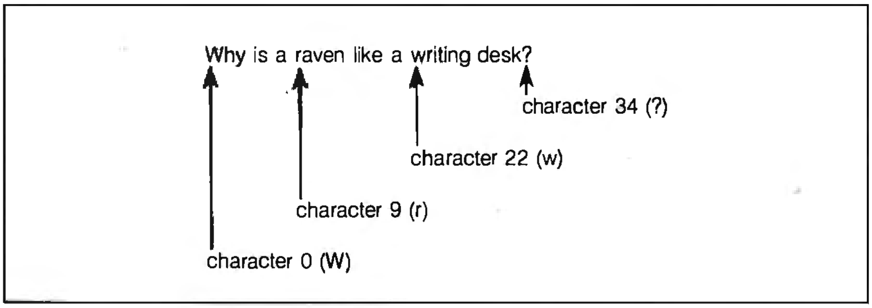

Figure 1: *An Andrew document 35 characters long.*

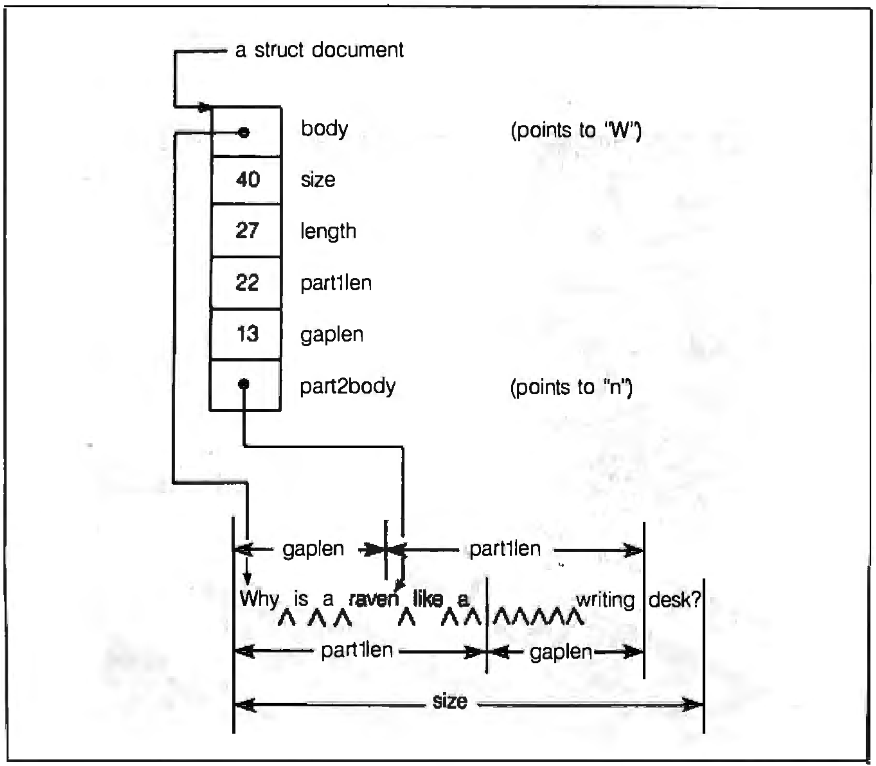

Figure 2: *The document data structure. The* body *field of the* struct document *points to a single array of characters containing the text, which is generally in two pieces with a gap between. This example shows the situation after deleting "writing" from figure 1. The address* part2body *is such that if* i>part1len, *the* ith *character is at* part2body[i].

the most recent insertion or deletion avoids that problem. If you insert a character in the first paragraph and then move to the last paragraph and make an insertion there, the system relocates the gap by moving all intervening characters, filling the old gap and leaving a new one. However, after too many insertions, you reach the second problem: The document text exceeds the array size. But some documents, by their nature, will never grow large. To adjust the size of the text array to accommodate both small stable documents and large growing documents, Andrew again uses a brute-force solution. When an insertion would make the text too large, a new array 50 percent larger than the old is allocated and the existing text is copied to it.

The solutions to both problems potentially require copying large portions of a document. After two years of experience with the system, however, I have never noticed a delay for copying the text. After all, a typical document is less than 100,000 characters, and a typical copy loop has only about six instructions. At 1 MIPS, the entire copy takes no more than 0.15 second when moving four characters per cycle. Most documents are shorter, so the time to copy the text is insignificant; just to paint a full screen of text takes longer.

The complete Andrew document data structure is shown in figure 2. With this structure, InsertString and DeleteChars are written in terms of two subroutines. GapTo(doc, position) moves the gap so it occurs just before the character at the given position. Then a deletion can be made by decreasing the size of the document and increasing the value that shows where the text after the gap begins. (The initial part of the text after the gap is thus deleted.) For insertions, the routine RoomFor(doc, size) is also used. It ensures that the gap is big enough for an insertion of size characters.

Some editors use an alternative data structure with a linked list of control blocks, one for each line. It is undeniable that such a structure can be much faster for insertion and deletion of characters; a copy never takes anywhere near as long as 0.15 second. But other delays are encountered, especially in a paging environment. Not only does the data structure take considerably more space—sometimes twice as much—but the control blocks and text lines can become scattered over numerous virtual memory pages. When that happens, a single screen repaint might require touching twice as many pages as there are lines on the screen. If they cannot all fit in memory, lengthy paging delays occur. The Andrew data structure, however, minimizes paging.

Although it is a bit of C arcanum, here is the full declaration of CharAt:

```
/* CharAt(d,n) accesses character n
   of document d.
   d and n must be side-effect-free. */
#define CharAt(d,n)
            ((n)<(d)->part1len \
```

Listing 1: *Finding a string in a document.*

```
/* find - search document doc forward from location pos for string str.
        Return the location of str or -1 if it's not there */
  int
find(doc, pos, str)
  struct document  *doc;      /* document to search */
  int pos;                    /* where to start looking */
  char *str;                  /* what to look for */
{
  int len, i;
  len = strlen(str);          /* compute length of string */
  while (pos+len <= doc->length) {
    /* check to see if str is in document starting at pos */
    i = 0;
    while ( i<len && str[ i ] == CharAt(doc, pos+i))
      /* the first i+1 characters of str match the
         characters in the document at positions
         pos, pos+1, pos+2, . . ., pos+i */
      i = i + 1;
    if ( i == len)              /* the entire string matches */
      return (pos);
    pos = pos + 1;              /* no match at pos, go on to next */
  }
  return (-1);                  /* no match at all, report failure */
}
```

Listing 2: *The global replace operation.*

```
/* subst - Replace every occurrence of string old in doc
           with string new */
subst(doc, old, new)
  struct document  *doc;      /* where to do the global replace */
  char *old;                  /* the string to be replaced */
  char *new;                  /* the string to replace it with */
{
  int pos, oldlen, newlen;    /* declare local variables */
  oldlen = strlen(old);       /* compute length of strings */
  newlen = strlen(new);
  pos = find(doc, old, 0);    /* find first instance of old */
  while (pos >= 0) {
    /* there is an instance, replace it */
    DeleteChars(doc, pos, oldlen);
    InsertString(doc, pos, new, newlen);
    pos = find(doc, old, pos+newlen);   /* find next instance */
  }
}
```

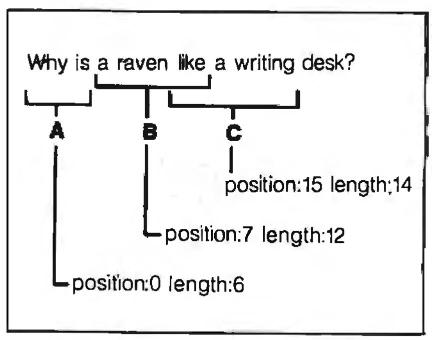

Figure 3: *Three markers on a document. Marker A refers to "Why is," B refers to "a raven like," and C refers to "like a writing." Note that markers can refer to overlapping text.*

```
? ((unsigned char *)
    (d)->body)[n] \
: ((unsigned char *)
    (d)->part2body)[n])
```

The test of n<d->part1len determines whether the desired character is before the gap. If so, the second line accesses it by subscripting directly into d->body, which is the text area; if it is not, the third line subscripts into an artificial array d->part2body, which begins d->part1len characters before the first character after the gap.

Marker Magic

As you check the code above, you will find nothing that updates the screen. This is done with the magic of markers. A marker is a data structure that refers to a portion of a document's text that starts at some character and extends for some length. Consider figure 3, which shows three markers attached to my document of 35 characters.

Marker magic occurs because markers are updated two ways by InsertString and DeleteChars. These routines adjust marker limits so they always refer to the same part of the text. If you insert the string talking in figure 3 at position 9, just before the r, the system increments the position value of marker C by eight, increases the length value of marker B by eight, and leaves marker A unchanged. While adjusting limits, the system sets a changed flag in a marker if the text it refers to is modified. For the insertion of talking, the system sets the flag only for marker B. (The text referred to by C has moved but not changed.) Once the flag has been set, it remains set until some routine outside the document package turns it off. Usually this is a routine associated with the one that created the marker in the first place.

Now you can deduce the fields of a marker control block. Each struct document has a pointer to the list of markers associated with the document, and each marker has a pointer, doc, to its document. The extent of the text referred to is given by position and length. If the referenced text is changed, the system sets the changed flag. Finally, the next and prev fields connect the markers together in a doubly linked list.

The routines to update markers are straightforward except for one decision: If an insertion is made at either end of the text and referred to by a marker, is the length field of the marker made bigger? In the Andrew system, the marker is made longer if the position of the insertion is a character that is referred to by the marker. Thus, the length of a marker m will increase only if

```
m->position
  <= InsertionPosition
    <m->position+m->length
```

This rule will never extend the length of a marker that has length zero.

Markers are essential for updating text displays. The display management portion of the editor keeps a marker for each line displayed on the screen. The line is redisplayed on the screen only if the text it refers to has changed. To make this possible, the editor is carefully partitioned between the routines that respond to user inputs and those that update the display.

At the highest level is a main loop that determines whether there is user input and processes it. The loop defers calling the screen-update routine until no input is pending. This main loop uses a data structure for each portion of the screen. The data structure representing the screen image for a document is the view, a structure that keeps all the information needed to format the document for display. Among the fields of the view are the following:

continued

Listing 3: *Updating a view. The work of understanding the style information is hidden within* DetermineSpacing *and* SendTextToDisplay.

```
/* Phase 1: Find lines that need to change in this view
              due to changes in doc. */
{
  int NextPosition;           /* position of start of next line */
  int y;      /* y coordinate of top of next line to display */
  int i;      /* i sequences through the lines displayed */
  NextPosition = view->ViewTop->position;
  y = 0;
  i = 0;
  while (y < view->height && NextPosition < doc->length {
    /* decide which lines need to be redisplayed and
       choose space width for justification */
    struct LineImage *ThisLine;       /* address of the ith line */
      /* ("ThisLine" is used for lack of Pascal's with statement) */
    ThisLine = &(view->Line[ i ]);
    if (NextPosition != ThisLine->m->position
                  || y != ThisLine->y) {
      ThisLine->m->changed = True;
      ThisLine->m->position = NextPosition;
      ThisLine->y = y;
    }
    if (ThisLine->m-> changed)
      NextPosition = DetermineSpacing(ThisLine);
    y = y + ThisLine->height;
    i = i + 1;
  }
  view->NumberOfScreenLines = i;
}
/* Phase 2: Erase text that is to be redrawn. */
{
  int i, j;
  For each group of consecutive changed lines {
    set i to the first in the group and j to the last;
    erase the rectangle that has an upper left corner of
        (view->left, view->Line[ i ]->y)
      and a lower right of (view->right,
        view->Line[ j ]->y + view->Line[ j ]->height - 1);
  }
}
/* Phase 3: Send new text to the display. */
{
  int i;     /* cycle through the lines */
  i = 0;
  while (i < view->NumberOfScreenLines) {
    /* now redisplay the changed lines */
    struct LineImage *ThisLine;       /* address of ith line */
    ThisLine = &(view->Line[ i ]);
    if (ThisLine->m->changed) {
      SendTextToDisplay(ThisLine);
      ThisLine->m->changed = False;
    }
    i = i+1;
  }
}
```

ViewTop, a marker whose position indicates the first character to be displayed on the top line of the image for this document;

Line, an array of LineImage data structures, one for each line to be displayed;

The LineImage for each line includes m, a marker for the text displayed on the line; y, the screen y coordinate of the top of the line; and height, the height of the line;

continued

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NumberOfScreenLines, the number of lines displayed for the view; and

left, top, width, and height, four fields that describe the subrectangle of the window devoted to the view. Left and top are the *x* and *y* coordinates of the upper left corner; width and height give the size of the window.

The coordinate system for Andrew windows begins with (0,0) in the upper left corner and extends with increasing *x* to the right and increasing *y* downward. Distances are measured in points, the printer's term for a unit about 1/72 inch. However, this is a misnomer because the implementation is really in terms of pixels on the screen; this works because many workstations have about 72 pixels to the inch. On workstations such as the RT PC that have more pixels to the inch, the image is smaller than it would be if set in true printer's points.

The marker for the ith line is view–>Line[i]–>m. Curiously, it must refer to text beyond the end of the ith line because insertion of a space in the first word of the (i+1)st line might require the ith line to be redrawn with a short new word at its end. Thus, the marker must include all the text on the line and the first word of the next line.

Using the markers for each line, the update routine reconciles the screen image with the new contents of the document in three phases (listing 3). The first phase determines which text lines have to be redrawn based on the changed flags in the Line array. In this process, the system calls a subroutine, DetermineSpacing, that marches across the line interpreting the formatting information so it can find the height and width of each character and the widths for spaces to perform justification. All this information is preserved in the LineImage structure for the line, and the value returned by DetermineSpacing is the position in the document of the first character for the next line. Note that an unchanged line might have to be redrawn if its *y* coordinate changes or if the previous line ends at a different position in the text.

The second phase of the update routine erases the old text from each portion of the display that is to be redrawn. The third phase then plots each line that has been identified as needing to be redrawn. The heart of this phase is a call on SendTextToDisplay, which uses the information recorded in the LineImage by DetermineSpacing and actually sends the characters to the screen.

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Programmable Hardware

PROGRAMMABLE HARDWARE seems almost a contradiction in terms. Traditionally, logic designers used fixed, ready-made components. Often they could only approximate designs with these prefabricated units because the exact functions needed couldn't be found in an off-the-shelf part. These chips, since they were general-purpose, took up a lot of board space.

The distinction between software and hardware began to blur with the advent of generic logic chips that could be programmed to meet a designer's exact specification. These chips had the added advantage of reducing chip count, increasing design security, and decreasing development time.

Programmable hardware devices range from full-custom chips to gate arrays and PLDs (programmable logic devices)—and they are everywhere: The Atari ST has a custom memory controller and glue chip. The Amiga's custom graphics chip and its animation chip are responsible for that machine's stunning graphics capabilities. Six PLDs in the Apple Macintosh enabled its designers to use only two circuit boards for the entire computer. While many articles in BYTE have discussed products that use programmable hardware, none has explained the theory behind the operation of these devices.

Most of the theme articles to follow will concentrate on user-programmable logic devices, since the cost of working with these devices is within the realm of possibility for our readers. However, to position PLDs in the scheme of programmable devices, Phil Robinson gives an overview of the field of programmable hardware. One of the problems with discussing programmable hardware is that there are many new acronyms and much new terminology. Vincent Coli lays the groundwork for understanding the terminology and architecture of PLDs. In a sidebar to Vincent Coli's article, John Birkner, the coinventor of the PAL device, gives a brief history of the events that led to the development of the PAL.

For those people who are not familiar with PALs but would like to know how to go about using them, Bob Freedman gives some practical advice on choosing the right PAL for a design and getting it programmed. Then, as an added bonus, he has put together a PAL programmer construction article. This programmer can handle a subset of the most popular PALs.

In August and September 1985, and July and August 1986, BYTE featured the Definicon DSI-032 and DSI-020 coprocessor boards. These boards, which add the power of a 32-bit microprocessor to an IBM PC, were loaded with PALs. Trevor Marshall gives some examples of how PALs helped in integrating the diverse components of these coprocessor boards. He also relates some of his experience gained designing with PALs.

Finally, another type of programmable hardware is a microcoded CPU. Microcoding is used in popular microprocessors—such as the 68000 and 80286—and aids in debugging or enhancing the instruction set. Phil Koopman explains the differences between microcoding and hard-wiring the instruction sets of microprocessors and gives the advantages and disadvantages of each method.

—Eva White, Technical Editor

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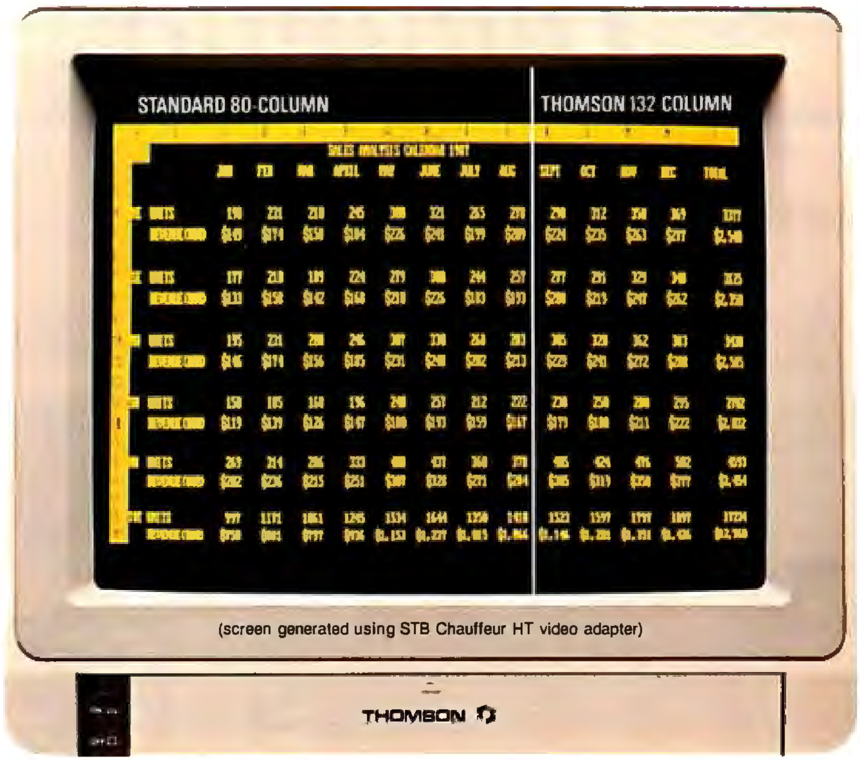

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Overview of Programmable Hardware

A look at the range of options available to the logic designer from full-custom chips to user-programmable logic devices

Phillip Robinson

FIVE YEARS AGO, if you opened up a microcomputer to identify the chips, you probably would have found a microprocessor, several ROMs, RAM chips in sets of eight, a floppy disk controller chip, and scores of smaller logic chips. These logic chips are often called "glue" because they electrically connect all the major chips.

If you open a microcomputer now, even though that computer is far more powerful than its ancestor, you'll find fewer chips. You'll still see the microprocessor, RAM, ROM, and peripheral controllers along with a few glue chips, but most of the glue components have been replaced by a few much larger chips. Those replacements are ASICs (application-specific integrated circuits).

ASICs

For all the same reasons that integrated circuits originally emerged—increased reliability, simplification of system design, reduced power use, reduced board-area requirements, improved performance because of increased signal speed—ASICs are taking over from SSI and many MSI off-the-shelf chips. Instead of using a dozen to a hundred standard-function integrated circuits, designers are now using a handful of chips designed specifically for a particular system or function. An additional advantage of this design strategy is that the presence of ASICs makes a board or computer much harder to copy.

The rush to customize has taken the IC industry by storm. ASIC sales are growing twice as fast as general chip sales, and as many as 50 percent of all chips sold in 1990 might be application-specific.

CAE

But how will all these ICs be designed, given a distinct shortage of experienced chip designers? It's one thing to suggest that everyone could have a fast, cheap, small system by simply building it around chips dedicated to one purpose. It's quite another to get such chips in hand.

That dilemma has two solutions. The first is CAE. The ASIC boom wouldn't have occurred at all without the advances in workstation hardware and software. CAE workstations let engineers diagram, simulate, and modify a chip entirely through software. Such tools can then directly output a tape that tells chip-manufacturing equipment how to make the masks for chip fabrication. (The mask is the stencil used to dictate where chip wires or devices will be placed.)

The other answer is programmable logic. Many semiconductor firms are now offering chips that the system designer can customize. Some can even be programmed, erased, and reprogrammed, all by the system designer or end user. The history of these programmable parts mirrors the previous development of ROMs.

ROMs

ROMs are not designed entirely anew for every system. The standard, permanent ROM chip is called a masked ROM because most of its layers are always the same, with differences in only the final metal mask. In essence, a ROM is an array of possible storage cells, and the final layer of metal determines which cells hold 0s and which cells hold 1s by the array interconnections.

ROMs are useful in many systems, including those with or without microprocessors. Certainly a ROM is a practical vehicle to store the boot code for a microcomputer, but you can also use it as a translation table, a character generator, or some other warehouse of data. Therefore, a ROM can function as a logic device, behaving simply as a chip that produces a certain output signal when supplied with a certain set of input signals.

Masked ROMs can cram a lot of data onto a relatively small chip area. Unfortunately, because the final metal layer is deposited at the chip factory, any repair of a masked ROM requires a long turnaround time. The error must be identified, the chip firm notified, the mask altered, and new chips fabricated.

Masked ROMs are typically manufactured in high volume to minimize the costs, so any detected bug means lots of worthless parts. The same costs are incurred whenever a masked ROM needs modification because the system or the program needs changing.

PROMs

The next answer the semiconductor industry had was the PROM, which is

continued

Phillip Robinson (2874 South Palisades, Santa Cruz, CA 95062) is a contributing editor for BYTE.

Removing a soldered chip almost guarantees it will be damaged.

essentially an array of fuses. System designers would buy a batch of standard PROMs off the shelf and then use a special programmer machine to implant their programs or data into the PROM.

Advanced programming tools only ask what data the designer wants to use. The programming machine blows or burns tiny fuses on the chip. This chip offers the great advantage of in-house modification. If the PROM is wrong in some way, a single engineer can burn a new one in a relatively short time. The PROM was the first programmable chip of this sort.

But each burnt PROM was permanently used. Any modification meant throwing the chip away. That wasn't acceptable to everyone. "Programmable is nice, reprogrammable is better" was the designers' creed.

EPROMs

EPROMs come as standard unprogrammed parts from the chip factory, just as PROMs do. EPROMs are easily identified by the clear window that covers the chip and admits ultraviolet light. But they don't depend on a permanent, fusible link to store information. Instead, they store charges on capacitors in an array.

The capacitors determine the on/off state of transistors, which then determine the presence of 1s or 0s in the array. Bathing such a chip in the correct wavelength and intensity of ultraviolet radiation for about 20 minutes lets the charge leak off the storage capacitors, thus purging the data. Once an EPROM has been erased, it can be programmed in much the same way as a PROM. A programming machine is told what data to implant, and it then applies the correct voltage for the proper time to the appropriate addresses.

EEPROMs

Reprogramming an EPROM still requires removing the chip from the system, placing it in an ultraviolet eraser, programming it in an EPROM burner, and returning the chip to the system.

Every time a chip is put into or removed from a socket, there are the dangers of static damage, leg bending, and package cracking. Military applications are even more problematic: Parts are soldered instead of socketed for reliability in the field. Removing a soldered chip almost guarantees that the chip will be damaged.

EEPROM chips avoid many of the problems of EPROMs. These chips are similar to EPROMs except that they don't have the clear window because they don't require ultraviolet light for erasure. Special voltages applied for specific times can erase an EEPROM, and these voltages can often be applied from within the host system. In other words, an EEPROM is in some ways no longer a ROM at all; it is a "read mainly" (in a simple mode), "write sometimes" (in a more complex and slower mode) memory. This comes at the cost of less density: fewer memory cells per chip than on a standard ROM or PROM. But the electrical erasability does yield some tremendous benefits. Systems can be reprogrammed regularly without disturbing the chips. Some systems, such as postage meters, have even been designed for EEPROM reprogramming over the phone.

Logic

What does all this progress in memories offer the logic designer? It is rarely efficient to use memory as a logic replacement: The speed and sequential abilities of logic are hard to duplicate in memory.

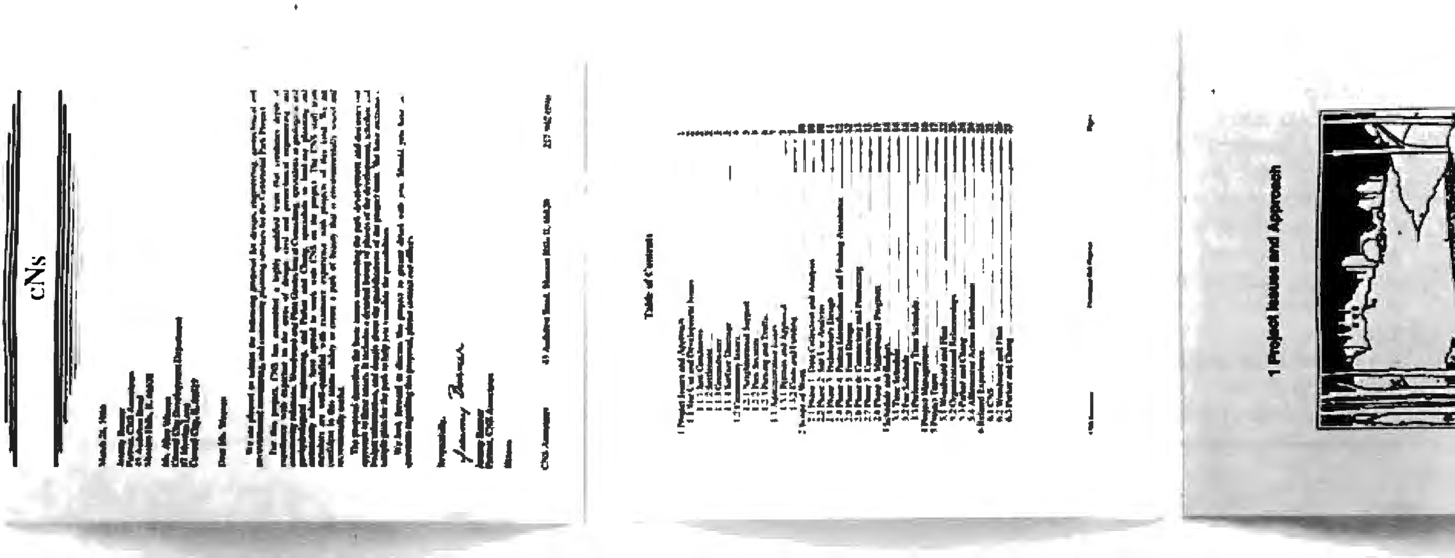
The fact is, logic devices are now following this same path of development. The same choice of dedicated versus programmable chip is now available to logic designers. The trade-offs are essentially the same.

I'll use the term "designed chips" to represent chips that have a permanent function once they leave the chip factory, even if the design was carried out elsewhere. I'll use the term "programmable" to refer to chips that can be implanted with a function either one or many times after they leave the chip factory. (The semiconductor industry has not yet settled on the names for these new devices.) Dedicated chips are cheaper in huge volume and offer higher performance, while programmable chips are cheaper to design and easier to modify (see table 1).

In the beginning, all chips were programmed or dedicated at the factory. The advent of inexpensive workstations, as well as CAD and CAE software on microcomputers, has meant that some chips could be designed at home or in the office and then fabricated in a factory.

Full Custom

The first design method is to fully customize a chip—that is, to design a chip



from scratch. One method is to employ hand or computer drafting tools and a knowledge of chip physics to draw the mask layers that determine a chip's function. This ranges from difficult to impossible. A single transistor drain out of place can make the entire chip little more than an expensive, exotically packaged resistor. Even experienced chip designers run into this kind of trouble.

All full-custom chips suffer from trouble in the testing department. Special test procedures and equipment must be designed in tandem with the chip to ensure that there is some way to verify chip performance. This can be the single biggest problem confronting a chip designer.

When an error is exposed, the designer must return to the masks, identify the flaw, redraw, convert the masks again into the proper format, and go back to the fabricator. Don't ignore this avenue merely because of the difficulties: A fully custom design can be fine-tuned to take up minimum chip area (which minimizes cost) and to perform at maximum speed. The MOSIS facility (BYTE West Coast, May 1985 BYTE) opens this process up even to interested parties who don't have any connection to a semiconductor firm.

Table 1: *Some comparisons of the logic chips described in this article.*

Factors	SSI/MSI	PLA	Chip type gate array	Standard cell	EPLD
Logic complexity (gates)	Low	Low (to 650)	High (to 50,000)	High (to 50,000)	Medium (to 2000)
Programmable (user-configurable)	No	Yes	No	No	Yes
In-circuit reprogrammable	No	No	No	No	Sometimes
Design time: schematic to prototype	Weeks	Days	Months	Months	Days
Design time: revision to prototype	Hours	Minutes	Months	Months	Seconds
Factory testability	100%	Statistical	Custom (100% of devices, only statistical of gates)	Custom	100%
Copyability	100%	Low	Low	Low	None

Silicon Compilers

Another path to the full-custom chip is the silicon compiler, which behaves in much the same way as a high-level-language compiler. It is a program that translates general statements of purpose into low-level descriptions of particular processes to achieve that purpose. The difference is that a silicon compiler produces a hardware description of a chip. The level of input language differs between various compilers, ranging from behavioral (which consists of statements about the chip's desired behavior) to structural (which specifies desired data-bus width, pin arrangements, ALU functions, etc.).

Silicon compilers are in their infancy, with the first ones appearing only in the last couple of years. Silicon Compilers Inc. was the first (and grabbed the generic name for its company tag) and has the best known product: Genesil. This compiler has already been responsible for products such as an Ethernet controller from Seeq Technology and the MicroVAX CPU from Digital Equipment Corporation. However, people are not flocking to silicon compilers as much as these firms would like. Apparently, old-time IC designers are reluctant to believe that a program can handle the art of chip design as well as they can. Some hand-optimization of the

continued

When you tackle a standard-cell design, you face the chip area armed with a software library of chip functions.

design, required after a silicon compiler completes its task, reinforces that idea.

The chip produced by a silicon compiler has several advantages: It doesn't require as much IC design experience as a full-custom chip, and it can be designed in a matter of weeks or months instead of years. The disadvantages are that it doesn't use the chip area as efficiently as a hand-designed chip would, and some functions that a designer might want aren't yet available in many silicon compilers.

Semicustom

If a chip designer is willing to go with semicustom devices, a plethora of possibilities exists. Probably the best known is the gate array.

Gate arrays are essentially a series of rows and columns of electronic gates—from 300 to 50,000 in number—surounded by a variety of I/O cells. These chips are called late-mask programmable chips because the semiconductor manufacturer processes the chips up to the last one or two metal layers, then offers the customer a software system to help design those final layers.

The customer uses the software to lay out the electronic functions, including the I/O interfaces, on the naked array. The software—which has a built-in repertoire of simple functions such as AND, OR, and NOT, as well as latches, buffers, and the like—finds the possible positions for these functions and attempts to route the necessary connections between them.

The final metal layers are physically placed on the chip at the IC factory, and the chip is plugged into the target system. Gate arrays offer the ability to fit lots of functions on a single chip and let the system designer avoid the actual transistor-to-transistor level of logic design. However, they do make the designer get down to the nitty-gritty of dealing with gates more than do standard-cell chips. And the wiring channels between functions often occupy as much as 30 percent to 50 percent of a gate ar ay, area that is unavailable for active elements. This reduces the gate count and increases the cost of the gate-array chips.

It typically takes two to four months from conception to prototype chip delivery and that long again to get the production chips. The process costs a lot up front—$20,000 or more—but the chips are cheap when made in volume. Any mistakes in the initial design quickly inflate cost and time estimates.

Standard Cells

When you tackle a standard-cell design, you face a blank page—the chip area—armed with a software library of chip functions. These functions are essentially imaginary small chips that you can lay out on the larger semicustom chip-to-be and then interface together using software. At this level, the system designer has to work only with blocks of logic instead of gates.

In addition, the cells of a standard-cell design are already tuned to high performance and minimum area (often taking up only one-third or one-sixth of what the same function designed from gates would take), so the entire chip might exhibit better characteristics than a gate-array design. Because each standard-cell chip must be fabricated from scratch once the design is complete—they are all mask-programmable as are silicon compiler chips and full-custom chips—gate arrays can often be completed about four weeks sooner than standard-cell chips.

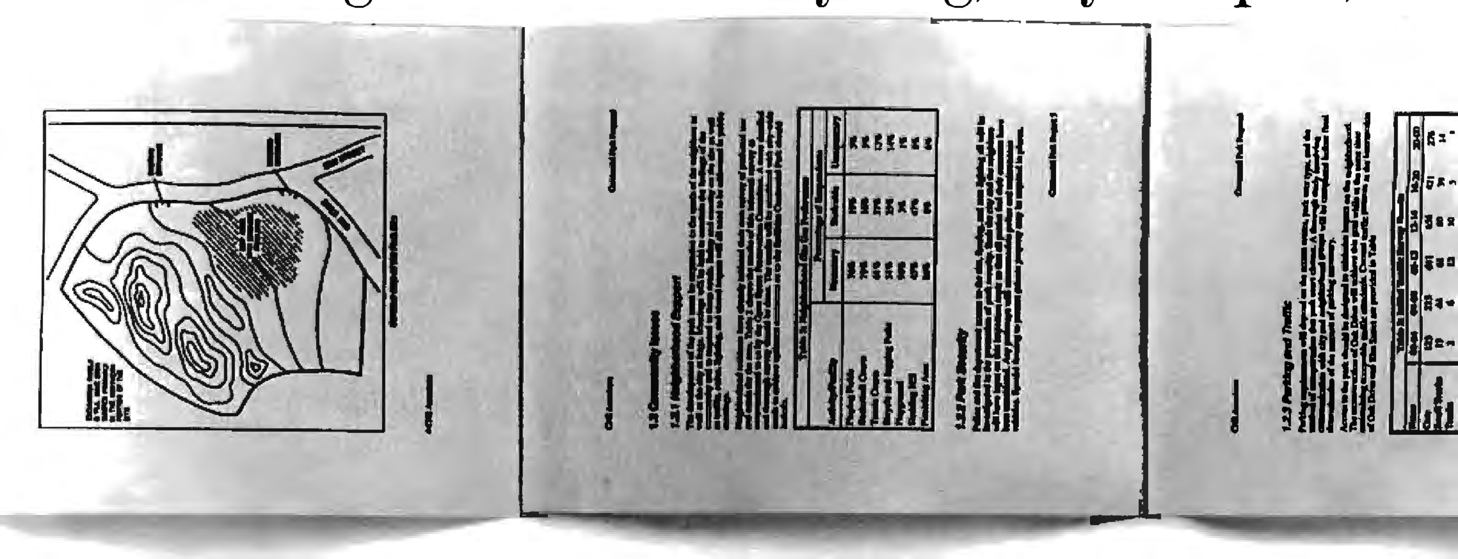
Standard-cell libraries include everything from simple AND gates to complete Z80 microprocessors. Some also include UV EPROM and EEPROM arrays. However, what they have is what you get. With a gate array, you can design anything you want up from the elemental gates. With a standard cell, you can connect only what is available.

Convergence of Technologies

The gate-array and standard-cell technologies continue to improve and, in some ways, to converge. Gate-array function libraries now sometimes offer CPUs, RAM, and other complex functions. Standard-cell libraries are incorporating gate-array cells and regions of random logic. Some libraries include analog functions. Still, standard-cell and silicon-compiler designs tend to take longer and cost more than gate arrays.

Microcode

The one other type of factory-programmable hardware is microcodable CPUs.



Microprocessors are often designed with a tiny processor at their heart that interprets internal machine language instructions called microcode and translates them into specific signals controlling the various registers and buses.

Microcode allows fixes to existing instructions or addition of new instructions without a major redesign of the chip logic. Some CPUs let the original equipment manufacturer write its own microcode program for this processor or sequencer.

Programmable Devices

System designers weren't content to stick with logic chips that left the factory in final form, just as they weren't content to stick with masked ROMs. The counterpart to PROMs, EPROMs, and EEPROMs are the programmable logic devices. This programmable hardware is also known as user-configurable integrated circuits.

These chips come in many forms and in both bipolar and CMOS technology. Some can be programmed only once, while others can be erased and reprogrammed. Those that require UV light for erasure are called EPLDs and those that are electrically erasable are called EEPLDs.

Programmable Logic Arrays

The history of programmable logic devices parallels the history of programmable ROMs. The first devices were one-time programmable logic arrays. A PLA is a chip with several gates on it that can be programmed in much the same way a PROM is programmed: Built-in fuses are blown by a special programming machine. The pattern of blown fuses leaves a particular web of logic on the chip.

These chips contain roughly 150 to 300 gates and can replace approximately three to six SSI and MSI TTL chips. Because they fit the functions into a single package, they save board space and power consumption and improve reliability. Like PROMs, they can be programmed fairly quickly and then plugged into a system.

If the PLA needs to be modified, it can be yanked from the board and replaced by a newly burned PLA. Because the chips are completely fabricated at the factory, their basic operation can be tested there. The actual logic implementation needs to be tested after the system designer has implanted it on the chip.

EPLDs

Altera introduced the first EPLD in 1984. The EP1800 is the most complex chip that the firm now offers. It contains about 2100 two-input gates and can replace 60 to 70 SSI, MSI, and custom logic chips. That density is available because the EPROM bit used in the chips as a switch is much smaller than the fusible link on PLAs. Altera refers to the part as a user-configurable gate array because of the density of the chip (i.e., the number of gates). The density puts it in the LSI arena. Intel's CMOS II E implementation ensures low power consumption. Altera and Intel are technology partners, and Intel operates as a second source for these EPLD parts. The chips are specified to run as fast as 25 megahertz. At 10 MHz, each one draws only 45 milliamperes. In the quiescent mode, it draws only 50 microwatts.

The EP1800 has 48 macrocells, each composed of EPROM transistors that configure its logic connections. Internally, a

If a PLA needs to be modified, it can be yanked from the board and replaced by a newly burned PLA.

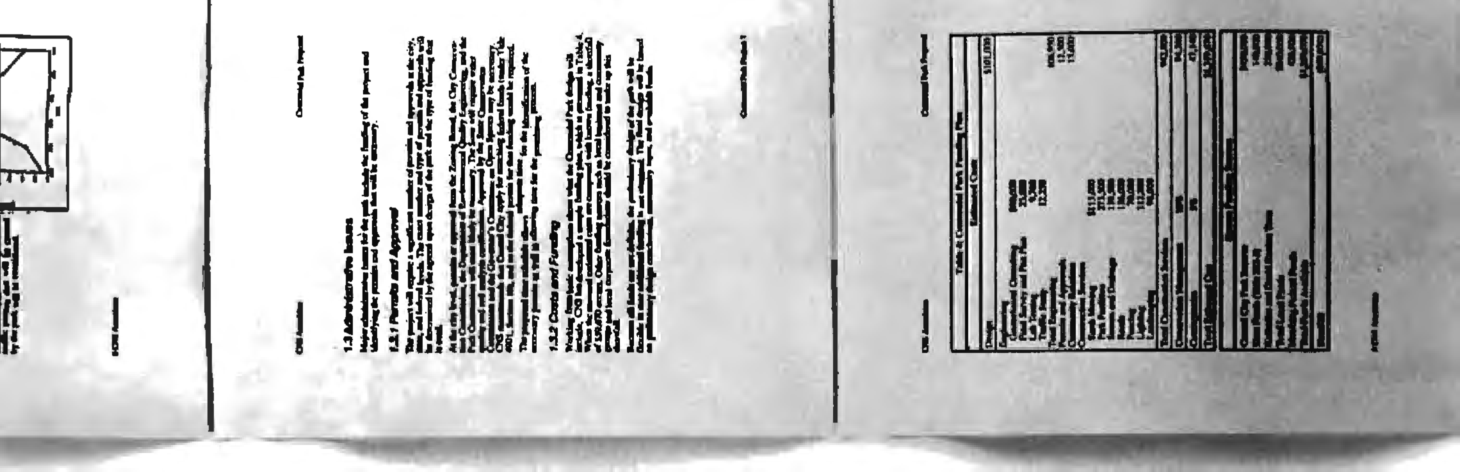
programmable-AND/fixed-OR PLA structure sets up a sum-of-products logic. Selected EPROM cells in the AND array dictate the final function. The I/O sections of the chip contain flip-flops for storage and EPROM bits for logic control, so they can operate as both combinatorial and sequential logic simultaneously.

The ability to work with both synchronous and asynchronous clocks is another advantage the EPLD has over the generic PLA. Because the chips aren't ruined by their first programming, they can be 100 percent tested by the manufacturer, an advantage sorely lacking in PLAs.

Although Altera does offer a one-time programmable version, the EPLD version is UV erasable and has the clear window, just as an EPROM does. The EPLD version is intended mainly for prototyping, and the one-time programmable version is for production runs.

Altera offers software to let you design the logic for your EPLD. The software lets you use a variety of design methods to enter your initial logic concept using a

continued



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CAD system, from P-CAD or Future Net to simple Boolean equations written with a text editor. These are translated into an Altera Design File, optimized, and finally output as a standard JEDEC file (an ASCII file containing information about the fuses to be blown) that will be used to program the EPLD.

Another software option also lets you simulate the performance of your device design. When the design is complete it can be transmitted to a programmer machine, which implants the design in the EPLD. The software is continually enhanced; one recent improvement is the addition of macrofunctions, familiar TTL functions that can be implemented by block. This is the same process that the gate-array and standard-cell folks pursue. In fact, it has the same effect of easing the design burden, or at least shifting that burden up the design ladder from basic logic to the system level. Although most gate-array and standard-cell design software is limited to workstations, Altera's EPLD software runs on the IBM PC and compatibles.

For those interested in the EPLD concept, Altera offers the EP1800-EVI evaluation chip. It contains 14 MSI TTL functions, and you can use it to ascertain the performance characteristics of the Altera chip family.

EEPLDs

The first electrically erasable PLDs required special electrical erasure conditions that wouldn't be available within most systems. These chips had to be removed from a system and reprogrammed in a special, outside tool.

Lattice Semiconductor has been producing two EEPLD chips, the GAL16V8 and the GAL20V8, that must be reprogrammed outside their system environment. The 16V8 is a 20-pin device that takes up to 16 inputs, runs them through an AND-OR-Invert array and produces up to 8 outputs. The 20V8 offers up to 20 inputs and 8 outputs in a 24-pin package. Asynchronous throughput can be as fast as 15 nanoseconds from input to output, and the chips are rated at a maximum of 90 mA power dissipation. Their output logic macrocells can be configured in synchronous or asynchronous mode, high or low polarity, and offer a tristate option.

Lattice has worked with Programmable Logic Technologies on its Logic Lab—a development tool for the Lattice EEPLDs. The Logic Lab attaches to an IBM PC or compatible through an RS-232C serial port and has two ZIF sockets for the programming of 20- or 24-pin EEPLDs. Along with the Logic Lab you get the software that can transform Boolean equations into fuse maps. Those maps are downloaded to a buffer that can implant the logic into the chip. Lattice has qualified the tool, though it hasn't officially endorsed it. The Logic Lab costs $479 and can program the 16V8, 20V8, ISPGAL, and 39V18 chips from Lattice. Production models have been shipping since the end of October.

International CMOS Technology is another firm in the EEPLD game. It has been sampling the PEEL18CV8 chip, a 20-pin device that can emulate the popular 20-pin programmable array logic devices.

(PEEL stands for programmable electrically erasable logic.) It is similar to the aforementioned Lattice chips and should be available in production in January or February. The PEEL22CV10 is a 24-pin PAL replacement.

A newer device from ICT is the 22CP210, a device with two EEPLD arrays on a single chip. It is similar to the Signetics 153 PLA and has a special metal mask option that lets it emulate the Signetics 173 PLA. And by late in the first quarter of 1987, the 22CX216 should be rolling out. That chip has 32 inputs, 2 arrays, and 16 outputs and will be able to emulate up to 100 different PAL devices.

ICT has developed its own programming tool that it is selling "at cost" to anyone interested in using its chips. The programmer is a plug-in board—with a ribbon cable extension—for IBM PCs and compatibles. The software that goes with it has the standard programming abilities as well as advanced features such as test vectors. It is available now and costs $795.

In-System EEPLDs

More closely related to the EEPROMs described earlier in this article are EEPLDs that are not only electrically erasable but can be erased and reprogrammed without removal from their electrical habitat.

In August of 1986, Lattice introduced the ISPGAL (in-system programmable) line of chips. The ISPGAL16Z8 sits in a 24-pin package and offers all the functions of the 16V8 chip described above. The 4 extra pins (beyond the 20 needed by a 16V8 device) are exclusively for programming, so there is no multiplexing or interference with other pins. As the name implies, the ISPGAL16Z8 can be reprogrammed right in the system.

The ISPGAL39V18 chip was scheduled for sampling in December of 1986. It is a 24-pin device with more inputs and outputs and new internal architecture. The 39V18 offers both programmable-AND and programmable-OR arrays on the chip along with 10 output macrocells.

RAM-based EEPLDs

Xilinx has taken another approach to in-system reprogrammability. The XC-2064 chip, introduced in November 1985, is a configurable logic-cell array that assumes its internal logical function by reading an internal static RAM upon the application of power. Change what is in that RAM and you have a new chip. Typically, systems take 12 milliseconds of power-up time to read the data into RAM from external EPROM, EEPROM, floppy disk, or some other nonvolatile source. If a battery backup circuit is included, the chip will retain its identity even when power is removed. You can also choose to specify that only some sections are automatically reset.

The XC-2064 is a CMOS chip that can run as fast as 20 or 33 MHz (there are two versions). It provides up to 2000 two-input gates (or 1000 to 1500 standard gate-array gates) and is in the same component density as the Altera chip. The gates are structured as 64 logic blocks in a gate-array-like architecture surrounded by 58 I/O pins that allow any mix of input, output, and bidirectional signals.

Each logic block has four logic inputs, a clock input, a combinatorial logic section, two logic outputs, and a programmable storage element. The inputs drive the combinatorial logic and thereby provide logic functions ranging from a simple NAND gate to a 3-of-4 majority decoder. The combinatorial section also accepts and generates positive-true and negative-true logic, eliminating the need for inverters.

Asynchronous and synchronous logic can be combined in different logic blocks. You can select whether to use TTL or HCMOS input thresholds on the I/O blocks. An on-chip oscillator and clock buffers allow flexible internal and external clocking.

Xilinx offers its customers the XACT development system. This design, verification, and debug system uses the IBM PC XT or PC AT as a host and allows the design of the EEPLD logic from schematic capture to simulation and timing analysis. The package also features a macro library and in-circuit emulation. A subset of the software is available as a Development System Evaluation Kit (EK-01) so you can experiment with the logic possibilities of the XC-2064 chip.

Conclusions

EPROMs have taken over from masked ROMs in all but the high-volume applications. Now EEPROMs are grabbing part of the EPROM market. Perhaps EPLDs and then EEPLDs will follow the same path and grab the logic market from PLAs and their kin. Young firms have grabbed the first toeholds in this market, but more established firms such as Seeq Technology, which are leading the EEPROM business, are considering entering the EEPLD business. They already have the basic cell technology; they only need to be convinced of the importance of the market and the role they can play. ■

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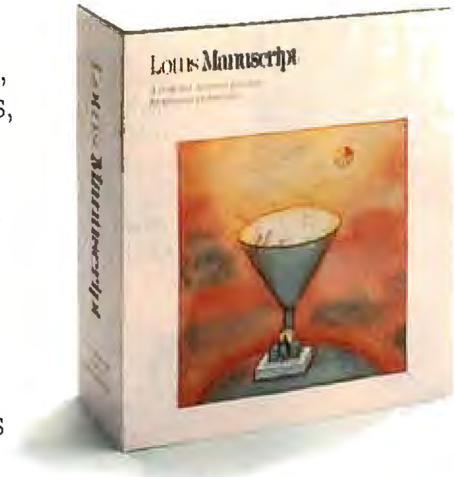

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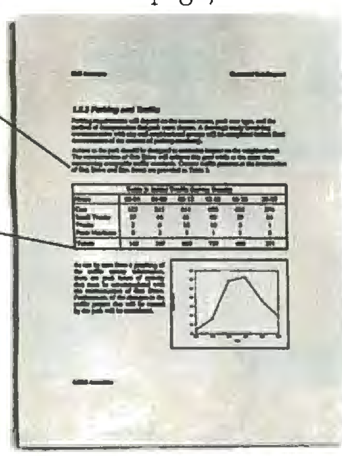

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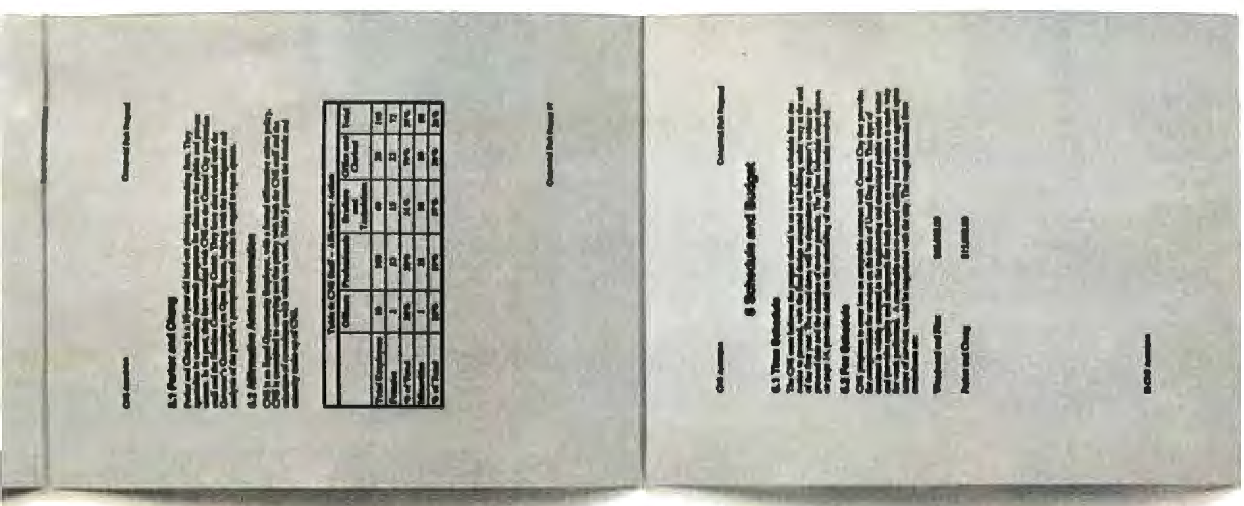


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Introduction to Programmable Array Logic

A look at the architectural differences between PALs and other programmable logic devices

Vincent J. Coli

PROGRAMMABLE LOGIC devices are integrated circuits that hardware designers can program to perform specific logic functions. Most PLD functions are available from many vendors and in several technologies with different speed, power, and cost options. As with standard 7400 chips, PLDs are available off your local distributor's shelf. PLDs offer one distinct advantage over standard 7400 discrete logic: They are user-programmable.

Most PLDs consist of two arrays of logic gates—an AND array followed by an OR array. The input signals to a PLD must first pass through an array of AND gates where combinations of the input signals are formed. Each group of AND combinations is called a minterm in Boolean algebra or a product line in PLD nomenclature. Then the product lines are summed in an array of OR gates. The input buffers generate both the true and complement of the input signals.

Three basic types of AND/OR array-based PLDs exist: programmable read-only memories (PROMs), programmable logic arrays (PLAs), and programmable array logic (PAL) devices. The types are distinguished by the programmability of their arrays.

In a PROM, the AND array is fixed and the OR array is programmable. In a PLA, both arrays are programmable. PAL devices have a programmable AND array and a fixed OR array. I will compare the PAL device to the PLA and PROM and then examine the architecture of some commonly used PAL devices. For a brief history of the PAL device, see the text box "Evolution of PALs" by John Martin Birkner on page 208.

PROMs

While most people think of PROMs as devices for storing fixed programs and memory, the PROM is also ideal for logic applications requiring less than 10 inputs—especially when many product lines are required. PROMs designed as logic devices are usually referred to as PLEs (programmable logic elements).

Figure 1 shows the PROM's fixed-AND/programmable-OR arrays. For a discussion of notation used to describe PLD devices, see the text box "PLD Notation Panel" on page 210. Every input combination is available in the AND array, whether that combination of inputs is required or not. Since the AND array is hard-wired, it is not possible to perform logic minimization between input combinations.

The OR array is programmed to select the AND gate combinations (or product lines). Since every OR gate is connected to each product line, outputs may share product lines. For those familiar with memory design, the fixed-AND array is often called the address decoder, while the programmable-OR array stores the memory bits. Another way of looking at this is that PROMs store the logic transfer function as a lookup table in memory.

The advantage of PROMs is that every input combination can be decoded. The disadvantage is that the number of input pins available is restricted because the array size must be doubled for each additional input. The arithmetic works like this: A PROM with n inputs and m outputs requires an OR array of 2^n lines deep by m lines wide. For example, a PROM with 10 inputs and 8 outputs requires an OR array of 2^{10} by 8 or 8192 fuse locations. An 11th input would require that the array size be doubled to 16,384. Cost and performance constraints limit PROMs to 13 inputs and 8 outputs. PROMs designed specifically for logic applications feature either 5 or 6 inputs and 16 outputs.

PLAs

The PLA structure offers the highest level of flexibility because both arrays are programmable. Figure 2 shows the PLA's programmable-AND/programmable-OR structure. Because their OR arrays are programmable, PLAs, like PROMs, can share product terms among outputs. For example, one product line would be saved if two outputs required the same input combination (i.e., product line).

Programmability in the AND array removes the restriction found in PROMs that the AND array must be large enough to provide all possible input combinations. This works because, statistically, only a

continued

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The Evolution of PALs

John Martin Birkner

Computers used to be constructed from SSI, MSI, PROM, and RAM chips connected in jigsaw-puzzle fashion on many printed circuit boards plugged into a connector backplane. The computer designer's task was to build a functional unit such as a processor, disk controller, I/O controller, or memory board. If the design overflowed onto another board, connectors and ribbon cables had to be added. This made the design more expensive and sometimes risky due to noise coupling. The name of the game was to get it all on one board.

Mixing and Matching TTL Chips

Designers who had studied switching theory, information theory, Boolean algebra, and Quine-McCluskey minimization at college soon found that their textbooks would not be of much use. They learned that the practical art of computer design did not consist of optimizing an architecture with an orthogonal instruction set. It consisted of mixing and matching the collage of existing TTL chips onto a single board until an approximation of the design goal was reached. They did not design state-control sequence logic from top-down state-graph theory, but rather, slapped down a 74174 hexadecimal register and some 7400 NAND gates. Control-logic design theories usually consisted of following signal lines around the logic schematic until, through superhuman powers of concentration, designers achieved clarity.

Designers found the information they needed in the catalogs of young semiconductor companies in California, Arizona, and Texas. A favorite was *The TTL Databook* by Texas Instruments. Most logic designers believed that 74-series TTL parts found in this book would be second-sourced and could be "designed in."

A processor design would begin with the block diagram consisting of an ALU, data path and register file, microprogram memory and sequencer, and then a small and obscure block called "control logic." It might have been a small block on the diagram, but the control logic usually represented the majority of the chip count.

The control logic consisted of SSI/MSI gates and flip-flops connected together in random fashion, and there seemed to be no way to reduce it. The control logic also represented the area of highest design errors and was easily recognizable on the printed circuit board as the area with all the "cuts and jumpers." The engineering change notice (ECN) was the standard remedy for such errors and was a constant source of agony between manufacturing and engineering. Manufacturing would use yellow wires to stand out on the green PC board. Engineering would use green jumper wires to camouflage embarrassing mistakes.

The engineering manager would "pilot release" the current revision PC board as soon as the green wire count was low enough to pacify manufacturing. The design engineers would then flee to the next design, where they were expected to cram even more functions onto the single PC board to beat the competition's new threat.

I was convinced that there must be a better way to build computers. So, in 1975, I packed my bags and headed for Silicon Valley. I remember seeing the first single-chip microprocessor systems on the market. They had one microcomputer chip surrounded by a sea of over 100 SSI/MSI chips. The new LSI chips needed either some good planning so that they could talk to each other or some good "glue chips" to hook them up.

The PROM, pioneered by Harris and Monolithic Memories, showed some promise as a universal and general-purpose glue logic element. Applications like memory-address decoding began showing up for the 32-word by 8-bit PROM. National Semiconductor pioneered the programmable logic array (PLA) in a 14-in, 8-out, 96-product-term, 24-pin fat (0.6 inch wide) DIP, benchmarked for 96-character EBCDIC-to-ASCII conversion.

Intersil made a field programmable logic array, or FPLA, in the National pinout, but with about half the product terms at 48. Signetics increased the package pins to 28, making the 16-in, 8-out, 48-product-term 82S100 FPLA. These first attempts at providing the computer designer with LSI glue were met with mild enthusiasm. The new glue chips were too big (fat DIPs) and were slow, expensive, and hard to use.

Monolithic Memories was the first company to take advantage of the bipolar fuse-link PROM technology to make some fast little FPLAs, as we first called them. We put them in industry-standard 20-pin skinny (0.3 inch) DIPs, for minimum PC board area. We also reduced the two programmable arrays down to one for 35-ns high-speed operation and lower cost. We mimicked the TTL data-sheet specs down to the same terminology, graphics, and printing style to make the computer design engineer secure in replacing old 74-series TTL chips. We added programmable three-state output enable for I/O pin allocation. We added output registers with feedback for direct implementation of state-machine control logic from state graphs.

We designed the programming algorithm to be compatible with existing PROM programmers, making low-cost programming possible. The first PAL programming module had a PAL in it. This presented a chicken-and-egg problem that we solved by emulating with some PROM and SSI chips. The first PAL to be programmed was, of course, the pattern for the PAL programmer module. I headed the project, specified the design, and sold the customers. H. T. Chua provided a clever and ingenious circuit design.

New Design Methodology

The new chips required a new design methodology. Actually, it was the same method that we learned in school, so we had to drag out our old textbooks and relearn Boolean logic and top-down state-machine design. We showed the designer how to "design your own chip" using Boolean logic equations. We wrote the first silicon compiler, PALASM (PAL Assembler), and published the FORTRAN source in the *PAL Handbook* (available from McGraw-Hill), along with numerous design examples.

The PAL chips replaced SSI/MSI chips at a chip-count reduction of 5 to 1. Data General gambled on the new single-sourced chips by designing them into the MV8000 computer (see *The Soul of a New Machine* by Tracy Kidder).

Apple put six PAL chips in the Macintosh. Soon the PAL chips were no longer single-sourced, as National Semiconductor, Texas Instruments, Advanced Micro Devices, and others joined in licensing the now-patented PAL chips from MMI. Now you can find these chips everywhere. Look at the PC expansion boards in this magazine; you can recognize PAL chips by their easy-to-read part-number system (e.g., PAL16L8 and PAL16R8).

John Martin Birkner is president of Structured Design Inc. and coinventor of the programmable array logic (PAL) device. He can be contacted at 988 Bryant Way, Sunnyvale, CA 94087.

limited number of product terms is required in any equation. Eliminating redundant combinations with logic minimization techniques, such as Karnaugh maps, can reduce the required number of product terms even more. Therefore, almost any combination of inputs can be decoded in a PLA.

PLAs were the first products offered specifically for logic applications. Due to programming limitations, early PLAs were available only in mask-programmed versions. Just like on a ROM, a logic designer would indicate on the vendor's PLA AND/OR logic map where the desired connections were to be made. The vendor would then tool up a custom metal mask for the PLA to implement the customer's logic. Today, most PLAs are user-programmable. However, mask-programmed PLA structures are used often in the control section of LSI/VLSI standard logic chips, such as microprocessors, and offered in standard-cell libraries.

In the world of engineering, there are always compromises. The facts reveal that a performance and silicon-die size penalty must be realized to provide the flexibility of programming both arrays. PAL devices are generally 5 to 10 nanoseconds faster than PLAs at the same power level and save the silicon area required to program and verify the second array. It turns out that the flexibility of a programmable-OR array is not required for most PLD applications, but it can be useful for complex state-machine and sequencer applications.

Because of the long history of PLAs, their nomenclature can be a little confusing. Early vendors of user-programmable PLAs called their products FPLAs to highlight their "field programmability" and to distinguish FPLAs from factory mask-programmed PLAs. Just as ROMs and PROMs could be easily distinguished, so could PLAs and FPLAs. However, since most of the PLAs offered today are programmed by the customer, many vendors have dropped the F prefix and simply call them PLAs. Furthermore, PLAs designed for sequencer applications are called PLSs (programmable logic sequencers).

PAL Devices

Figure 3 shows the programmable-AND/fixed-OR array structure of a PAL. As with the PLA, having the AND array programmable lets the user program only the desired input combinations. But fixing the OR array requires that certain product lines be tied to specific outputs—typically, eight product lines per output.

Many people use PAL and PLD synonymously. Several PLD vendors add an E prefix to PLD, to come up with EPLD, which signifies ultraviolet erasable PLDs. Just as there are PROMs and EPROMs, now there are PLDs and EPLDs.

The name HAL (hard array logic), refers to mask-programmed, or ROM, versions of PAL devices. If the volume of devices needed were large, converting a design to a HAL might be appropriate once the design is thoroughly debugged with the PAL.

While all PAL devices are characterized by a programmable-AND/fixed-OR array structure, there is a whole line of PAL devices with different options. They come with varying numbers of inputs and outputs. They might have feedback paths from the output back to the array. Some of these pins can be programmable I/O pins. They can have active-high or active-low outputs, or the output polarity might be programmable via an XOR gate and a fuse. Some come with registers at their outputs and are good for making sequential circuits. Let's look at two commonly used PAL devices: the 16L8 and the 16R8.

The PAL16L8

One popular combinatorial PAL is the PAL16L8 (figure 4). Notice how the pins on the left side and bottom of the logic diagram (pins 1 to 9 and pin 11) are used for inputs and the pins on the right (pins 12 to 19) are available as outputs. Pins 12 and 19 can be used only as outputs, but six of the outputs (pins 13 to 18) are also

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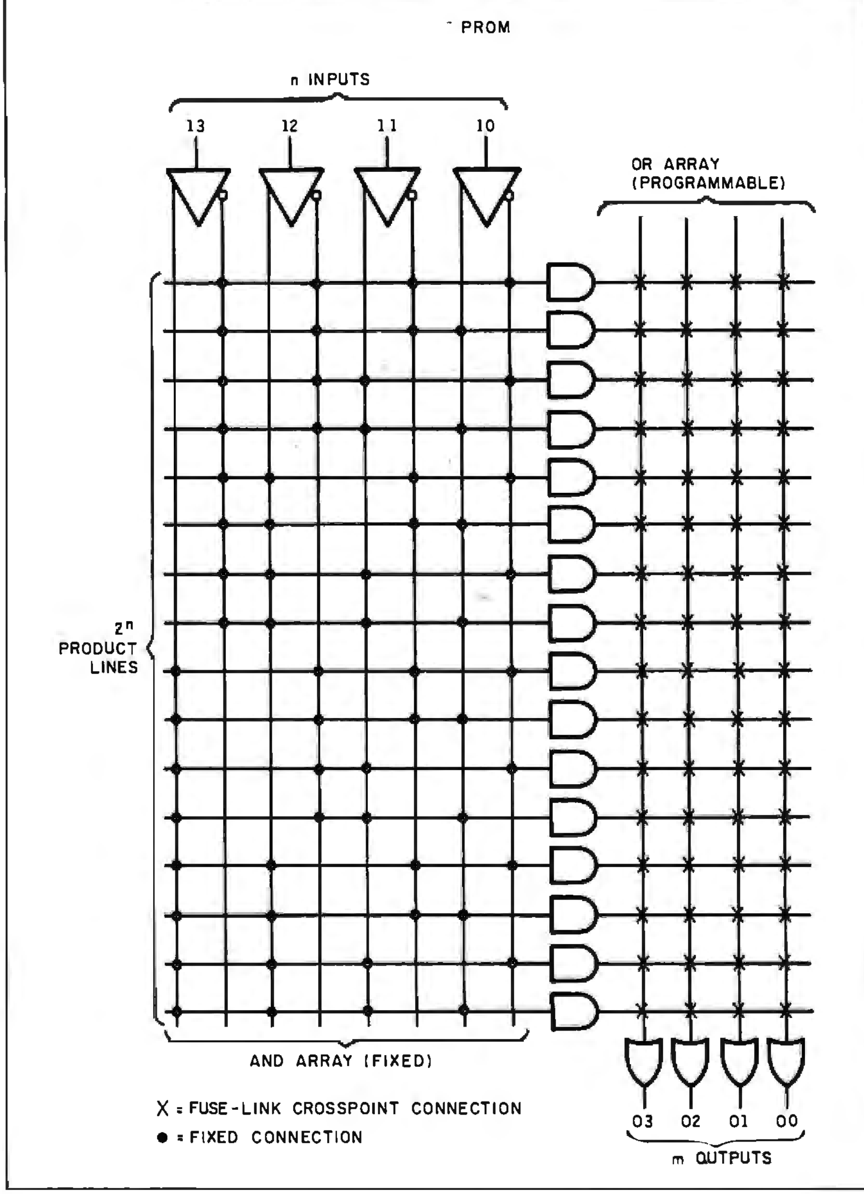

Figure 1: *A simplified diagram of the fixed-AND/programmable-OR array structure of the PROM. Figures in this article are reprinted from Monolithic Memories'* PAL Handbook *(3rd ed.) with permission from Monolithic Memories.*

PLD Notation Panel

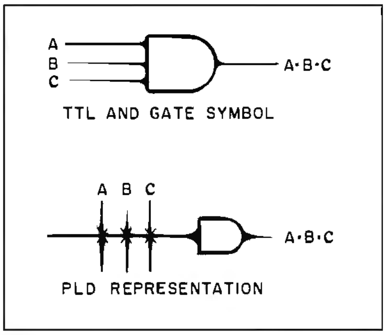

Figure A: *Differences in the logic notation for a TTL AND gate and a PLD AND gate.*

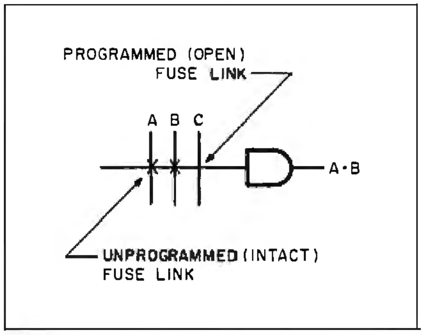

Figure B: *The partially programmed product line to implement A*B.*

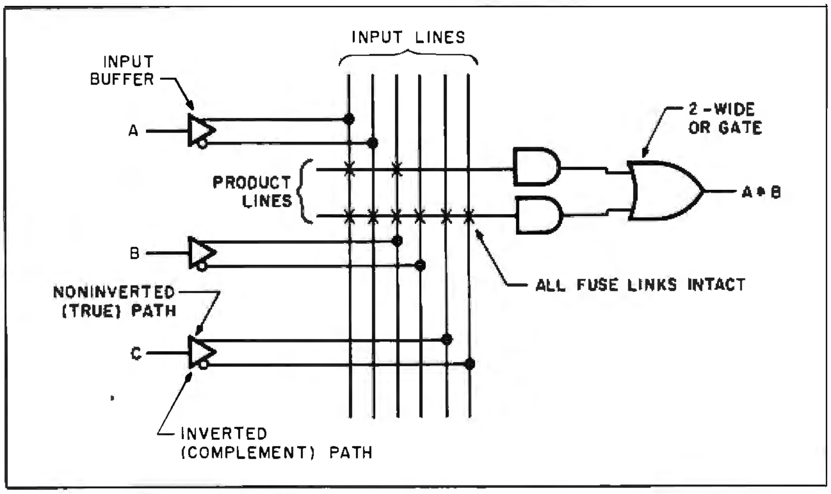

Figure C: *Portion of the PLD array programmed to implement A*B. Having all fuses intact in the second product line causes a logic zero to be input to the second AND gate, which does not contribute to the sum at the OR gate.*

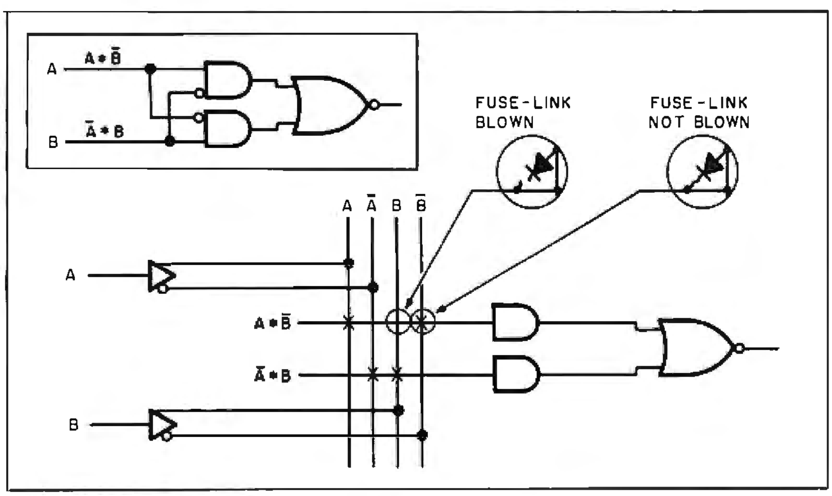

Figure D: *The PAL device implementation of the function /Output = A*B + /A*B. The standard combinatorial logic diagram of the function /Output = A*/B + /A*B is shown in the inset to figure D above.*

Because PLD structures are much different from ordinary TTL gates, new logic notations were developed for them. Figure A shows the logic convention adopted for a three-input AND gate. The PLD representation for an AND gate is called a "product line." Note that the three vertical lines are the inputs (A, B, and C), which are connected to the AND gate inputs through fuse links. An unprogrammed (or closed) fuse link is represented by an X at the intersection of an input line with a product line. If you wanted to disconnect one of those inputs from AND gate C, for example, you would remove the appropriate X from the point of intersection for the C input line with the product line to signify a programmed (or open) fuse link. This product line, which now implements the A*B function, is shown in figure B.

Since every input is available to every product line in a PLD, it is convenient to show the input lines as long lines running vertically through the array. Also, two input lines are associated with each input pin because both input polarities are available in a PLD. Therefore, the input buffer is shown with both a noninverted (true) and inverted (complement) output path; each path is hardwire connected (shown as a dot) to an input line.

Figure C shows a portion of a PLD array illustrating the input lines and buffers. Notice that an OR gate is added to the structure. All the fuse links in the lower product line are left intact, leaving the product line in a logic low (since true inputs are ANDed with complements), while appropriate fuse links in the upper product line are programmed to implement the A*B function from figure B.

It is common to implement two or more levels of logic gates such as an AND/OR/invert circuit in a PLD. For example, consider the following function implemented in a PAL device:

/Output = A*/B + /A*B.

Shown in figure D are the standard combinatorial logic diagram (see inset) and the PAL logic equivalent for this function.

Notice the details added to figure D that magnify the programmed fuse link for B in the upper product line. This magnification details each fuse link and its associated diode for a bipolar PAL device. A CMOS PAL device is similar, except an ultraviolet cell would substitute for the fuse link.

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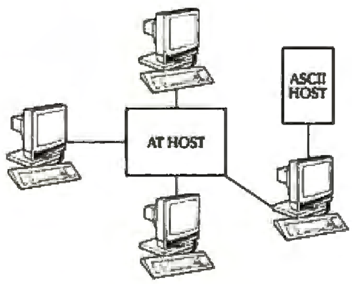

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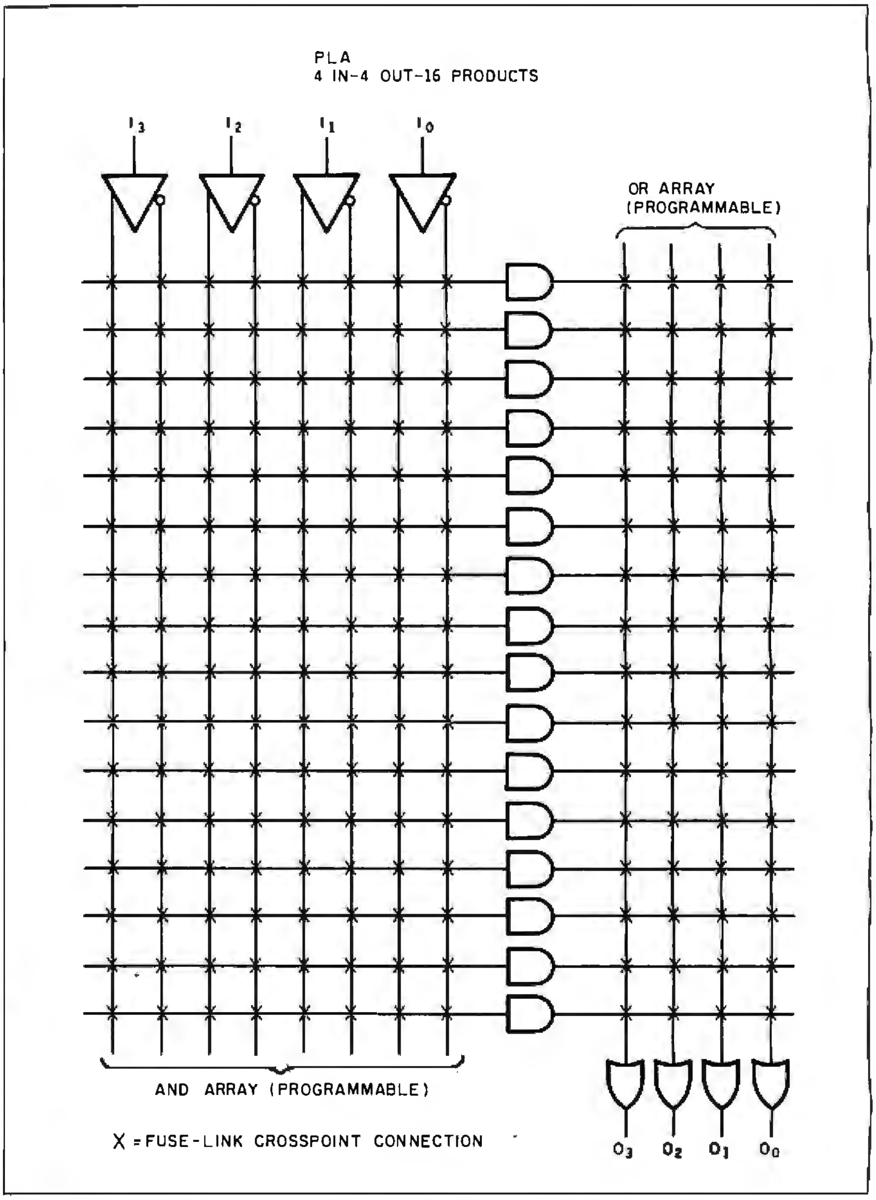

Figure 2: *A simplified diagram of a PLA showing that both arrays are programmable.*

available as inputs via the feedback line connection after the inverting output buffer. This feature, called programmable I/O, lets the user program each of these six pins to be either an input or output. I'll discuss programmable I/O in more detail later on. Now the PAL16L8 part-numbering scheme should be a little more obvious; 16 signifies the maximum number of potential inputs (10 dedicated inputs and 6 programmable I/O), while 8 signifies the number of outputs and L signifies the output type, which is active low for this PAL part type.

Refer to the logic diagram in figure 4 and you'll see that the vertical lines running through the array, numbered 0 through 31, are the input lines. Notice that each input or I/O pin is associated with two input lines; one input line is connected to the true (or noninverted) sense of the input buffer, while the other input line is connected to the complement (or inverted) sense. This allows availability of both input-signal polarities to the array.

The horizontal lines running through the array, numbered 0 through 63, are the product lines. You can think of each of these product lines as an AND gate with 32 inputs, which corresponds to the total number of input lines. Actually, both the true and complement of every input signal are connected via fuses to each product line before the device is programmed. This is the programmable-AND array in the PAL structure. To program the array, the user selects different combinations of

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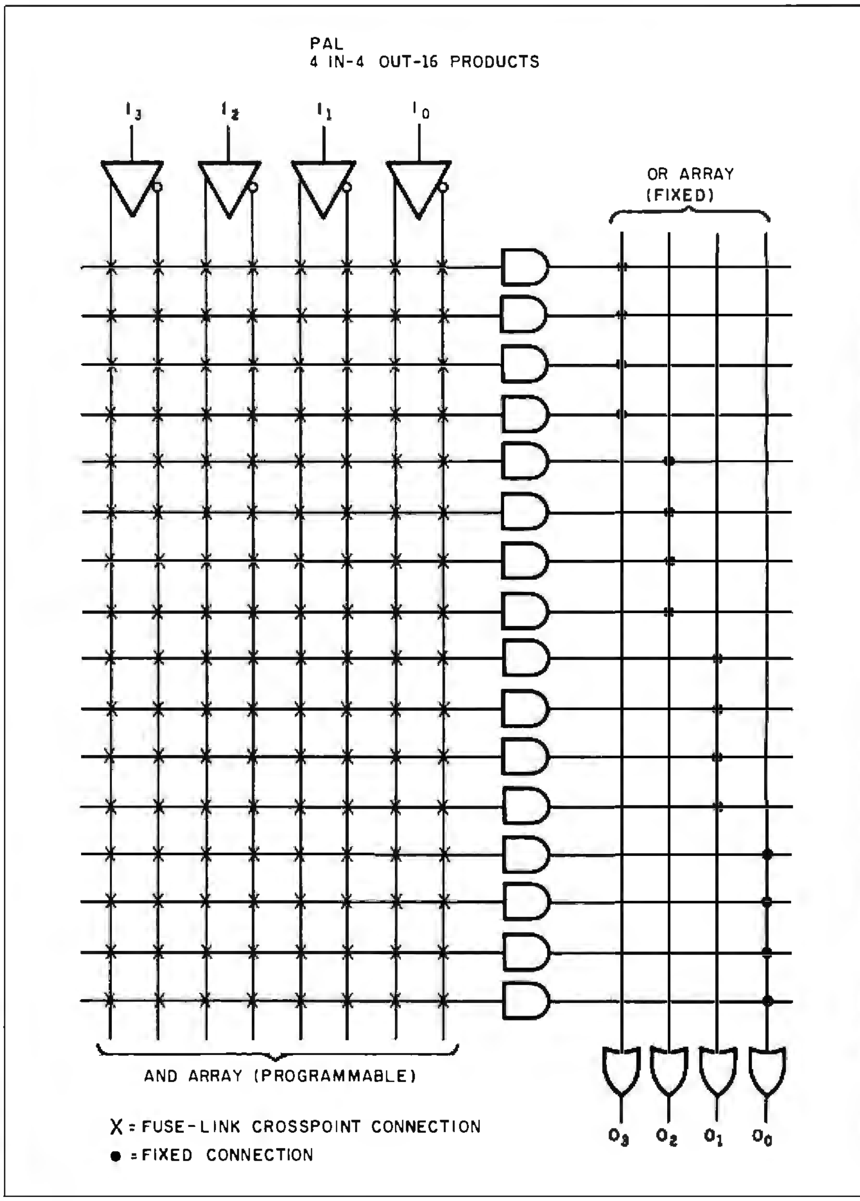

Figure 3: *A simplified diagram showing the programmable-AND/fixed-OR array structure of a PAL device.*

input signals by disconnecting, via the blown fuse, the unwanted input signals in a product line. In total, 2048 fuses are available in this PAL device (64 product lines by 32 input lines).

Notice that each output pin has eight product lines associated with it. The lower seven product lines of each group are summed at the OR gate, while the upper product line is connected to the inverting output buffer. The lower seven product lines and the OR gate provide the sum-of-products logic power for the PAL device. The OR gate determines whether any of the product lines are active, or true, and then the output buffer inverts the signal from the OR gate for output. Note that a product line with all fuses left intact will not affect the sum at the OR gate, since the logical result of each input ANDed with its complement is false.

Programmable I/O

This upper product line associated with each output controls the three-state logic in the output buffer. When this product line is active, or true, the output is enabled and the sum-of-products logic determines the output state. However, when this product line is inactive, or false, the output is disabled with the three-state buffer in the high-impedance state. This lets the output pin drive a three-state bus just like a 74S240 octal buffer. Furthermore, since most PAL devices feature an output drive capability of 24 milliamperes, they are quite handy for bus interfacing.

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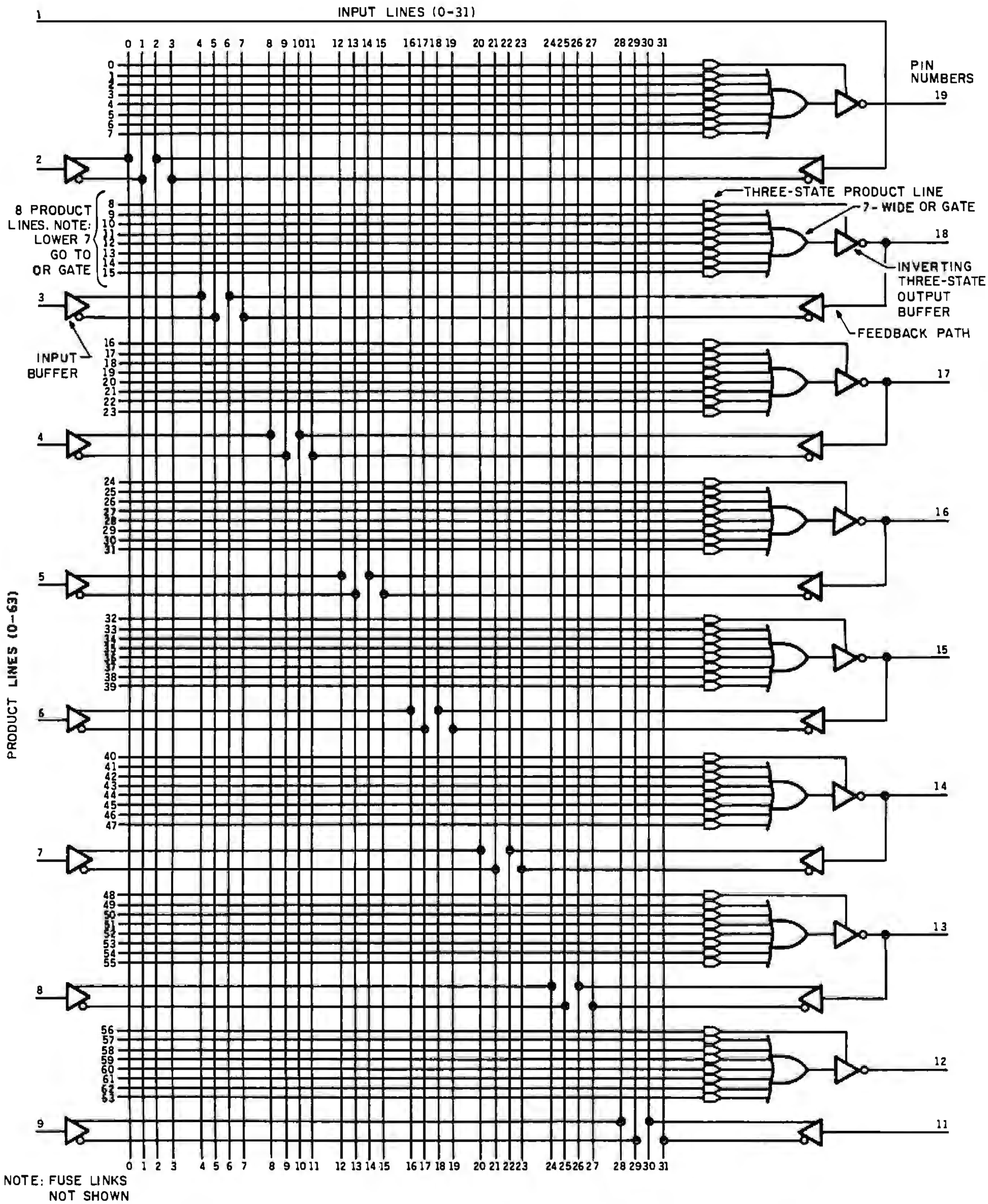

Figure 4: *The actual logic diagram of the combinatorial PAL16L8. The fuse links are not shown so that a logic designer may place an X at those points where a fuse should be left intact.*

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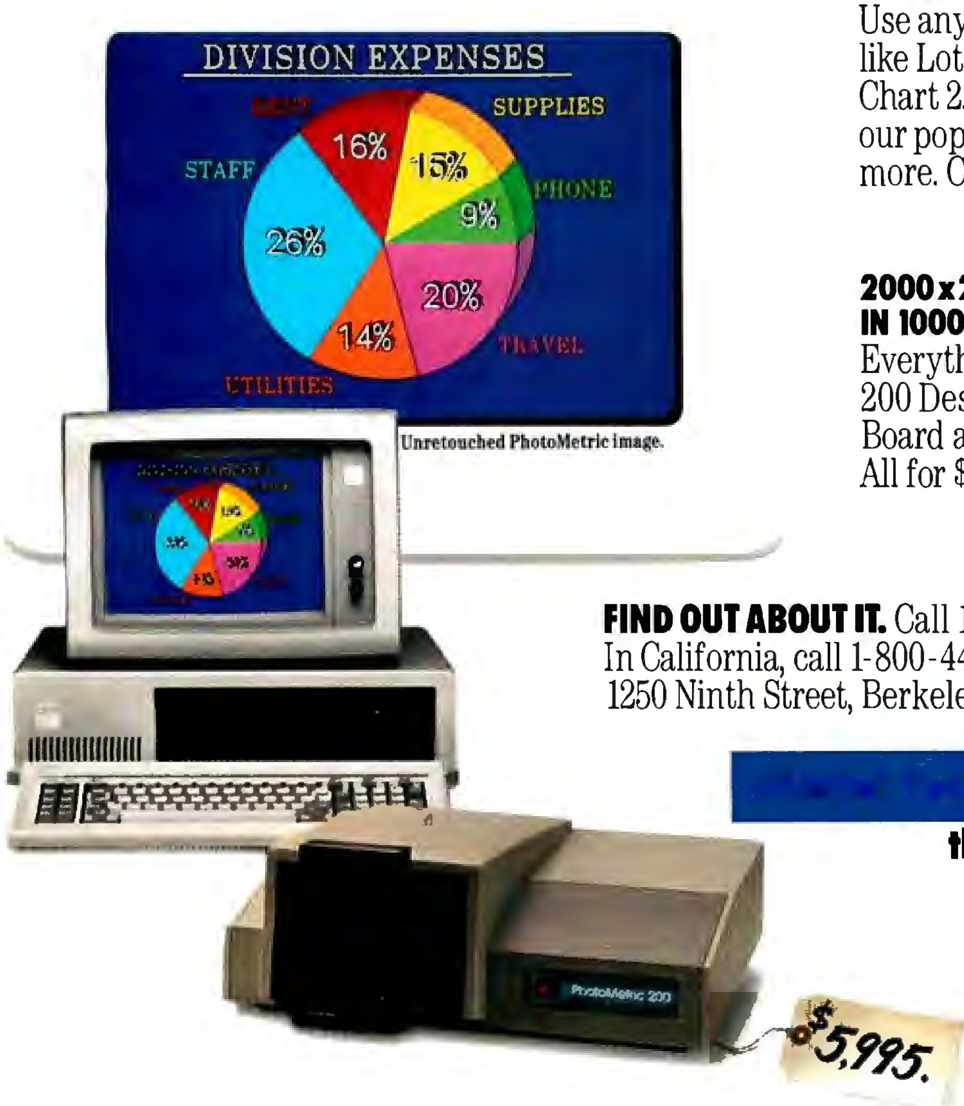

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The three-state product line, along with the feedback path on six of the outputs, makes the programmable I/O feature work. The pin is an input to the AND array when all the fuses in the three-state enable product line are left intact, while the pin is an output when all the fuses are programmed. Note that a product line will always be true, regardless of input combinations, when all fuses are programmed. The programmable I/O feature lets the user allocate pins for input or output as required by the application.

An even higher level of flexibility is possible if you let the logic in the product

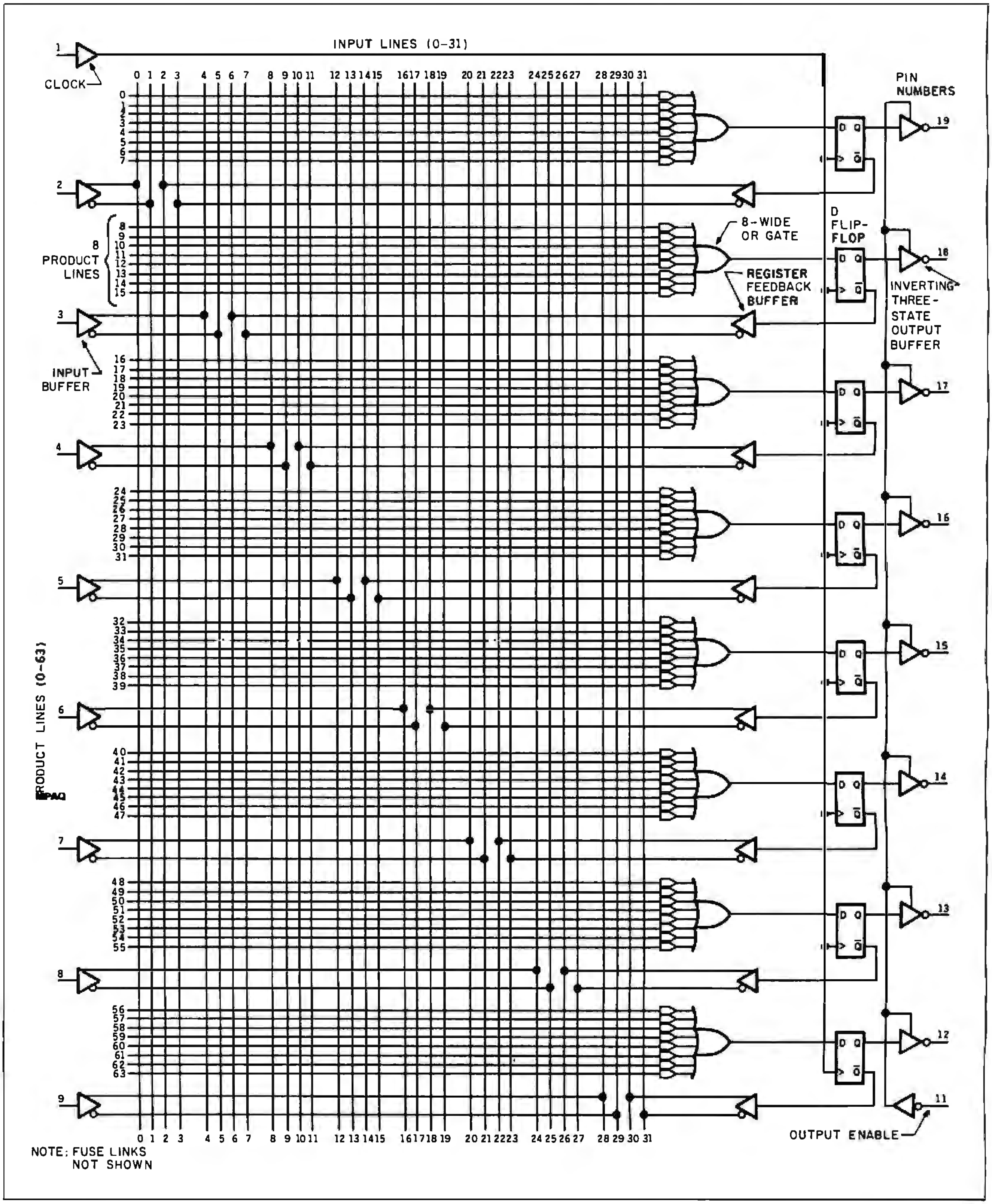

Figure 5: *The actual logic diagram of the PAL16R8. Notice the D-type flip-flops at the outputs.*

line determine the pin's direction. This is done by programming a condition in the product line for which the pin will be an output. You can use this feature to allocate available pins for I/O functions or to provide bidirectional transfer for operations such as shifting and rotating data.

The PAL16L8 is used in applications such as complex decoders, encoders, multiplexers, comparators, and replacement of SSI/MSI random logic. Another way of viewing this is that the PAL16L8 programmable AND array contains 2048 fuses. You can program these fuses to create almost any configuration of up to 250 AND, OR, and inverter gates, which is roughly 250 equivalent gates.

PALs with Registered Outputs and Feedback

The structure of registered PALs is similar to that of the PAL16L8 except for the addition of the registered outputs. In the PAL16R8, each of the eight registers is actually a D (data) flip-flop that is clocked on the rising edge (see figure 5). The clock signal (pin 1) is shared by all eight flip-flops. Each OR gate sums eight product lines and is the D input to the flip-flop. The Q output from the flip-flop is available both for feedback into the PAL array and for output from the device. Either polarity of the feedback signal is available.

This feedback lets the PAL device "remember" the previous state, and it can alter its function based upon that state. Thus, registered PAL devices are ideal for implementing single-chip state sequencers and state machines.

Conclusion

PROMs are limited in the number of inputs they can handle, since every input combination is made available. They are useful for applications that require a large number of product terms but few inputs.

PLAs are the most flexible of the AND/OR array PLDs with both arrays programmable. This flexibility makes them slower, since the signal has to propagate through two programmable arrays. PAL devices with their programmable-AND/fixed-OR array structure can accommodate more inputs than PROMs because, statistically, not every input combination is required. With only one array programmable, they are faster than PLAs.

PAL devices with registered outputs are particularly useful for building sequential circuits. PAL devices also can provide feedback, altering the function of a given state based on the condition of the immediately prior state. The overriding advantage of all PLDs, however, is the integration of multiple functions onto a single programmed circuit to save board space and reduce chip count and cost. ■

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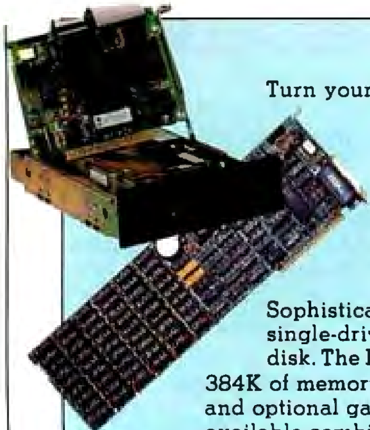

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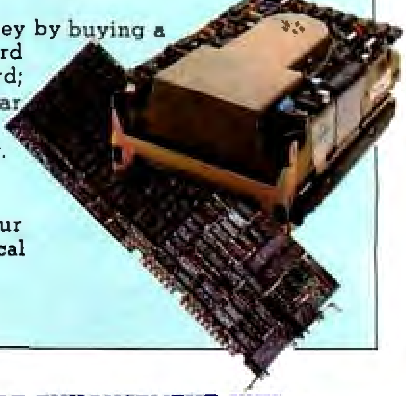

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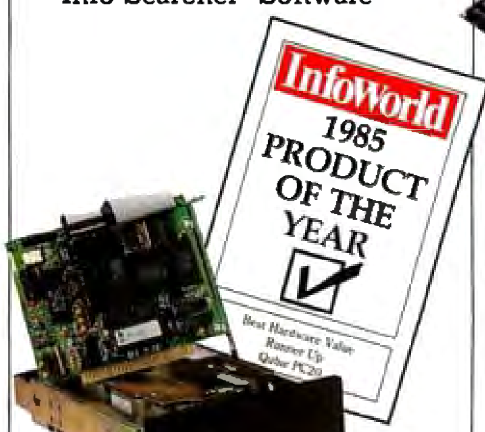

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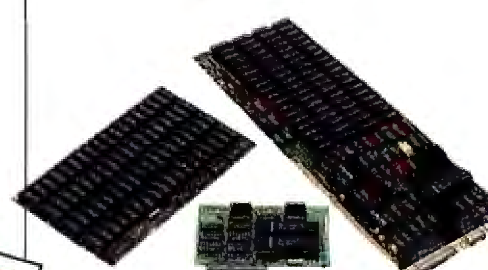

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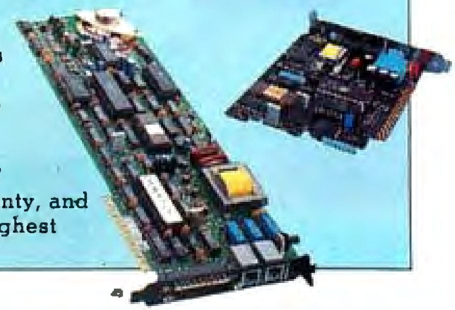

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Getting Started with PALs

Useful tips on choosing a PAL and having it programmed

Robert A. Freedman

ANYONE DOING DIGITAL logic design with TTL these days ought to be using PALs. The PAL (programmable array logic) is a device that you can use to implement and replace various SSI and MSI circuits in a TTL design. You can use it to make gates, flip-flops, counters, decoders, registers, and finite-state machines. PALs can replace up to 10 TTL SSI chips each, saving board space and making the design process a lot easier. However, using PALs involves some tradeoffs, shortcuts, and problems of which a logic designer should be aware.

Types of PALs

Early PALs were purely combinatorial and had sparse arrays (i.e., they did not use all possible positions in the fuse array). Table 1 shows some of the basic PALs available. Some simple examples are the 10L8 and the 14L4. These have 10 and 14 inputs and 8 and 4 outputs, respectively. Then came PALs with feedback and tristate outputs such as the 16L8, and registered PALs such as the 16R4, 6, and 8. Next came the PALs with exclusive-OR of the product terms (16X4). These are good for making counters and adders. The 24-pin versions had extra input pins, such as the 20L8. More recently, PALs with programmable output polarity (16P8A) and product-term sharing (20S10 and 20RS4-10) have been released. Also, there are the giant megaPALs (32R16 and 64R32).

The Advanced Micro Devices AmPAL-22V10 is a second-generation PAL with output logic macrocells. A macrocell in a PAL is a logic block between the fuse array and the output pin that you can configure by programming certain fuses to act in any of several ways. Independently of the other outputs, each output can be either registered or combinatorial, have active high or active low, have programmable output enable or bused output enable, have registered or combinatorial feedback paths, and allow bidirectional I/O from the output pin. Some programmable logic devices have macrocells that let the register act as an SR-type flip-flop or a JK-type flip-flop, as well as the familiar D-type flip-flop as in standard PALs.

PALs come in different speeds. The suffix on the part number tells the part's speed and power consumption. Parts with standard speed (50 nanoseconds) and power (typically 0.2 watt) have no suffix. A 16L8A is a 25-ns part; a 16L8B is a 15-ns part. A −2 and −4 suffix means the device is a ½- or ¼-power part, respectively. Texas Instruments uses −15 or −10 on its PALs to indicate speed in nanoseconds.

Minimize Types in Inventory

Since so many PAL types are available, you should know that it is necessary to stock only a few types because some PALs are a subset of others. For example, you can use a 16L8 in place of a 10L8, 14L4, or 12L6. The 16L8 is only a little more expensive than the others, but it is flexible enough to replace them.

The trend is toward making generic PALs, that is, PALs that can replace most others. The AMD AmPAL-22V10 is designed as a generic PAL. You can program its output macrocell to emulate the output structure of any existing 20-pin PAL. Since you can configure this part to look like many other PALs, it is not necessary to stock the other types. For someone getting started using PALs, a good selection would be the 16L8, 16R4, 16R6, and 16R8. These are widely available, inexpensive, and will handle most combinatorial or sequential logic.

Different Brands

PALs of the same type from different manufacturers might have varying programming specifications. The material used to make the fuses determines the amount of power, the peak voltage, and the timing intervals required to reliably blow a fuse. The same PAL type can be constructed in several ways, each of which provides access to the fuse array via different pins on the chip. This means that a 16L8 from AMD might not program on a machine made to program TI PALs, and vice versa.

Newer PALs

Some of the newer PAL-like devices have features that make development easier,

continued

Robert A. Freedman has an S.B.E.E. in computer science from MIT and works as a freelance consultant designing with microcomputers. He can be contacted at (617) 683-4659 or P.O. Box 1348, Lawrence, MA 01842.

Most distributors will program their devices for a fee if you supply a master.

such as a large number of product terms and independently configurable outputs. You must be careful, however, not to use those features if you are planning on replacing them in the final circuit with a PAL that does not have them.

Some of the newer programmable logic devices are erasable. You can do your debugging with the reusable PLD, then move the same logic equations to a PAL in the final product without wasting a lot of one-time programmable PALs. Another advantage with erasable PLDs is that they let the manufacturer test the logic device and then erase it, thereby avoiding selling defective devices.

CMOS ultraviolet EPROM PLDs use EPROM cells instead of bipolar fuses to configure their logic. They are UV-light erasable and consume little power. Sprague makes the 16LC8 and 16RC4, 6, and 8 in CMOS. Altera and Intel make the UV-erasable EP-300 and EP-1200. The EP-300 can replace most 20-pin PALs, and the EP-1200 is like a small custom LSI application-specific integrated circuit in complexity.

EEPROM PLDs are electrically erasable. Lattice Semiconductor Corporation's generic array logic, GAL-16V8, and International CMOS Technology's PEEL 18CV8 are CMOS EEPROM devices. They are designed to emulate all common 20-pin PAL functions and to be electrically erasable and reusable.

CMOS PLDs can be programmed on "universal" programmers but not on most simpler PAL-only device programmers designed to burn fuses in bipolar PALs. CMOS PLDs are programmed in a similar way to EPROMS. While all CMOS UV-light erasable and electrically erasable PLDs are currently several times the cost of bipolar PALs, they are cost-effective because they are reusable.

Programming PALs

The PAL's logical functions are described in terms of a set of Boolean equations. These are then translated to a fuse map by a compiler that knows the target PAL's structure. Alternatively, you can obtain a fuse map by marking up a diagram of a PAL in the form of a coding sheet with the locations of the fuses. The axes of the coding sheet are numbered in a way that lets you determine the fuse number. Each location on the diagram corresponds to a location on the fuse map. The resulting fuse map is expressed in a Joint Electron Device Engineering Council (JEDEC) file format that can be read by most PAL programming hardware.

The JEDEC file can optionally contain simulation vectors, which are another way of expressing the PAL's functions. The simulation vector is a list of all expected inputs and the resulting outputs. These are used to test the PAL or verify the correctness of the equations. The JEDEC file is then loaded into the PAL programmer, and the fuses are blown. The simulation vectors can then exercise the PAL to see if it has been programmed successfully.

Table 1: *Examples of some 20-pin PALs, their designations, and some notable features.*

PAL nomenclature
- nnXmmA = 16L8A
- The left digits nn specify the number of inputs.
- The right digits mm specify the number of outputs.
- The letter X specifies features such as the output polarity.
- The suffix letter A specifies the speed.

Types of PALs
- Combinatorial PALs—Outputs are a direct function of inputs.
  - 10H8, 12H6, 14H4, 16H2—high outputs
  - 10L8, 12L6, 14L4, 16L2—low outputs
  - 16L8—active-low tristatable outputs with feedback
  - 16P8—programmable output polarity
- Registered PALS—Outputs are buffered by D-type flip-flops.
  - 16R8, 16R6, 16R4 —registered output PALs
  - 16X4, 16A4 —with exclusive-OR, good for counters
  - 16RP8, 16RP6, 16RP4 —programmable output polarity

Table 2: *This table illustrates some of the nonstandardization among manufacturers of PAL devices. The PALs all have different programming and control voltages; even the faster B-type MMI PALs require different voltages from the standard speed. NSC and TI have adopted MMI's programming pin-out, while AMD PALs have a different pin-out.*

PAL manufacturer	MMI	MMI-B	NSC	TI	AMD
Programming voltage	11.75 V	10.0 V	11.75 V	10.5 V	20.0 V
Control voltage	11.75 V	10.0 V	11.75 V	10.5 V	11.0 V
Programming pin-out	MMI	MMI	MMI	MMI	AMD

Designing with PALs

Specification sheets and catalogs of PALs are available from distributors or from vendor sales offices, usually without charge. In addition, you'll need a set of design tools, a source for PALs, and a means of getting them programmed.

Many semiconductor houses provide development software to support and introduce their proprietary PLD chips to potential customers. Virtually all semiconductor houses that make PALs provide a software tool to convert logic equations into fuse maps for programming both their proprietary parts and the industry-standard parts that they sell. In addition, manufacturers of PAL programmers provide software development tools for PALs.

Examples of PAL development software include ABEL from Data I/O Corporation, AMAZE from Signetics Corporation, A+Plus from Altera, CUPL from Assisted Technologies (division of P-CAD), PALASM from Monolithic Memories Inc. (MMI), PLAN from National Semiconductor Corporation (NSC), and PLPL from AMD.

Some of this software is even available as source code. PALASM version 1 has been published in FORTRAN. (See Trevor G. Marshall's article, "PALs Simplify Complex Circuits," on page 247 for details on obtaining PALASM 1 and 2.) Michael Stolowitz wrote a compiler for PALs in FORTH published in MMI's *System Design Handbook.* [Editor's note: *MMI supplied us with a PAL compiler written in BASIC. It is available on disk, in print, and on BIX; see the insert card following page 424. It is also available on BYTEnet; see page 4.*]

At the time of this writing, P-CAD is advertising a "PAL Starter Kit" that contains a tutorial booklet and disk, four high-speed TI PALs (16L8, 16R4, R6, R8), and the CUPL compiler that works only with the four PALs included in the kit. (For information, call (800) 227-6703 or (800) 632-7979 in California, or send $49.95 plus $3 postage to Starter Kit, P.O. Box 306, Half Moon Bay, CA 94019.)

Simulation Methods

Many of the above software packages provide for simulation of the PAL equations to verify their correctness. This is useful to avoid wasting chips and to help verify the correctness of the PAL equations.

Simulation can occur at the software or hardware level. At the software level, a set of test vectors is generated that is basically a list of the outputs expected for a given set of inputs. If these test vectors are generated independently of the equations, they can be used to determine if the equations are correct. Software emulation of the PAL equations should produce identical outputs to those specified in the test vector.

Some PAL programmers are set up to take test vectors from a JEDEC file and to apply these to the actual PAL after it has been programmed. The outputs are compared to the predicted values to determine whether the PAL has been programmed correctly. This is known as signature analysis. A PAL under test should produce the same results as a known-good master PAL.

Locating PALs

Large distributors like Arrow, Hamilton/Avnet, and Future Electronics have offices in major cities nationwide and carry most important lines of PALs. Active Electronics is one of the few retail mail-order houses to carry PALs. By far the best source of PALs is the spot IC brokers advertising in the back of weekly papers such as *Electronic News* and *Electronic Buyer's Guide*. Both have several pages of ads selling surplus lots of new ICs, including PALs. Their prices are much lower than distributors, and some list toll-free numbers. The only drawback is that you might have to buy 50 or 100 pieces at a time.

Getting PALs Programmed

If you program PALs only occasionally or if you just want an exact copy of an existing PAL, it makes sense to take advantage of the service that most large distributors provide. They will program the devices they sell for a nominal fee if you supply a master for them to copy. From distributors, you can get 24-hour turnaround at a cost of $5 to $25. Entering data from equations or fuse maps is more expensive. The only problem is the "oops" factor: You had better be right the first time, because each iteration will cost you a day and some bucks.

Buying a PAL Programmer

Commercially available PAL programmers cost between $500 and $5000. They are expensive because top-of-the-line programmers have a universal architecture designed to handle most types of programmable devices. These are really PROM programmers with adapter modules for PALs, such as the Data I/O LogicPak.

Other programmers are designed in advance to handle every kind of PAL, programmable logic element, or PROM that is likely to be produced. These operate on the programmable-pin principle. Each pin of the test socket can be programmed by software to be either input or output. Each pin can be read by an analog-to-digital converter or driven by a digital-to-analog converter. The high-current drivers necessary to blow the fusable links in the PALs or PROMs can be precisely controlled by software and the results noted with equal precision. These units usually have their own embedded microcomputers

continued

or can interface to a PC. They can be updated for new device types, either by the change of an EPROM or by a floppy disk. Universal programmers are made by Structured Design, Stag Micro Systems, and others. See the MMI *PAL Handbook* for a list.

Some PAL programmers have the design software, such as PALASM, built in. A recent trend is to place the design software in a host computer and have the programmer accept and be driven by a JEDEC format file that contains the fuse map, device type, and documentation for the part to be programmed. This improves data interchange between software and programmers from a variety of vendors.

The low-end models are usually specifically designed to program only certain types of PALs, such as only 20-pin types from certain manufacturers. The fact that these have a case, a power supply, and a built-in microcomputer sets a base minimum that a manufacturer must charge.

Programming Difficulties

If commercial PAL programmers are so expensive, why not build your own? There are lots of construction articles and boards for EPROM programmers (see Steve Ciarcia's "Build an Intelligent Serial EPROM Programmer," October 1986 BYTE). Why not for PALs? EPROMs are relatively easy to program; you need to apply a single high voltage (12.5 to 25 V) on one pin and then, when the address and data are stable, you pulse the programming pin.

For the most part, with EPROMs the programming pins are physically different from the operational pins. With PALs, the operational pins share the programming pin functions. The voltage level on the pins determines whether you are in normal operation mode or programming mode; the higher voltage level is called a super (or zener) voltage. For example, during normal operation, a PAL requires TTL levels (low = 0.0 to 0.8 V and high = 2.4 to 5.0 V). When a higher voltage is applied to the appropriate pins (11.75 V for MMI PALs, 10.5 V for TI PALs), it places the PAL in a programming mode. Then each output pin can be pulsed to the super-voltage for about 20 microseconds, with a slew rate (rise time of the pulse) of 1.5 V per microsecond. The blown fuse then must be verified at both a low and high voltage on the PAL's V_{CC} pin to be sure it is correctly blown.

PALs have less standardization of programming parameters than EPROMs. Each PAL manufacturer has slightly different voltages or timing specifications, and the newer PALs use different programming strategies for added features than for the basic fuse array. Table 2 shows some of the different voltages and pin-outs for PALs from different manufacturers.

AMD uses 20 V to burn array fuses, and its programming pin-out is radically different from MMI's pin-outs. Even among MMI's PALs, programming voltage varies between the standard and higher-speed PALs. Programmable polarity, product sharing, register preload, and security fuses all require different voltages on different pins (some doing triple duty) from those used in the fuse array, and each manufacturer uses a different architecture for implementing these features.

I have put together a PAL programmer construction article (see "A PAL Programmer" on page 263). By limiting the set of PALs, this programmer can handle to certain 20- and 24-pin MMI-type PALs, I was able to reduce the cost and complexity enough to make this a feasible project.

Issues of Security

Manufacturers of PALs provide security fuses that, when blown, inhibit the ability to read or verify the contents of the PAL's fuse array, while still letting the PAL func-

continued

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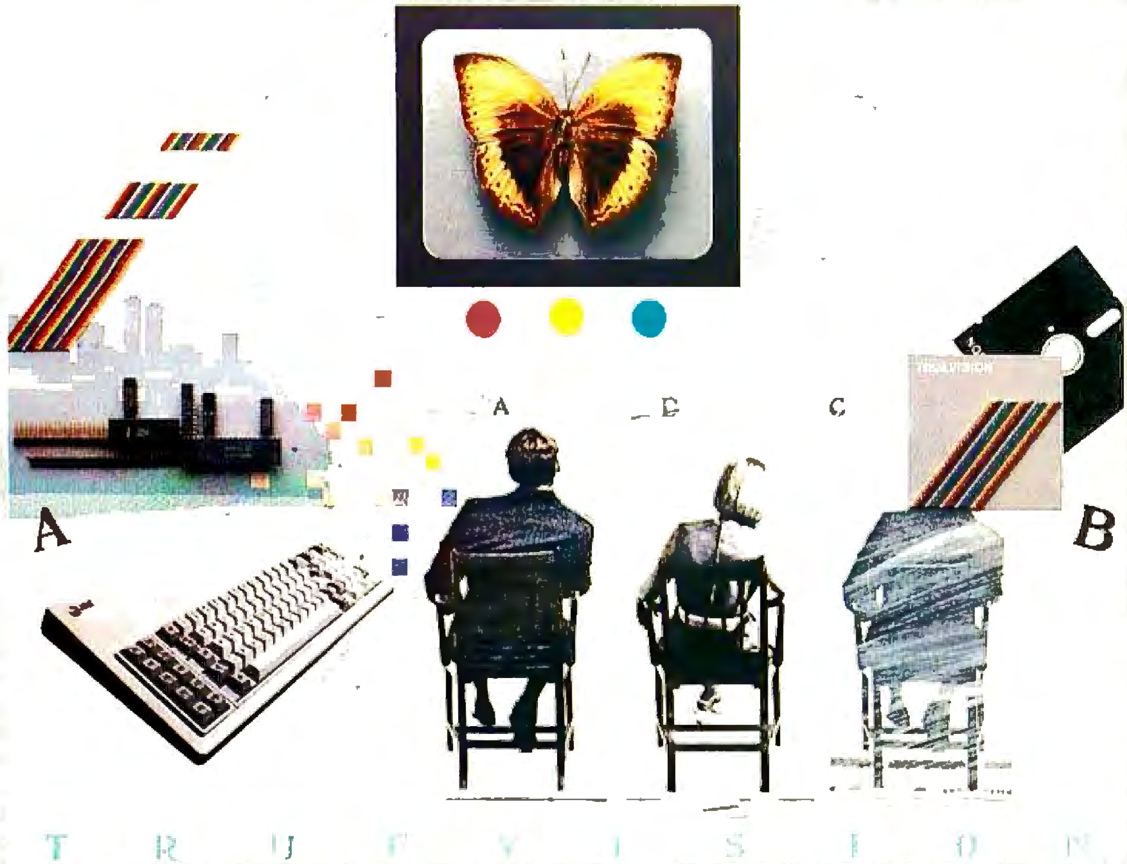

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tion properly in a circuit. A surprising number of equipment manufacturers do not bother to blow the security fuses on the PALs that they use. They rely on "security by soldering." If someone is willing to risk the destruction of a PAL or board in an attempt to desolder the PAL, the prize is the opportunity to read the equations from the PAL. A PAL programmer can be used to read the fuse map from a PAL whose security fuse is intact, and it is trivial to write a program to convert a fuse map back into the PAL equations.

When the security fuse is blown, you might still be able to determine the equations if the PAL is purely combinatorial by trying all possible inputs and noting how the outputs change state. This gives an exhaustive map of all inputs versus all outputs, which is a Boolean function: Outputs = F(Inputs). This function can be reduced using the Quine-McCluskey procedure to yield the simplified PAL equations.

The equations for registered PALs are more difficult because the value of the output depends not only on the current input but also on the current state. Because certain combinations of outputs (states) are either inaccessible or take long sequences of input transitions to reach, it takes many more trials to determine the equations of a registered PAL. But the same principles that make PALs difficult to read also make them difficult to test. Manufacturers are now beginning to design their PALs with preloadable output registers. This means that you can preset the outputs to any desired state for testing or reading.

The preload feature works by pulling one of the input pins to a super-voltage. This disables the output drivers and lets data be loaded into the registers via the output pins. You can then re-enable the PAL by removing the super-voltage, and testing may proceed as with a combinatorial PAL. The best part of this is that it works even when the security fuse is blown, thus rendering the security fuse useless.

Issues of Reliability

Despite what the chip makers say, a lot of duds get sold to PAL customers, even from reputable authorized distributors. The problem is that the whole fuse array can't be tested before being programmed. There is always a certain programming yield loss (i.e., units that fail to program). This runs around 2 percent to 5 percent in good lots. From time to time, a bad lot of PALs will find its way to distributors' shelves. Distributors will usually take back PALs claimed to be defective in manufacture.

continued

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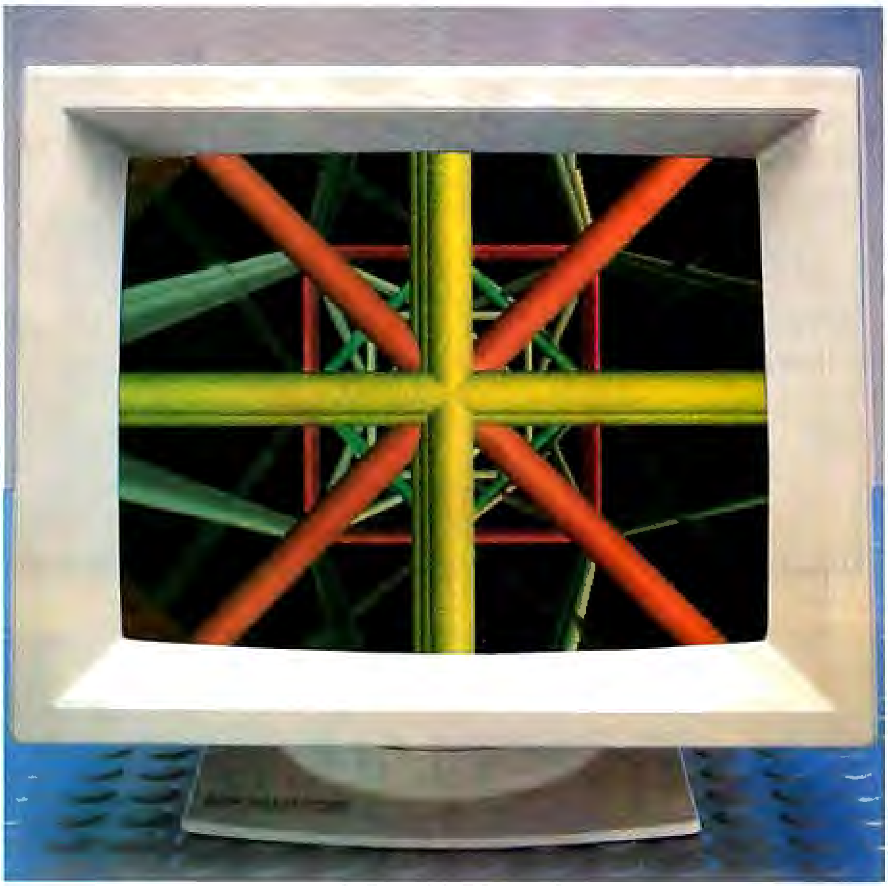

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GETTING STARTED

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Conclusion

In the old days, you were either a hardware or a software person. Today, the distinction is blurred. Logic design used to be accomplished by drawing a schematic diagram of a bunch of gates and flip-flops, then connecting them together to perform the desired function, wiring them up on a breadboard, and using an oscilloscope to debug the design.

Today, logic design is accomplished using the same tools that software programmers use. Instead of drawing diagrams, a logic designer writes equations. Instead of using Karnaugh maps to simplify logic, the designer uses logic-minimization software. State machines are designed by writing programs that look a lot like programs written in FORTRAN or C. Logic designs are explored and debugged using a simulator program rather than an oscilloscope.

And what about all those SSI circuit chips that you've sweated over for years and that you will hardly ever use again now that you're into PALs? Will you miss them? About as much as the vacuum tube. ■

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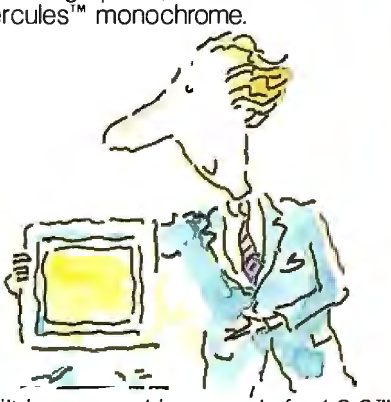

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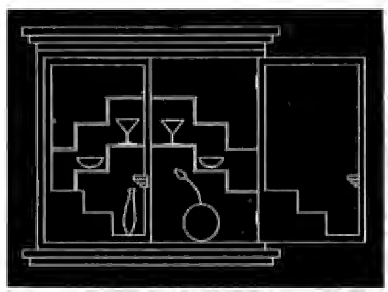

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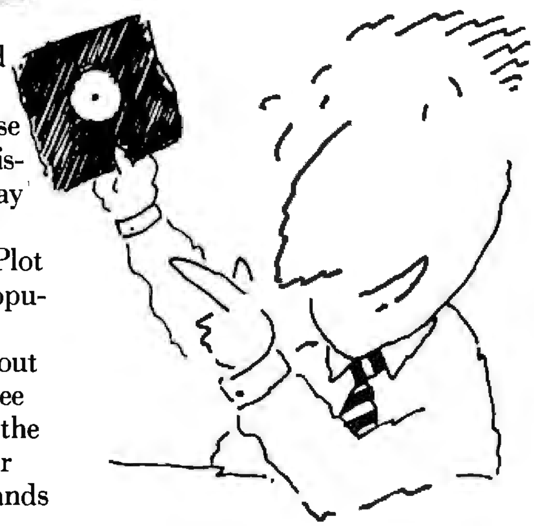

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Microcoded Versus Hard-wired Control

A comparison of two methods for implementing the control logic for a simple CPU

Phil Koopman

THE INSTRUCTION decoding and execution control sections of modern computers are prime areas for using programmable hardware. Two of the most widely used methods for designing CPU control sections in microprocessors, minicomputers, and mainframes are microcode and hard-wired logic. Each method has its advantages, and both are natural applications for programmable hardware devices.

Architectural Description

I'll start by giving the specifications for a simple computer architecture, then walk through the implementation of this architecture using both microcoded and hard-wired design strategies. While both approaches require the same description and specification groundwork, they use different schemes to generate control signals.

I will examine the CPU architecture of Toy, a fictitious computer designed especially for this article. The CPU has an accumulator (ACC), an arithmetic logic unit (ALU), an instruction register (IR), a program counter (PC), some random-access memory (RAM), and some control logic. Figure 1 is a block diagram of the Toy architecture. All data paths are 16 bits wide with 12-bit memory-address paths. You can directly implement the ALU, ACC, IR, PC, multiplexer, and RAM sections of Toy using commonly available chips. Toy's control-logic section will require detailed design and the use of customized hardware or a large number of combinatorial logic gates.

The Toy instruction format shown in figure 2 consists of a 4-bit op code and a 12-bit address field. The 16 implemented op codes are shown in table 1. Op codes 8 through 15 do not make use of the instruction's address field.

Since Toy is a single-accumulator machine, the instructions ADD, SUB, AND, OR, and XOR combine the contents of a memory location with the accumulator and return the result to the accumulator. The instructions STORE and LOAD transfer the accumulator to and from RAM. The instructions NOT, INC, DEC, and ZERO operate on the accumulator alone. While JMPZ is the only branching instruction, you can program an unconditional branch by following ZERO with a JMPZ. Finally, the four unused op codes act as null operations (NOPs) to eliminate the annoyance of dealing with illegal op codes.

Control Logic

The control-logic section translates the op-code bit patterns into CPU-control and timing signals. Figure 1 shows the op-code inputs to the control-logic unit and the control-signal outputs required to run the rest of the CPU. The signals ALU0 through ALUCIN control the ALU. (I based the bit assignments on those for the 74181 ALU chip. See *The TTL Data Book*, listed in the Bibliography.) If ALUMODE is a 1, then the ALU will perform a logical operation; if it's a 0, the ALU will perform an arithmetic operation. ALU0 through ALU3 control which arithmetic or logic operation the ALU is performing. ALUCIN acts as the carry-in for the ALU.

When the signal CLOCK[ACC] is a 1, the ACC register is loaded with the value of its inputs at the rising edge of the system clock. This is usually referred to as "clocking in" the contents of the ACC. When the signal CLOCK[IR] is a 1, the contents of the IR are clocked in from the RAM output. This is the mechanism used to decode the next op code. When ADDR=IR is a 1, the RAM address multiplexer places the contents of the IR address field onto the RAM address bus. When it is a 0, the PC is used to address RAM. I use the descriptor ADDR=PC to mean ADDR=IR is 0. When CLOCK[PC] is a 1 and the ACC is 0, the PC is loaded from the IR address field. When INC[PC] is a 1, the program counter is incremented by 1 at the end of the current clock cycle. When WRITE[RAM] is a 1, the RAM cell addressed by the RAM address bus is loaded with the output of the ALU; when this signal is a 0, the ALU is driven from the output of RAM.

Functional Specifications

Now for the heart of how the Toy instruction set is implemented. In the Toy CPU, all instructions can be executed in just one or two clock cycles. Table 2 shows the actions required to complete each op code's function. Those actions in table 2 that are

continued

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not the control signals shown in figure 1 are macros for the ALU control bits whose value is given in table 3. Let's examine some representative op codes in detail.

The STORE op code stores the contents of ACC into RAM. For the first cycle of this instruction, the low 12 bits of the IR address RAM. The ALU routes the ACC contents through without modification, then writes them out to RAM.

STORE requires two clock cycles since RAM is being used for accessing a data value during the first clock cycle. The second clock cycle is the same for all two-cycle instructions; it is simply a decoding of the next op code.

The contents of the RAM address pointed to by the PC are put onto the RAM address bus to fetch the op code. They are then clocked into the IR, and

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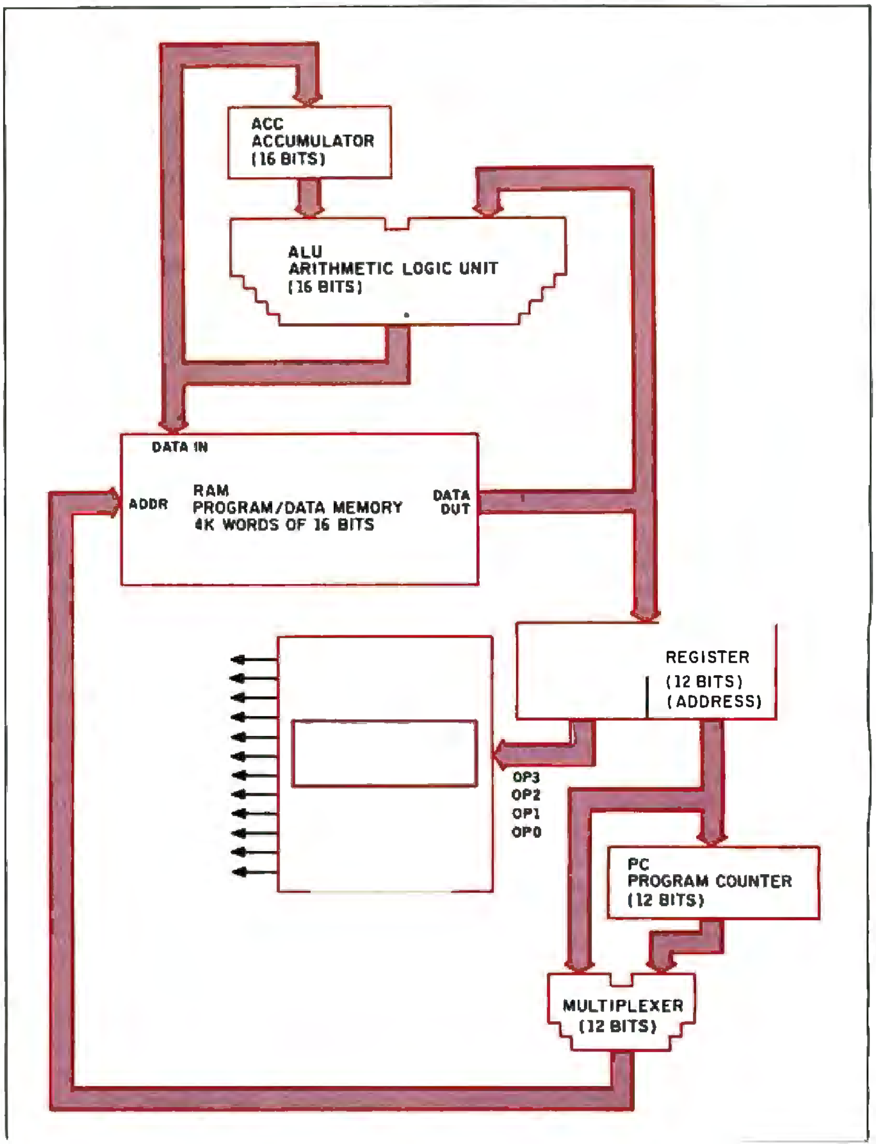


Figure 1: *Toy architecture block diagram.*

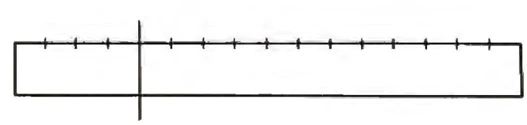


Figure 2: *Toy instruction set format.*

CONTROL LOGIC

Table 1: *Toy instruction set.*

Op code	Operation	Description
0	STORE	store accumulator in RAM at address
1	LOAD	load ACC from RAM at address
2	JMPZ	jump to address if ACC is zero
3	ADD	add RAM to ACC
4	SUB	subtract RAM from ACC
5	OR	logical OR RAM into ACC
6	AND	logical AND RAM into ACC
7	XOR	logical XOR RAM into ACC
8	NOT	logical one's complement into ACC
9	INC	add 1 to ACC
10	DEC	subtract 1 from ACC
11	ZERO	place 0 in ACC
12	NOP	null operation — unused op code
13	NOP	null operation — unused op code
14	NOP	null operation — unused op code
15	NOP	null operation — unused op code

Table 2: *Toy functional specification. Note that ADDR=PC is equivalent to the ADDR=IR signal being 0. Also, I have used descriptive macro names for the ALU control bits (see table 3).*

Op code	Operation	Cycle	Specification
0	STORE	1	ADDR=IR ; ALU=ACC ; WRITE[RAM]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
1	LOAD	1	ADDR=IR ; ALU=RAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
2	JMPZ	1	CLOCK[PC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
3	ADD	1	ADDR=IR ; ALU=ACC+RAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
4	SUB	1	ADDR=IR ; ALU=ACC–RAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
5	OR	1	ADDR=IR ; ALU=ACCorRAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
6	AND	1	ADDR=IR ; ALU=ACCandRAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
7	XOR	1	ADDR=IR ; ALU=ACCxorRAM ; CLOCK[ACC]
		2	ADDR=PC ; CLOCK[IR] ; INC[PC]
8	NOTA	1	ALU=notACC ; CLOCK[ACC] ; ADDR=PC ; CLOCK[IR] ; INC[PC]
9	INCA	1	ALU=ACC+1 ; CLOCK[ACC] ; ADDR=PC ; CLOCK[IR] ; INC[PC]
10	DECA	1	ALU=ACC–1 ; CLOCK[ACC] ; ADDR=PC ; CLOCK[IR] ; INC[PC]
11	ZERO	1	ALU=0 ; CLOCK[ACC] ; ADDR=PC ; CLOCK[IR] ; INC[PC]
12–15	NOP	1	ADDR=PC ; CLOCK[IR] ; INC[PC]

finally the PC is incremented so that it is pointing to the next op code.

JMPZ accomplishes a conditional branch by loading the contents of the PC with the address in the IR. For this to be a conditional branch, the control signal to the PC loader must be ANDed with a signal that is only true if all the bits of the ACC are 0. Since the PC is loaded with the new instruction address at the end of the first clock cycle, the second cycle is a normal decoding instruction for this new address, identical to the second cycle of STORE.

The single-clock-cycle instructions, such as NOTA, do not require a RAM access for an operand. This means that the usual second-cycle decoding sequence can occur during the same clock cycle as the ALU operation that modifies the ACC contents. In the case of NOTA, the RAM input to the ALU is ignored while the ALU computes the one's complement (logical inverse) of the current ACC contents.

Table 3: *Macros for the ALU control bits (based on bit assignments in the 74181 ALU chip).*

Macro	ALU0	ALU1	ALU2	ALU3	ALUMODE	ALUCIN
ALU = ACC	1	1	1	1	1	x
ALU = RAM	0	1	0	1	1	x
ALU = ACC + RAM	1	0	0	1	0	0
ALU = ACC − RAM	0	1	1	0	0	1
ALU = ACC OR RAM	0	1	1	1	1	x
ALU = ACC AND RAM	1	1	0	1	1	x
ALU = ACC XOR RAM	0	1	1	0	1	x
ALU = NOT ACC	0	0	0	0	1	x
ALU = ACC + 1	0	0	0	0	0	1
ALU = ACC − 1	1	1	1	1	0	0
ALU = 0	1	1	0	0	1	x

Table 4: *Control signal value specification.*

Values for first clock cycle of each instruction

Control signal	Op code 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ALU0	1	0	x	1	0	0	1	0	0	0	1	1	x	x	x	x
ALU1	1	1	x	0	1	1	1	1	0	0	1	1	x	x	x	x
ALU2	1	0	x	0	1	1	0	1	0	0	1	0	x	x	x	x
ALU3	1	1	x	1	0	1	1	0	0	0	1	0	x	x	x	x
ALUMODE	1	1	x	0	0	1	1	1	1	0	0	1	x	x	x	x
ALUCIN	x	x	x	0	1	x	x	x	x	1	0	x	x	x	x	x
CLOCK[ACC]	0	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0
CLOCK[IR]	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
ADDR = IR	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
CLOCK[PC]	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
INC[PC]	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
WRITE[RAM]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Values for second clock cycle of each instruction

Control signal	Op code 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ALU0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ALU1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ALU2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ALU3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ALUMODE	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ALUCIN	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
CLOCK[ACC]	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
CLOCK[IR]	1	1	1	1	1	1	1	1	x	x	x	x	x	x	x	x
ADDR = IR	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
CLOCK[PC]	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
INC[PC]	1	1	1	1	1	1	1	1	x	x	x	x	x	x	x	x
WRITE[RAM]	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Control-Logic Outputs

Table 4 gives a complete listing of all the control-logic output values that you need to specify the Toy functional description. Each X corresponds to a signal whose value does not matter, either because the controlled resource is unused (as in the ALU signals for op code 2) or because the second clock cycle is unused for op codes 8 to 15. These "don't-care" signals become crucial when you are designing hard-wired control circuitry.

Hard-wired Control

A CPU designed with hard-wired control uses random logic such as AND, OR, and NOT gates and either flip-flops or counters to decode each op code and control the processing flow. The hard-wired design process usually consists of identifying all the states needed to implement the instruction set, then deriving the Boolean logic equations required to control the computer's resources for each step.

Figure 3 shows the hard-wired implementation of the functional specifications given in table 4. It requires a controller with two states: first clock cycle and second clock cycle. The flip-flop in figure 3 is forced to the CLOCK1 state whenever a new instruction is clocked into the IR and changes to the CLOCK2 state whenever the IR is not clocked.

The most tedious part of a hard-wired control design is creating the logic gate networks to decode instructions into control signals. I have derived the required logic equations shown in figure 4 from the functional specifications in table 4. Figure 5 shows the Karnaugh map for deriving the first equation (ALU0) in figure 4. (See W. Fletcher's *An Engineering Approach to Digital Design* [Prentice-Hall, 1980] for a discussion of Karnaugh maps.)

The don't-care conditions are vital in reducing the complexity of the gate networks, since they allow freedom to ignore some op-code bits or state bits to minimize decoding logic. A good example of a don't-care condition is the ALU control signals; they do not depend on whether the controller is currently in the CLOCK1 or CLOCK2 mode.

continued

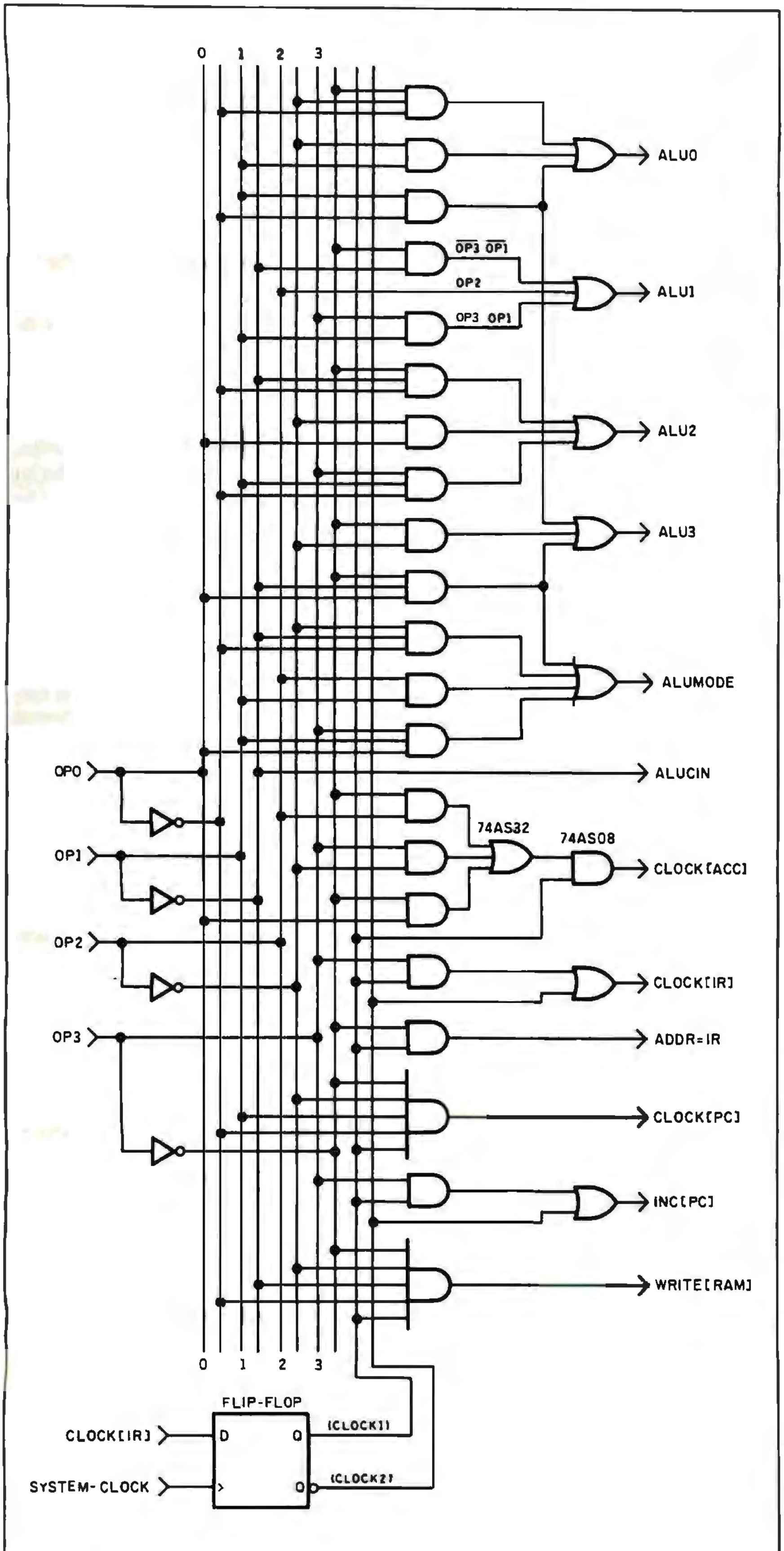


Figure 3: *Hard-wired controller schematic. Note that none of the ALU signals depend on whether the controller is in the CLOCK1 or CLOCK2 mode.*

$$\text{ALU0} = \overline{\text{OP3}}\ \overline{\text{OP2}}\ \overline{\text{OP0}} + \overline{\text{OP2}}\ \text{OP1} + \text{OP1}\ \overline{\text{OP0}}$$

$$\text{ALU1} = \overline{\text{OP3}}\ \overline{\text{OP1}} + \text{OP2} + \text{OP3}\ \text{OP1}$$

$$\text{ALU2} = \overline{\text{OP3}}\ \overline{\text{OP1}}\ \overline{\text{OP0}} + \text{OP2}\ \text{OP0} + \text{OP3}\ \text{OP1}\ \overline{\text{OP0}}$$

$$\text{ALU3} = \overline{\text{OP3}}\ \overline{\text{OP2}} + \overline{\text{OP3}}\ \overline{\text{OP1}}\ \text{OP0} + \text{OP1}\ \overline{\text{OP0}}$$

$$\text{ALUMODE} = \overline{\text{OP2}}\ \overline{\text{OP1}}\ \overline{\text{OP0}} + \overline{\text{OP3}}\ \overline{\text{OP1}}\ \text{OP0} + \text{OP2}\ \text{OP1} + \text{OP3}\ \text{OP1}\ \text{OP0}$$

$$\text{ALUCIN} = \overline{\text{OP1}}$$

$$\text{CLOCK[ACC]} = (\text{OP3}\ \overline{\text{OP2}} + \overline{\text{OP3}}\ \text{OP2} + \overline{\text{OP3}}\ \text{OP0})\ \text{CLOCK1}$$

$$\text{CLOCK[IR]} = \text{OP3}\ \text{CLOCK1} + \text{CLOCK2}$$

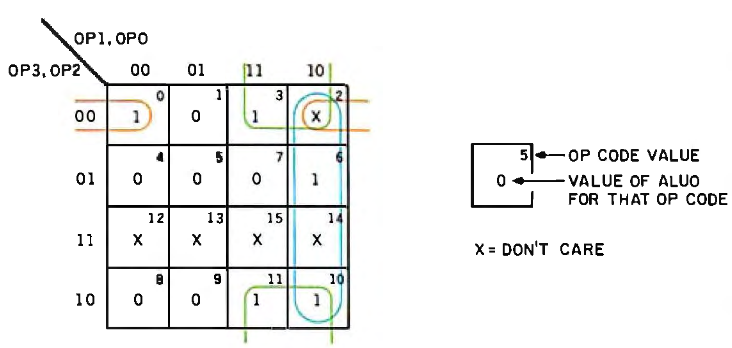
$$\text{ADDR=IR} = \overline{\text{OP3}}\ \text{CLOCK1}$$

$$\text{CLOCK[PC]} = \overline{\text{OP3}}\ \overline{\text{OP2}}\ \text{OP1}\ \overline{\text{OP0}}\ \text{CLOCK1}$$

$$\text{INC[PC]} = \text{OP3}\ \text{CLOCK1} + \text{CLOCK2}$$

$$\text{WRITE[RAM]} = \overline{\text{OP3}}\ \overline{\text{OP2}}\ \overline{\text{OP1}}\ \overline{\text{OP0}}\ \text{CLOCK1}$$

Figure 4: *Logic equations for Toy's hard-wired implementation.*



	OP CODE NUMBERS	CORRESPONDING BIT VALUES	EQUATION
REGION	: 2, 6, 10, 14	OP1 = 1, OP0 = 0	$\text{OP1} \cdot \overline{\text{OP0}}$
REGION	: 2, 3, 10, 11	OP2 = 0, OP1 = 1	$\overline{\text{OP2}} \cdot \text{OP1}$
REGION	: 0, 2	OP3 = 0, OP2 = 0, OP0 = 0	$\overline{\text{OP3}} \cdot \overline{\text{OP2}} \cdot \overline{\text{OP0}}$

$$\text{ALUO} = \overline{\text{OP3}} \cdot \overline{\text{OP2}} \cdot \overline{\text{OP0}} + \overline{\text{OP2}} \cdot \text{OP1} + \text{OP1}\ \overline{\text{OP0}}$$

Figure 5: *To show how the Boolean equations in figure 4 were derived from table 4, here is the Karnaugh map used to minimize the ALUO Boolean equation. The Xs are the don't-care bits, and the number in the upper right corner of each box is the op code.*

To implement the hard-wired controller, the complementary outputs of the CLOCK1/CLOCK2 flip-flop and the inputs from the current op code in the IR are fed throughout the system by the lines at the left of figure 3. These inputs are then fed through logic-gate combinations specified by the equations in figure 4. You can implement these logic-gate combinations with TTL logic gates or, if you want to save board space, program them into hardware, such as a PAL.

As an example of how these decoding gates work, consider the generation of the signal INC[PC]. The INC[PC] signal should be a 1 for op codes 8 to 15 on the first clock cycle and for op codes 0 to 7 on the second clock cycle. But, since op codes 8 to 15 are all single-cycle op codes, any signals generated from them during the second cycle can be ignored. This gives the result that INC[PC] can be 1 for all op codes during the second cycle. The logic for INC[PC] then becomes the AND of the highest op-code bit (OP3) and CLOCK1, with the result ORed with CLOCK2.

Because the time required for a signal to pass through a simple logic gate is only a few nanoseconds with most current technologies, hard-wired control can provide the fastest possible decoding of machine language instructions. It also is the most flexible design method for specifying unique and complex control flows within a CPU because the designer can specify any decoding gate combinations and any control-flow hardware.

One drawback to using hard-wired control methodology is that it requires a considerable amount of Boolean algebra manipulation. Another drawback is that the CPU must be completely and correctly specified before you design a hard-wired control unit.

Any additions or modifications to the specification can require a major redesign of the control unit. If you want a feel for the impact a design change can have on a hard-wired controller, try redoing the logic equations with two op codes switched, such as op codes 5 and 9, or with op code 15 defined as a two-cycle logical NAND instruction.

Microcoded Control

Microcoded design differs from hard-wired design in that the control-logic gates are replaced by a memory array (usually a ROM) to generate the required control-logic signals. While ROMs are slower than random logic within the same price and performance categories, using a ROM simplifies the design process and significantly reduces time and costs for implementing a CPU control circuit.

Figure 6 shows the schematic for a

microcoded control circuit for Toy. The op code and a flip-flop similar to the one used in the hard-wired controller are fed in as an address to the microprogram ROM. The outputs of the ROM directly drive the control signals for the CPU. Each ROM location contains the proper bit settings to control a single clock cycle of an op code's execution, as shown in figure 7.

The control signals for the first cycle of each op code are placed in the even memory addresses (which are addressed when the flip-flop in the controller outputs a 0 for the first clock cycle), and the second cycle op codes are placed in odd memory addresses. I have arbitrarily assigned the value 0 to all don't-care bits from table 4 and copied the rest of the bits directly from table 4 to figure 7.

The main advantage to microcoded control is that it lets the designer change the CPU's functional description by changing the bits in any ROM address without having to redesign the machine's logic-decoding gate structure. Microcoded machine design also lends itself to simply structured, low-component-count computers such as those built using bit-slice technology. Most modern microproces-

continued

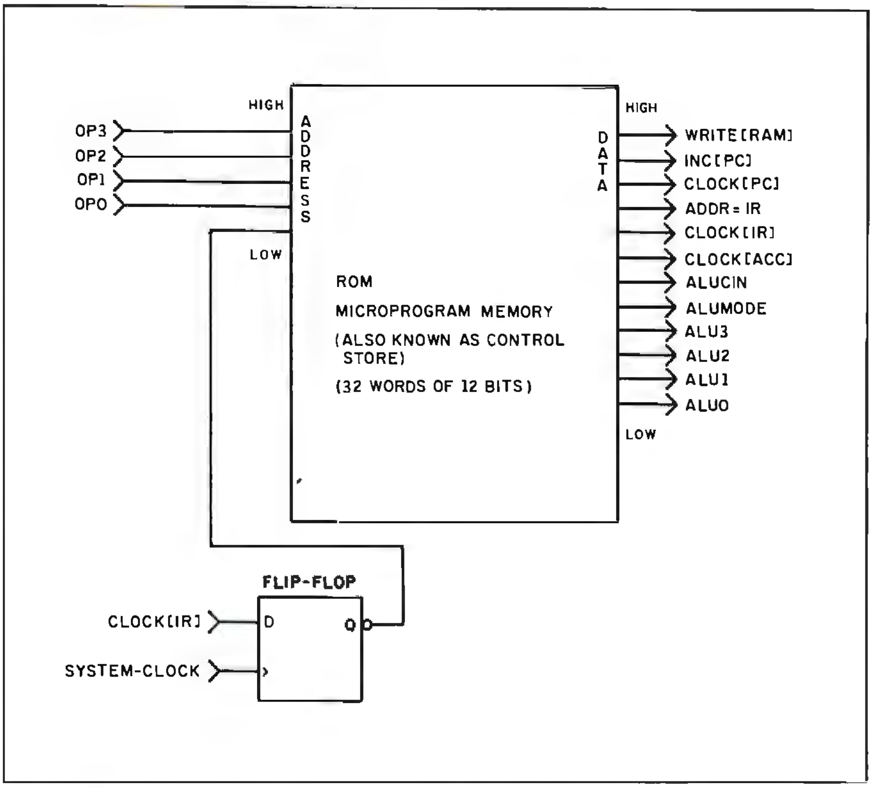
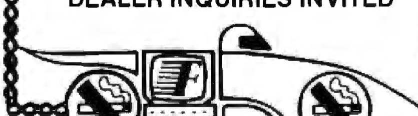


Figure 6: *Microcoded controller schematic.*



OP CODE	ROM ADDRESS	WRITE[RAM]	INC[PC]	CLOCK[PC]	ADDR=IR	CLOCK[IR]	CLOCK[ACC]	ALUCIN	ALUMODE	ALU3	ALU2	ALU1	ALU0
0	0	1	0	0	1	0	0	0	1	1	1	1	1
	1	0	1	0	0	1	0	0	0	0	0	0	0
1	2	0	0	0	1	0	1	0	1	1	0	1	0
	3	0	1	0	0	1	0	0	0	0	0	0	0
2	4	0	0	1	1	0	0	0	0	0	0	0	0
	5	0	1	0	0	1	0	0	0	0	0	0	0
3	6	0	0	0	1	0	1	0	0	1	0	0	1
	7	0	1	0	0	1	0	0	0	0	0	0	0
4	8	0	0	0	1	0	1	1	0	0	1	1	0
	9	0	1	0	0	1	0	0	0	0	0	0	0
5	10	0	0	0	1	0	1	0	1	1	1	1	0
	11	0	1	0	0	1	0	0	0	0	0	0	0
6	12	0	0	0	1	0	1	0	1	1	0	1	1
	13	0	1	0	0	1	0	0	0	0	0	0	0
7	14	0	0	0	1	0	1	0	1	0	1	1	0
	15	0	1	0	0	1	0	0	0	0	0	0	0
8	16	0	1	0	0	1	1	0	1	0	0	0	0
	17	0	0	0	0	0	0	0	0	0	0	0	0
9	18	0	1	0	0	1	1	1	0	0	0	0	0
	19	0	0	0	0	0	0	0	0	0	0	0	0
10	20	0	1	0	0	1	1	0	0	1	1	1	1
	21	0	0	0	0	0	0	0	0	0	0	0	0
11	22	0	1	0	0	1	1	0	1	0	0	1	1
	23	0	0	0	0	0	0	0	0	0	0	0	0
12	24	0	1	0	0	1	0	0	0	0	0	0	0
	25	0	0	0	0	0	0	0	0	0	0	0	0
13	26	0	1	0	0	1	0	0	0	0	0	0	0
	27	0	0	0	0	0	0	0	0	0	0	0	0
14	28	0	1	0	0	1	0	0	0	0	0	0	0
	29	0	0	0	0	0	0	0	0	0	0	0	0
15	30	0	1	0	0	1	0	0	0	0	0	0	0
	31	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7: *Contents of ROM for the microcode.*

sors and large computers use microcoded design techniques because the design costs associated with hard-wired control are too high.

In some cases, a computer will use RAM instead of ROM for its microcoded memory, providing a "writable control store." A sophisticated programmer can use this to modify and extend the machine's instruction set for special applications. By using multiple sets of ROM or RAM within a machine, the programmer can make a computer emulate more than one machine-code instruction set for different computing environments.

The method of microcoding I used in Toy is called horizontal microcoding, since each bit of the ROM directly feeds a control line for the CPU. A hybrid design method known as vertical microcoding compacts some control signals together to save ROM bits. It then uses decoding logic much like that used by the hard-wired approach to regenerate the signals.

In general, hard-wired control is used for computer designs that are simple or that require fast execution speeds, while microcoded control is used in complex computer designs to keep design costs low. Both design methods can implement CPUs that are much more complex than the Toy architecture. ■

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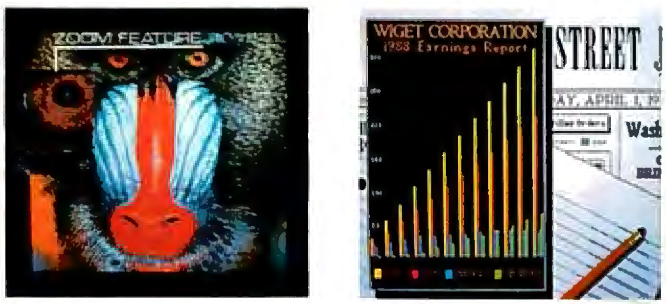

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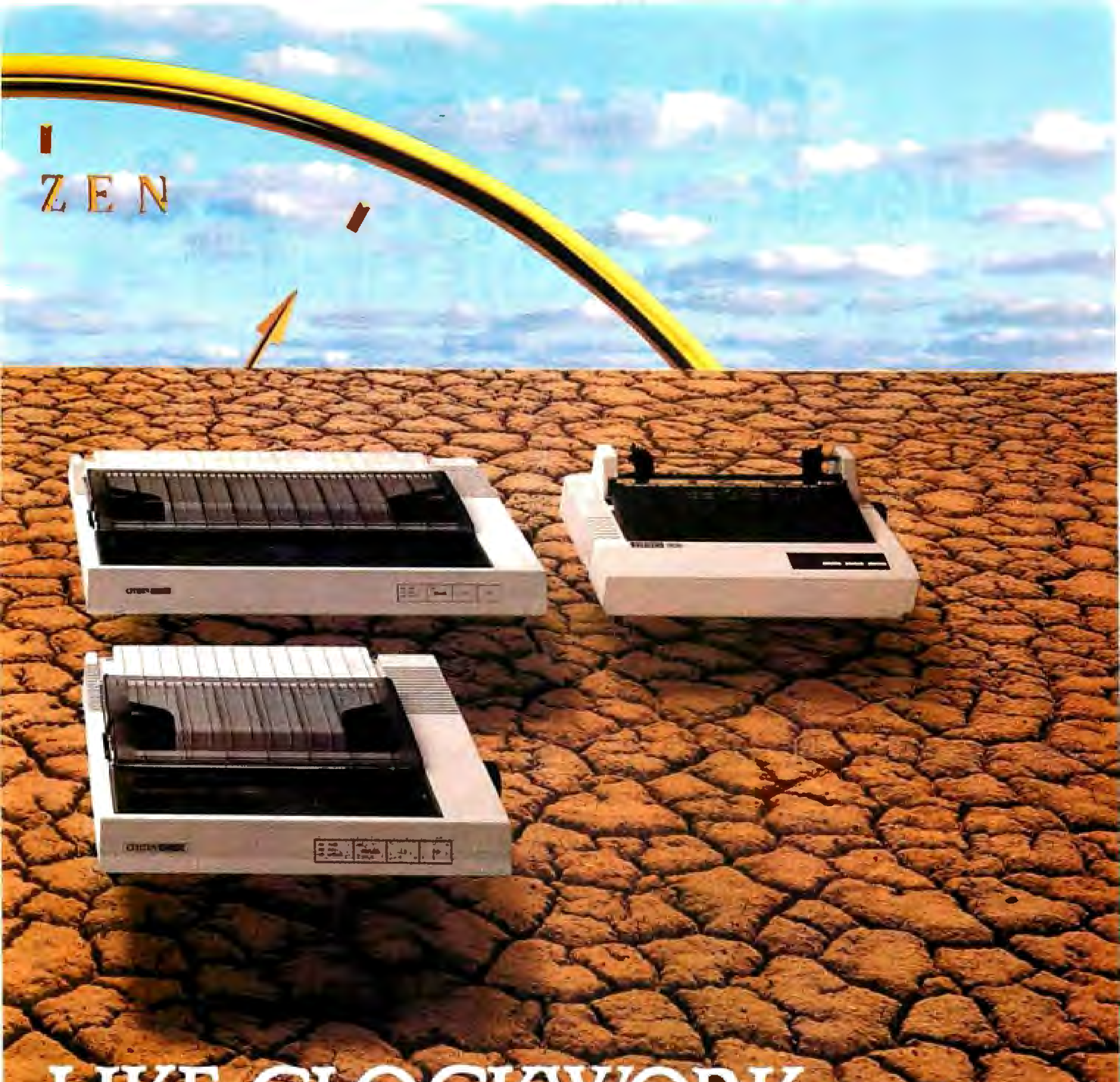
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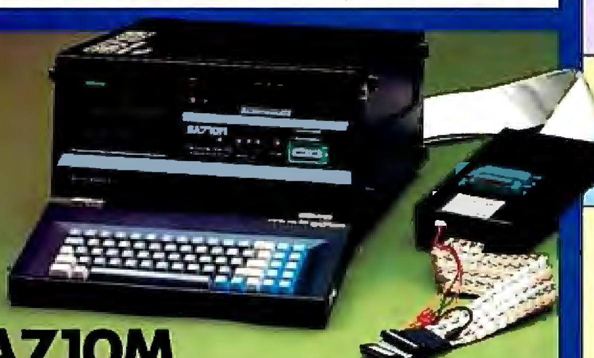

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Trevor G. Marshall

THE PAL (programmable array logic) is not some recent, gee-whiz technology. You'll find PALs on your personal computer motherboard and in almost every other personal computer peripheral you examine. They sneaked into hundreds of designs while you weren't looking.

I remember yawning when, in 1980, John Birkner (the father of the PAL) showed me how to turn an ordinary-looking 20-pin DIP into an equally ordinary-looking DIP that supposedly, after programming, would contain six fundamental basic gates. "So what?" I said. "I know all about 74LS00-series gates and what I can do with them. Why should I want to create six different gates inside a DIP and pay 20 times the price of an LS00 for it?"

Four years passed before I realized what a mistake I had made. The PAL is a software element, not a hardware device. It allows designers to alter the topology of their logic designs even after the circuit boards have been fabricated. With PALs you can commit to production much earlier in the design cycle because an algorithmic change can solve any design or debug problems that might arise.

Without PALs, the DSI-32 (see "The DSI-32 Coprocessor Board," August and September 1985 BYTE) and the DSI-020 (see "The Definicon 68020 Coprocessor," July and August 1986 BYTE) coprocessor boards would never have been possible. Some of the eight PALs on the DSI-32 went through dozens of design iterations before the final product was shipped. The PALs were reprogrammed to correct deficiencies in the CPU and memory management unit, incompatibilities with some of the host personal computers, and errors in the basic design.

So much for history. I want to look at how PALs can help you implement your latest design and at how easy they are to use. I will focus on the commodity PALs, particularly the 16L8 and 16R4 types. These are inexpensive, typically costing less than $2 in production quantities. They are, however, adequately powerful to act as a training ground for a budding designer and to implement most synchronous or asynchronous logic designs. They are available with as little as 10-nanosecond maximum propagation delay, and you can program them with low-cost hardware. Manufacturers include Monolithic Memories, Texas Instruments, National Semiconductor, and Advanced Micro Devices.

Combinatorial PALs

Figure 1 shows the logic for a combinatorial cell from the 16L8. The hardware consists first of a grid of fuses that feed into AND gates followed by an OR gate, then a tristate inverter with a feedback term. Not all the elements have exactly the same topology, but they are similar. [Editor's note: *For more discussion of the architecture of the 16L8, see Vincent J. Coli's "Introduction to Programmable Array Logic" page 207.*]

A simple example illustrates the 16L8's software structure. I have used the syntax of the PALASM version 1 development software. (Monolithic Memories put this software into the public domain.) I'll name the 10 inputs A, B, C, D, E, F, G, H, I, and J (active high) and the output /O1 (active low). Note that the outputs are always inverted from the inputs in the 16L8 due to the inverter between the OR gate and the output. This inversion is denoted with the slash. So /O1 = A means that the O1 output will contain an inverted copy of the input A. Each of the inputs can be used to control the tristate enable, so the equation IF (/B) /O1 = A means that the inverter output was tristate (disabled) until B was negated (pulled low).

An equation for this cell can be quite complex:

```
IF (/A*B*/C*D*E*/F*G*H*/I*J)/O1 =
   A*B*C*/D*/E*/F*/G*H*I*J
   + /A*/B*C*/D*/E*/F*/G*H*I*J
   + A*/B*C*/D*E*/F*/G*H*I*J
   + A*B*/C*/D*/E*/F*/G*H*I*J
   + A*B*/C*D*/E*/F*/G*H*I*J
   + A*B*C*/D*E*F*G*H*I*J
   + /A*B*C*D*/E*F*G*H*/I*J
```

Note that the symbol * means logical

continued

Trevor G. Marshall has published over 50 papers in fields ranging from electronic music to biomedical engineering. He is director of engineering at Definicon Systems and can be contacted via modem at the Thousand Oaks Technical Database at (805) 492-5472 or (805) 493-1495 or by mail at Definicon Systems Inc., 31324 Via Colinas #108/9, Westlake Village, CA 91362.

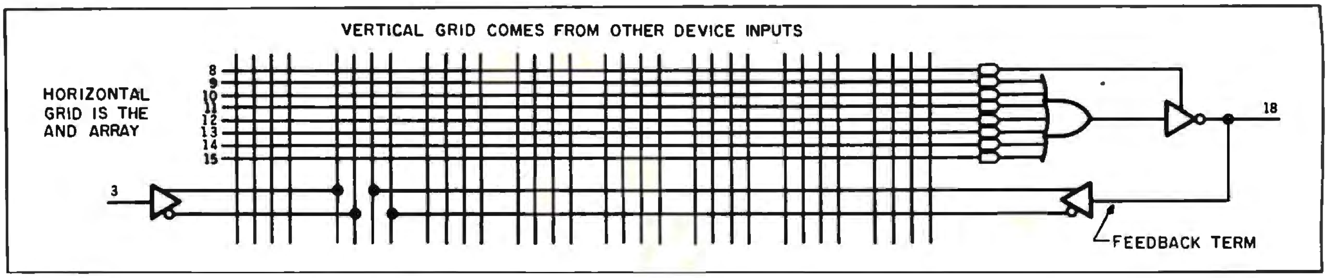

Figure 1: *A logic cell from a 16L8 PAL. Notice the inverter between the OR gate and the output.*

AND; the symbol + means logical OR.

At this point, I have used up the horizontal AND array for the tristate term and the seven OR terms for the actual output. I still have not used the feedback terms from /O1 and the other device outputs. They can be used in the tristate control term or in the actual logic equations.

In summary, this is the *software* structure of the combinational PALs:

```
IF (TRISTATE TERMS) OUTPUT =
        INPUT TERMS
    + MORE INPUT TERMS
```

Any input can be used true or inverted. The inputs most easily form AND associations. OR associations of many AND subsets yield the device's remaining flexibility.

A Basic Example

The DPORT20 PAL from the DSI-020 design is a simple example. Figure 2 shows the portion of the schematic containing this PAL and its associated counter. The DPORT20 PAL implements a simple DMA controller. After arbitration, this PAL takes control of the bus from the 68020 CPU and produces signals that, to the peripherals, appear identical to those the 68020 would have generated. Thus, the host PC can access the RAM, DUART, etc., using this PAL as the timing controller.

The 74F161A counter is normally held reset until the hold acknowledge 8086 (HLDA86) becomes true. At this time it begins counting to start the DMA cycle. The clock signal for the 74F161A comes from a 25- or 40-MHz oscillator, depending on whether you are using a 12.5- or 20-MHz 68020. As shown in figure 3, each output sequences within 1 to 2 nanoseconds of each other, yielding a synchronized binary count to the PAL's inputs.

Initially, I'll concentrate on generating the AS (address strobe) signal. AS must go true between counts 2 and 9 inclusive (figure 3). In addition, as this signal is normally generated by the 68020, the output pin can be driven only during the DMA cycle. Since the 16L8 has a built-in inverter on each output, the AS signal is active low, meaning it will go low when it's true. This is denoted by a slash (/) before the AS symbol in the pin list. In text and equations, I will deal with AS, as well as the other active-low designators, as an active-high designator. The PALASM software knows from the pin list whether a designator is actually active low and handles the inversion automatically. This saves you from having to think in negative logic. Listing 1 shows the pin list and equation defining the AS signal.

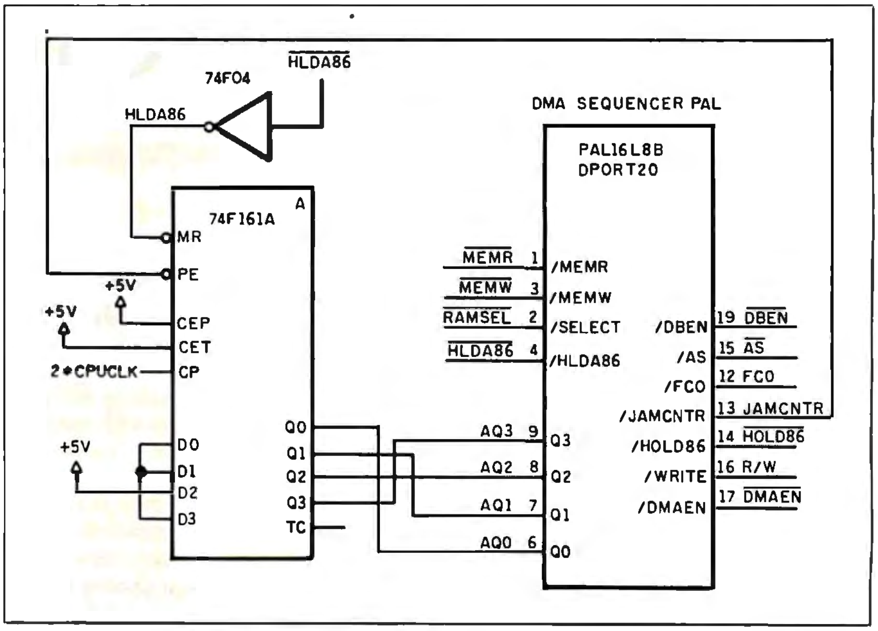

Figure 2: *The DPORT20 portion of the DSI-020 schematic.*

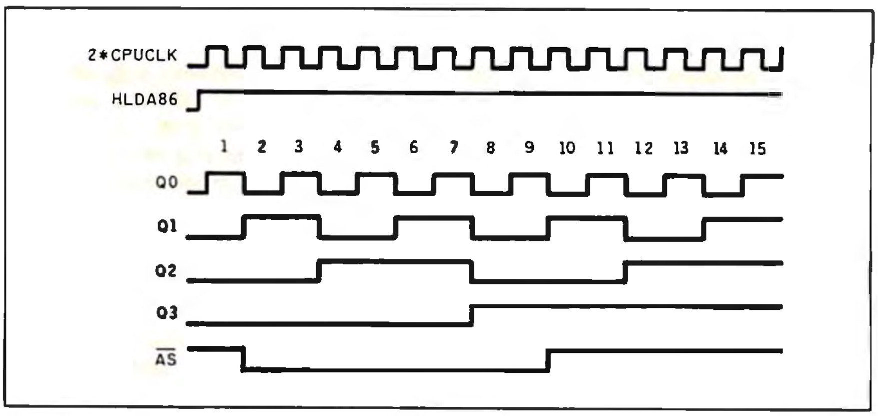

Figure 3: *Timing diagrams for the DPORT20.*

A 16L8 PAL has 20 pins. Pins 1 to 10 are named on the first line, pins 11 to 20 on the second. The symbol NC means no connection; this pin is not used. You should always leave some unconnected inputs and outputs in your PAL designs.

continued

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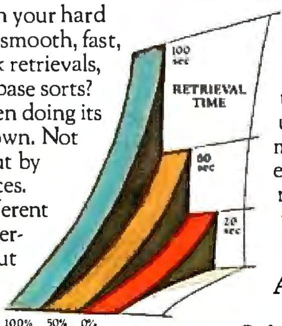

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They will be useful during debugging. The order in which you allocate the pins does not matter.

It is often convenient to reallocate the pins after you have begun routing of the circuit-board traces. Swapping PAL pins can significantly ease the routing task. On the 16L8, six of the pins are I/O pins that you can use as inputs instead of outputs. Be careful, however: Pins 12 and 19 are dedicated outputs and also have no feedback term.

Listing 1: *PALASM pin list and equation defining the AS signal for the DPORT20 PAL of the DSI-020 board.*

```
/MEMR /SELECT /MEMW /HLDA86 NC Q0 Q1 Q2 Q3 GND
NC /FC0 /JAMCNTR /HOLD86 /AS /WRITE /DMAEN NC /DBEN VCC

IF (HLDA86) AS = /Q3*/Q2*Q1*/Q0 ; 0010 is count=2
  + /Q3*/Q2*Q1*Q0               ; 0011 is count=3
  + /Q3*Q2*/Q1*/Q0              ; 0100 is count=4
  + /Q3*Q2*/Q1*Q0               ; 0101 is count=5
  + /Q3*Q2*Q1*/Q0               ; 0110 is count=6
  + /Q3*Q2*Q1*Q0                ; 0111 is count=7
  + Q3*/Q2*/Q1*/Q0              ; 1000 is count=8
  + Q3*/Q2*/Q1*Q0               ; 1001 is count=9
```

```
MONOLITHIC MEMORIES 20-PIN PALASM (tm) VERSION 1.7F
(C) COPYRIGHT 1983,1984 MONOLITHIC MEMORIES
PROGRAM LIMITS: 250 LINES 9999 CHARACTERS 150 VECTORS
WHAT IS THE SOURCE FILENAME (d:filename.ext) ?: testas1.pal
OUTPUT FILENAME - PRESS <ENTER> FOR NO OUTPUT FILE ?:
READING INPUT FILE

............
PAL DESIGN FILE READ - 12 LINES 656 CHARS
ASSEMBLING INPUT FILE

.OUTPUT PIN NAME =  AS OUTPUT PIN NUMBER = 15
MINTERM IN LINE NUMBER 16
      + Q3 * /Q2 * /Q1 * Q0 ; 1001 IS COUNT=9
MAXIMUM OF 8 PRODUCT LINES ARE VALID FOR PAL16L8
 TOO MANY MINTERMS ARE SPECIFIED IN THIS EQUATION
```

Figure 4: *The file of listing 1 contains too many product terms to fit in a cell of a 16L8. PALASM flags this as an error.*

```
FUNCTION TABLE
Q3 Q2 Q1 Q0 /HLDA86 /AS  ;Pins to be tested, in this order
-----------------------------------------------------------
XXXX H Z  ;Check that the ouput goes tristate
LLLL L H  ;not asserted for 0
LLLH L H  ;or for 1
LLHL L L  ;but true from count of 2
LLHH L L  ;through
LHLL L L
LHLH L L
LHHL L L
LHHH L L
HLLL L L
HLLH L L  ;9
HLHL L H  ;deasserted at 10
HLHH L H  ;and should not come back
HHLL L H  ;through
HHLH L H
HHHL L H
HHHH L H  ;15
-----------------------------------------------------------
```

Figure 5a: *Function table for the DPORT20 PAL.*

The signals generated by the DPORT20 PAL of interest to this discussion are Q0, Q1, Q2, Q3, HLDA86, and AS. From the equation in listing 1, the AS output will be true during counts 2 through 9. To check this equation, I'll add a header and run listing 1 through the PALASM assembler as file TESTAS1.PAL. The assembler output in figure 4 shows a fatal error.

As I pointed out earlier, this cell of the 16L8 has a maximum of eight product lines (including the tristate control), and I have used nine. At this point, the theoreticians start mumbling magic words like "Karnaugh map" and "set theory," but you and I know the world isn't that complex. Look at the first two lines:

```
/Q3*/Q2*Q1*/Q0 ; count 2
 + /Q3*/Q2*Q1*Q0 ; count 3
```

What I am trying to say here is that if *either* Q0=0 (line 1) *or* Q0=1 (line 2), then, provided /Q3 *and* /Q2 *and* Q1 are true, the output should be true. Q0 is a "don't-care" factor and can be eliminated:

```
/Q3*/Q2*Q1 ; counts 2,3,            (1)
```

Similarly, lines 3 and 4 become

```
 + /Q3*Q2*/Q1 ; counts 4,5,         (2)
```

Lines 5 and 6 become

```
 + /Q3*Q2*Q1 ; counts 6,7,          (3)
```

Lines 6 and 7 become

```
 + Q3*/Q2*/Q1 ; counts 8,9,         (4)
```

Similarly, merging the new terms 1 and 3 results in

```
/Q3*Q1 ; counts 2,3,6,7
```

Thus, I can write

```
IF (HLDA86) AS =
   /Q3*Q1 ; counts 2,3,6,7
    + /Q3*Q2*/Q1 ; counts 4,5
    + Q3*/Q2*/Q1 ; counts 8,9
```

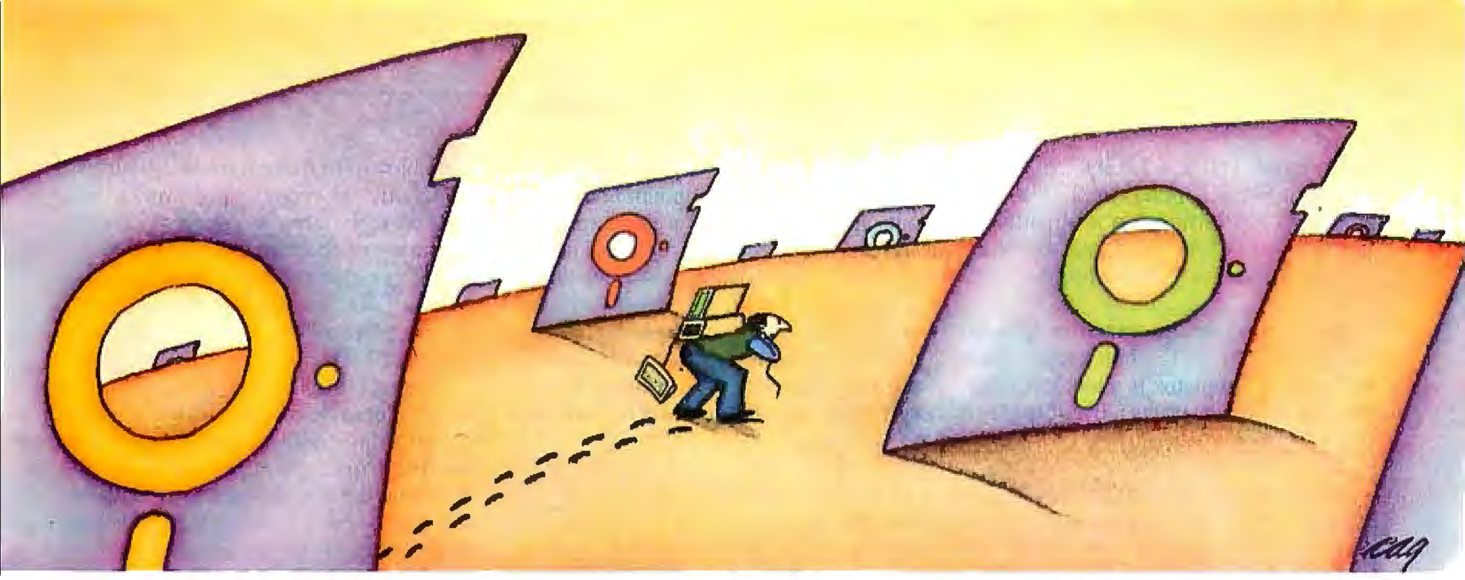
This time PALASM is happy and I now have four terms spare for later use during the debug phase.

Logic Simulation

PALASM software contains a logic simulator that lets you specify a series of conditions on the input pins and what you expect the outputs to do. You must construct a function table in the following format:

X on an input means to test with both a 1 and a 0.

continued



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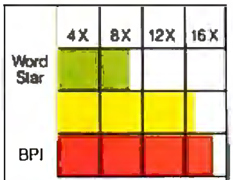

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H means TRUE, HIGH, or 1; L means FALSE, LOW, or 0.
Z means high impedance (tristate).
Dashes (signs) delineate the start and end of the test vectors.

Figure 5a shows the function table for the DPORT20 PAL. The output from PALASM's simulator is shown in figure 5b. The simulator prints a list of the logic states for all 20 pins. It places the values specified in the function table on the inputs and then checks that the outputs are correct. If it detects an error, the simulator tells you which output was in error.

Many PAL programmers use this simulation table to place voltages on the PAL pins during the test phase and ensure that the programmed part performs to your specifications. If the security fuse has been blown (to make it more difficult for somebody to copy your work), this method is the only way to verify correct operation of the programmed PAL.

```
MONOLITHIC MEMORIES 20-PIN PALASM (tm) VERSION 1.7F
(C) COPYRIGHT 1983,1984 MONOLITHIC MEMORIES
PROGRAM LIMITS: 250 LINES 9999 CHARACTERS 150 VECTORS
WHAT IS THE SOURCE FILENAME (d:filename.ext) ?: testas2.pal
OUTPUT FILENAME - PRESS <ENTER> FOR NO OUTPUT FILE ?:
READING INPUT FILE

................................
PAL DESIGN FILE READ -    32 LINES  1001 CHARS
ASSEMBLING INPUT FILE

.
E=ECHO  O=PINOUT   S=SIMULATE   F=FAULT   TESTING
P=PLOT  B=BRIEF    I=INTEL HEX  J=JEDEC   H=HEX
D=DOC   C=CATALOG  Q=QUIT
ENTER OPERATION CODE: s
DMA SEQUENCER                           ; as you see fit

   1 XXX1XXXXXXXXXXZXXXX1
   2 XXX0X0000XXXXXHXXXX1
   3 XXX0X1000XXXXXHXXXX1
   4 XXX0X0100XXXXXLXXXX1
   5 XXX0X1100XXXXXLXXXX1
   6 XXX0X0010XXXXXLXXXX1
   7 XXX0X1010XXXXXLXXXX1
   8 XXX0X0110XXXXXLXXXX1
   9 XXX0X1110XXXXXLXXXX1
  10 XXX0X0001XXXXXLXXXX1
  11 XXX0X1001XXXXXLXXXX1
  12 XXX0X0101XXXXXHXXXX1
  13 XXX0X1101XXXXXHXXXX1
  14 XXX0X0011XXXXXHXXXX1
  15 XXX0X1011XXXXXHXXXX1
  16 XXX0X0111XXXXXHXXXX1
  17 XXX0X1111XXXXXHXXXX1
PASS SIMULATION
```

Figure 5b: *Result from PALASM simulation of the AS output using the function table of figure 5a.*

```
                11 1111 1111 2222 2222 2233
 0123 4567 8901 2345 6789 0123 4567 8901

32 ---- ---- -X-- ---- ---- ---- ---- ---- HLDA86
33 ---- ---- ---- ---- ---- X--- ---- -X-- /Q3*Q1
34 ---- ---- ---- ---- ---- -X-- X--- -X-- /Q3*Q2*/Q1
35 ---- ---- ---- ---- ---- -X-- -X-- X--- Q3*/Q2*/Q1
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

LEGEND: X : FUSE NOT BLOWN (L,N,0) - : FUSE BLOWN (H,P,1)
NUMBER OF FUSES BLOWN = 119
```

Figure 6: *Fuse plot of the AS output of the DPORT20 PAL.*

You can also ask PALASM to produce a plot of the fuse map for you. Figure 6 is the plot of the AS output of the DPORT20 PAL.

When a term has been processed, it is shown alongside the fuse array that it represents. Masochists are thus able to check that the correct fuses have been blown. Note that the four unused terms have intact fuses, and it is possible to add extra terms to a PAL by reprogramming it. If you need to change a term in which the fuses have been blown, however, you can put your old PAL in the closest trash can.

This is probably a good time to mention the new ultraviolet erasable and electrically erasable CMOS programmable logic devices. [Editor's note: *The companies that make these parts refer to them as EPLDs and EEPLDs, but the author is talking about programmable-AND/fixed-OR architecture devices.*] The main advantage of these devices is that you can reprogram them many times and so save money in a development cycle. However, they are much more expensive than the bipolar types and usually require specialized programming hardware that far exceeds the total cost of all the bipolar PALs you will ever discard.

In addition, programmable-AND/fixed-OR devices have only recently become available in even medium-speed grades. You also need to consider that the erasable parts are generally singly sourced components.

Remember that the main advantage of the bipolar commodity PALs is their speed. Two of the PALs on the DSI-020 board are B parts (16L8B, with 15-ns maximum delay), and erasable devices would not have been fast enough. When you are designing with 40-MHz clocks, the extra 10-ns delay in the EPLD and EEPLD parts becomes critical.

One other output of the DPORT20 PAL that deserves mention is the JAMCNTR output. Its function is to ensure that the counter "dead-ends" at 15 rather than sequencing through from 0 again. Its control equation is simplicity itself:

IF (VCC) JAMCNTR = Q3*Q2*Q1*Q0

The IF(VCC) is optional; it means that the output is always enabled. The reason it deserves mention is because it is an excellent example of how a PAL can help you correct design errors. The initial design of the DPORT20 controller did not dead-end the counter, and the DMA controller kept cycling round and round. A

continued

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few cut traces and assignment of this spare output fixed the problem.

Clocked or Synchronous Devices

One of the clocked cells from a 16R4 is shown in figure 7. Note that all eight OR minterms are available to the programmer since the tristate control and the clock come from dedicated pins. This is an inflexible structure, and many new PAL designs allow more programmed control of the flip-flops. Nevertheless, with ingenuity the ubiquitous 16R4, 16R6, and 16R8 are adequate for most synchronous designs.

DSI-32 HOLD PAL

The DSI-32 design uses a 16R4 to arbitrate DMA priorities. Two distinct subsystems, the dynamic RAM refresh controller and the 8086 dual-port DMA circuitry, can request the bus from the 32032. Since the 8086 requests are asynchronous with the system clock, the priority arbitration circuitry involves two levels of latching: first of the asynchronous requests, then of the arbitrated acknowledge outputs.

Figure 8 is the schematic of the HOLD PAL from the DSI-32 article. Note that the 32032 CPU clock signal, CTTL, goes into the clock pin for the flip-flops (pin 1) and also into the AND array. The HOLD86 input signals that the 8086 wants the 32032 bus, the RFIO that the refresh circuit wants it. HOLD requests the CPU to tristate the address and data buses. The 32032 asserts HLDA (hold acknowledge) to signal that the buses are free. HLDA86 is the acknowledge signal to the 8086 that it has won the bus; RFSHACK tells the refresh controller it is in control. I will discuss T1 later; POWERON and ADSO are unimportant. Listing 2 shows the PALASM file for the HOLD PAL.

Note that RFIOI and HOLD86I are two internal nodes whose outputs are not connected to the external world but merely fed back into the array. The first task is to synchronize the asynchronous input requests with the 32032 CPU clock (CTTL). This is done using the first two equations of listing 2.

The := symbol means "clock this data after the low-to-high transition of the clock." The RFIOI and HOLD86I outputs will now contain copies of the RFIO and HOLD86 inputs, sampled on the preceding positive clock edge. The third equation of listing 2 shows that when one of them is active, the corresponding subsystem is requesting the 32032 CPU bus. A combinatorial output is ideal for this.

When the 32032 indicates that the bus is free (HLDA signal is asserted), the PAL must resolve whether one or both DMA circuits are requesting the bus and arbitrate which one gains control. This is best done by using a "feed-forward" or "look-ahead" algorithm, as shown in the fourth equation of listing 2.

The first term of this equation says "if the 8086 is requesting the bus (HOLD86I is asserted) and the 32032 has released it (HLDA is asserted), then, provided both arbitration outputs (HLDA86 and RFSHACK) are currently inactive, give the bus to the 8086 on the next clock cycle by asserting HLDA86 to acknowledge that the 8086 has the bus."

The second term covers the case where the 8086 hold request, HOLD86I, arrives after the 32032 has released the bus to the refresh controller (HLDA and RFSHACK are true). In this case, the arbitrator will wait until the refresh request signal has gone away (RFIOI is inactive). The 8086 acknowledge, HLDA86, will then be asserted in the next clock cycle. Assume that RFSHACK will be removed on the same clock edge as its request (RFIOI).

After the 8086 has been acknowledged (HLDA86 is true), the third term will keep it true until the first clock cycle after the hold request (HOLD86I) has been removed. The refresh acknowledge arbitrator is shown in the fifth equation of listing 2.

Once again the first term checks to see if both acknowledge outputs are inactive. In this case, however, as the refresh is the lower-priority task, the HOLD86I signal is also checked to make sure that there is no simultaneous 8086 hold request until after the 8086 cycle has ended. This is necessary to ensure that the two acknowledge outputs are never asserted simultaneously. The second term again detects when the alternative DMA cycle is about to end, while the third term ensures that the output will be asserted for as long as the refresh request persists.

In case you are wondering, I did not dream these equations up in a flash of inspiration. It took many hours of doodling with pen and paper and some ideas from an application note called "An 8-bit Priority Interrupt Encoder with Registers" by Vincent Coli, *PAL Handbook* (3rd ed.), published by Monolithic Memories (MMI). This book is invaluable.

PALs to the Rescue

The DSI-32 prototypes did not work. The early 32032 parts that were shipped back in 1984 seemed to intermittently cease operation when the HOLD input was asserted at random. National Semiconductor suggested that if we synchronized the HOLD requests with the 32032 CPU cycles we might find a CPU state at which the 32032 would continue to operate correctly. What a task—the HOLD PAL now needed to keep track of which T state the CPU was executing and only assert HOLD selectively. The CPU has five types of T states: Tidle, T1, T2, T3, and T4 (see figure 9). The only way to distinguish them is by examining the bus signals and synchronizing them with CTTL, which is in phase with the 32032 CPU synchronization clock.

We felt that two of the signals in figure 9 could help us. The first was ADS, the

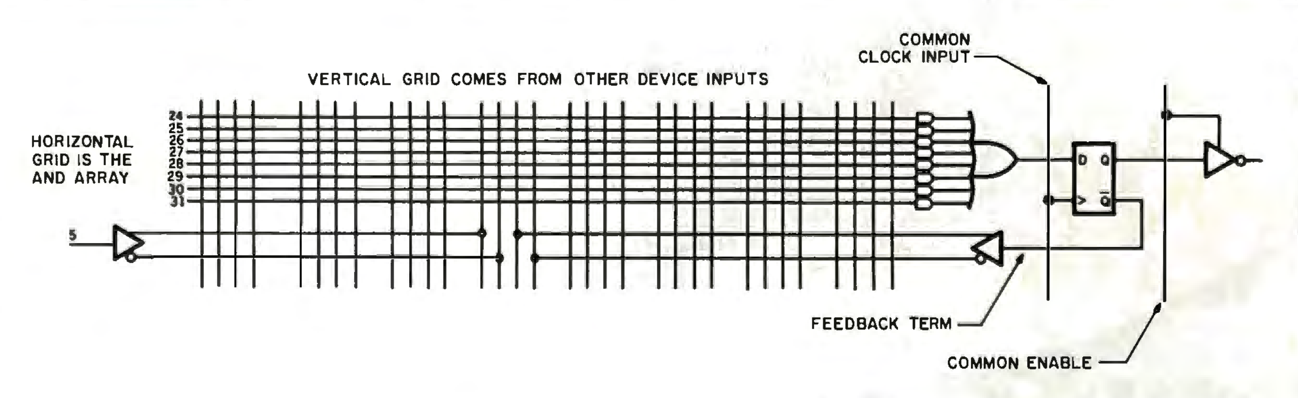

Figure 7: *Clocked logic cell from a 16R4 PAL.*

address strobe, and the second was TSO, the timing strobe output. Because ADS was always asserted in T1, if we could somehow latch it until the following clock edge we would know when T2 occurred. T2 turned out to be one of the two usable T states; T4 was the other, during which a HOLD request would be serviced correctly. ADS, however, is a very short signal. It must be stretched to the next positive edge of CTTL for the 16R4's flip-flops to recognize it.

The flip-flops in the 16R4 could not be used, as their clock is hard-wired from CTTL. A 74LS74 would have been an eminently good solution; however, the printed circuit board was already fabricated and we didn't have room for another chip. The final realization used one of the spare combinatorial outputs of the 16R4, named T1. It used the following equation, which says that when ADS pulses and CTTL is low, the T1 will be asserted and latched until CTTL goes high and tristates the T1 output:

IF(/CTTL) T1 = ADS + T1

Thus, the T1 output is a stretched copy of ADS, delayed sufficiently so that the 16R4's flip-flops can use it to latch bus requests during the CPU T state, T2. The T1 output needed a 2200-ohm pull-up resistor to work effectively at 10 MHz. We revised the equations that latch the asynchronous inputs to latch requests only when T1 is true or, if HOLD is already asserted, to keep holding and ignore synchronization with T2.

RFIOI := RFIO*T1 + RFIO*HOLD

HOLD86I := HOLD86*T1 + HOLD86*HOLD

The following equation causes a bus request to be sent to the 32032:

IF(VCC) HOLD = HOLD86I + RFIOI

The priority resolver was unchanged.

We added the ability for the aforementioned equations to synchronize with the T4 state by using the TSO signal:

IF(/CTTL) T1 = ADS + T1

RFIOI := RFIO*T1 + RFIOI*TSO + RFIO*HOLD

HOLD86I := HOLD86*T1 + HOLD86*TSO + HOLD86*HOLD

IF(VCC) HOLD = HOLD86I*/TSO*/T1 + RFIOI*/TSO*/T1 + HOLD86I*HOLD + RFIOI*HOLD

The HOLD PAL on the DSI-32 went through two more major changes. Terms were added to prevent HOLD requests, while the 32032 MMU was accessing the bus and the refresh acknowledge cycles were stretched to improve the RAS (row address strobe) precharge dynamic RAM timing parameter.

It is not exaggerating to say that the 16R4 HOLD PAL allowed Definicon to ship the DSI-32 several months earlier

continued

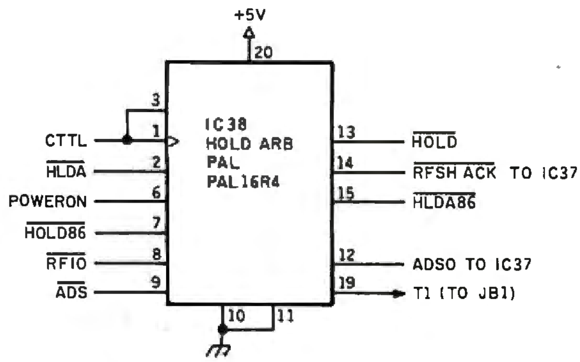

Figure 8: *The HOLD PAL portion of the DSI-32 schematic.*

Listing 2: *The PALASM file for the DSI-32 HOLD PAL.*

```
PAL16R4
IC2
(C) Copyright 1984,1985 Definicon Systems Inc.
Hold arbitration PAL for DSI-32 Rev B, TM, 12/5/84, first try
CLK /HLDA CTTL NC NC NC /HOLD86 /RFIO /ADS GND
/EN /ADSO /HOLD /RFSHACK /HLDA86 /RFIOI /HOLD86I NC NC VCC

RFIOI := RFIO
HOLD86I := HOLD86

IF(VCC) HOLD = HOLD86I + RFIOI

;First resolve the higher priority, the 8086
HLDA86 :=  HOLD86I * HLDA * /RFSHACK * /HLDA86
        + HOLD86I * HLDA * RFSHACK * /RFIOI
        + HOLD86I * HLDA86

;Resolve the refresh acknowledge
RFSHACK := RFIOI * HLDA * /RFSHACK * /HLDA86 * /HOLD86I
        + RFIOI * HLDA * HLDA86 * /HOLD86I
        + RFIOI * RFSHACK
```

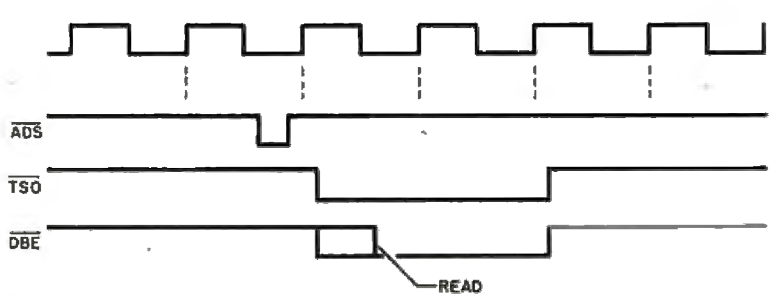

Figure 9: *Key 32032 CPU signals. The ADS and TSO signals were used to synchronize the HOLD PAL to CPU states T2 and T4.*

than a conventional 74LS00-series logic design would have.

What Can Go Wrong

Everybody tells you that PALs are designed so that all internal delays are matched and output glitches can't occur. Photo 1 is an oscilloscope photograph of the AS output of the DPORT20 PAL discussed earlier. This particular photograph was taken with a 20L10 PAL (the 24-pin equivalent of the 16L8).

If you examine the cell schematic for the 20L10, it's identical (except for fewer minterms) to that of the 16L8. Its performance, however, differs. On the top trace, you can see the Q0 output of the counter. Note the 9-ns-wide glitches. The outputs of the 74F161A are synchronized to within

continued

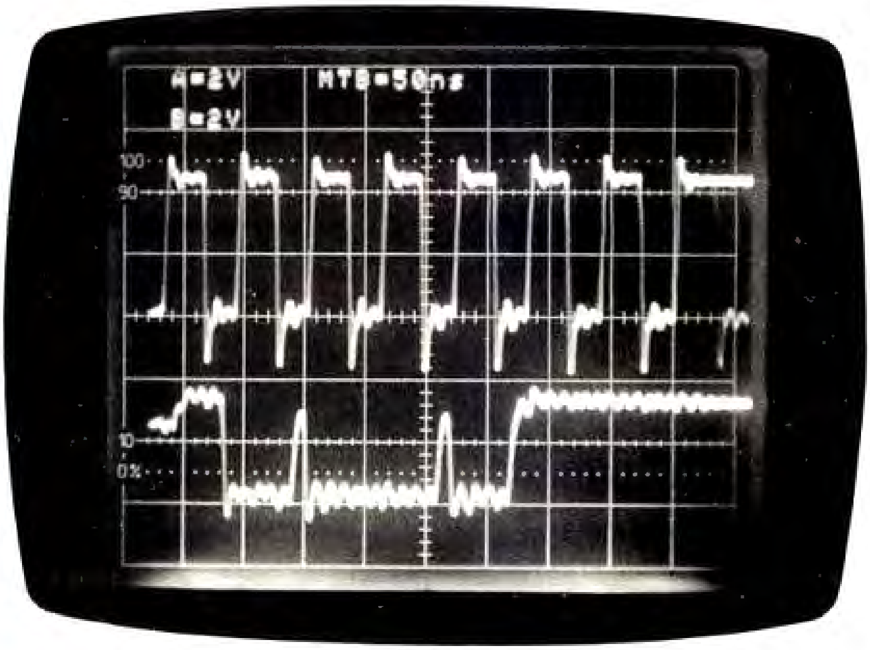

Photo 1: *The AS output of the DPORT20 PAL. The top trace is the Q0 input; the bottom trace is the AS output. Notice the 9-ns-wide glitches in the AS output between Q0 counts 4 and 5 and counts 8 and 9.*

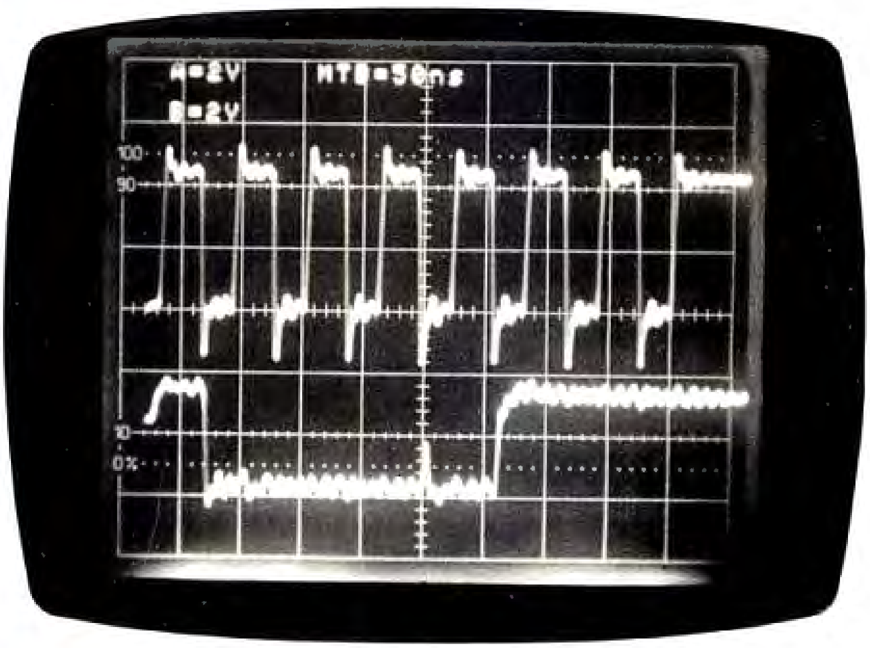

Photo 2: *Glitching of the AS output of the DPORT20 PAL implemented in a 16L8B device occurs only between counts 7 and 8.*

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Listing 3: *The conversion of the PALASM version 1 file for the HOLD PAL into the format used by PALASM version 2.*

```
; created by PDSCNVT V2.21 - MARKET RELEASE (07-24-86)
; (C) - COPYRIGHT MONOLITHIC MEMORIES INC, 1986
 TITLE PDS CONVERSION FILE
 PATTERN EXAMPLE
 REVISION 1.00
 AUTHOR JOHN DOE
 COMPANY MONOLITHIC MEMORIES
 DATE 11/19/84
;PAL16R4
;IC2
;(C) Copyright 1984,1985 Definicon Systems Inc.
;Hold arbitration PAL for DSI-32 Rev B, TM, 12/5/84, first try

CHIP zzz PAL16R4 CLK /HLDA CTTL NC NC NC /HOLD86 /RFIO NC GND
     /EN NC /HOLD /RFSHACK /HLDA86 /RFIOI /HOLD86I NC NC VCC
EQUATIONS
RFIOI := RFIO         ;Latch the asynchronous inputs, first refresh request
HOLD86I := HOLD86     ;and now the access request from the 8086

HOLD = HOLD86I  ;immediately we get a request to tell the CPU
       + RFIOI
;Resolve the priorities, waiting for the HLDA before acknowledging
;First resolve the higher priority, the 8086
HOLD.TRST = VCC
HLDA86 :=  HOLD86I * HLDA * /RFSHACK * /HLDA86
          + HOLD86I * HLDA * RFSHACK * /RFIOI
          + HOLD86I * HLDA86

 ;Then resolve the refresh acknowledge
 RFSHACK := RFIOI * HLDA * /RFSHACK * /HLDA86 * /HOLD86I
           + RFIOI * HLDA * HLDA86 * /HOLD86I
           + RFIOI * RFSHACK

 ; FUNCTION
;SIMULATION
;-----------------------------------------------------------------------------
;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA
;CLOCKF CLK
;clock everything inactive

;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;clock everything inactive

;SETF EN /HOLD86 RFIO RFIOI /HOLD86I HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;RFIO recognized

;SETF EN /HOLD86 RFIO RFIOI /HOLD86I HOLD HLDA /HLDA86 RFSHACK
;CLOCKF CLK
;and acknowledged
```

the resolution of the scope (1 to 2 ns). And those glitches are being generated by the difference between the low-to-high and high-to-low propagation delays of the logic internal to the PAL.

Photo 2 is a scope photograph of the output of a 16L8B, showing that the glitch in this case is a lot faster but still a problem. You can remove the remaining glitch, between counts 7 and 8, by allocating an unused output, say CNT7:

```
IF (VCC) CNT7 = /Q3*Q2*Q1*Q0

IF (HLDA86) AS =
   /Q3*Q1 ; counts 2,3,6,7
 + /Q3*Q2*/Q1 ; counts 4,5
 + Q3*/Q2*/Q1 ; counts 8,9
 + CNT7
```

The glitch occurring at the input transition from 7 to 8 is masked by the delay in the output buffer for the CNT7 term.

So be warned. When you have outgrown the capabilities of the 16L8 and 16R4, be sure to evaluate the advantages and disadvantages of the PAL families you choose.

Obtaining PALASM

I have been using the syntax of PALASM version 1. MMI has released PALASM version 2.21, which contains many enhancements and support for a range of PALs with advanced architectures. Unfortunately, it's much more tedious to write code using its new syntax. Listing 3 shows the PALASM 2.21 representation of the HOLD PAL file we discussed earlier in listing 2. This .PDS file was created by running the .PAL file from PALASM 1 through a conversion utility, PDSCNVT. I can probably put up with the representation for the logic, but the tedium of keying in all those simulation vectors is something I can do without.

PALASM 1 is in the public domain; for

```
;SETF EN /HOLD86 RFIO RFIOI /HOLD86I HOLD HLDA /HLDA86 RFSHACK
;Check DIAGON function

;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA
;CLOCKF CLK
;clock everything inactive

;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;clock everything inactive

;SETF EN HOLD86 /RFIO /RFIOI HOLD86I HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;HOLD86 recognized

;SETF EN HOLD86 /RFIO /RFIOI HOLD86I HOLD HLDA HLDA86 /RFSHACK
;CLOCKF CLK
;and acknowledged

;SETF EN HOLD86 /RFIO /RFIOI HOLD86I HOLD HLDA HLDA86 /RFSHACK
;Check DIAGON function

;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA
;CLOCKF CLK
;clock everything inactive

;SETF EN /HOLD86 /RFIO /RFIOI /HOLD86I /HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;clock everything inactive

;SETF EN HOLD86 RFIO RFIOI HOLD86I HOLD /HLDA /HLDA86 /RFSHACK
;CLOCKF CLK
;both arrive at once

;SETF EN HOLD86 RFIO RFIOI HOLD86I HOLD HLDA HLDA86 /RFSHACK
;CLOCKF CLK
;8086 wins

;SETF EN /HOLD86 RFIO RFIOI /HOLD86I HOLD HLDA HLDA86 /RFSHACK
;CLOCKF CLK
;8086 goes away, hold active

;SETF EN /HOLD86 RFIO RFIOI /HOLD86I HOLD HLDA /HLDA86 RFSHACK
;CLOCKF CLK
;rfsh wins now
;---------------------------------------------------------------------------
;DESCRIPTION
;The HOLD PAL arbitrates between two possible sources of bus requests to
;the 32032, refresh and PC bus access.
```

information on how to obtain version 2.21, you can contact MMI. I hope that somebody will take the source code and write a good simulator. Note that the fourth edition of the *Programmable Logic Handbook* is written for PALASM 2.21; the third edition is in PALASM 1 syntax.

I have obtained a copy of the old PALASM source code 1.3 written in FORTRAN-77. The compiled executable copies of later versions (1.7f) are available for the IBM PC; the FORTRAN source will be of most value to those readers interested in how PALASM works and those without access to IBM PCs. [Editor's note: *The programs are available from Trevor Marshall's Thousand Oaks Technical Database, (805) 492-5472 or (805) 493-1495, in the C:\ PALASM subdirectory. They are also available on disk, in print, and on BIX (see the insert card following page 424 for details), or on BYTEnet (see page 4).*]

Summary

PALs offer a circuit designer the chance to overcome the inflexibility of hardware designs. This results in fewer changes to the circuit board during the debug phase and easier field upgrade during the operational phase of a product's life. As the variety of PAL configurations proliferates and the cost drops, it becomes increasingly difficult to justify the continued use of discrete logic devices. ■

ACKNOWLEDGMENTS

I wish to thank Definicon Systems Inc. for creating the environment in which it was possible to develop these devices and for permission to use examples of the proprietary PAL codes from our coprocessor products. George Scolaro worked with me on the DSI-32 PALs, and Chris Jones on the DSI-020 PALs.

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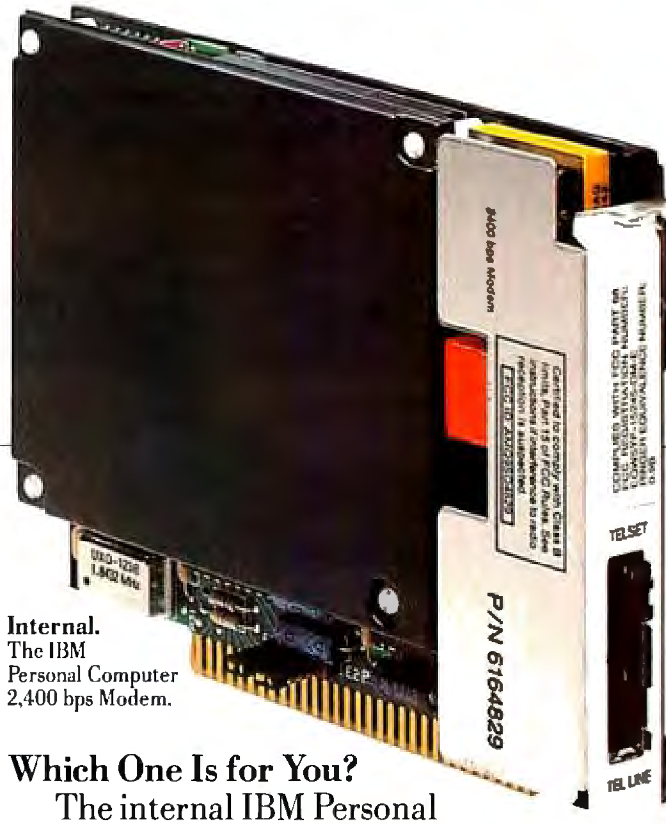

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A PAL Programmer

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Robert A. Freedman

FOR THE PAST several years, I have been looking for an inexpensive PAL programmer, but I've had no luck. It seems that nothing on the market is under $500. There are plenty of inexpensive EPROM programmers but not PAL (programmable array logic) programmers. Everyone I've talked to thinks that PAL programmers are too difficult to build at low cost or that the only market worth chasing is the multithousand-dollar universal programmer market. These universal programmers are generally too expensive for the hobbyist who has to pay for one out of his own pocket or the engineer at a large company who can't justify an expenditure of several thousand dollars for a programmer at her desk when there is one down the hall or in the next building.

Since I could not buy the kind of PAL programmer I wanted, I decided to design one myself. Many people would probably like to program a few PALs and don't want to buy an expensive universal programmer. The text box "The ZAP-A-PAL Programmer" on page 266 shows the 20- and 24-pin PAL devices that this programmer can handle.

The PAL Programming System

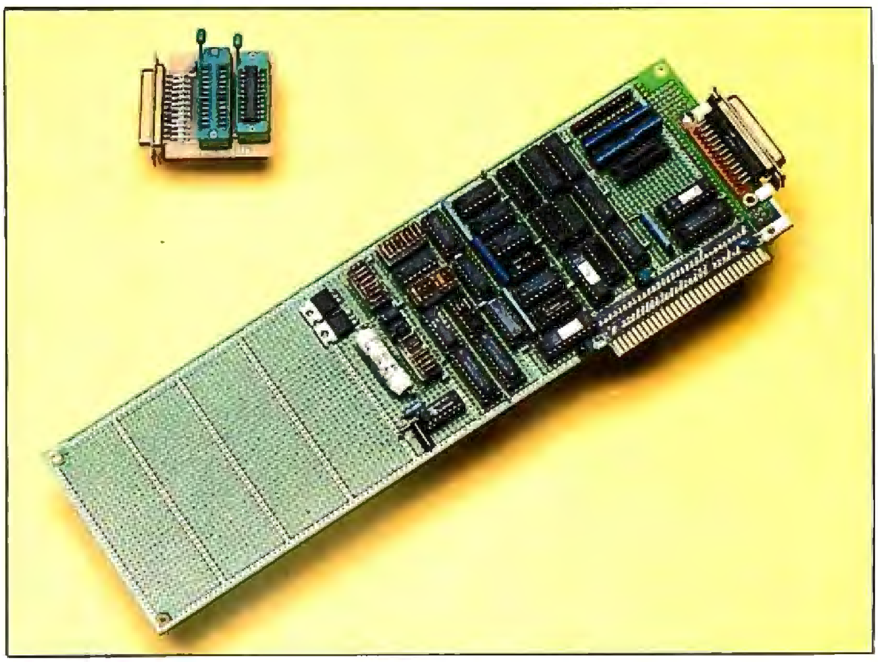
ZAP-A-PAL is configured as an IBM PC adapter card (see photo 1). This eliminates the need for a case and power supply. Also, a detachable PAL socket card with 20- and 24-pin zero-insertion-force sockets is for mounting the PALs. This card allows programming with the cabinet closed and plugs into the ZAP-A-PAL board in back of the computer during operation. Industry standard DB-25 connectors make the connection. You can use a short 25-pin shielded cable so that you can move the socket board to the front of the computer for easy access while mounting and dismounting PALs.

I wrote a program, ZAPAL, whose job is to read a JEDEC file and interpret the fuse map to drive the ZAP-A-PAL card and program the PAL. [Editor's note: *The interface program fragment ZAPAL.C (source code) is available on disk, in print, and on BIX; see the insert card following page 424 for details. It is also available on BYTEnet; see page 4.*] You will need to supply the logic design com-

continued

Robert A. Freedman has an S.B.E.E. in computer science from MIT and works as a freelance consultant designing with microcomputers. He can be contacted at (617) 683-4659 or at P.O. Box 1348, Lawrence, MA 01842.

Photo 1: *The ZAP-A-PAL board.*



piler of your choice. You can use any logic compiler provided that it runs on the IBM PC and generates a JEDEC format file for output.

Limitations

ZAP-A-PAL programs only the array fuses in bipolar PALs. At this stage of development, it does not program security fuses. ZAP-A-PAL will not program erasable CMOS programmable logic devices, and it does not program some of the PALs recently introduced by Monolithic Memories Inc. and others. ZAP-A-PAL does not program Advanced Micro Devices PALs, which use a different programming strategy than MMI, National Semiconductor, and Texas Instruments. I am working on enhancements to ZAP-A-PAL to overcome many of these limitations.

Design Philosophy

To ensure a high degree of success for anyone attempting to duplicate this project, I set some guidelines to follow in the design of ZAP-A-PAL.

- Self-calibrating—no worry about drift or out of tolerance
- No precision resistors required
- No potentiometers
- Software entirely in C language
- No dependence on software timing loops
- Where possible, use of inexpensive, commodity components
- Open architecture, expandable to new device types
- Low cost; see the text box "The ZAP-A-PAL Programmer" on page 266.

PAL Programming Principles

To understand the operation of ZAP-A-PAL, you must first understand how a typical PAL is organized. Refer to the device logic diagram for the 16L8 PAL in figure 4 of Vincent J. Coli's article "Introduction to Programmable Array Logic" on page 207. The axes of the array are numbered. The input lines are numbered across the top, and the product terms are numbered down the left.

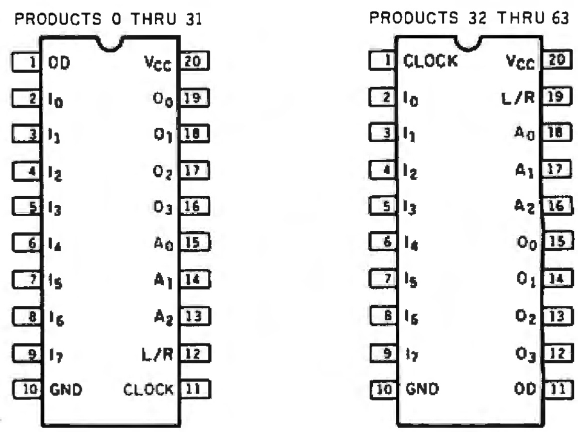
In this discussion, the following terms represent

L = "1" = V_{IL} = low = logic 0 = GND
H = "0" = V_{IH} = high = logic 1 = +5 volts
Z = "0" = resistor to +5 V (high impedance)
HH = "2" = V_{IHH} = super-voltage = 11 V
HH = "4" = V_{IHH} = program pulse = 11 V

The fuse number is computed as the product term times 32 plus the input line or `fuzno = prod_lin * 32 + input_lin`. By analyzing the fuse number, you can compute all the addresses necessary to program that fuse. The input lines are organized in groups of four—that is, 0–3, 4–7, 8–11, ..., 28–31. The two low-numbered input lines in each group are connected to the noninverting and inverting inputs coming from the left of the PAL diagram, while the two high-numbered input lines in each group are connected to the noninverting and inverting input lines coming in from the right of the diagram.

Figure 1 shows the programming pin configuration for 20-pin PALs.

The PAL is divided into two halves: Product lines 0 through 31 are in the first



Input Line Select

Input Line Number	Pin Identification I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Figure 1: *Voltage configuration to program a 20-pin PAL. Adapted from* The PAL

half, and product lines 32 through 63 are in the second half. Depending on the half you are trying to program, the meaning of the OD and CLOCK pins reverses: OD is on pin 1 for the first half of the array, and CLOCK is on pin 1 for the last half of the array. The positions of the O_x, L/R, A_0, A_1, and A_2 pins also change.

If the fuse number is less than halfway through the array, the fuse is in the first half of the PAL and vice versa. For example, the 16L8 has 2048 fuses and 64 product terms. So if (fuzno<2048/2) then the fuse is in the first half of the PAL; otherwise it's in the second half.

You select the input line group by placing a logic value of Z on the appropriate

continued

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}

HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10 kΩ to 5.0 V)

Product Line Select

Product Line Number	Pin Identification O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Handbook, *3rd ed., by Monolithic Memories Inc.*

I_x pin where ($I_0 <= I_x <= I_7$). A logic value of Z on the L/R pin selects the low-numbered inputs in a group, while a value of HH on this pin selects the high-numbered inputs. Therefore, you can compute L/R as: (LR = fuzno & 2 ? Z : HH). The input signal polarity is determined by the variable input_lin. If input_lin is even, the input is noninverting, and if input_lin is odd, the input is inverted. The product terms are grouped eight to an output. To find the output pin (O_x) that a fuse is on, compute Ox = fuzno / (32 * 8). To find the address (A_0, A_1, or A_2) of the product term of that output, compute addr = fuzno % 8, or modulo 8. Each 0 bit of the 3-bit address is set to Z. Each 1 bit of the address is set to HH.

Circuit Description

In this discussion, pin numbers P1 through P24 refer to both the 20-pin and the 24-pin sockets. The actual 20-pin socket pins are mapped onto the 24-pin socket's pins. Figure 2 shows the details of the socket-board schematic.

What follows is a description of how I translated the PAL programming principles just reviewed into a board that can generate the voltages and signals required to program these devices. This will start with the pin-driver circuitry that is responsible for presenting these voltages to the socket board and its power supply. What will be described next is what's required to read the PAL to verify that the proper fuses have blown, followed by a description of the IBM PC to ZAP-A-

continued

The ZAP-A-PAL Programmer

The ZAP-A-PAL can program both 20-pin and 24-pin PALs. It plugs into an IBM PC and uses commercially available logic design software. The total cost of building ZAP-A-PAL is less than $200.

The types of PALs that ZAP-A-PAL will program are listed below:

20-pin	10L8	10H8	12L6	12H6	14L4	14H4
	16L2	16H2	16C1	16A4	16X4	
	16R4	16R6	16R8	16L8		
	16R4BP	16R6BP	16R8BP	16L8BP		
24-pin	12L10	14L8	16L6	18L4	20L2	
	20C1	20L10	20X10	20X8	20X4	
	20R4	20R6	20R8	20L8		

It will do MMI standard PALs with A, B, and D speed suffixes and −2 and −4 power suffixes for available types. It will do National Semiconductor and Texas Instruments PALs from the above list.

The following is a list of parts needed to construct the ZAP-A-PAL board. Prices may vary from those given.

Printed Circuit Board, WW JDR MicroDevices	1
Socket Module PC Board	1
24-pin ZIF Socket 3M-Textool	1
20-pin ZIF Socket	1
RS-232C D-Sub 25-S Rt. Ang. R. S. Cat #276-1521	1
RS-232C D-Sub 25-P	1
UNC5810A Sprague	3
UNC5821A	4
UNC5895A	1
IRFD-9123 HEXDIP Power FET	1
7406	1
LS138	1
LS245	1
LS251	2
LS259	1
LS273	2
LS390	1
PAL 16L8	2
PAL 16R8	1
DAC-08 EP	2
LM-317 T-220, Adjust. Reg.	2
LM-324, Quad Op-amp	1
LM-336, 2.5-V Reference	1
LM-339, Quad Comparator	3
TL-497ANC	1
1N4001 Diode	6
1N4740A, 10-V Zener	1
1N4935 Fast Recov. Diode	1
100-ohm ¼-watt 5 percent Res.	1
240-ohm ¼-watt 5 percent Res.	2
1.0-kohm ¼-watt 5 percent Res.	1
1.2-kohm ¼-watt 5 percent Res.	2
2.0-kohm ¼-watt 5 percent Res.	1
2.2-kohm ¼-watt 5 percent Res.	1
2.7-kohm ¼-watt 5 percent Res.	1
5.11-kohm ¼-watt 5 percent Res. (1 percent better, but 5 percent okay)	8
5.6-kohm ¼-watt 5 percent Res.	1
15-kohm ¼-watt 5 percent Res.	1
8-pin IC Sockets	1
14-pin IC Sockets	8
16-pin IC Sockets	16
18-pin IC Sockets	3
20-pin IC Sockets	7
24-pin IC Sockets	1
DALE IHA-203 100 μH or any 100-250 μH @ 1 amp	1
100-pF Mica Cap	1
0.01-μF Monolithic Caps	2
0.1-μF Monolithic Caps put one cap on each IC power pin	30
15-μF @ 20-V Tantalum Cap	4
22-μF @ 25-V Tantalum Cap	2
100-μF @ 16-V Aluminum Cap	1
1.0-ohm 1-watt Resistor	1
Resistor SIP 1.0K x 7	1
Resistor SIP 2.2K x 9	3
Resistor SIP 4.7K x 7	2
Resistor SIP 4.7K x 5	2

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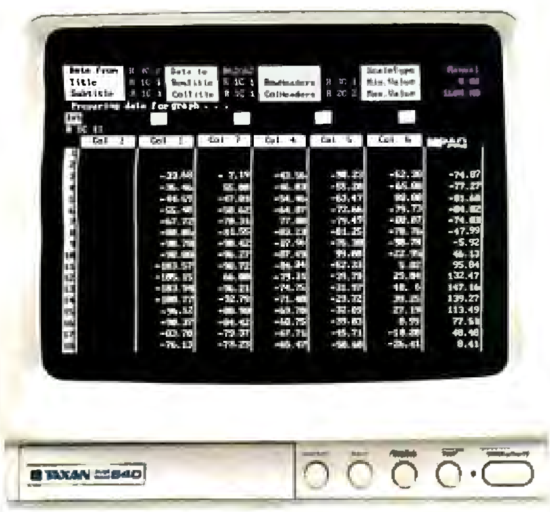

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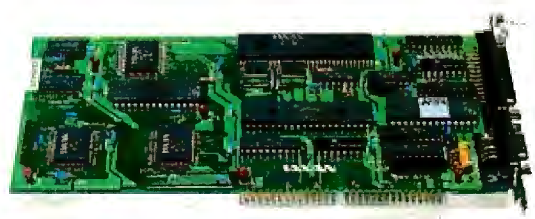
Model 635	Superior text display and business graphics
Model 650	Personal CAD/CAM graphics, 0.28mm dot pitch



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ZAP-A-PAL uses serial-input BiMOS latched drivers as pin drivers.

PAL interface circuitry and calibration procedures.

Pin Drivers

Sprague has a series of chips called serial-input BiMOS latched drivers that I use as pin drivers in ZAP-A-PAL. The two types are source drivers and sink drivers. Both have n-bit shift registers, n-bit latches, and high-current, high-voltage, Darlington output transistors. I constructed a shift register 28 bits long using three strings of these shift registers, making it possible to drive each PAL pin either to ground, to V_{IHH}, or to Z. Resistor SIPs (single in-line packages) are used to apply V_{IH} to all socket pins. These establish the logic high level Z on any pins not overridden by one of the pin-driver outputs being asserted and enabled. Each string is controlled by data bits 0, 1, and 2 written into the I/O port of ZAP-A-PAL and presented on lines SHD0, SHD1, and SHD2 as illustrated in figure 3.

The first string consists of four UCN5821A 8-bit sink driver chips and is fed by data bit 0. This string pulls the PAL socket pins down to near ground. You can disable the second chip in the chain with the signal $\overline{\text{ENCL}}$ via software control. This floats either pin P1 or pin P13—either of which can be a CLOCK input to the PAL—to allow reading of the state of the selected fuses.

The second string consists of three chips: a UCN5810A 10-bit source driver, a UCN5895A 8-bit source driver, and another UCN5810A. This string is controlled by data bit 1 and applies the voltage V_{IHH} to the PAL being programmed. The first chip drives L/R, A_0, A_1, and A_2 to V_{IHH}, as required on the 10 PAL output pins. The UCN5895A pulls up the OD signal (either pin P1 or P13, depending on the half of the PAL you're writing to) to V_{IHH}. This chip's outputs are enabled by the signal $\overline{\text{ENCH}}$, which is also under software control. The last chip in this string applies V_{IHH} to any of the PAL socket's 10 input pins (P2 through P11).

The third string consists of a single UCN5810A. Fed by data bit 2, this chip applies programming pulses to any of the PAL socket's 10 output pins (P14 through P23). Since this chip is parallel with the

continued

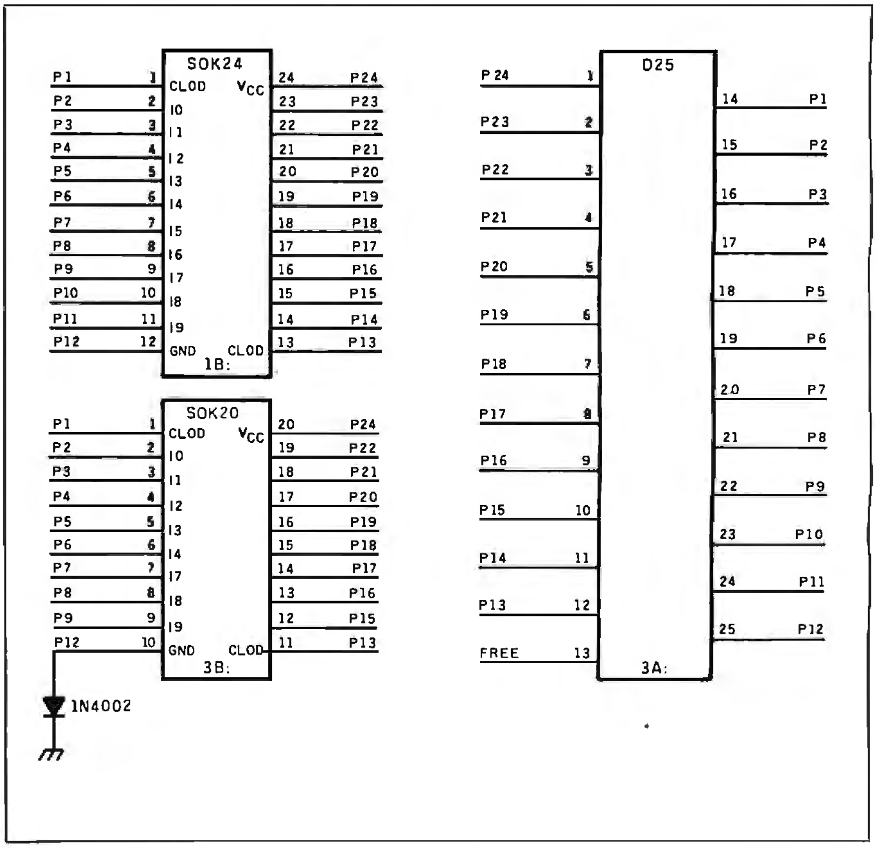

Figure 2: *Schematic for the socket board.*

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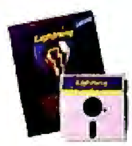

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You can disable the Darlington outputs within each chip without affecting the contents of the latches.

first chip of the second string, you must take care that the two chips act only on mutually exclusive pins. This chip's output enable pin is controlled directly from a timing PAL (PAL-2) to be described later.

By sending the pin configuration data serially, you can build in protection against driving a pin high and low at the same time. You accomplish this by passing the data stream through a PAL (PAL-3) that ensures that no more than one driver is active for each bit. You can disable the Darlington outputs within each chip without affecting the contents of the latches. This allows precise timing control of the application of voltage pulses to the pins of the PAL being programmed.

Since only one driver at a time can be on for a given pin, the data sent to the shift register can take on only a limited number of values. See figure 4 for these values and how they relate to the shift register and PAL pins.

You load the shift register by doing an output instruction to I/O address 102 with the desired value (0, 1, 2, 4) in AL. For example, in C this would be outportb (0x102,1). You must load the shift register with 28 values, although only 20 or 24 of these values are actually used. This is because the position of each value in the shift register determines the output on a designated PAL pin, and this register can be loaded only serially. See table 1 for several examples of the shift register's contents for a programming operation. Once all 28 shift-register positions are loaded, you must strobe them into the latches by writing a 1 followed by a 0 to I/O address 108, toggling the STR line. [Editor's note: *All addresses are in hexadecimal.*]

Power Supply

The 12 V from the IBM PC's power supply is not quite high enough to provide the 11.75 V needed for MMI's PALs because of the voltage drops in the drivers, so a booster circuit was designed (see figure 5). This is a switching regulator using the TL-497 chip. It operates by momentarily

continued

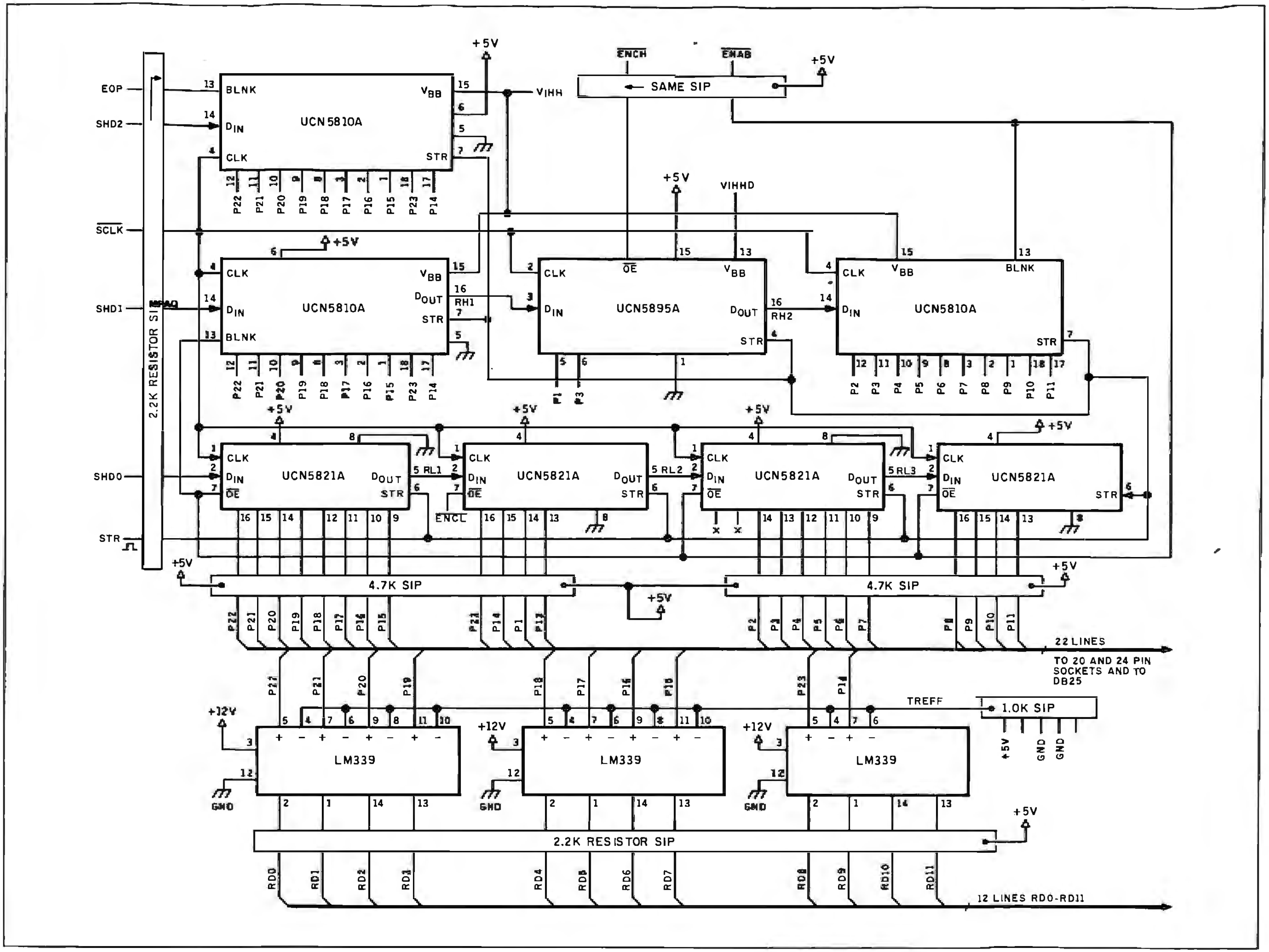

Figure 3: Schematic for the pin drivers and verify circuits.

shorting an inductor between 12 V and ground. When the coil is disconnected from ground, the energy is dumped through a diode into an output capacitor, raising its voltage with each pulse. The switching regulator chip monitors the voltage on the capacitor and, when it is high enough, the pulsing stops.

A resistive divider sets the output voltage to approximately 15 V. This is regulated down to the desired voltages by linear regulators driven by digital-to-analog converters. Thus, software can define the various voltages needed for different PAL types. The booster output is software-selectable from 15 V through 23 V, but currently only 16 V is necessary.

Logic Verify Circuitry

During the verify portion of the ZAPAL programming procedure, you must read the logic level presented on the output pin after it has been pulsed to see if the fuse was blown. This presents a problem, as you must read a TTL level from a pin that a moment ago had a 12-V high-current pulse on it. What is needed is a device that can withstand the programming pulse and live to discriminate a TTL level to some degree of precision.

The LM-339 quad comparator is inexpensive and common. Three LM-339s read the 10 possible output pins, leaving two comparators free for other use. The reference inputs of the 10 comparators are tied to a reference made out of a resistor SIP. A SIP is preferred because the ratio of the resistors is more important than their absolute values for determining the reference voltage. Since SIP resistors are manufactured together, their resistive values are closely matched. The open collector outputs of the LM-339s are pulled up by other resistor SIPs to +5 V and are connected to the inputs of a pair of 74LS251 octal multiplexers. These are run to bit 0 of the data bus and respond to I/O read commands to the 16 consecutive locations at hexadecimal 100 through 10F.

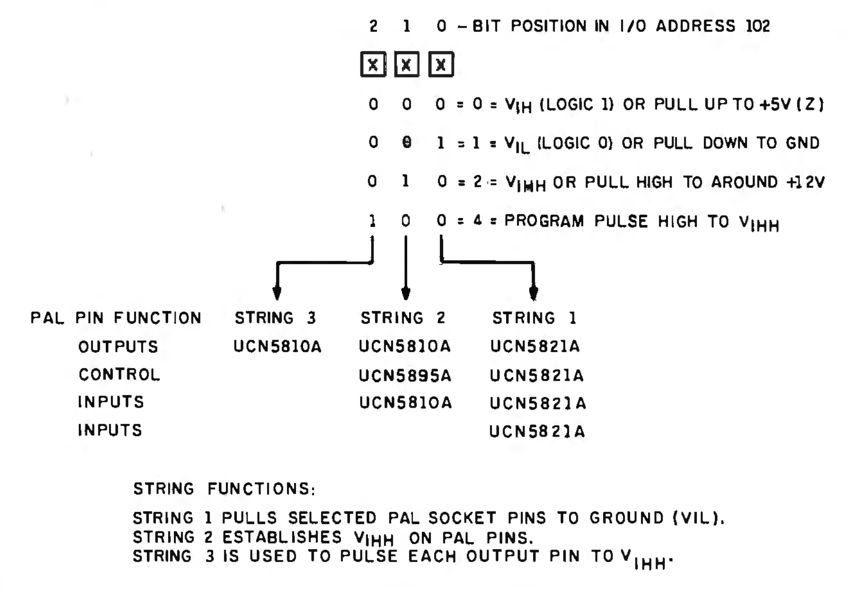

Figure 4: *Relationship between a programming value written into ZAP-A-PAL's I/O port and the pin drivers.*

Table 1: *Examples of data values for the pin drivers. This is how the data is loaded into the shift register. Since the shift register is loaded serially, the unused portions of the register (designated by the lack of a pin number) must be padded with zeros to position the driver values at the correct PAL pin. Note that the pin numbers refer to the pin numbers on the 24-pin socket.*

	Outputs	Control	Inputs	
Pin number	2 2 2 1 1 1 1 1 2 1 2 1 0 9 8 7 6 5 3 4	1 1 3 - - - - - -	1 1 2 3 4 5 6 7 8 9 0 1	
	0,0,0,0,0,0,0,0,0,0,	0,0,0,0,0,0,0,0,	0,0,0,0,0,0,0,0,0,0,0,0	Clear
	0,0,0,0,0,0,0,0,0,0,	2,1,0,0,0,0,0,0,	0,0,0,0,0,0,0,0,0,0,0,0	OD lo
	0,0,0,0,0,0,0,0,0,0,	1,2,0,0,0,0,0,0,	0,0,0,0,0,0,0,0,0,0,0,0	OD hi
20-pin	4,0,0,0,0,0,0,2,0,0,	2,1,0,0,0,0,0,0,	1,2,2,2,2,2,2,2,2,2,0,0	Fuse #2
20-pin	0,0,0,0,0,0,0,4,0,0,	1,2,0,0,0,0,0,0,	2,2,2,1,2,2,2,2,2,2,0,0	Fuse #1100
24-pin	2,2,2,0,0,0,0,0,2,4,	1,2,0,0,0,0,0,0,	1,2,2,2,2,2,2,2,2,2,0,0	Fuse #3200

IBM PC Interface

A PAL 16L8 (PAL-1) decodes address lines SA9 through SA3, $\overline{IOW}$, $\overline{IOR}$, and AEN on the IBM bus to produce four strobes for an 8-bit programmable latch (LS259), a 1-of-8 decoder/demultiplexer (LS138), and two eight-input multiplexers (LS251). Referring to figure 6, you can see that the LS251s read back individual signals to the IBM PC on bit 0 of the data bus as described above. The LS138 further decodes three strobes: two for the LS273 DAC latches and one (SCLK) that clocks data into the pin-driver shift registers. The shift data is sent to the BiMOS shift registers, one pin for each assertion of SCLK. The shift data is sent via bits 0, 1, and 2 of the data bus.

A 74LS259 is used as a set of programmable latches. You can program each bit to stay high or low until next accessed. These configure the ZAP-A-PAL board by software and actuate various parts of the circuit. All latches in the 74LS259 come up cleared on a computer reset. I/O address 10A enables the outputs of the UCN5895A. It puts V_{IHH} on the OD pin of the PAL to set it up for programming. Address 10B enables the UCN5821A sink driver to pull the CLOCK pin on the PAL low and to pulse it to V_{IH} momentarily to clock the data onto the output pins for the verify operation. When address 10E is 0, it inhibits operation of the booster switching regulator, thus reducing power consumption. Address 10D can select the booster output voltage to one of two levels: 0 provides about 15 V, and 1 gives about 24 V. Address 10F controls the level of the TRIG signal, which initiates a program cycle when toggled. Check table 2 for a summary of the ZAP-A-PAL board's I/O addresses and an explanation of their functions.

One critical aspect of this project is the duty-cycle requirements in the PAL programming specification. Basically, the

continued

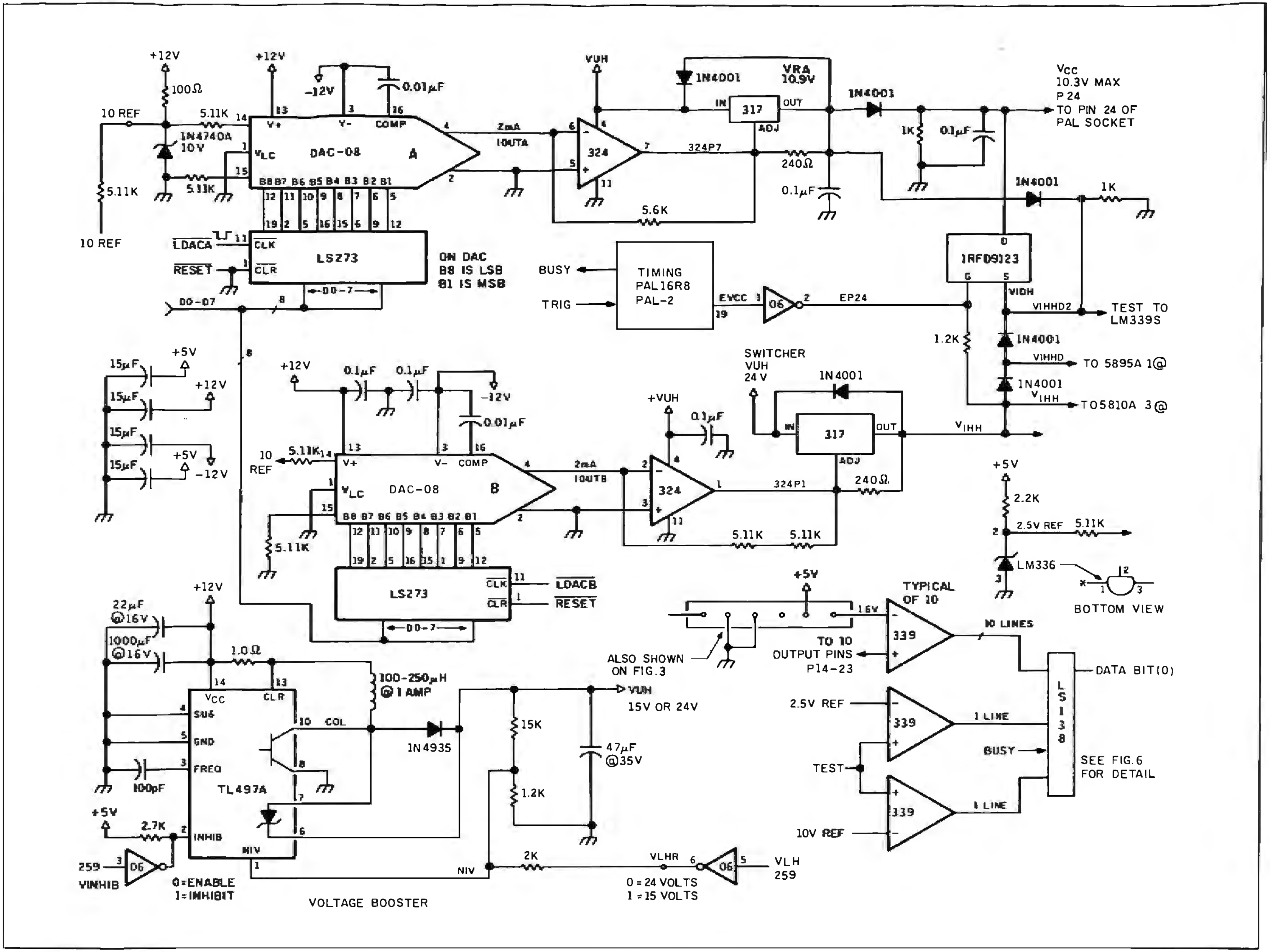

Figure 5: Schematic of the programmable voltage generator circuits.

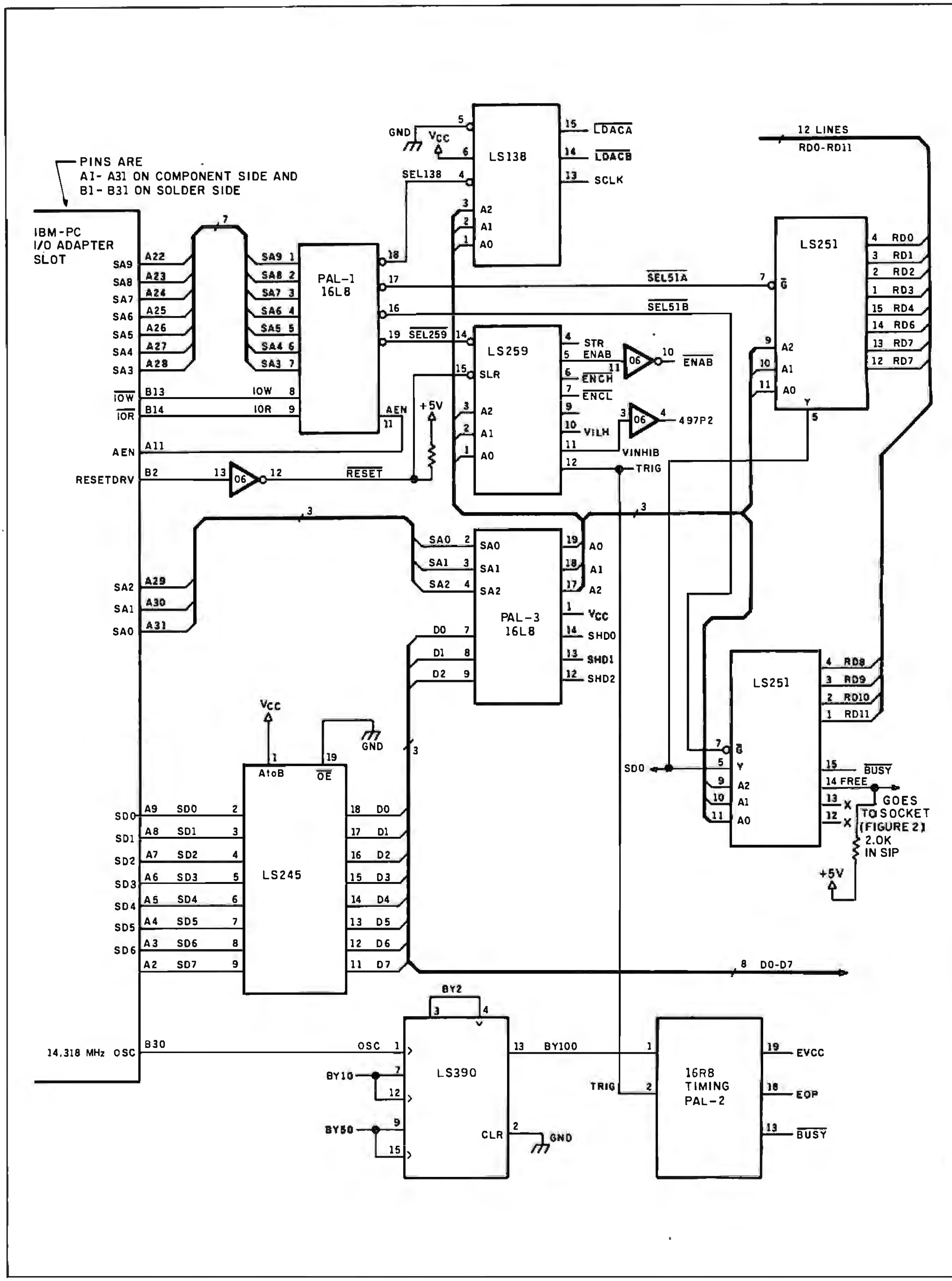

Figure 6: *Schematic of the IBM PC interface to ZAP-A-PAL.*

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Table 2: *I/O address map. Sixteen consecutive locations are required out of the IBM PC's address space. I chose hexadecimal 100 through 10F, but you can easily change this by modifying the address decoder PAL (PAL-1).*

Hex I/O Address	Input	Output
100	Pin 22	Load DAC-A
101	Pin 21	Load DAC-B
102	Pin 20	SCLK—write data to shift register
103	Pin 19	——
104	Pin 18	——
105	Pin 17	——
106	Pin 16	——
107	Pin 15	——
108	Pin 23	Strobe shift data into latches (pulse STR)
109	Pin 14	——
10A	TEST vs. 10.0-V ref	$\overline{\text{ENCH}}$—enable 0D
10B	TEST vs. 2.5-V ref	$\overline{\text{ENCL}}$—enable CLOCK
10C	BUSY	——
10D	——	VLH—booster: 0 = low, 1 = high
10E	——	VINHIB—0 = inhibit booster, 1 = enable
10F	——	TRIG—1 = do program cycle

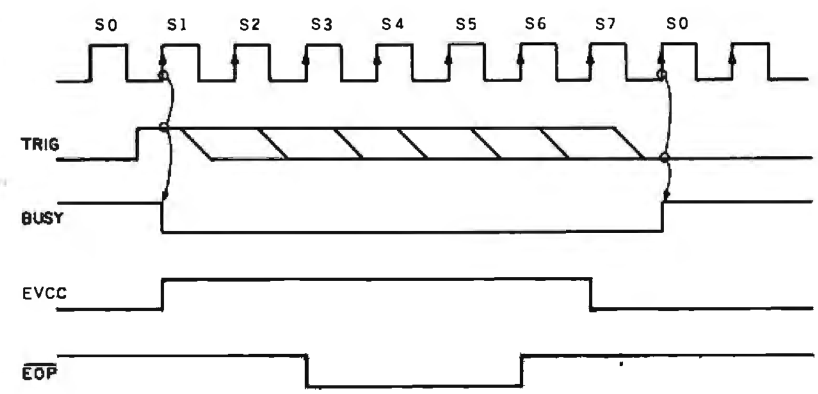

Figure 7: *Timing waveforms of PAL-2, finite state machine.*

V_{CC} pin (24 or 20) must not be at V_{IHH} for more than 60 microseconds at a time and with less than a 20 percent duty cycle. Also, the programming pulse on the output pins must be less than 50 μs and nominally 20 μs long. It is possible to meet these timing constraints using software timing loops, but I don't recommend it. Besides, these requirements provide an excellent opportunity to use a PAL for a finite state machine to control the critical timing of the ZAP-A-PAL board.

A 74LS390 chip divides the 14.31818-megahertz oscillator frequency from the IBM PC bus by 100, yielding a square wave with a period of 6.9841 μs. This becomes the clock input of a PAL 16R8 (PAL-2) that acts as a finite state machine to generate two signals: EVCC and EOP. See the timing diagram in figure 7. EVCC drives an IRFD 9123 P-channel HEXFET power MOSFET transistor via a 7406 open-collector inverter. The HEXFET pulls up the V_{CC} pin of the target PAL from its normal 5-V level to V_{IHH} to apply programming power to the PAL. EOP enables the source driver outputs of a UCN5810A for the duration of the programming pulse to apply V_{IHH} to the selected output pin. The PAL 16R8 also has a BUSY output that can be read via a 74LS251 at I/O address 10C to signal that an operation is in progress. A program pulse is initiated by asserting the TRIG input of the PAL 16R8 by writing a 1 in bit 0 at address 10F. Within 10 μs, BUSY will be asserted. The program asserts TRIG, then waits for BUSY to be asserted. The program then clears TRIG and waits until BUSY clears, indicating that the pulse is complete.

There is a classic chicken-and-egg paradox here: You need to program PALs to construct the PAL programmer, but you can't program PALs until the project is done. Fortunately, each circuit where

continued

Listing 1: *CUPL code to program PAL-3 to protect against conflicts at the pin drivers.*

```
/*************************************************************************/
/* PAL-3 - This device protects against conflicts at the Pin Drivers.  */
/*      Also buffers A0, A1, and A2.  It can be replaced by an LS245    */
/* Allowable Target Device Types:  PAL16L8                              */
/*************************************************************************/

pin [1..20] = [P1,SA0..2,P5,P6,SD0..2,GND,P11,SHD2..0,!P15..16,A2..0,VCC] ;

A0 = SA0 ;          These just buffer the address lines
A1 = SA1 ;
A2 = SA2 ;

SHD0 = SD0 & !SD1 & !SD2 ;   These protect against conflicts
SHD1 = SD1 & !SD0 & !SD2 ;
```

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Listing 2: *CUPL code to program PAL-1, the address decoder PAL.*

```
Address Decoder PAL expressed in CUPL Logic Design Language


/*************************************************************************/
/* PAL-1 - This device decodes I/O addresses to provide strobes for the */
/* following chips: LS259, LS138, LS151(A), LS151(B)                    */
/* Allowable Target Device Types:        PAL16L8                        */
/*************************************************************************/

pin [1..20] = [A9..A3,!IOW,!IOR,GND,     /* Pin List     */
               AEN,P12..15,!SEL51B,!SEL51A,!SEL138,!SEL259,VCC] ;

field IOADR = [A9..A3] ;                      /* Address Field Spec.   */

SEL138   = IOW & !AEN & IOADR:[100..107] ;    /* Logic Equations       */

SEL259   = IOW & !AEN & IOADR:[108..10F] ;

SEL51A   = IOR & !AEN & IOADR:[100..107] ;

SEL51B   = IOR & !AEN & IOADR:[108..10F] ;
```

```
Address Decoder PAL, same logic expressed in PALASM Logic Design Language

IF(VCC) SEL259 = /AEN *  A3 * /A4 * /A5 * /A6 * /A7 *  A8 * /A9 * IOW

IF(VCC) SEL51A = /AEN * /A3 * /A4 * /A5 * /A6 * /A7 *  A8 * /A9 * IOR

IF(VCC) SEL51B = /AEN *  A3 * /A4 * /A5 * /A6 * /A7 *  A8 * /A9 * IOR

IF(VCC) SEL138 = /AEN * /A3 * /A4 * /A5 * /A6 * /A7 *  A8 * /A9 * IOW
```

```
Address Decoder PAL, same logic expressed as a CUPL Fuse Plot

Pin #19
 0000 --------------------------------               LEGEND  X : fuse not blown
 0032 x--x-x---x---x---x--x----x-----x                       - : fuse blown
Pin #18
 0256 --------------------------------
 0288 x--x-x---x---x---x---x---x-----x
Pin #17
 0512 --------------------------------
 0544 x--x-x---x---x---x---x-------x-x
Pin #16
 0768 --------------------------------
 0800 x--x-x---x---x---x--x--------x-x
```

Listing 3: *CUPL code to program PAL-2, the timing PAL.*

```
/*************************************************************************/
/* PAL-2 - This PAL controls timing for the VCC and output pin pulses.  */
/*                                                                      */
/* Allowable Target Device Types:        PAL16R8                        */
/*************************************************************************/

pin [1..20]      = [clk,TRIG,P3..9,GND,!OE,!P12,!BUSY,!Q0..3,!EOP,!EVCC,VCC] ;

field state = [Q2..0];

$define [S0..7] 'b'[000..111]
```

continued

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```
sequence state {

        present S0      if TRIG next S1 out BUSY out EVCC ;
                        default next S0 ;
        present S1              next S2 out BUSY out EVCC ;

        present S2              next S3 out BUSY out EVCC out EOP ;

        present S3              next S4 out BUSY out EVCC out EOP ;

        present S4              next S5 out BUSY out EVCC out EOP ;

        present S5              next S6 out BUSY out EVCC ;

        present S6              next S7 out BUSY ;

        present S7      if !TRIG next S0 ;
                        default next S7 out BUSY ;      }
```

PALs are used in this design can be constructed using other components until the ZAP-A-PAL is usable.

With a little extra work, you can bootstrap yourself up to a usable and fail-safe design. You can replace the address decoder PAL (PAL-1) with gates and inverters. You can replace the timing PAL (PAL-2) with a circuit using one-shots, or counters, to produce similar timing pulses. The PAL 16L8 used to filter the shift data and buffer the address lines (PAL-3) is wired so that it can be replaced by a 74LS245 plugged into the same socket. The CUPL files for these three PALs are included in listings 1, 2, and 3 for those who have access to a PAL programmer. Listing 2 shows the equation expressed in both CUPL and PALASM terminology.

Programmable Voltage Generators

The two programmable voltage generators each consist of an octal 74LS273 register driving a DAC-08 8-bit digital-to-analog converter. Each DAC then feeds into an LM-324 operational amplifier (op-amp) section that acts as a current-to-voltage converter. Each op-amp output drives an adjustable voltage regulator that supplies the high current needed during programming, but at a voltage precisely controlled by the DAC. The feedback resistors on the op-amps determine the full-scale voltage that the circuit produces. Since the DAC current is software-programmable, the voltage out of the op-amp is also software-programmable. To compute the desired value of the feedback resistor, divide the desired full-scale output voltage by the maximum current from the DAC.

DAC-A generates the V_{CC} voltage for the PAL. The maximum voltage needed for this pin is around 10 V. The feedback resistor for DAC-A can be somewhere around 5.6 kohms to give a full-scale output of 10.9 V.

DAC-B generates the V_{IHH}, which is the programming voltage for the PALs. The full-scale range for DAC-B is set at around 20 V by a feedback resistor made of two 5.11-kohm resistors in series. The plan here is to use a resistor DIP containing closely matched individual resistors in place of all the 5.11-kohm discrete resistors used in the wire-wrap prototype. As with the reference voltages on the logic verify circuitry, the ratio of the values of the resistors is important, not the absolute values chosen.

Calibration and Setup

During initial checkout, you should make some measurements to determine the voltage offset between the output of the DAC-B voltage generator, V_{IHH}, and the actual pins of the PAL socket. The drop across the forward biased diode that connects pin P12 to the ground pin of the PAL you're using (gnd_drop) should also be measured under load. The diode compensates for the saturation voltage of the sink drivers so that a logic low is really near 0 V when referenced to the PAL's GND pin. This drop should be between 0.5 and 0.8 V. These offsets should be included with the value applied to the DAC to compensate for drops in the drivers and the diode.

Calibrating the programmer requires finding the values needed for each DAC to cause a transition on the comparator output when the output crosses the 2.5-V and 10-V reference voltages. Knowing the DAC value at two voltage points lets you calculate the slope of the line in a plot of voltage versus DAC setting. You can then use this plot to find the setting required to generate any voltage within the range of the DACs. You can do all this by software or manually.

Alternatively, you can ignore the reference voltages and use a voltmeter to measure from P12 to P24 of the PAL socket while stepping the digital input value to DAC-A until you get the desired voltage; then take note of this setting for later use. DAC-B is similarly calibrated by measuring V_{IHH} between P12 and one of the output pins with the shift register being loaded to activate that pin and a junk PAL (or resistor) in the socket to provide a realistic load on the driver.

The actual value of the reference voltages should be measured at least once with a voltmeter and the values entered into the program as actual_10V (for 10 V) and actual_2P5 (2.5 V). If you don't have a voltmeter, just enter the nominal values of 2.5 V and 10 V, and you won't be too far off.

The AutoCal subroutine in ZAPAL.C first finds the DAC setting for each DAC corresponding to the transition point at each of the two reference voltages. These transition point values are called DAC_A_low, DAC_A_high, and DAC_B_low, DAC_B_high. The program then calculates the slope of a line between the two points and, using the DAC setting at one of the reference voltages, has all it needs to know to compute the DAC setting for any other voltage, assuming that the DAC output is linear. The slope of the line connecting the two reference points is calculated as follows:

```
slope_a =
   (actual_10V - actual_2P5)
   / (DAC_A_high - DAC_A_low);
slope_b =
   (actual_10V - actual_2P5)
   / (DAC_B_high - DAC_B_low);
```

Then, when you want to find the DAC setting to yield any wanted voltage within the range of the DAC, you can compute it using the following C code:

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Listing 4: *A code extract from ZAP-A-PAL's driver program, ZAPAL.C, showing how you set up the data in the shift register to address a particular fuse.*

```
/*      ZAPAL.C - Byte Magazine ZAP-A-PAL Programmer for IBM PC        */

/*      Version 1.9 - (C) by Robert A. Freedman - 23 Oct 1986 - 8:00 PM */

#define base  0x100
#define DAC_A base+0
#define DAC_B base+1
#define SCLK  base+2

#define STROBE base+0x8
#define ENAB   base+0x9         /* Enable BiMOS drivers */
#define ENCH   base+0xA
#define ENCL   base+0xB
#define VLH    base+0xD
#define VINHIB base+0xE
#define TRIG   base+0xF

#define BUSY            (~inportb(base+0xC) & 1)

static int verpin,vad,fuse;     /* Pin # to verify, I/O adr, State        */
static int veradr[10] = {9,7,6,5,4,3,2,1,0,8};  /* Mux adr for Pins 14 - 23 */

uchar pins[32]; /* Set up pin values here, then shift out to hardware    */

/*              Outputs           Control                 Inputs
        2 2 2 1 1 1 1 1 2 1     1                               1 1
        2 1 0 9 8 7 6 5 3 4   1 3                 2 3 4 5 6 7 8 9 0 1      */
static uchar clear[28] =
        {0,0,0,0,0,0,0,0,0,0, 0,0,0,0,0,0,0,0, 0,0,0,0,0,0,0,0,0,0}; /* Clear */
static uchar odlo[28] =
        {0,0,0,0,0,0,0,0,0,0, 2,1,0,0,0,0,0,0, 0,0,0,0,0,0,0,0,0,0}; /* OD lo */
static uchar odhi[28] =
        {0,0,0,0,0,0,0,0,0,0, 1,2,0,0,0,0,0,0, 0,0,0,0,0,0,0,0,0,0}; /* OD hi */

static int pind[24] =   /* Maps Pin numbers to Shift Register Position   */
        {10,18,19,20,21,22,23,24,25,26,27,28,11,9,7,6,5,4,3,2,1,0,8};

int     n,i,ir,ix,ino,af,T20,fuzno;

int do_a_fuz(fuzno) int fuzno;  /* Set up to read or write a fuze */
{       int half,pin;
        pin = ( fuzno / ( T20 ? 32 : 40 ) );    /* Product-Line #  */

        outportb(ENAB,0);        /* Disable BiMOS drivers        */
        outportb(ENCL,1);        /* Disable BiMOS drivers CLOCK  */
        outportb(ENCH,1);        /* Disable BiMOS drivers OD     */

        half = ( T20 ? 32 : 40 );       /* Set OD and CLOCK pins        */
        pin( 1, (pin >= half?1:2) );    pin(13, (pin >= half?2:1) );

        (pin >= half ? ldsr(odhi) : ldsr(odlo) ); /* Shift OD & Clock */

        outportb(ENCL,0);        /* Enable BiMOS drivers CLOCK   */
        outportb(ENCH,0);        /* Enable BiMOS drivers OD      */

        selfuz(fuzno);  ldsr(pins);     /* Set up and load Shift-registers */

        outportb(ENAB,1);        /* Enable BiMOS drivers */

        return( verifuz() );     /* Read and return state of addressed fuze      */
}
zot()   /* TRIGger the timing PAL to zap the fuze          */
{               while (  BUSY ) { outportb(TRIG,0); };
                while ( !BUSY ) { outportb(TRIG,1); };
                while (  BUSY ) { outportb(TRIG,0); };
                return(0);
```

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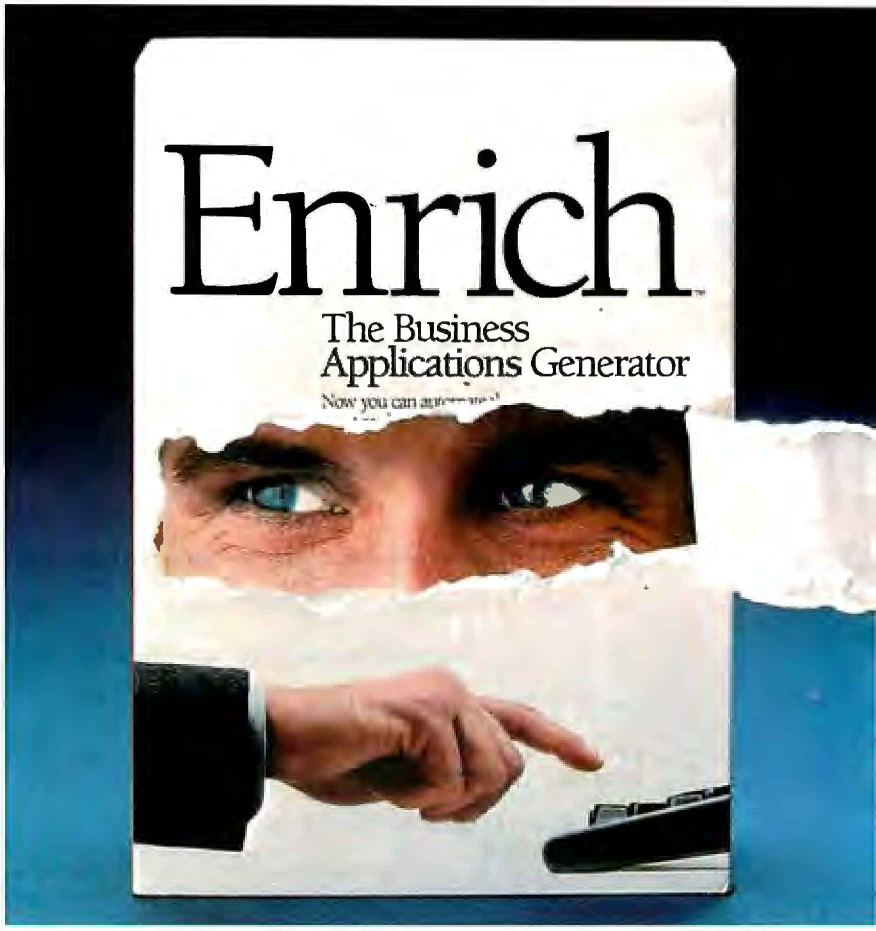

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```
}
int verifuz()   /*      Return state of fuze     */
{
        /* Assume the shift-registers are all set up by selfuz(fuzno);  */
        outportb(ENCL,1);        /* Pulse CLOCK pin by floating  */
        outportb(ENCL,0);        /* CLOCK to Z momentarily       */

        vad = veradr[verpin-14] + base; /* Compute Mux adr of Pin       */
        fuse = inportb(vad) & 1;        /* Read the state of the fuse   */
        /* On 16L8, 16R8 etc PALs, 0 = Blown, 1 = Intact fuse   */
        return(fuse);
}
selfuz(fuzno) int fuzno; /* Analyzes fuze-number and sets up all pins   */
{       int an,half,of,ox,lino,pl,pln,i;

        half = ( T20 ? 32 : 40 ); /* T20 is true for 20, false for 24 pin PAL */

        ldsr(clear);    /* Clear out old fuze info      */

        /*      Compute and place input pins    */

        lino =( fuzno % half );

        pln = ( fuzno / half );
        if (pln > (T20?63:79) ) return(ERROR);

        lr = 0; if   (lino & 2)  lr = 2;        /* Find which half      */

        ix = 0; if (!(lino & 1)) ix = 1;        /* Find the state of Pin x */

        /* Now find where to put the selected input pin, ie [I0..I9]    */

        for (i=0;i<10;i++) pin(2+i,2);  /* Pull all input pins to VIHH  */

        ino = lino / 4; pin(2+ino,ix);  /* Then set Selected pin to TTL */

        /*      Compute and Place Output Pins    */

        pin( 1, (pln >= half?1:2) );    /*      Set OD and CLOCK pins   */
        pin(13, (pln >= half?2:1) );

        pl = pln; if(pln >= half) pl = pln-half;
        an =  pl % 8;                           /* A0..An = pl mod 8    */
        ox = (pl / 8) & (T20?0xF:0x1F);         /* Select Outp Pin to pulse */
        for (i=14;i<=23;i++) { pin(i,0); };     /* Clear all Outputs    */

                        af = (T20?16:15 ); of = (T20?22:23 );
        if ( pln >= half ) { af = (T20?19:19 ); of = (T20?18:18 ); };
        if ((pln <  half) && !T20 ) an = bitinv(an,4);
        an = an & (T20? 7 : 0xF );

        for ( i = (T20?2:3); i >= 0; i--) {  /* Set Address bits  */
                pin(af+i,( an % 2 ? 2 : 0 ) ); an = an / 2;     };

        pin(of-ox,4);           /* Set Output Pin to Pulse              */
        verpin = of-ox;         /* Save pin to verify fuse state        */
        pin( (pln < half ? (T20?15:14) : (T20?22:23) ),lr); /* Set L/R  */
 }      /* Now all the pins are set for programming or verification     */

 int pin(n,val) int n,val;      /* Read or Store value of a pin */
 {int v; uchar *p;        if (n == 0 || n > 24 ) val = 0xE;
                          p = pins + *(pind + n - 1 );
                          v = *p; *p = val; return(v);
 }
 ldsr(p) char *p;       /* Load pins into Hardware Shift Register       */
 {       int i; i=27; while ( i >= 0 ) { outportb(SCLK,p[i--] ); };
        outportb(STROBE,1) ;    /* Strobe all bits into BiMOS latches   */
        outportb(STROBE,0) ;
 }
```

Listing 5: *An annotated JEDEC file.*

```
CUPL          2.11a  Serial# 2-99999-001
Device        p1618  Library DLIB-e-22-8
Created       Thu Oct 09 11:42:26 1986
Name          ZAPAL1 PAL Programmer Address Decoder.
Partno        #12345
Revision      01
Date          8/ 1/86
Designer      Angus Boole
Company       Bovonics Ltd.
Assembly      BYTE ZAPAL programmer
Location      4F
*QP20         ; Specifies the number of pins on the PAL
*QF2048       ; Specifies the number of fuses in the array
*G1           ; Specifies the state of the security fuse
*F0           ; Default state for fuse links not defined below
*L0000 11111111111111111111111111111111        ; Each digit represents a fuse
*L0032 01101011101110111011011110111110        ; 0 means fuse NOT blown
*L0256 11111111111111111111111111111111        ; 1 means fuse IS  blown
*L0288 01101011101110111011101110111110
*L0512 11111111111111111111111111111111
*L0544 01101011101110111011101111111010
*L0768 11111111111111111111111111111111
*L0800 01101011101110111011011111111010
*C1C08                                         ; 16 bit checksum of fuse bits
```

vcc_want = nominal + gnd_drop;
vihh_want = nominal + gnd_drop + offset;

for example:

vcc_want = 5.00 + gnd_drop;
vihh_want = 11.75 + gnd_drop + offset;

dac_a = vcc = DAC_A_low + (vcc_want − actual_2P5) / slope_a;

dac_b = vihh = DAC_B_low + (vihh_want − actual_2P5) / slope_b;

It should be noted that the range of the DACs does not go to 0 V, and that they are not the same. If you set a DAC to a voltage outside its range, it will clamp, and the output will be inaccurate. The range of each DAC is determined by the value of the feedback resistors around the LM-324 op-amps that were chosen to encompass the needed voltages without dissipating excess power in the LM-317s. The voltage ranges for each DAC are

DAC-A range: $2.0 <= V_{CC} <= 11.0$
DAC-B range: $2.0 <= V_{IHH} <= 15.0$

Programming Algorithm

The procedure for blowing a fuse is as follows. Load DAC-A with the correct voltage for the V_{CC} pin. Load DAC-B to set the voltage to V_{IHH}. Load the shift registers with all pins set to 0 except the OD pin to 2 and the CLOCK pin to 1. Pulse the strobe (STR) line to load the data latches. This will set OD to V_{IHH}. Load the shift registers with the proper values for the input (I_0 through I_x) and address (A_0, A_1, A_2) lines with the L/R pin specified, keeping OD as before. Also, set the selected output pin driver to a value of 4. Again, pulse the STR line to load the data latches.

To program the fuse, write 1 to the TRIG latch, wait until BUSY is asserted (or at least 10 μs), then write 0 to TRIG. Wait until BUSY is cleared. You can verify the bit by pulsing the CLOCK pin from low to high and then to low again. This is done by pulsing $\overline{\text{ENCL}}$. The logic level at the selected output pin may be read as bit 0 at the proper I/O address for that pin (check the input section of table 2). If the level is not correct, you can zap the fuse four more times, reading it after each try and waiting between tries so as not to exceed the 20 percent duty-cycle restriction.

When you are done with that fuse, load the shift registers with all pins to 0 except the OD pin to 2 and the CLOCK pin to 1. Pulse the STR line to unload the data latches. This will keep OD at V_{IHH}. Either select the next fuse by loading a new input line and address as above, or load the shift register with all 0s to exit from program/verify mode. A verify operation is as above, except that you don't assert TRIG to blow the fuse. See listing 4 for a code example.

Software Description

I wrote the ZAPAL program to support an interface between commercially available logic design software and the ZAP-A-PAL hardware. The JEDEC format file is produced as the output of a logic design compiler, such as CUPL or PALASM version 2. The JEDEC file contains a fuse map of the target PAL, parametric information, and some documentation (see listing 5).

Support Available

See my article, "Getting Started with PALs" on page 223 for details on obtaining logic design software.

I am preparing a printed circuit board that I am willing to make available at nominal cost to those who wish to build ZAP-A-PAL. I do not intend to offer a kit of parts for this project, but if you cannot find a particular component, I will try to help you out. I will make an assembled board available for those who lack the time or resources to build one for themselves. I am interested in communicating with anyone who has questions about this project or who has found a way to improve on my design. ■

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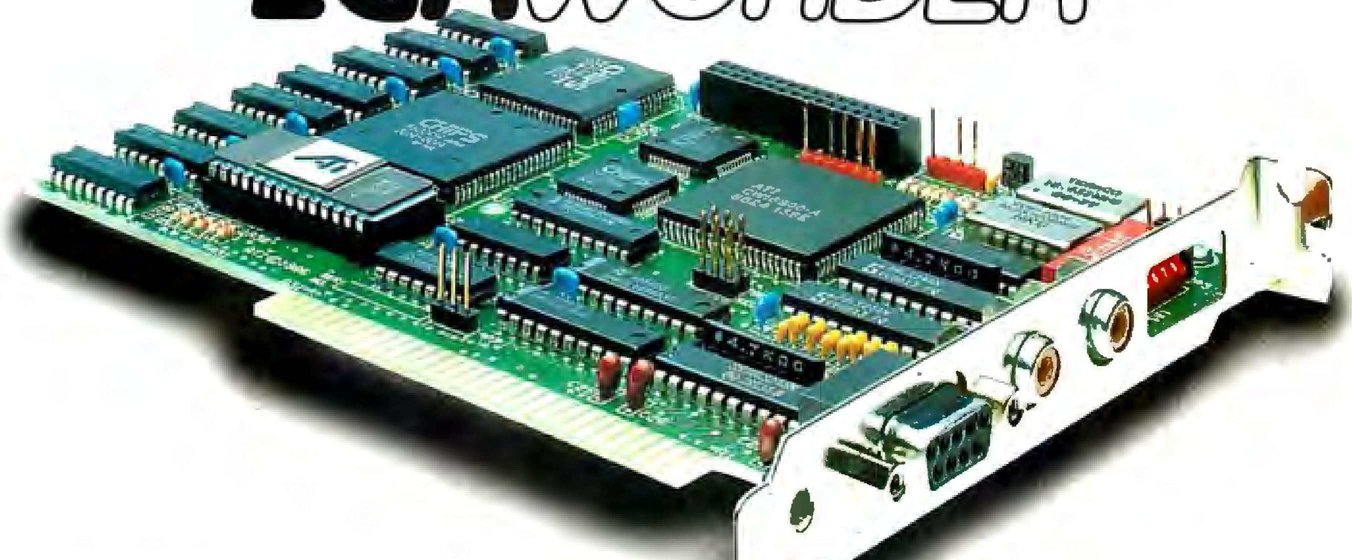

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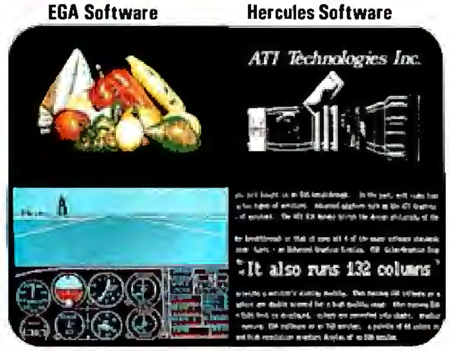

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Reviews

THE STRIDE 440 is a 12-MHz 68000 machine that will appeal to those who require raw computing power and multiuser capabilities. Paul A. Sand concludes that the Stride 440 is a good high-performance tool for program development and other technical applications, although other advanced PCs may fill your bill.

Wayne Rash Jr. takes a look at the Data General/One Model 2. According to Wayne, the Model 2 answers nearly all the criticisms of the Model 1, especially the screen. Its amber electroluminescent display is now as easy to read as a standard CRT. To compensate for the extra power drain, Data General offers an optional battery pack.

The Video Technology Laser 128 is a briefcase-size Apple II clone that offers 128K bytes of RAM, a 5¼-inch floppy drive on its right side, and a variety of standard ports. Valus E. White concludes that the Laser 128 is almost fully hardware compatible with the Apple II series, although he had some problems while running his software collection.

Chris H. Pappas and William H. Murray have reviewed 12 EGA boards. They tested each board with a monochrome display for text resolution, a color display, and an NEC MultiSync monitor. Their conclusions are interesting. All the boards passed the tests for compatibility; Chris and William therefore suggest that you base your purchase on a variety of other factors, particularly the options you require.

Wayne Rash Jr. also compares nine PC AT multifunction cards. He preferred the Cheetah Combo/70 and Card/70, but he raises an important point in his conclusion: Of what use are these cards right now?

Jonathan Angel takes a look at the All Card AT1/M, an expansion board that breaks the 640K-byte barrier with a proprietary memory management unit that can manipulate the 8088's virtual address space more rapidly than boards conforming to the Lotus/Intel/Microsoft expanded memory specification.

Jaime Cuevas Dermody and Jayesh Punater provide the results of Arizona State University's evaluation of 12 IBM PC AT compatibles. Their tests measure computation speeds, hard disk speeds, and software compatibility.

Paul A. Sand also reviews three Modula-2s for the IBM PC and compatibles. In comparison to Modula Corporation's Native Code Modula-2 for the IBM PC and PCollier Systems' Modula-2PC, Logitech's Modula-2/86 compiler generated the fastest and most compact code, and it was closest to supporting the full Modula-2 as defined by Niklaus Wirth. The text box discusses Logitech's Turbo Pascal to Modula-2 Translator, which allows you to overcome the 64K-byte limitation on Turbo Pascal programs.

Frederick D. Davis examines MTBASIC, perhaps the first multitasking BASIC for the IBM PC. Fred found several important features to be disappointing, but the implementation offers enough features to attract some interest.

We have three application reviews this month. Mike Van Horn looks at RuleMaster, an expert system for MS-DOS machines. He found it to be powerful enough to build full-scale expert systems. Warren Block examines Scribble!, a word processor for the Amiga. The program has many fine features, but Warren found the user interface to be inconsistent and the flickering display a distraction. Finally, Mick O'Neil reviews Laser Author, a word processor for the Macintosh. He enjoyed working with the application, but he found that some important features were lacking.

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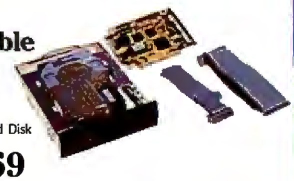

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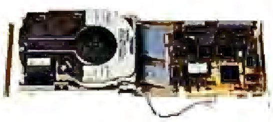

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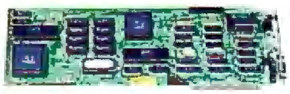

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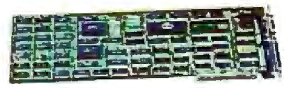

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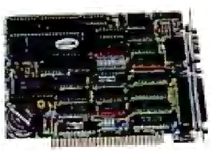

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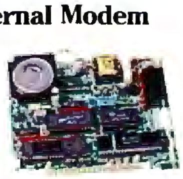

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REVIEWER'S NOTEBOOK

In our second attempt, Stan Wszola and I got WildFire by Software Wizardry (1106 First Capitol Dr., St. Charles, MO 63301, (314) 946-1968) up and running on my Zenith Z-151. We have no idea what the original problem was, but the packaging and documentation are now much improved, and we are very impressed. The Z-151 ran the Sieve of Eratosthenes in 192 seconds. With an 8-MHz NEC V20, it ran in 182 seconds. With WildFire installed, it took only 109 seconds. WildFire includes a V20 and a new chip set that dramatically increases the clock speed. In addition to faster processing, you also gain a hard system reset and a switch between low and high speed.

I am also impressed with Toshiba's T3100. The laptop market may be small, but this 15-pound, 8-MHz IBM PC AT clone is filled with features. It has a 10-megabyte hard disk, 640K bytes of RAM, a 720K-byte 3½-inch drive, and an optional 5¼-inch floppy disk drive. The gas-plasma screen is very readable. The Sieve ran on the system in 51 seconds.

Mike Vose and I tested a product called in-synch from American Video Teleconferencing Corporation (110 Bi-Country Blvd., Farmingdale, NY 11735, (516) 420-8080). This application for IBM PCs and compatibles allows two PCs to transfer data and to share applications in a conference-like environment. We had no trouble installing the program, although we needed two copies because the current version is copy-protected. We were able to transfer files very easily, and we had no trouble "getting in synch." We set up an interactive environment in which we could communicate and watch each other work within an application. It was fun. It works. But I'm not sure how I could use it to my advantage. Anyone have some good ideas?

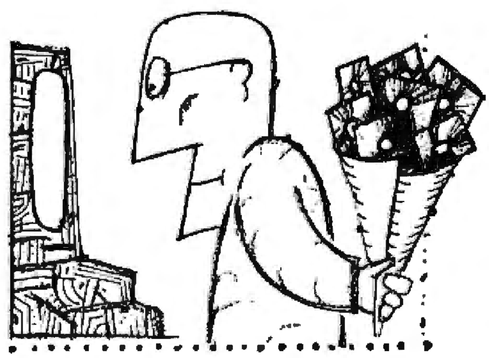
I found another useful software item at the Northeast Computer Faire in Boston in October. Beacon Software International (120 Fulton St., Boston, MA 02109, (617) 523-0090) introduced jot!, a memory-resident multikey macro facility for the IBM PC that is similar to, but less expensive than, Productivity Plus's PRD+. Both programs translate your abbreviations automatically to stored, and presumably longer, text strings. Surprisingly, jot! was not obviously incompatible with SuperKey, SideKick, or Cruise Control (or anything else for that matter), and I found it easy to work with.

We have received a couple of kindred items for the ST and the Amiga. ST-Toolbox from Paperlogic Ltd. (12 Nottingham Place, London W1M 3FA, U.K., telephone: 01-935 0480) provides a command-line interface and batch file capability. System commands include leaving the toolbox; changing, making, and removing the directory; clearing the screen; echoing; and displaying the date and time. You can set the data rate and type, compare files, copy, rename, erase, merge, sort, and search for text strings. You can also display hexadecimal listings of files, count words and characters, and transliterate text files.

For the Amiga, there is Zing! from Meridian Software (P.O. Box 890408, Houston, TX 77289-0408, (713) 488-2144), a series of utilities that extends the operating system. With Zing! installed, you have access to 10 new options, including a file system window that can display up to 100 different files and directories in each page. To use the features, you can assign function keys, or you can use the mouse or a series of menus. Other options include a disk-copy window, a task-monitor window, and a format disk-window, as well as saving the current screen to IFF format.

Our reviewer of the Amiga version of TDI Modula-2 likes the product overall but has found several errors with version 2.00A. Meanwhile, TDI will be releasing an improved version when Commodore/Amiga releases the new version of the Kickstart system software. We'll complete the review then.

Thanks to all of you who answered my request for comments and suggestions

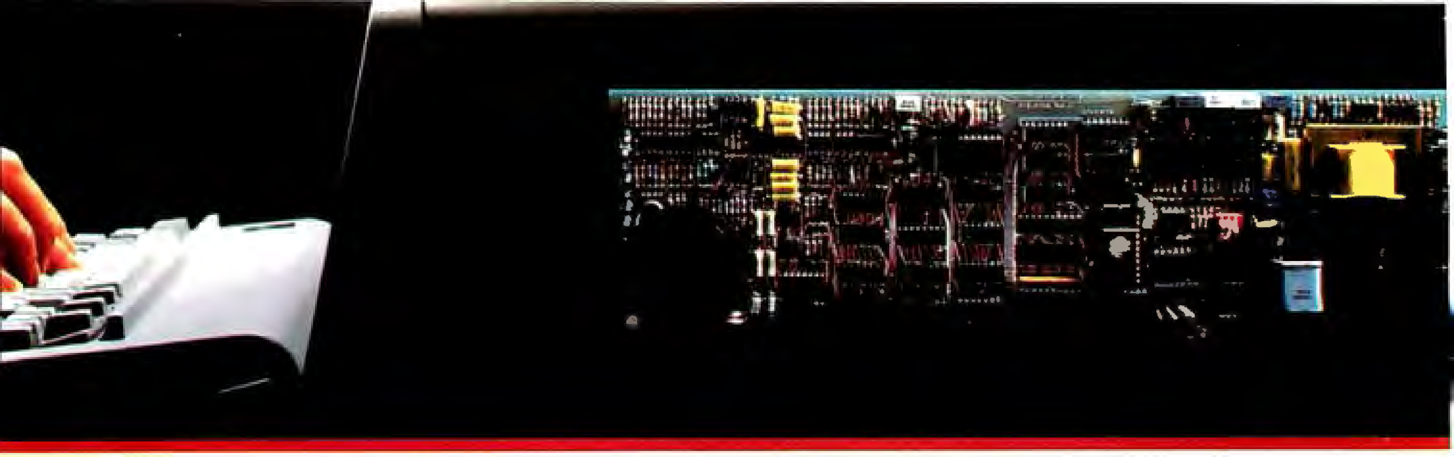


concerning the future of our reviews. I've read them all, and I am pleased that so many of you enjoy the section and that you understand that BYTE insists upon a rigorous ethical code.

We apply our rules very strictly. No manufacturer can know who is reviewing a product until the review appears; none of our reviewers can have even the slightest conflict of interest with the manufacturers; we will not review beta hardware or software; we return all reviewed products to the manufacturers; and all reviews involve intense testing and benchmarking of products. None of our reviews are written from press releases. As many of you noted, these rules mean that we are sometimes not the first to go to press with a review, but I'm immodestly proud of the consensus that ours are the most comprehensive. We shall do our best to stay that way.

Amazingly, almost all the letters either praised or condemned clone reviews. If you're in the market for a clone, they're indispensable. However, if you already own one or have decided that you won't need one, the reviews simply take up space. We will continue to review them comparatively, since there is interest and they make up over 80 percent of our new product arrivals. But the recent reviews of 68000 machines should convince you, I hope, that we're not overly committed to the IBM family. Most of you have enjoyed the comparative reviews, but the final verdict, of course, is not in. Keep those cards and letters coming.

—Jon Edwards
Senior Technical Editor, Reviews



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The Stride 440

Paul A. Sand

A 12-MHz 68000 machine that provides you with raw computing power

The Stride 440 computer system is an interesting blend of traditional and advanced ideas. Like Apple's Macintosh, Commodore's Amiga, and Atari's 1040ST, it incorporates the Motorola 68000 processor. Unlike those systems, however, the Stride 440 uses the 68000 to provide you with raw computing power rather than a more elaborate operating system.

Hardware

The system unit is about the same size and weight as an IBM PC XT, with sufficient room to hold two half-height floppy disk drives and a hard disk. The basic memory configuration on the Stride 440 is 1 megabyte, expandable to 4 megabytes. An optional port board also contains room for installation of 4 more megabytes of RAM, for a total of 8 megabytes. The system that I reviewed contained 1 megabyte of memory.

In addition to the Stride 440, Stride Micro offers the Stride 420 and the Stride 460. The 420 is a lower-cost version of the 440 with limited expansion capability; the 460 has greater expansion capability at a higher price.

The Stride 440 runs its 68000 processor at 12 MHz; in comparison, a Macintosh's 68000 runs at approximately 7.8 MHz, an Amiga's runs at 7.2 MHz, and a 1040ST's runs at 8 MHz. A standard Stride 440 comes with a 640K-byte floppy disk drive; you can add a second floppy disk drive and a 20-, 34-, 47-, or 68-megabyte Winchester hard disk. If you choose a hard disk, the unit will still accommodate a second floppy disk drive or a streaming tape drive for hard disk backup. The system that I reviewed contained one floppy drive and a 33-megabyte hard disk. [Editor's note: *Since this review was written, Stride Micro has changed from using a 33-megabyte hard disk to a 34-megabyte hard disk.*]

The system also includes a real-time clock with battery backup power, 10 RS-232C serial ports, and a Centronics parallel port. The serial ports use RJ-11 (telephone-type) jacks, which are much more compact and easier to connect and disconnect than the more traditional DB-25 connectors.

In addition, Stride offers the following items for expansion: a hardware floating-point processor that uses the National Semiconductor 16081 chip; a memory management option that allows the Stride 440 to run UNIX; a port board that adds 6 serial ports (to the 10 already available) and room for 4 megabytes of additional RAM (in addition to the 4-megabyte capacity of the base system); an IEEE-488 interface board; a graphics board that allows the Wyse terminal to display high-resolution monochrome graphics; and additional hardware that allows connection to a Corvus Omninet network.

Note, however, that the basic Stride 440 has only one empty slot available for the boards mentioned above; if you choose the graphics board, for example, you could not add the IEEE-488 board or the port board. The Stride 460 provides more expansion capability.

Terminal and Keyboard

The 440 connects to ordinary terminals, but Stride Micro recommends Wyse Technology's WY-50 terminal, which Stride Micro supplied with my review unit. The Wyse terminal operates at up to 38,400 bits per second, a rate usable for graphics output with the Stride 440's graphics option. The Wyse's 14-inch diagonal display has a 1-square-foot base, giving it a reasonably small footprint. The display screen sits on a swivel mount on the base, allowing you to adjust it easily to nearly any viewing position.

You can select an extremely legible 80-column text display or a more-difficult-to-read 132-column display. The 132-column display might be useful in limited applications, such as viewing a spreadsheet. When used in graphics mode, the Wyse terminal has a resolution of 784 by 325 pixels.

The Wyse's low-profile keyboard provides a full character set, 16 function keys, and a numeric keypad. The placement of the most commonly used keys is standard, with less common symbols in seemingly

continued

Paul A. Sand (Computer Science Department, University of New Hampshire, Durham, NH 03820) teaches computer science and has written two books on Pascal.

Stride 440 -

Company
Stride Micro (formerly Sage Computer)
4905 Energy Way
P.O. Box 30016
Reno, NV 89502-0016
(702) 322-6868

Size
System unit: 17 by 19 by 6 inches
Monitor: 13 by 13 by 12 inches
Keyboard: 7½ by 17½ by 1¼ inches

Components
Processor: Motorola 68000 running at 12 MHz
Memory: 1 megabyte of RAM
Mass storage: One 640K-byte 5¼-inch floppy disk; options for 20-, 34-, 47-, or 68-megabyte hard disks
Display: 80 or 132 columns by 24 rows (text); 784 by 325 pixels (graphics)
Keyboard: 100 keys; 16 function keys; numeric keypad
Power source: 140 watts, switching

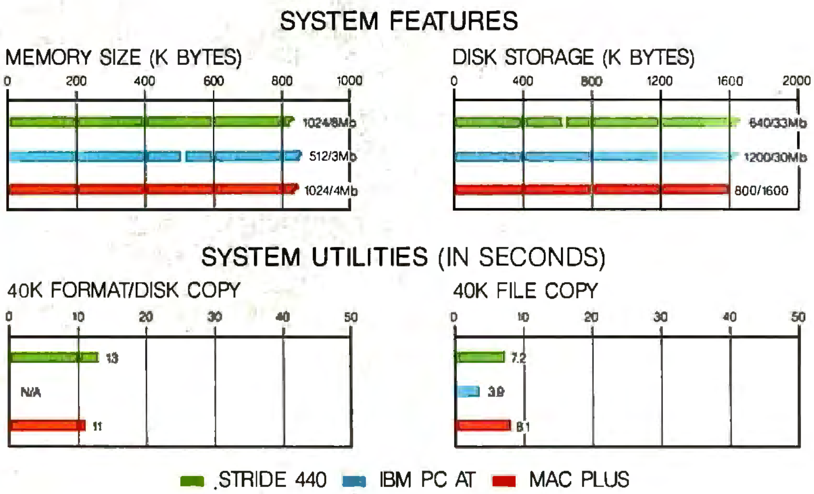
Software
Liaison operating system
(p-System version IV.21 with LAN software)

Options
Second floppy disk drive: $495
Streaming tape drive: $1995
NOD cursor control: $395
Graphics board: $395
Port board: $795
Wyse WY-50 terminal: $595
Memory management option: $650
UNIX System V
  Tape version: $1195
  Floppy version: $1895

Documentation
Operating system reference guide, 300 pages
Owner's manual, 740 pages
Stride Software Directory, 342 pages

Price

Stride 440 with a 20-megabyte hard disk:	$6995
With a 34-megabyte hard disk:	$8495
With a 47-megabyte hard disk:	$9395
With a 68-megabyte hard disk:	$9995



Benchmark	STRIDE 440 Pascal/p-code time	STRIDE 440 Pascal/native code time	STRIDE 440 Modula-2 time	IBM PC AT Basic	MAC PLUS Basic
Disk Write	52.10	52.20	52.80	26	15
Disk Read	26.40	26.40	26.40	24	10
Calculations	6.48	6.24	1.42	27	79
Sieve	3.85	0.343	0.158	80	125

The Memory Size graph shows the standard and optional memory available for the computers under comparison. The Disk Storage graph shows the highest capacity for a single floppy disk drive and the maximum standard capacity for each system. The System Utilities graphs show how long it takes to format and copy a 40K-byte file using the system utilities. The Disk Write and Disk Read benchmark results show how long it takes to write and then read a 64K-byte sequential text file to a blank floppy disk. The Calculations result shows how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The Sieve results show how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. (For the BASIC program listings, see BYTE's *Inside the IBM PCs*, Fall 1985, page 195.) Tests were performed on a Stride 440 running at 12 MHz. All times are in seconds.

random positions around the central alphabetic keys. The most irritating aspect of the keyboard is the small size of the Shift keys; they are barely bigger than the letter keys. I also found the audible feedback from each keystroke distracting; the sound is more like a high-pitched beep than a click. The system's documentation did not explain how to disable the sound.

The NOD

With my review unit, Stride Micro provided a device called the NOD. It is a pointing device, like a mouse, trackball, or joystick, except that it does not require you to use your hands. The NOD shines infrared light at a piece of reflective tape that you place on a wand behind your ear. A sensor inside the NOD detects the difference in the reflected light caused by movement of your head and translates it into serial data. With software support, your head motions can control cursor movements. The NOD uses a normal serial interface and can be used on other computer systems.

I used the NOD in conjunction with a demonstration chess program. I was able to enter my moves successfully, but it was not easy. Relatively precise aiming of the NOD at the reflective tape is important; I sometimes threw the NOD offtrack when I shifted my sitting position. I often found that I could not use the NOD to point at all areas of the screen.

Pictures in Stride Micro's promotional literature show the NOD perched on top of the Wyse display, but the ledge is barely large enough and of doubtful stability to accommodate the NOD in an actual installation. In addition, the photos in the literature do not show the two cables that you must attach to the NOD to make it work (one for power, one for the serial signals).

Software

A wide variety of operating systems run on the Stride 440. The machine comes with Liaison, the p-System from Pecan Software Systems. UNIX System V from AT&T Information Systems and CP/M-68K from Digital Research are also available from Stride Micro for an additional fee. Also available from individual vendors are several other operating systems including Idris, RM/COS, BOS, Tripos, MOSYS, Mirage, FourByteForth, PDOS, and S/1. The key to this flexibility is the Stride 440's multiuser BIOS, which allows the computer to run different operating systems simultaneously for different users.

Liaison is the latest version of the venerable UCSD Pascal operating system. This system includes a screen-based editor

continued

There is not a great variety of applications software available for the Stride 440.

and a file management program. Utilities for system configuration, telecommunications, and sharing resources with a local area network are also included.

The basic p-System does not include programming languages although, for the purposes of this review, Stride Micro provided me with Pecan Software System's Program Development Package, which contains a Pascal compiler and a 68000 assembler. The Pascal compiler allows compilation into either p-code or native code. I also received a Modula-2 compiler from ScenicSoft Inc. that produces true 68000 machine code. FORTRAN-77 and BASIC are also available for the p-System.

Aside from the programming languages, editors, and other software development utilities, there is not a great variety of applications software available for the Stride 440, due mainly to the relative lack of popularity of any of its operating systems among nontechnical computer users. For the Stride 440, there are no equivalents of Microsoft Word, Lotus 1-2-3, or dBASE III. However, if you decide that the computing power and multiuser capability of the Stride 440 are too good to pass up, some word processors, database managers, and spreadsheets are available. Of course, I advise that you examine them carefully before you buy them.

Benchmarks

I ran the four standard BYTE language benchmarks on the Stride 440 using UCSD Pascal and Modula-2 as the programming languages. I translated the Fileio and Floating-Point Calculation benchmarks from the BASIC listings supplied by BYTE, taking care to preserve the spirit of the benchmarks. I took the Sieve of Eratosthenes prime-number benchmark from "Eratosthenes Revisited: Once More through the Sieve" by Jim and Gary Gilbreath (January 1983 BYTE); the only difference was that fewer numbers were tested for primeness in the standard benchmark. [Editor's note: *The benchmarks are available on disk, in print, and on BIX. See the insert card following page 424 for details. Listings are also available on BYTEnet. See page 4.*]

I timed all the benchmarks to the nearest 0.01 second using the Stride 440's real-time clock. For Pascal, I ran both p-code and native code. It is interesting to note that compiling to native code instead of p-code did not greatly speed up either disk I/O or floating-point calculation. It appears that the underlying hardware limits I/O-intensive programs, and most of the time used in floating-point calculations is spent in the underlying library code (which is in machine language anyway), so that relatively little time is saved by recompiling the outer controlling code into native code. The Modula-2 compiler, on the other hand, generated code that was over four times faster than UCSD Pascal's native code generator.

By contrast, the Sieve benchmark is primarily concerned with integer arithmetic and logical operations, the 68000's strong point. Recompiling the Sieve in native code provides a speedup of more than a factor of 10.

In writing and compiling the language benchmarks, I was impressed with the speed and ease with which I was able to move from editor to compiler and back. My previous p-System experience was

continued

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Inquiry 305

My first attempt to write code to time the language benchmarks resulted in nonsensical elapsed times.

with its incarnation as Apple Pascal. The Stride 440 retains all the features I liked in Apple Pascal but is much faster, making it a nice programming environment. The Modula-2 system from ScenicSoft was also easy to use and seems well integrated into the p-System.

I also carried out the standard operating system benchmarks, measuring the time it takes to format a floppy disk and the time it takes to copy a single 40K-byte file from one disk to another. (See page 296 for the results.)

Documentation and Support

The Stride 440's manuals are massive: The two-volume owner's manual is 740 pages long, the reference guide to the operating system contains 300 pages, and Stride Micro also provides a useful 342-page *Stride Software Directory* that contains references to commercially available software that runs on the Stride 440.

The documentation is uniformly dry and technical; it is not suitable for nontechnical users, although it has good indexes. My experience may not reflect the overall quality of the manuals, but I continually found erroneous information, including spelling errors and sample Pascal program segments that could not possibly run correctly.

During my initial setup of the system, for example, I could not get it to perform its initial boot-up using the method described in the documentation. Only a series of long-distance calls to Stride Micro revealed the problem (the serial port for the terminal was initially set to an incorrect speed) and the method for making it work (holding down both the Reset button at the rear of the system unit and the space bar on the keyboard when turning on the system).

In addition, my first attempt to write code to time the language benchmarks resulted in nonsensical elapsed times. After trying nearly everything else, I found the bug was due to a Pascal record definition that I had taken directly from one of the manuals. When I reversed the order of the fields in the definition from the order given in the manual, the code worked.

Unfortunately, Stride Micro's phone support was less than adequate. I typically received useful help only after repeated calls.

Summary

Stride Micro's promotional literature states with refreshing honesty that "our computers are not for everyone." This is certainly true; the Stride 440 is aimed at technical users who are comfortable dealing with the intimate details of operating systems, programming languages, and hardware.

The Stride 440 will appeal to people who need the raw computing power and the multiuser capability it provides. The system is geared toward performance, not toward making novice users feel comfortable.

Stride 440 users will, however, need to put up with the lack of high-quality, low-cost software, as well as relatively weak technical support. In sum, the Stride is a good high-performance tool for program development and other technical applications, although potential buyers should not overlook other advanced personal computers as well. ■


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The Data General/One Model 2

Wayne Rash Jr.

With the introduction of the improved version of its laptop Data General/One, Data General has answered nearly all the criticisms that were published about its earlier version (see my review of the Data General/One, November 1985 BYTE). The new version, called the Data General/One Model 2, is a much more useful portable computer. You're still not going to want to replace your office computer with a Model 2, but that's mostly because of the compromises required to make an IBM PC-compatible computer into a briefcase-size portable.

This laptop is a great improvement over the original model

The most criticized feature of the Data General/One Model 1 was the screen. In some situations it was virtually unreadable. That's no longer an issue with the amber electroluminescent display (ELD). The ELD screen is as easy to read as a standard CRT. The ELD's large power requirements used to eliminate the possibility of using battery power, but Data General now offers an optional battery pack that supplies two hours of portable power.

A much improved LCD screen is also available. While it's not as readable as the ELD screen, it will work fine with normal room lighting. The new gold-colored LCD screen shows much greater contrast than did earlier versions, although its use in dim light would be improved with backlighting such as on the Zenith Z-171 PC and the Toshiba T1100 Plus. The screen has a much greater range of tilt adjustment than it did previously, which makes it easier to achieve reflection-free viewing.

Office use of the Model 2 is enhanced by the ability to use an external color monitor. This can be a significant asset with the LCD screen. The color adapter card slides into the rear of the Model 2 and will support most color monitors.

You must program the Model 2 to use an external monitor through the MODE command, or some software will not use it. In addition, you must set a switch in the proper position. This can cause a problem, since the switch is labeled either *0* and *1* or *on* and *off*. There is no indication of which setting refers to which screen. Data General should relabel the switch *internal* and *external* to eliminate confusion.

The Hard Disk

Most users of IBM PC compatibles are getting used to working with a hard disk on their office computers. In many cases, they want one on the portable, too. To satisfy this need, Data General has stuffed a 10-megabyte hard disk into the Model 2. It replaces the rear floppy disk drive and operates quietly and quickly. Using the hard disk with the LCD screen will reduce battery-charge life by 30 percent.

Conveniences

Data General obviously gave some thought to convenience for users. For example, it has added a carrying handle that swings out from beneath the keyboard. The external power supply now requires only a single cable and provides both power and battery charging.

Due to a major improvement, you no longer have to send your computer to your dealer if you want to add an internal modem, memory expansion, or the color monitor card. Instead, you remove a cover from the rear of the computer and install the accessory yourself.

Service

You may still have to mail your computer to Data General if it breaks and you're not near a dealer, but now that option is a lot more acceptable. For example, you can get a loaner machine from Data General so that you will be out of service for only a day or so. In addition, the repair service is set up so that you will get the same computer back when it's repaired—important for inventory control or for those who lease a computer. Previously, fast service meant swapping computers with Data General.

Conclusions

The Data General/One Model 2 is much improved over the original model of two years ago. The screen is legible, the machine supports a hard disk, and some con-

continued

Wayne Rash Jr. is a member of the professional staff of American Management Systems Inc. (1777 North Kent St., Arlington, VA 22209), where he consults with the federal government on microcomputers.

Data General/One Model 2

Company
Data General Corp.
4400 Computer Dr.
Westborough, MA 01581
(800) 343-8842

Size
13½ by 11½ by 3 inches; 11 pounds

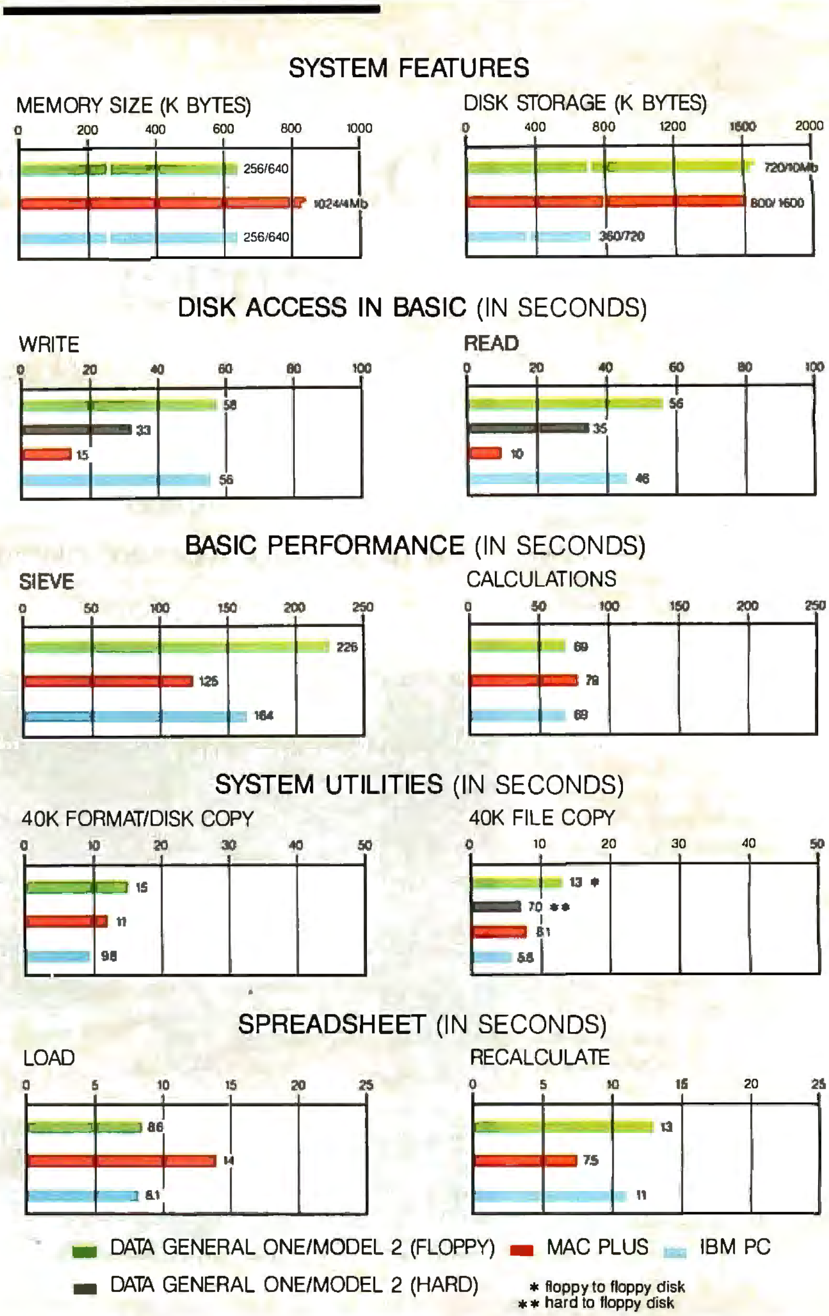
Components
Processor: 80C88
Memory: 256K bytes of RAM (standard)
Mass storage: Two 3½-inch 720K-byte double-sided, quad-density microfloppy disk drives, or one 10-megabyte hard disk drive and one floppy disk drive
Display: 80-character by 25-line display
Keyboard: Proprietary, with numeric keypad superimposed
I/O interfaces: One serial port (second port optional); one parallel port
Graphics resolution: LCD: 640 by 256 pixels; ELD: 640 by 200 pixels

Software
MS-DOS version 2.11

Options
External 5¼-inch disk drive, expansion chassis with disk drive, internal modem, battery, memory expansion, color monitor card, carrying case, thermal printer, GW-BASIC

Documentation
Data General/One Owner's Manual, Guide to MS-DOS, Pocket Reference Guide

Price
LCD model with two 3½-inch disk drives and 256K bytes of RAM: $1995
LCD model with one 3½-inch disk drive and 10-megabyte hard disk drive: $2995
ELD model with two 3½-inch disk drives and 256K bytes of RAM: $2995
ELD model with one 3½-inch disk drive and 10-megabyte hard disk drive: $3995



The Memory Size graph shows the standard and optional memory available for the computers under comparison. The Disk Storage graph shows the highest capacity for a single floppy disk drive and the maximum standard capacity for each system. The graphs for Disk Access in BASIC show how long it takes to write and then read a 64K-byte sequential text file to a blank floppy disk and a blank hard disk. (For the program listings, see BYTE's *Inside the IBM PCs*, Fall 1985, page 195.) The Sieve graph shows how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. The Calculations graph shows how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The System Utilities graphs show how long it takes to format and copy a 40K-byte file using the system utilities. The Spreadsheet graphs show how long it takes to load and recalculate a 25-by 25-cell spreadsheet in which each cell equals 1.001 times the cell to its left. The spreadsheet used was Microsoft's Multiplan. Tests on the DG/One Model 2 were done using MS-DOS 2.11, GW-BASIC 2.02, and Multiplan 1.2. One Data General computer tested had two 720K-byte drives and 256K bytes of memory; the other had one 720K-byte drive, a 10-megabyte hard disk, and 256K.

venience items have been added. Still, all is not perfect. The Model 2 remains unable to support IBM PC communications software, and the LCD screen should have backlighting.

With the greatly expanded market, laptop computer buyers will find a lot more variety out there as well. Where once the DG/One Model 1 was nearly alone in the field of small portable IBM PC-compatible computers, that field has grown considerably and now includes such major players as IBM and Zenith. The Data General/One Model 2 is a much better machine than the Model 1 was, but whether it is the best machine available can only be determined by the requirements of the individual user. ■

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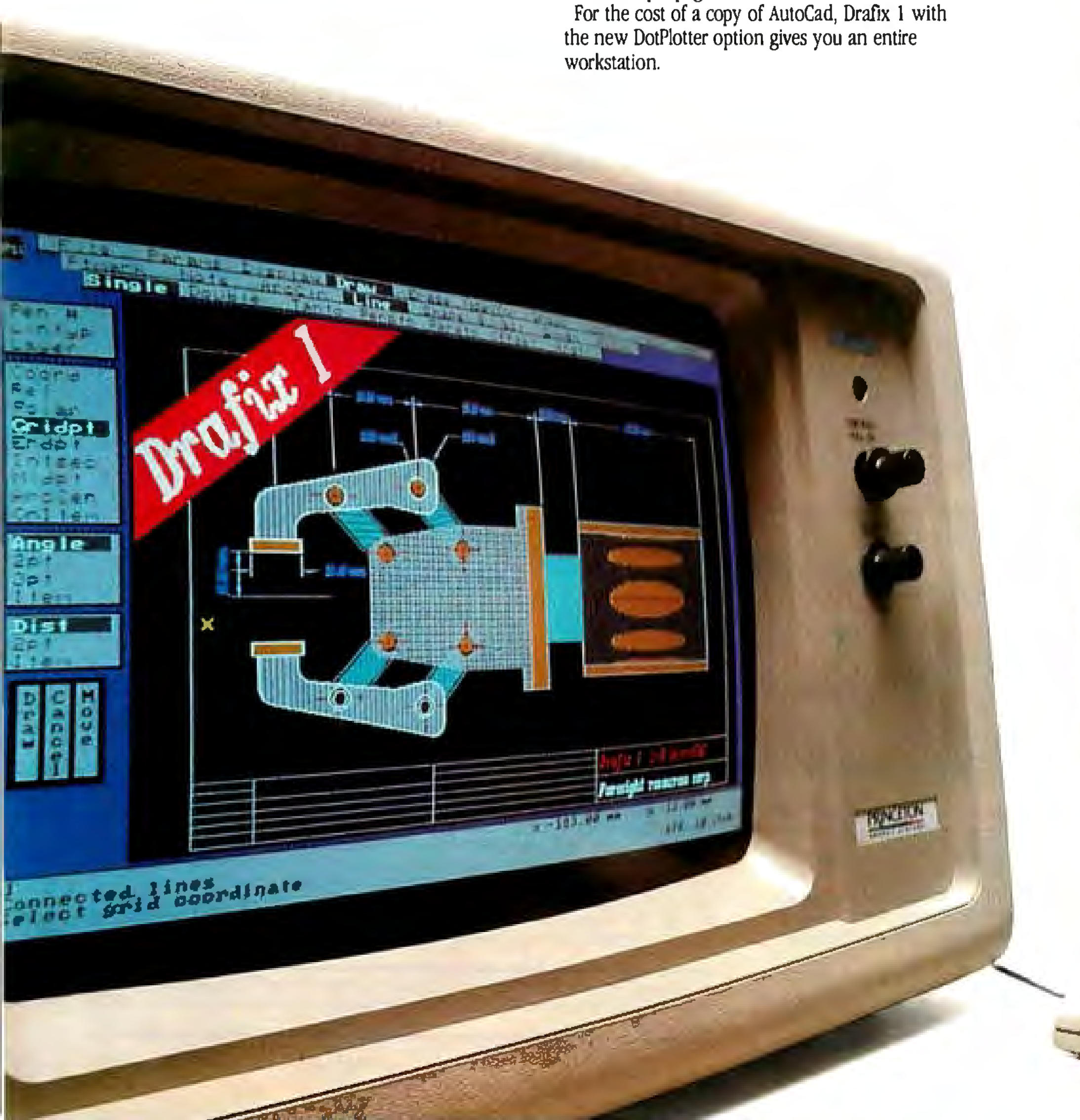

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The Video Technology Laser 128

Valus E. White

A compact and easy-to-use Apple II–compatible computer system

The Laser 128 is a 65C02 microprocessor-based system that has 128K bytes of RAM and a version of Microsoft BASIC in ROM. It is manufactured by Video Technology of Hong Kong and distributed in the U.S. by Central Point Software.

The system is advertised as the most Apple-compatible microcomputer offered and is said to be able to run most Apple programs. As I reviewed this machine, I tried to determine just how compatible it is.

The Laser 128 is relatively small; I managed to pack it into a briefcase. It measures 14½ by 12¼ by 3¼ inches and weighs 12 pounds. The machine has a half-height 5¼-inch floppy disk drive on the right side. The connectors across the back include a mouse/joystick port, a parallel printer port, a video expansion port (for RGB monitors), a composite video output port, a modem serial port (DIN plug), a DIN serial printer port, and a DIN power plug.

The left side of the Laser 128 has a 50-pin Apple II+/IIe–compatible accessory slot designed to receive either an expansion box, which houses two accessory cards, or a single accessory card inserted directly into the slot.

Keyboard

The keyboard has 10 function keys programmed with the most common control keys on the Apple II line of computers. The numeric keypad has 18 keys including Pause, Break, and Enter keys. The Pause key (Control-S) temporarily halts and restarts program execution. The Break key (Control-C) stops execution altogether.

The keyboard has two triangle keys; the white triangle corresponds to the open apple key on the Apple IIe or IIc, and the black triangle corresponds to the closed apple key. The four cursor-control keys are arranged in the same fashion as those on the Apple IIe and IIc. The gray oversize Esc, Tab, Ctrl, Shift, Caps Lock, Delete, and Return keys contrast with the other keys to make them easier to find.

The regular letter and number keys are laid out in QWERTY fashion. A keyboard switch permits you to change from a standard QWERTY keyboard to the Dvorak layout.

The tiny Reset key is located on the left side of the keyboard above the Esc key. On the upper right side of the keyboard are switches for selection of 40- or 80-column displays, monochrome or color video output, and serial or parallel printers. Indicator lights alert you when the drive is accessed, when Caps Lock mode is activated, and when the power is on. The keyboard is more crowded but more comfortable to use than that of the Apple IIc.

Documentation

The Laser 128 comes with a user's guide that is actually two books in one volume. The book is well organized and illustrated and is geared to the first-time computer user. The first section familiarizes you with the computer through instructions and extensive diagrams. The second section is a BASIC language guide. This is followed by various appendixes dealing with error statements and ASCII codes.

The documentation for the Laser 128 lacks a list of key memory addresses (e.g., location of the graphics soft switches) and instructions for using the double-high-resolution modes. Otherwise, it is very well done.

Testing

I tested the Laser 128 in various ways for performance and compatibility with the Apple II series.

For example, I made side-by-side comparisons with both an Apple IIc and a II+. I also selected software to test compatibility in the areas of general use, graphics, BASIC and Pascal applications, and ProDOS operation. In addition, I studied the similarity of the architectures of the Laser 128 and the Apple machines.

Hardware Tests

Because the Laser 128 is equipped with only one internal floppy disk drive, I plugged in a Disk II controller and two additional disk drives. The Apple II series

continued

Valus E. White (1433-C Chanute Place, Washington, DC 20336) is a microcomputer programmer and staff consultant for the U.S. Department of Defense.

Laser 128

Type
8-bit Apple II compatible

Company
Central Point Software
9700 Southwest Capitol Hwy.
Suite 100
Portland, OR 97219
(503) 244-5782

Size
14½ by 12¼ by 3¼ inches; 12 pounds

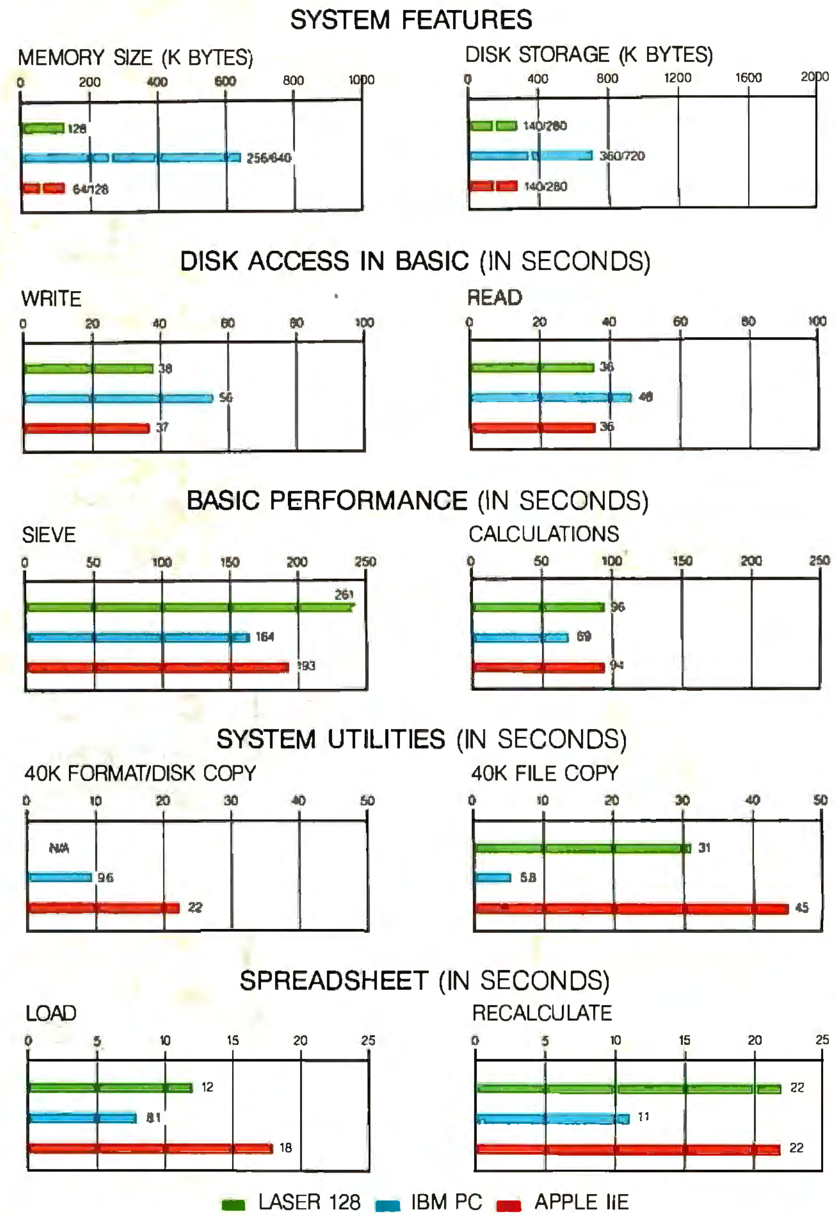
Components
Processor: Western Technologies' 65C02 running at 1 MHz
Memory: 128K bytes of RAM
Mass storage: One built-in 5¼-inch half-height single-sided floppy disk drive, 140K-byte formatted capacity; port for second disk drive in rear of system
Expansion: One Apple-compatible expansion slot corresponding to Apple slot 7

Software
Comes with an Applesoft-compatible version of Microsoft BASIC and Copy II Plus version 6.0, a disk editing and copying utility; runs DOS 3.2, DOS 3.3, Apple Pascal, Apple CP/M, and Apple ProDOS operating systems

Documentation
196-page user's guide

Price

Basic system:	$395
Hardware updates:	$25 each
Parallel, serial, and RGB cables:	$25 each



The Memory Size graph shows the standard and optional memory available for the computers under comparison. The Disk Storage graph shows the highest capacity for a single floppy disk drive and the maximum standard capacity for each system. The graphs for Disk Access in BASIC show how long it takes to write and then read a 64K-byte sequential text file to a blank floppy disk. (For the program listings, see BYTE's *Inside the IBM PCs*, Fall 1985, page 195.) The Sieve graph shows how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. The Calculations graph shows how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The System Utilities graphs show how long it takes to format and copy a disk (adjusted for 40K bytes of disk data) and transfer a 40K-byte file using the system utilities. The Spreadsheet graphs show how long it takes to load and recalculate a 25- by 25-cell spreadsheet in which each cell equals 1.001 times the cell to its left. Tests on the Laser 128 and the Apple IIe used ProDOS and DOS 3.3 with Microsoft's Multiplan. The IBM PC was tested with PC-DOS 2.0.

polls from slot 7 down looking for a disk drive controller, so I expected the Disk II to boot, since the Laser 128's accessory slot corresponds to slot 7. It worked successfully with DOS 3.3 and ProDOS but not with Pascal because Pascal expects to boot from slot 6. I had up to four drives available under ProDOS: the internal floppy disk drive, the RAM disk recognized by ProDOS, and the two external drives. I didn't use the drive port on the rear of the Laser 128 for this test. I installed a drive in the second drive port in the back of the machine and removed the contoller card from the slot to run the Pascal p-System.

I also tried using an Axlon 128K-byte memory board, an Apparat EPROM burner, a clock/calendar board, and a Pkaso parallel printer card with the Laser 128. I used the Pkaso to dump graphics as well as text. Everything worked well. Apparat's software would not boot on the Laser 128, although it worked well on the Apple II+.

I also used the parallel and mouse ports on the back of the Laser 128, but I didn't use either serial port due to my lack of serial devices. I used a generic Apple IIc mouse and Mousepaint successfully. There was no difference between the IIc and the Laser 128 with respect to the operation of the mouse.

The Laser 128's parallel port is a plain Centronics interface. The Laser 128 allows an optional readjustment of the parallel port configuration each time you boot a new software package. You must hit the P key upon boot-up and then step through a reconfiguration menu. This process, which also applies to the serial ports, was convenient. The Laser 128 also lets you adjust the sensitivity of the mouse.

Software

I tested the Laser 128 with a wide range of software with mixed results. AppleWorks ran flawlessly, but I encountered problems with the other software. Apple Writer 1.0 worked on neither the Apple IIc nor the Laser 128. It loaded and ran, but the characters were unreadable because the old version of AppleWorks uses the high-order bit to compensate for the lack of lowercase display capability of the early Apple IIs.

The Laser 128 ran all features of Apple Writer II except for importation of Apple Writer 1.1 files. Multiplan ran on the Laser 128, but the mouse characters moved distractingly. Attempting to use The Spreadsheet 2.0 marketed by Magicalc without the IIe enhancement produced glaring mouse characters on the Laser 128 at the spreadsheet borders in 40-column mode, but it ran correctly in 80-column mode. I used Extra K by Beagle Brothers to test out the additional memory that brings the machine up to 128K bytes. The operation was slow on the Laser 128. Extra K allows for the simultaneous operation of a ProDOS environment and a DOS 3.3 environment within a single 128K-byte machine. This was a good test to see if on-board memory is handled the same way.

The graphics programs I tested revealed flaws in the Laser 128's compatibility with both the Apple IIc and the II+. Using Alpha Plot on a II+ and a IIc, I was able to produce drawings and label them with print that was right-side up, sideways, and upside down. With the Laser 128 I was able to draw, but an attempt to invoke the text routines was met with the hi-res screen drawing random lines and locking up the computer, forcing me to turn the machine off and back on again. Mousepaint with the Apple mouse worked well on the Laser 128. I ran Galactic Trader by Broderbund to test both the graphics and the machine's ability to use DOS 3.2. Both worked correctly. Copy II Plus version 6.0

continued

comes with the Laser 128, but I used my own copy, which worked flawlessly. I also tested some homebrew programs in Pascal and BASIC; all worked correctly.

Strengths and Weaknesses

The Laser 128 has several strong points. The parallel printer port and the numeric keypad are built in. The accessory slot on the left side of the computer is convenient; it opens the architecture of the machine.

The keyboard, though noisy, is comfortable and easy to use. The placement of the arrow keys away from the numeric keypad is of immeasurable value in doing spreadsheets.

As with all computers, the Laser 128 does have its weaknesses. It is not 100 percent software-compatible with the Apple II. It does, however, seem almost totally hardware-compatible as far as accessories are concerned. The failure of the Apparat board to function is puzzling, however, and the graphics incompatibilities are disappointing. The fact that Central Point Software packs a questionnaire sheet with the computer asking customers to list any incompatibilities they have found shows that the company is interested in resolving this issue.

Central Point Software says it will provide updates for $25 and that if you send a broken machine in, it will be fixed. However, I would have preferred local distributors and authorized repair facilities.

Help on how to exploit some of the hardware features is nowhere to be found in the documentation. Since the Laser 128 does not have a large following or support system like the Apple II machines, there should be more information on the hardware and software in the documentation.

Conclusions

The Laser 128 is not 100 percent compatible with the Apple II series due to hardware and firmware differences, but the machine will run software that does not bypass the resident disk operating system and address the hardware directly. This means that most of the software written for the Apple II series is compatible with the Laser 128, including AppleWorks.

The Laser 128 is easy to use, fun, and convenient. It is small enough to travel with. The design is well thought out. The combination of IIc convenience and an expansion slot is perfect for those who want an Apple II–class computer. The system's technical weaknesses are relatively minor, and the $395 list price makes it an attractive alternative. The Laser 128 is perfect for someone looking for a second computer or an inexpensive first computer that runs the largest pool of software available today. ■

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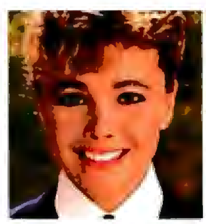

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EGA Times 12

Chris H. Pappas and William H. Murray

An examination of a dozen EGA boards from several companies

In this review we will examine 12 different EGA (enhanced graphics adapter) boards: the AST-3G Model 1 from AST Research, the MegaGraph Plus from ATronics, the Basic Time EGA from Basic Time, the Everex Enhancer EV-654 from Everex Systems, the Spectra EGA Card Model 4800 from Genoa Systems, the TurboEGA from Orchid Technology, the AutoSwitch EGA from Paradise Systems, the QuadEGA+ from Quadram, the SigmaEGA! from Sigma Designs, the EGA Plus from STB Systems, the Eva from Tseng Laboratories, and the VEGA from Video-7.

We tested 11 of these boards on an IBM PC AT running at 9 MHz with an 80287 coprocessor. The TurboEGA was tested on an IBM PC. We tested each board on an IBM monochrome display for text resolution (and Hercules compatibility where applicable), an IBM color display, and an NEC multisync monitor. Tables 1 and 2 list and compare the important features of each board.

The IBM EGA Standard

IBM, which introduced the EGA and enhanced color display and established the standard that clone makers have tried to meet, describes the EGA as "a graphics controller that supports both color and monochrome direct-drive displays in a variety of modes." In other words, the EGA directly drives the IBM color display, monochrome display, and enhanced color display. The various display modes are shown in table 3. MODE.ASM is an assembly language program that lets you switch screen modes, a frequently needed function, via a BIOS interrupt. This program will run on any of the EGA boards reviewed here. [Editor's note: *MODE.ASM is available on disk, in print, and on BIX. See the insert card following page 424 for details. Listings are also available on BYTEnet. See page 4.*] More information on the use of BIOS routines can be found in the IBM *Technical Reference* manual.

Prior to the EGA, many user-configured systems included both monochrome and color display adapters and monitors to take advantage of both high-quality monochrome text and graphics, but a two-monitor system has its own set of problems. The EGA solved the dual-display problem but required a new BIOS, which is included on IBM's EGA board and is described in the IBM *Technical Reference* update of August 2, 1984. Clone makers then faced the problem of duplicating that BIOS. However, due to copyright restrictions, they could not merely copy IBM's code but instead had to duplicate its operation.

The EGA boards that we tested for this review succeeded; they worked according to specifications and, except for some minor time variations, performed identically to IBM's.

Since the EGA clone manufacturers write the BIOS routines, the door is open for a little free advertising. Every time you boot up your computer, instead of being greeted with a blank screen until system checkout is complete, many boards now greet you with an advertising message. We found this annoying, so we tried to delete it. However, reprogramming the EPROM chip would not work because the system checks to make sure the message is there before bringing the EGA on board. Annoying or not, the advertisements are unavoidable.

Quality Standardization

A kind of quality standardization has occurred among EGA boards. Chips and Technologies produces a high-quality four-chip set for the clone makers that very closely duplicates IBM's functions. The great majority of the boards we reviewed here use this set.

Much of the work of duplicating IBM's EGA functions involves duplicating external registers—more than 50 of them. If you want to program these registers, you will need the August 2, 1984, edition of the IBM *Enhanced Graphics Adapter* manual. It describes, in abbreviated form, the name, use, and addressing method of each of these registers.

All the boards that we reviewed successfully ran software from the major areas of interest, including word processing, spreadsheets, business graphics, and CAD. We even tested each board with software provided by Softel Incorporated. Softel boldly states that "if the manufacturer's product can run our demo, then the board is, in our opinion, compatible with the IBM EGA board."

Standard Features

To install any of the 12 EGA boards, you need only define the monitor type and the number of display adapters present and set the jumpers for an optional parallel port. All the boards tested came with the 256K bytes of memory necessary to implement 16 out of 64 colors on both the color and enhanced displays. The additional memory—192K bytes above IBM's minimum configuration of 64K bytes—also supports up to eight pages, depending on the mode. Each board is capable of driving any one of the three types of displays and can be configured to be your system's primary or secondary display adapter.

Other standard features include two ROM character fonts, the ability to generate 512 user-definable characters (which

continued

Chris H. Pappas and William H. Murray are professors at Broome Community College (Binghamton, NY 13902). Chris has an M.S. in computer science from the Thomas Watson School of Advanced Technology, SUNY Binghamton, and William has an Ed.D. in science education from Temple University.

Table 1: *EGA features at a glance. All power-draw measurements are in watts.*

Product name	Company	Price	Card size	Chip count	Chip type	Board layout	Power draw	Warranty
AST-3G Model 1*	AST Research Inc. 2121 Alton Ave. Irvine, CA 92714 (714) 863-1333	$550	full	41	CHIPS	DIP	4.900	2 years
MegaGraph Plus	ATronics International Inc. 491 Valley Way Milpitas, CA 95035 (408) 943-6629	$549	1/2	23	CHIPS	DIP	4.750	1 year
Basic Time EGA	Basic Time Inc. 3040 Oakmead Village Dr. Santa Clara, CA 95051 (408) 727-0877	$349	full	43	CHIPS	DIP	4.250	1 year
Everex Enhancer EV-654	Everex Systems Inc. 48431 Milmont Dr. Fremont, CA 94538 (415) 498-1111	$399	3/4	39	CHIPS	DIP	3.850	1 year parts; 6 months labor
Spectra EGA Card Model 4800	Genoa Systems Corp. 73 East Trimble Rd. San Jose, CA 95131 (408) 945-9720	$449	full	41	CHIPS	DIP	4.125	1 year
TurboEGA	Orchid Technology 47790 Westinghouse Dr. Fremont, CA 94539 (415) 490-8586	$945	full	59	CHIPS	DIP	12.000	1 year
AutoSwitch EGA	Paradise Systems Inc. 217 East Grand Ave. South San Francisco, CA 94080 (415) 588-6000	$599	1/2	31	Paradise	DIP	4.000	1 year
QuadEGA+	Quadram Corp. One Quad Way Norcross, GA 30093 (404) 923-6666	$495	1/2	28	CHIPS	surface	5.250	2 years
SigmaEGA!	Sigma Designs Inc. 46501 Landing Parkway Fremont, CA 94538 (415) 770-0100	$495	1/2	18	CHIPS	DIP	1.750	1 year
EGA Plus	STB Systems Inc. 601 North Glenville, #125 Richardson, TX 75081 (214) 234-8750	$495	full	41	CHIPS	DIP	3.450	2 years
Eva	Tseng Laboratories Inc. Newtown Industrial Commons 205 Pheasant Run Newtown, PA 18940 (215) 968-0502	$525	full and piggy-back	61 (incl. piggy-back)	Tseng Labs.	DIP	7.150	1 year
VEGA**	Video-7 Inc. 550 Sycamore Dr. Milpitas, CA 95035 (408) 943-0101	$499	1/2	28	CHIPS	surface	5.000	2 years

*Since this review was completed, the manufacturer has discontinued this model.
**Since this review was completed, the manufacturer has released a new model, the VEGA Deluxe.

is more than enough for a custom character set), and smooth panning and scrolling. Each manufacturer implements the ROM character fonts in its own style; for instance, some show zeros with a superimposed slash, and some show uppercase *O*s as ovals, while others show them as rounded boxes.

Optional Features

Several of the 12 boards include additional software and hardware options, including Hercules graphics emulation (720- by 350-pixel resolution on the monochrome monitor), software selection of video output modes to override the cold-boot default settings, and external toggle

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* AC voltage: 200mv — 750v, 5 ranges
* Resistance: 200 ohms — 20M ohms, 6 ranges
* AC/DC current: 200uA — 10A, 6 ranges
* Capacitance: 2000pf — 20uf, 3 ranges
* Transistor tester: hFE test, NPN, PNP
* Temperature tester: 0° — 2000° F
* Conductance: 200ns
* Fully over-load protected
* Input impedance: 10M ohm

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* Resistance: 200 ohms — 20M ohms, 6 ranges
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* Input impedance: 10M ohm
* 180 x 86 x 37mm, weighs 320 grams

DMM-700 $49.95

3.5 DIGIT AUTORANGING DMM

Autorange convenience or fully manual operation. Selectable LO OHM mode permits accurate in-circuit resistance measurements involving semi-conductor junctions. MEM mode for measurements relative to a specific reading. Probes and battery included.

* Basic DC accuracy: plus or minus 0.5%
* DC voltage: 200mv — 1000v, autoranging or 5 manual ranges
* AC voltage: 2v — 750v, autoranging or 4 manual ranges
* Resistance: 200 ohms — 20M ohms, autoranging
* AC/DC current: 20mA — 10A, 2 ranges
* Fully over-load protected
* Audible continuity tester
* Input impedance: 10M ohm
* 150 x 75 x 34mm, weighs 230 grams

DMM-100 $29.95

3.5 DIGIT POCKET SIZE DMM

Shirt-pocket portability with no compromise in features or accuracy. Large, easy to read .5" LCD display. 2000 hour battery life with standard 9v cell provides over two years of average use. Probes and battery included.

* Basic DC accuracy: plus or minus 0.5%
* DC voltage: 2v — 1000v, 4 ranges
* AC voltage: 200v — 750v, 2 ranges
* Resistance: 2k ohms — 2M ohms, 4 ranges
* DC current: 2mA — 2A, 4 ranges
* Fully over-load protected
* Input impedance: 10M ohm
* 130 x 75 x 28mm, weighs 195 grams

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* Bright 5" CRT
* TV Sync filter

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* Basic DC accuracy: plus or minus 1%
* DC voltage: 2v — 500v, autoranging
* AC voltage: 2v — 500v, autoranging
* Resistance: 2k ohms — 2M ohms, autoranging
* Fully over-load protected
* Input impedance: 11M ohm
* 162 x 28 x 17mm, weighs 75 grams

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Table 2: *EGA special features (as advertised by the manufacturers).*

Product name	AST-3G Model 1	MegaGraph Plus	Basic Time EGA	Everex Enhancer EV-654	Spectra EGA Card Model 4800	TurboEGA	AutoSwitch EGA	QuadEGA+	SigmaEGA!	EGA Plus	Eva	VEGA
Operating system												
PC, XT, and AT	X	X	X	X	X		X	X	X	X	X	X
Compatibles	X	X	X	X	X		X	X		X	X	X
PC and XT only						X						
Hardware options												
Parallel port	opt.		X	X	X					X	X	
Feature adapter	X	X	opt.		X	X	X	X	X		X	X
RCA jacks	X	X	opt.			X	X	X	X		X	X
Light-pen connector	X	X	X		X	X	X	X	X	X	X	
DIP switch location												
Rear panel	X	X				X	X	X	X			X
Onboard			X	X	X					X	X	
Software												
Hercules emulation		X				X	X	X	X		X	X
CGA, MDA emulation	X	CGA	X	X	X	X	X	X	X	X	X	X
Manufacturer's diagnostics	X				X			X	X		X	X
ROM date					X	X	X	X	X			X
scrnsave						X		X	X			X
Electronic disk, print buffer, extended/expanded memory support										X		

Table 3: *Valid EGA modes. Attachment of proper display options is required for safe and effective use. Resolution measurements are in pixels, and text dimension measurements are in characters. Note: Calls to video modes with improper equipment can result in damage to cards and monitors.*

Mode	Type	Maximum resolution	Text dimension	Display	Pages
0	Alpha	640 by 200	40 by 25	Color (b/w)	8
1	Alpha	640 by 200	40 by 25	Color	8
2	Alpha	640 by 200	80 by 25	Color (b/w)	8
3	Alpha	640 by 200	80 by 25	Color	8
4	Graphics	320 by 200	40 by 25	Color	1
5	Graphics	320 by 200	40 by 25	Color (b/w)	1
6	Graphics	640 by 200	80 by 25	Color (b/w)	1
7	Alpha	720 by 350	80 by 25	Monochrome	8
D	Graphics	320 by 200	40 by 25	Color	8
E	Graphics	640 by 200	80 by 25	Color	4
F	Graphics	640 by 350	80 by 25	Monochrome	2
10	Graphics	640 by 350	80 by 25	Hi-res EGA	2

switches to alter the cold-boot defaults.

For an EGA board to function properly, the main system BIOS must be dated after October 27, 1982. Several of the boards come with a program that verifies your system's BIOS date, along with a diagnostics program to verify that the selected monitor modes function properly. Additional options include an LPT1-, LPT2-, or LPT3-configurable parallel port and a clock/calendar.

IBM's EGA includes a feature adapter and an associated pair of RCA jacks. IBM has not announced the purpose of these features. As a result, the EGA clone manufacturers are divided as to whether or not to duplicate them. Several of the boards that we tested did not include them, which may or may not present a future compatibility problem.

Additional Features

Although the majority of the features for all 12 boards are listed in tables 1 and 2, some of the boards have additional capabilities that make them unique. These unique traits are important only if they affect your use of the board.

The parallel port connector on the AST-3G Model 1 is cabled to the EGA board, which permits its insertion into an empty rear-panel adapter slot or allows it to hang free. The Everex Enhancer EV-654 board is shipped with a mode-control program that allows software selection of monitor type, resolution, and the board's primary- or secondary-monitor driver status. The Spectra EGA Card Model 4800 comes with software that lets you select monitor modes.

The TurboEGA board comes with an 80286 microprocessor, enabling graphics to run on an IBM PC or PC XT at close to PC AT speeds. The board also contains a socket for an optional 80287. The 80287 was not installed on our test board, which invalidated our speed test comparisons

continued

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with the other boards. To complicate matters, our IBM EGA board had 128K bytes of memory and was a poor comparison to the 256K TurboEGA board.

The AutoSwitch EGA card can automatically select the appropriate mode for the software/hardware configuration currently needed; it worked flawlessly. A disk that comes with the board includes a PEGA.COM program that permits software selection of autoswitch mode or monitor resolution.

From a hardware perspective, both the QuadEGA+ and VEGA boards are engineering marvels, with their predominantly surface-mounted chip design. The SigmaEGA! board also has an impressive design that uses mostly VLSI, which dramatically reduces power consumption.

If you're a novice at board installation and operation, you may want to consider the EGA Plus board, which is shipped with a comprehensive installation program supported by a help facility that explains various board options. These options include StopList, a program that allows slow-motion screen display of data; Quick Start (for IBM PC users only), which permits you to set memory switches to a minimum configuration to facilitate quick, cold boots; and Warm System Reset, which enables a nondestructive boot. After the system is initialized, the EGA Plus board will utilize all available memory. For Symphony and Framework users, the EGA Plus board is shipped with EGA drivers that enable these programs to fully utilize the additional capabilities of the EGA monitor.

The Eva board is the only full-size board that we tested with a piggyback board. The piggyback board is known as the CMII option and enables the EGA board to emulate Hercules and Color Graphics Adapter modes. Depending on internal hardware options, the piggyback board could present an insertion problem. The parallel port adapter hangs from the rear of the system on a cable that can be inserted in an empty slot.

Software included with the board contains an installation program, text-mode selection (132 by 25, 28, or 44 characters, or 80 by 25 or 43 characters), and replacement ANSI.SYS drivers for the enhanced modes. The Eva board is only partially compatible with software written for the CGA or the Hercules graphics card unless the optional CMII daughterboard is installed. The Eva board comes bundled with additional drivers, enabling Lotus 1-2-3 and Symphony to run in all available Eva text modes.

Test Results

We tested the 12 boards with the latest versions of Lotus 1-2-3, WordPerfect, Energraphics, and AutoCAD. These products conform to IBM's rules for graphics display; hence, there were no difficulties with any of the boards. We also tested a demonstration program from Connell Scientific Graphics that illustrates much of the graphics glitter that the EGA is capable of producing; an assembly language program from *80386/80286 Assembly Language Programming* (Murray and Pappas, Osborne/McGraw-Hill, 1986) that makes calls to the BIOS routines when drawing a sine wave; and the Softell program, which tests for compatibility with the IBM EGA board. All 12 boards performed these tests flawlessly with occasional minor differences in speed.

Well-behaved software will run on any of the boards tested. However, software developed for the color graphics card that writes directly to hardware registers, bypassing BIOS and all warnings for compatibility, is considered poorly behaved. Such software must be individually tested to find out if it will operate correctly on a specific board, regardless of CGA compatibility. All the boards come with sufficient documentation to allow proper EGA board installation and operation.

The only problem that we encountered during testing was a minor one on the Eva board, whose ROM character font set did not include a null character, which was expected by the Connell Scientific demonstration program. Tseng Laboratories says that the problem has been fixed in the boards it is currently shipping.

Conclusions

Since all the boards that we tested passed all the tests for compatibility, the decision for purchasing a specific board rests on features such as size, price, and options. Other factors to consider include card length, ease of access to monitor-selection DIP switches, parallel port, clock/calendar, Hercules graphics emulation, and a light pen or feature adapter. Before selecting an EGA board, you should contact either the board manufacturer or the publisher of your favorite software to see if they will run together. Our experience indicates that if there is a problem, one of the two will have the fix. Any of the 12 EGA boards reviewed here will let you start enjoying the world of EGA color. ■

Nine PC AT Multifunction Cards

Wayne Rash Jr.

One of the attractions of the IBM PC AT and its many clones is the ability to handle great amounts of memory. The Intel 80286 microprocessor used in these machines will address up to 16 megabytes of memory. Thus, a variety of boards that add significant amounts of memory to PC AT–compatible computers have appeared on the market. These boards frequently add some other functions, such as serial and parallel ports, as well. Unfortunately, MS-DOS still restricts you to 640K bytes of main memory. However, some other operating systems, such as XENIX and Concurrent PC DOS, can use more memory. A few programming languages can also go beyond the 640K-byte limit.

Some applications can make use of a type of additional memory, called *expanded* memory, that conforms to the Lotus/Intel/Microsoft expanded memory specification (EMS). Some memory boards use *extended* memory, an IBM addition, which these applications programs can't use. Either type can be set aside as a RAM disk to speed up operations that require a lot of disk accesses.

The Cards and Their Features

I reviewed nine multifunction cards for the PC AT and its clones: Cheetah International's Combo/70 and Card/70, Quadram's Liberty-AT and Quadboard-AT, AST Research's Advantage!, Tecmar's Maestro AT, Everex Systems' Magic Card 16, Sigma Designs' Maximizer AT, and PC's Limited's AT Multifunction Card. I tested each board in an Epson Equity III running at 6 MHz with one wait state, a 6-MHz Zenith Z-241 with no wait states, and an 8-MHz Zenith Z-248, also with no wait states. The various features of all the boards are compared in table 1.

All but the Cheetah Card/70 and the Quadram Liberty-AT included communications ports, and the AST Advantage! included a game port. The number and configuration of the ports varied from manufacturer to manufacturer, as did the methods of installing them and attaching devices to them.

Many PC AT clones don't come with 640K bytes of memory. Normally they leave the factory with 512K bytes, and the expansion board fills in the rest. In those cases, you have to add 128K bytes in 64K-byte chips along with the other memory you're adding. This reduces the total amount of memory you can add with the card. A few cards have other schemes that use the 256K-byte chips these cards are normally packaged with.

All the boards that I reviewed add at least 1.5 megabytes of memory to your PC AT or clone. Some used a piggyback board for additional memory. They all worked properly in a 6-MHz PC AT clone. In addition, all the boards fit a normal PC AT 16-bit slot, although the ones with piggyback boards may intrude on an adjacent slot.

The Cheetah Cards

I examined two Cheetah cards for this review: the Combo/70 and the Card/70. Both contain 70-nanosecond RAM chips and are guaranteed to operate properly in a machine running at 8 MHz with no wait states, even with a full 16 megabytes of memory. The Combo/70 contains 1.5 megabytes of RAM, as well as one serial and one parallel port. The Card/70 is a memory card only and contains 2.5 megabytes of RAM.

Each board comes with two pieces of software: a program for moving applications into the 70-ns memory and an installation program. Since the cards run at full speed regardless of the speed of the computer, Cheetah says that applications operate much faster in the 70-ns memory. In order to use this feature, you must have 256K bytes of memory in your computer before installing one of Cheetah's cards.

The installation program is one of the best available. By running a setup program included with the cards, you can obtain a picture or a printout of the proper switch settings. The installation process is so simple that you may only need to use the manual if you want to install a RAM disk.

Cheetah's manual contains photographs that show you the switch and jumper locations. It is well organized, clearly written, easy to use, and very well done.

Quadram's Cards

For this review, Quadram submitted the Liberty-AT, which includes memory only, and the Quadboard-AT, which also includes one parallel and two serial ports. The connectors for these ports are enclosed in a separate mounting box that attaches to the board with a cable. This box is supposed to hang on the back of the computer, but this practice won't work with all PC AT clones.

The Quadram boards are the only ones I reviewed that support the EMS. This support means that many programs can use the extra memory on the board directly, rather than simply as a RAM disk. You can use all or part of the memory as a RAM disk if you wish, you can flip a switch and convert the Quadram boards into extended memory, and you can add another megabyte of memory in the form of a piggyback board that plugs into sockets on the main board.

The Liberty-AT comes with a desktop utility called PolyWindows Desk. Both boards came with the Quad Master III utilities, which include expanded-memory drivers, RAM disk drivers, spooler utilities, and a utility to swap ports. The expanded-memory driver is particularly awkward to use. The syntax is poorly explained in the manual, and you must tell the driver how much memory is available in terms of 16K-byte pages, a number you have to figure out for yourself. In addition, the software doesn't check its own

continued

environment adequately: I was able to convince it that I had a RAM disk twice the size of available memory using the Quadram software and hardware.

Of the nine boards reviewed, the manuals for the Quadram boards are the most difficult to use. The explanations and organization are unclear, and I had difficulties setting up the boards and the software drivers so that they would work properly.

Advantage!

AST Research bundles an amazing amount of software with its boards. The Advantage! comes with Borland's SideKick and Quarterdeck's DESQview. Both worked with the Advantage! board, as well as with the other multifunction boards I reviewed. The Advantage! board also includes a disk that contains RAM disk software, a print spooler, and some other programs.

The Advantage! has a minimum number of features, but you can add more. My review board came with an additional piggyback memory board and a game port. The piggyback board plugs into the main board and adds 1.5 megabytes to the memory already there. It is fairly bulky, however, and can crowd the expansion slot next to it, but it protrudes slightly less than the piggyback board from Quadram. Installing the game port requires inserting a couple of integrated circuits.

AST Research provides a lot of documentation with the Advantage! card, mostly because of all that software. The documentation includes the applications' standard documentation in addition to AST Research's hardware and software manuals. Both of the AST Research manuals have clear explanations, although you must ignore the references to items other than the Advantage! card.

Maestro AT

The Tecmar Maestro AT card looks a little different from the others because it packs 11 chips into a row instead of the usual 9. Thus, you get 90 memory chips in the space usually required for 80. As a result, this card contains 2.5 megabytes of memory plus one serial and one parallel port. There is no piggyback board. Installing the card is relatively simple, partly because it has only a single DIP switch to set; the other cards that I reviewed had anywhere from three to six.

The Maestro AT comes with the usual RAM disk software and print spoolers as well as a memory-resident menu program that includes an appointment calendar, a calculator, a check-writing program, an inventory program, a tic-tac-toe game, an electronic address book, a text editor, and more.

The Maestro AT's manuals are well written, easy to follow, and bound—a major convenience. Most of the manuals for the other boards reviewed come with loose pages in shrink-wrapped plastic.

Magic Card 16

Everex Systems' Magic Card 16 comes with several pieces of software, including a diagnostic program and an installation program. The diagnostic program is part of the installation process. You must tell the installation program about your particular equipment configuration, and it will tell you how to set the switches and jumpers that you need to install the memory. Then you run the diagnostic program.

When I tried it, the diagnostic program wouldn't work. It reported defective memory where there was none, and defective ports when they worked fine. I confirmed that the hardware was indeed running properly by using Zenith's ROM-based memory diagnostic program.

Along with a RAM disk, a print spooler, and a forms manager, the Magic Card 16 includes PC-Write, the shareware word processor from Quicksoft, and the

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Table 1: *The nine PC AT Multifunction cards and their features.*

Name	Combo/70	Card/70	Liberty-AT	Quadboard-AT
Company	Cheetah International 107 Community Blvd. Suite 5 Longview, TX 75602 (800) 243-3824	Cheetah International 107 Community Blvd. Suite 5 Longview, TX 75602 (800) 243-3824	Quadram Corp. One Quad Way Norcross, GA 30093 (404) 923-6666	Quadram Corp. One Quad Way Norcross, GA 30093 (404) 923-6666
Maximum RAM	1.5 megabytes	2.5 megabytes	2 megabytes	1.5 megabytes
Piggyback memory	No	No	1 megabyte	1 megabyte
Serial ports	1	No	No	2
Parallel ports	1	No	No	1
Game ports	No	No	No	No
RAM disk	Yes	Yes	Yes	Yes
Print spooler	No	No	Yes	Yes
Installation software	Yes	Yes	No	No
Other software	Program relocation software Microsoft Windows	Program relocation software Microsoft Windows	Port-swapping software PolyWindows Desk	Port-swapping software
Runs on 8-MHz Z-248	Yes	Yes	Yes	Yes
Supports EMS	No	No	Yes	Yes
Manuals	Hardware/software (loose-leaf)	Hardware/software (loose-leaf)	Hardware (loose-leaf) Quad Master III	Hardware (loose-leaf) Quad Master III
Price	$395	$395	$455 to $985	$500 to $990

PC-Write manual on disk. The manual for the Magic Card 16 is clear, but not overly detailed.

Maximizer AT

Sigma Designs' Maximizer AT is one of only two boards that I reviewed that failed to operate on the 8-MHz Zenith Z-248. Depending on the speed of your computer, you might want to confirm that this board operates on your machine before you buy it.

With that exception, the board performed properly. Setup is covered clearly in the manual, and the installation was without incident. The Maximizer AT comes with one parallel and one serial port and includes a handy 9-pin to 25-pin adapter for the serial port. It also includes a piggyback memory board to add an extra 2 megabytes to the card's existing 2 megabytes of memory.

The only software included with the Maximizer AT is a print spooler. You must use the standard MS-DOS VDISK program to create a RAM disk. The Maximizer AT manual is fairly short, but it is usable and provides an adequate explanation of the installation of the piggyback board.

AT Multifunction Card

PC's Limited's AT Multifunction Card is the second card that failed to run on the 8-MHz Zenith Z-248. Again, if your system is faster than the standard 6 MHz, you should be certain this card will run before buying it. The AT Multifunction Card includes a piggyback board with 1.5 megabytes of memory in addition to the 1.5 megabytes of memory on the main board itself. The card also includes one parallel

Advantage!	Maestro AT	Magic Card 16	Maximizer AT	AT Multifunction Card
AST Research Inc. 2121 Alton Ave. Irvine, CA 92714 (714) 863-1333	Tecmar Inc. 6225 Cochran Rd. Solon, OH 44139-3377 (216) 349-0600	Everex Systems Inc. 48431 Milmont Dr. Fremont, CA 94538 (415) 498-1111	Sigma Designs Inc. 46501 Landing Parkway Fremont, CA 94538 (415) 770-0100	PC's Limited 1611 Headway Circle Bldg. 3 Austin, TX 78754 (512) 339-6800
1.5 megabytes	2.5 megabytes	2 megabytes	2 megabytes	1.5 megabytes
1.5 megabytes	No	No	2 megabytes	1.5 megabytes
1	1	1	1	1
1	1	1	1	1
1	No	No	No	No
Yes	Yes	Yes	No	No
Yes	Yes	Yes	Yes	No
No	No	Yes	No	No
SideKick (Borland) DESQview (Quarterdeck)	Banner, calculator, appointment calendar, check writing, alarm reminder, encryption and decryption, forms manager, text editor, sorting, electronic address book, constant time display, inventory, tic-tac-toe	PC-Write (Quicksoft) Forms manager	None	None
Yes	Yes	Yes	No	No
No	No	No	No	No
Hardware (loose-leaf) Software (loose-leaf) Borland SideKick (bound) Quarterdeck DESQview (loose-leaf)	Hardware–technical (bound) Software–technical (bound) Software–user's guide (bound)	Hardware/software (loose-leaf)	Hardware/software (bound)	Hardware (bound)
$595 to $1745	$399 to $1395	$330	$395	$199

and one serial port.

The manual is very brief, the illustrations are unclear, and there are confusing lists to show you how to set the DIP switches on the board. No software is included with the AT Multifunction Card.

What To Look For

When deciding which card to buy, the ultimate test is operation. The multifunction card must be able to operate on your computer, and it must provide the features you need. If you have a standard 6-MHz IBM PC AT and you're a skilled user, then any of these boards will suit you. If you have a different computer, the choice is more complicated. As you increase the speed of the computer, some memory boards will no longer work, usually because the memory chips are too slow to keep up. This effect seems to get worse as you add more boards. If you must have a great deal of memory, say 12 to 16 megabytes, and a fast computer, you may find that the only boards that will work are the Cheetah Combo/70 and Card/70, which have 70-ns RAM.

Your level of experience also makes a great difference. If you are inexperienced in adding cards to your computer, then you probably will not want to deal with a manual that is confusing. Ideally, you will be able to use a program that does the hard part and just tells you how to set your switches. The two Cheetah cards, again, lead the way here, although the Magic Card 16 also does well.

If there is one thing that characterizes these boards, it is lots of DIP switches. And where they are in slim supply, there are lots of jumpers. Either way, it can be

continued

very confusing. This situation is made even worse by the failure of many board manufacturers to show where the switches or jumpers are located.

When you couple the vast numbers of switches and jumpers with an inexperienced user, you have the ingredients for intimidation. Software-based instructions would help a lot; so would reducing the number of switches required.

Conclusions

All these boards operated properly at slow speeds. They provided extra memory and, where applicable, added parallel and serial ports to the computer. Under MS-DOS, however, all that memory is of limited usefulness.

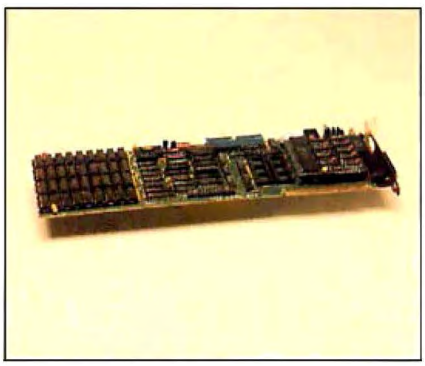
I liked the Cheetah Combo/70 and Card/70 the best. Cheetah International obviously paid close attention to the end user in designing these products and the accompanying software. They will also operate on a fast computer. In addition, I liked the Advantage! and the Magic Card 16. The Advantage! card includes all that software, which certainly adds to its value. The Magic Card 16 also comes with some excellent software, and it is quite easy to set up.

Of what use are these cards? Only those that support the EMS (Quadram Liberty-AT and Quadboard-AT) are directly usable by applications programs at this time. The other cards can be used only as RAM disks until MS-DOS provides the addressing for the additional memory. Most PC AT clones already include serial and parallel ports, so that is usually not reason enough to buy one of these cards. In fact, there may not be a lot to be gained by buying a multifunction card at this time. ■

Wayne Rash Jr. is a member of the professional staff of American Management Systems Inc. (1777 North Kent St., Arlington, VA 22209), where he consults with the federal government on microcomputers.

The All Card AT1/M

Jonathan Angel



All Card AT1/M

Type
Multifunction EMS memory board (expandable to 6 megabytes) for IBM PC compatibles running at 4.77 MHz that can remap memory with optional MMU to provide up to 952K bytes of contiguous RAM under PC-DOS or MS-DOS control.

Company
All Computers Inc.
102 Bloor St. W
Suite 1200
Toronto, Ontario
Canada M5S 1M9
(416) 960-0111

Documentation
66-page hardware reference manual
22-page software reference manual

Price

Without memory:	$595
With 512K bytes of RAM:	$695
With 1 megabyte of RAM:	$795
Daughterboard (unpopulated) for 5-megabyte expansion:	$195
High-speed option:	$100

The amount of memory MS-DOS and PC-DOS can directly recognize, 640K bytes, has been an unyielding barrier for programmers and users alike. Now the 640K wall is crumbling. More than a dozen companies sell expansion boards that conform to the Lotus/Intel/Microsoft expanded memory specification (EMS), which uses bank switching to make the computer's Intel 8088 processor think it has a bigger address space.

Unfortunately, the Lotus/Intel/Microsoft method works only with software applications that are specially prepared by their original manufacturers. All others are stuck at 640K. In addition, bank switching imposes a significant performance degradation when software uses the expanded memory intensively.

All Computers has come up with a solution: the All Card AT1/M, a multifunction board complete with a clock/calendar and serial port for $595. You can add up to 1 megabyte of RAM or up to 6 megabytes of memory with an optional daughterboard, which costs $195. The All Card AT1/M has a proprietary memory management unit on a chip. The MMU can manipulate the 8088's virtual address space more rapidly than bank switching. It also allows applications programs to access up to 952K bytes of RAM. The MMU will also let you run software written for the EMS.

A New Shell Game

Both PC-DOS and MS-DOS can use only contiguous free RAM, which is just the first 640K bytes (supplied partly on the main circuit board and partly on memory-expansion cards) in a fully loaded IBM PC XT. The rest is fragmented: A video board supplies RAM at the 704K to 768K addresses, the hard disk ROM is at 800K to 816K, and the ROM containing BASIC and the BIOS is at 960K to 1024K.

You can't use the remaining memory addresses for much of anything—a fact that the Lotus/Intel/Microsoft specification exploits. An EMS memory manager finds the address where the hard disk ROM leaves off and then installs a pageframe that's 64K bytes wide. This pageframe, divided into four 16K-byte windows, gives the 8088 a virtual address space of up to 10 megabytes.

However, software must be specially written for the EMS; programs have to know to look to the pageframe and then ask the EMS memory manager to swap segments. The process is slow; therefore, the EMS memory is appropriate for only data, not program code.

A superset specification of the EMS pageframe, called EEMS (and supported by AST Research, among others), speeds things up somewhat. EEMS allows up to 64 16K-byte windows that can be anywhere in the 8088's address space. Program code below 640K can be switched in and out of contiguous RAM, allowing multitasking in the entire 8 megabytes of virtual address space. However, EEMS is far from ideal; the windows are still limited to only 16K bytes each, and frequent switching of those 16K-byte chunks creates considerable overhead.

The All Card AT1/M adds expanded memory, but the MMU contains a translation table that allows it to dynamically alter what the 8088 sees. Instead of being limited to swapping 16K-byte chunks, it can swap as little as 4K bytes or the 8088's entire 1024K-byte address space at once. It's still an electronic shell game, but an elaborate one.

Installation

To a point, installing the All Card AT1/M is just like installing any other expansion card. It has four rows of sockets for memory chips, and you can install either 64K or 256K dynamic RAM chips; you just set a jumper on the card to tell it which type of chip you are using. You also use jumpers to set the serial port address and disable the on-board clock if your machine has one. By moving DIP switches, you can tell the card that either all its RAM is to be expanded memory or some of it is to backfill conventional memory, which would be the case if your computer doesn't already have 640K bytes. All Computers includes an interactive program you can run to help you choose the right switch and jumper settings. The board fits into any full-length expansion slot. However, the chip sockets at the front of the card come very close to the edge, and you may have to replace the card bracket in your computer, or remove it altogether, to get the AT1/M to fit.

The next step is tricky. Using a chip extractor tool, which was missing from my review unit, you must remove the 8088 processor from your computer's main circuit board and replace it in a labeled socket on the AT1/M. Then you must connect a ribbon cable from the AT1/M to the 8088's original socket. The documentation, which is lacking in illustrations, leads you through this process clearly enough until it says that the suggested ribbon cable orientation will "usually" be correct. Getting the connection backward could damage your computer's main circuit board. More explicit instructions would certainly dispel some high anxiety. In fact, at first I decided to put the AT1/M in place temporarily without relocating the 8088. The result was an unexplained error message. Fortunately, when I finally worked up enough courage to relocate the microprocessor, everything worked fine.

Utility Software

The AT1/M comes with a disk that contains utility programs for the board. Two of the programs are for the clock: one for setting the clock and one for reading the time. You should include the latter in your AUTOEXEC.BAT file. The clock is more versatile than some; it switches to daylight saving time automatically, and it lets you alter the clock's interrupts.

Also on the disk are four DOS device drivers. You must place the first, ALLMOS.SYS, as the first device entry in your system's configuration file; it merely activates the card. The second driver, ALLEMM.SYS, installs a 64K-byte pageframe that is compatible with the Lotus/Intel/Microsoft EMS. The third, MLDRIVER.SYS, works with the Multi-Link Advanced program to run several concurrent tasks in up to 704K bytes per program. The last driver, ALLDISK.SYS, activates the RAM disk with up to 3.5 megabytes, provided you have that much memory on the AT1/M and daughterboard.

All the drivers are mutually interdependent; that is, on a 1-megabyte AT1/M, you could devote either 1 megabyte of RAM to the RAM disk or make 1 megabyte available to the EMS through the pageframe, but not both at once. However, none of the above device drivers do more than their equivalents supplied with EMS or EEMS boards.

The most interesting program on the disk is ALLSIZE.EXE, which shows off the unique attributes of the MMU. When you run this program, the MMU remaps the 8088's address space to make more room for DOS. Video memory, hard disk ROM, and the BIOS are all swapped out (except for IBM BASIC), and up to 320K bytes of extra RAM are moved in. DOS then has contiguous RAM of up to 952K bytes for program code. The MMU is fast; it can even restore BIOS and hard disk ROM to

continued

the real address space when requested by an interrupt. The only compromise is that because most applications do not call the video RAM neatly, it must always be located between 960K and 1024K. DOS could be made even bigger.

Compatibility Questions

Because the MMU dynamically relocates BIOS memory, there is never a compatibility problem with programs that use BIOS services for video display. Unfortunately, many software packages bypass the BIOS and write directly to the screen, expecting the video memory to begin at 704K. However, you can run many programs that bypass the BIOS by changing the size of DOS to only 704K bytes. In my tests, this added a precious 64K bytes of workspace to Borland's Reflex.

Better still, All Computers includes a program called ALLPREP that patches popular applications programs such as Lotus 1-2-3, Framework, GEM, SideKick, Symphony, and TopView so they write to video memory located at 960K instead of 704K. Most worked with no problems. Even TopView, when modified for a 952K-byte DOS, worked well and allowed me to run five copies of WordStar simultaneously. Normally TopView, which takes up 256K bytes, leaves room for two copies of WordStar in a 640K-byte machine. SideKick didn't work, however, even though I used the version listed on the ALLPREP menu. All Computers says it plans to offer new modifications for SideKick that will let all but a 2K-byte kernel reside in expanded memory.

I also found that Digital Research's Concurrent PC DOS 4.1 did not work with ALLSIZE.EXE. All Computers promises to work with users to modify any software package not already supported by ALLPREP. If suitable work is done, most software packages should run with the All Card AT1/M. But beware of added complications with IBM's Enhanced Graphics Adapter, which requires an additional 64K bytes of video memory.

Performance

My computer ran slower when the AT1/M was connected than when it was not. When I ran the BYTE Sieve and Calculations benchmarks, my system ran about 23 percent slower than normal with the board connected, and the Disk Read benchmark was slowed down a whopping 86 percent.

However, running ALLSIZE imposed no further penalty. You could run Lotus 1-2-3 on the All Card AT1/M with ALLSIZE.EXE using up to 952K bytes of RAM without having to thrash about in the much slower EMS memory. All Computers also offers a high-speed option that includes an NEC V20 processor for $100. All Computers claims the option speeds up the board by at least 40 percent, but an evaluation unit was not available at the time of this review.

In the EMS mode, software cannot access the AT1/M's expanded memory any faster than it does on other EMS boards because the ALLEMS.SYS driver is limited to the 64K-byte pageframe.

I admire the technical elegance of the All Card AT1/M. However, the AT1/M costs more than some other EMS and EEMS boards currently available and, compared to its competitors, it lacks some support software such as a print spooler. Finally, little software supports the MMU's protected memory mode. The AT1/M is not compatible with VDISK in extended memory mode.

Still, an MMU is the only choice for anyone who desperately needs to squeeze more bytes out of DOS—at least until Microsoft offers upgrades running in 80286 and 80386 protected mode. ■

Jonathan Angel (12 Buryfields, Bury, Huntingdon, Cambridgeshire PE17, U.K.) is a freelance writer and columnist.

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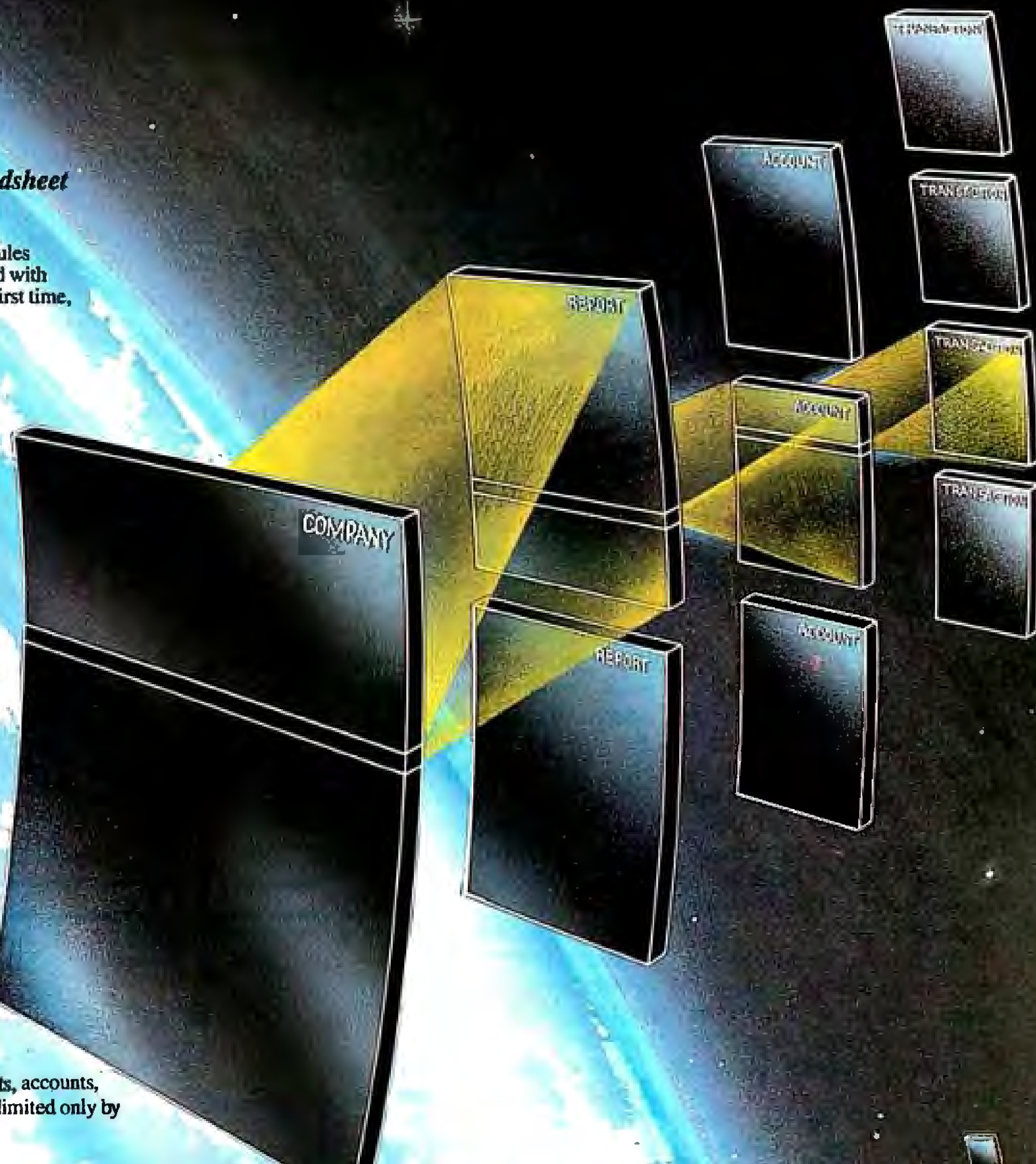

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Inquiry 314

Speed and compatibility tests on 12 m 'hines off · some surprising results

IBM PC AT Compatibles

[Editor's note: *From time to time, we learn of product evaluations conducted by colleges, universities, and similar institutions. The results cannot be compared directly with normal BYTE reviews; however, the information is interesting and potentially valuable in its own right. If you are a member of a personal computer evaluation team and would like to have your findings published, contact the BYTE Review Editor at the address show on the masthead.*]

From June to August 1986, the College of Business a d the Microcomputer Resource Facility at Arizona State University tested 12 IBM PC AT compatibles. The tests measured computation speeds, hard disk speeds, and software compatibility.

Speed Tests

Table 1 summarizes the results of the speed tests, subject to the following notes and explanations. Except as noted in the table, all computers tested had 20-megabyte hard disks and switchable microprocessor clock speeds of 6 MHz with no wait states and 8 MHz with one wait state.

The Norton Sysinfo Speed test measures basic computer sp l relative to that of an IBM PC. (Sysinfo is part of The Norton Utilities software package.)

The Track Access tests measure the time required to perform track-to-track movement in random and sequential modes. The 512K-byte File Access tests measure how long the computers take to read a 512K-by file in random and sequenti modes. The 64K-byte File Access in BASIC and the Prime-Number Sieve tests show how well the computers perform on the file access and computation benchmarks. The Sieve program was a compiled version. (For the program listings, s YTE's *Inside the I 'M PCs*, F 1985, page 195.) The Spr sheet Recalculation test sures how long the compı ıke to increment each cell in a 100-by 25-cell Lotus 1-2-3 worksheet.

In the t a dash (——) indicates th t could not be run du e incompatibility nce of a h disk.

e extremely fast Track A times of the Kamerman TCS-7000 and the Tandon PCA-20 are pparently due to disk-caching oftware built into the BIOS f these systems.

Software Compatibility

Table 2 summarizes the results of our attempts to run a variety of popular software pack- s on ea 1 of the 1 achines. In the tab , XX indicates the program ould not run properly, N/A dicates the software could not be tested because no graphics card was installed, and OK means the software ran properly. ■

Jaime Cuevas Dermody is an assistant professor of finance at Arizona State University. Jayesh Punater is a computer engineering student and works in the Microcomputer Resource Facility on campus. They can both be reached at Arizona State University, Microcomputer Resource Facility, Ritter A-138, Tempe, AZ 85287.

compatibles. Information for the IBM PC AT is included

Computer	Norton Sysinfo Speed	RAM	Tra	
ALR PC 2/286 (6 MHz only)	7.4	512	—	—
AMAX AT 3000	9.2	512	8.40	23.17
AT&T PC 6300 Plus (6 MHz)	7.2	512	21.15	57.83
Compaq Deskpro 286	7.7	512	5.52	21.20
Epson Equity III	7.7	640	18.28	53.02
IBM PC AT (new version)	7.7	512	6.91	21.09
ITT XTRA (0 wait states*)	9.2	640	4.28	12.46
Kamerman TCS-7000	7.5	1024	0.66	4.19
Sperry PC/IT	8.9	640	5.40	15.76
Tandon PCA-20	7.7	512	0.65	4.17
TI Business-Pro	5.7	640	15.15	52.04
WYSEpc 286	9.2	640	20.04	38.08
Zenith Z-200 Advanced PC	6.6	512	7.14	23.83

Table 2: *Software compatibility tests.*

Computer	dBASE III	Microsoft Flight Simulator
ALR PC 2/286 (6 MHz only)	OK	N/A
AMAX AT 3000	OK	OK
AT&T PC 6300 Plus (6 MHz)	OK	OK
Compaq Deskpro 286	OK	OK
Epson Equity III	OK	N/A
ITT XTRA (0 wait st s)	OK	OK
Kamerman TCS-7000	N/A	OK
Sperry PC/IT	OK	OK
Tandon PCA-20	OK	OK
TI Business-Pro	OK	OK
WYSEpc 286	OK	OK
Zenith Z-200 Advanced PC (6 MHz only)	OK	OK

for comparison. Sequential and Random Track Access times are in milliseconds; all other times are in seconds. RAM sizes are in K bytes.

512K-byte File Access			64K-byte File Access in BASIC		Prime-Number Sieve	Spreadsheet Recalculation
Random Write	Random Read	Sequential Read	Read	Write		
5.16	7.14	2.56	—	—	—	—
5.88	5.50	3.30	—	—	—	—
5.30	9.80	2.83	10.24	12.87	18.31	60.03
6.40	4.97	3.79	8.96	9.17	15.82	53.13
6.62	6.67	3.92	9.08	11.50	15.81	53.55
5.88	5.62	3.38	8.97	11.28	19.44	59.23
3.74	4.86	1.82	6.59	7.87	12.52	41.85
5.85	5.96	3.52	—	—	—	—
5.19	4.58	2.69	8.90	11.01	14.22	47.89
6.43	9.39	3.73	9.06	11.30	16.14	54.43
4.53	8.21	2.41	—	—	—	—
6.10	8.98	3.38	7.08	9.39	13.12	43.49
5.00	6.15	3.02	—	—	—	—

IBM PC-DOS 3.0	IBM Advanced Diagnostics	Lotus 1-2-3	Microsoft Multiplan	The Norton Utilities
OK	OK	N/A	OK	OK
OK	OK	OK	OK	OK
OK	XX	OK	OK	OK
OK	OK	OK	OK	OK
XX	XX	N/A	OK	OK
OK	OK	OK	OK	OK
OK	OK	N/A	OK	OK
OK	OK	OK	OK	OK
OK	OK	OK	OK	OK
XX	OK	OK	OK	OK
OK	OK	OK	OK	OK
OK	OK	OK	OK	OK

ALR PC 2/286
Advanced Logic Research Inc.
10 Chrysler Ave.
Irvine, CA 92718
(714) 581-6770

AMAX AT 3000
Supreme Company
1630 Oakland Rd., A103
San Jose, CA 95131
(408) 971-6400

AT&T PC 6300 Plus
AT&T Information Systems
1776 On the Green, Room 4B25
Morristown, NJ 07960
(800) 922-0354

Compaq Deskpro 286
Compaq Computer Corp.
20555 FM 149
Houston, TX 77070
(713) 370-0670

Epson Equity III
Epson America Inc.
OEM Division
3415 Kashiwa St.
Torrance, CA 90505
(213) 534-4500

ITT XTRA
ITT Information Systems
2350 Qume Dr.
San Jose, CA 95131
(408) 945-8950

Kamerman TCS-7000
Kamerman Labs
8054 Southwest Nimbus Ave.
Beaverton, OR 97005
(503) 626-6877

Sperry PC/IT
Unisys Corp.
Information Systems Group
P.O. Box 500, Mail Station B-200
Blue Bell, PA 19424
(215) 542-4011

Tandon PCA-20
Tandon Corp.
20320 Prairie St.
P.O. Box 2107
Chatsworth, CA 91311
(818) 993-6644

TI Business-Pro
Texas Instruments
P.O. Box 225012, Mail Station 57
Dallas, TX 75265
(800) 232-3200

WYSEpc 286
Wyse Technology
3571 North First St.
San Jose, CA 95134
(408) 433-1000

Zenith Z-200 Advanced PC
Zenith Data Systems
1000 Milwaukee Ave.
Glenview, IL 60025
(312) 391-8860

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RamFont is a radical new hardware mode that combines the speed of text mode with the flexibility of graphics mode.

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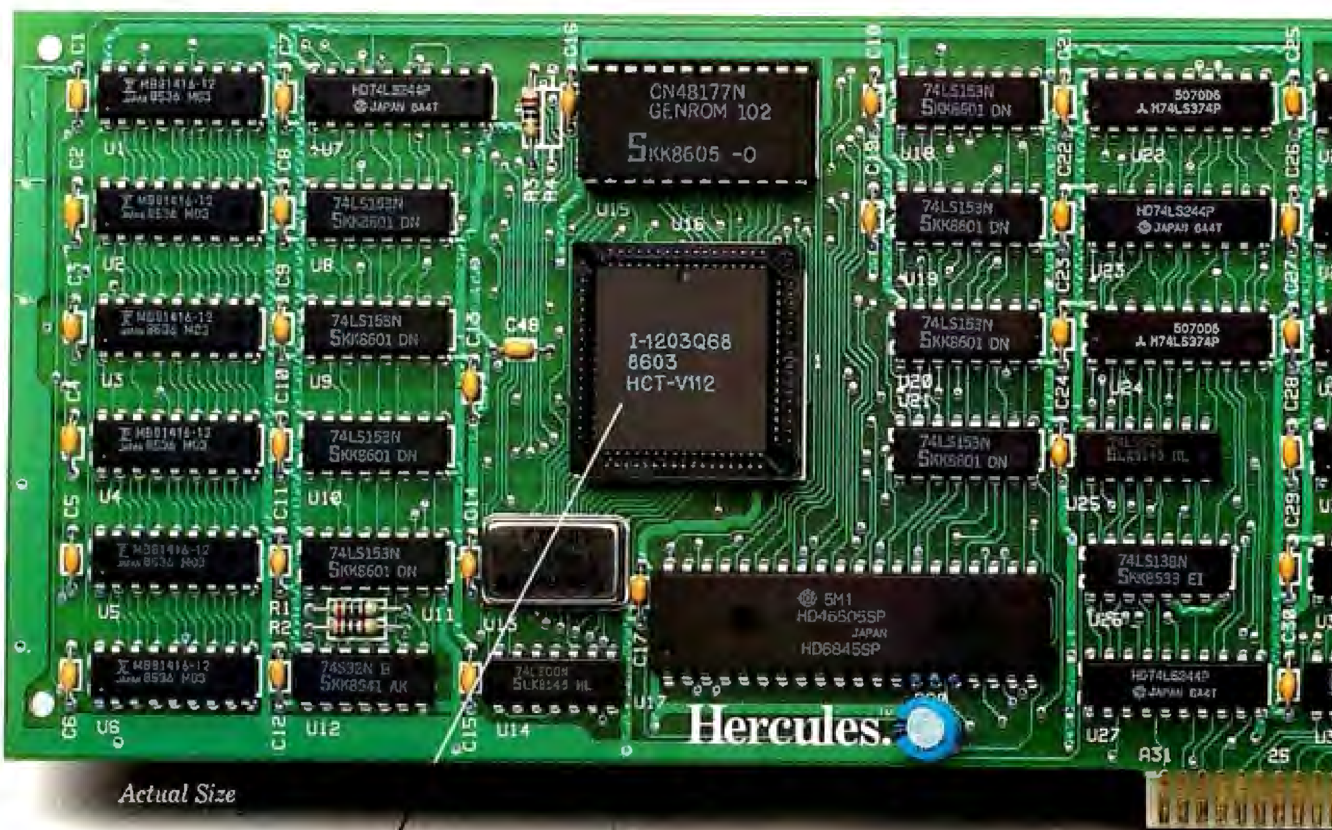
The world according to RamFont.

In the old days (before the Graphics Card Plus), programs like Lotus® 1-2-3®, Symphony,™ Framework™ and Microsoft® Word had to use graphics mode to display multiple fonts and variable text sizes, or to mix text with graphics.

But graphics mode is a whole lot slower than text mode. Up to eight times slower.

Enter RamFont.



Actual Size

The heart of the Graphics Card Plus: the V112 microchip, Hercules' next generation video processor that makes the RamFont mode possible.

It lets all the programs we just mentioned (and plenty more in the future) do all the things we just described, all on one screen.

At precisely the same speed as text mode.

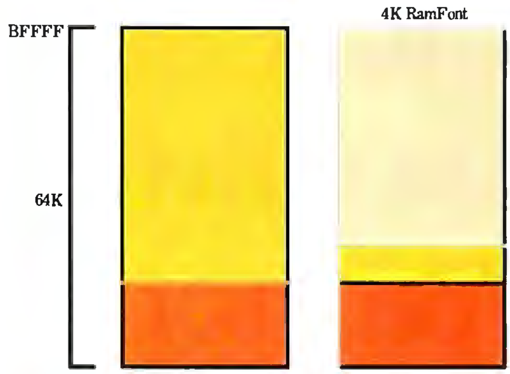
How RamFont works.

Like text mode, RamFont uses a 16-bit word to represent a character on the display.

Unlike text mode, however, the 48K RamFont mode uses a 12-bit character code instead of an 8-bit code.

Which allows you to choose from an astonishing 3072 different characters.

While setting the size of your screen cells from eight to nine pixels wide and from four to 16 scan lines tall.



The new RamFont mode displays 3072 programmable characters at the speed of text mode, or replaces the standard character set with one of your choice in 4K RamFont mode.

To help you design your own RamFont characters and symbols, we've included a font editor called FontMan.™

Along with a set of 25 sample fonts to start your library.

And since the 4K RamFont mode can accept 8-bit character with your favorite font is as simple as loading it into RAM.

Just for the record, RamFont supports the standard character attributes of reverse, high-intensity, blink and underline.

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Three Modula-2 Programming Systems

Paul A. Sand

A clear winner emerges from a trio of Modula-2 implementations

In this review I will examine three implementations of the Modula-2 language developed for the IBM PC and compatibles: Native Code Modula-2 for the IBM PC from Modula Corporation, the Modula-2PC compiler from PCollier Systems, and the Modula-2/86 Software Development System from Logitech.

The three packages reviewed here are all program development systems for Modula-2. In addition to Modula-2 compilers, the packages all provide tools and utility programs to help the programmer develop Modula-2 programs.

Similarities

With only a few exceptions, all these systems support the full Modula-2 syntax and language features. All support the fundamental Modula-2 concept of separate compilation, with definition modules describing the outside appearance of a module and implementation modules defining the algorithms and data structures by which the module does its job.

All the packages follow similar three-step strategies in turning a Modula-2 program into an executing program. First, the Modula-2 source file must be compiled, generating an object file. Since Modula-2 programs usually require the services of other separately compiled modules, a second explicit link step is necessary to find the required modules' object code files and combine them with the program's object code. Finally, you can run the linked program. This step can be carried out by the linker program itself; it may require a separate run command, or you can simply give the program's name if the linker produces an MS-DOS .EXE file. All three of the systems reviewed here produce MS-DOS .EXE files either as an option to the linker or as a separate program.

All the systems provide precompiled library modules that your programs can easily use with the Modula FROM . . . IMPORT . . . declaration. They all provide a few common library modules that closely follow the descriptions in Niklaus Wirth's *Programming in Modula-2*; for example, the library modules InOut, RealInOut, FileSystem, Storage, and Terminal are available in all three systems, and programs from Wirth's book (and other sources) that use these modules will most likely run unchanged under any of these systems.

Outside this core set of library modules, however, there are wide differences in both name and function among the library modules provided with the three systems.

Finally, all three systems offer support for overlays, the creation and coordination of multiple concurrent processes, and access to DOS system calls by means of provided library modules.

Native Code Modula-2

Modula Corporation's Native Code Modula-2 for the IBM PC comes on three disks that contain two versions of the compiler, five versions of the linker, 27 precompiled library modules, and three demonstration programs.

For systems with less than 512K bytes of memory, the compiler is divided into three separate files. If you have 512K or over, the compiler comes as a single 238K-byte file.

The five versions of the linker are more difficult to explain: If you have an 8087 math coprocessor chip installed, you use one of a pair of special linkers that link 8087 code to your object code; if not, you use the normal linker pair. One linker in each pair generates an .EXE file as output, while the other simply combines your program with the necessary library modules and runs it without creating a directly executable file. The fifth linker joins separately compiled modules with their imported modules and produces a linked (but not directly executable) file; this fifth linker allows faster loading of programs when they are actually run.

All this sounds more complex than it really is; to compile a single-file Modula-2 program and to generate an .EXE file takes only two commands.

The 450-page manual for Native Code Modula-2 is clear and full of examples, although it contains little tutorial material. The manual clearly describes installation of the software on both dual-floppy and hard disk drive systems. It includes a complete discussion of module compatibility (i.e., under what situations a given program's source file must be recompiled) and common programming errors. The best feature in the manual is its exhaustive discussion of each library module provided with the system; all procedures in the library modules are completely described, often with examples of their use in real programs.

Modula-2PC

The Modula-2PC software package by PCollier Systems comes on two disks; one contains the compiler and linker, and the other contains 16 library modules and three demonstration programs.

You can compile and link a program into an .EXE file with two commands. Unlike the other systems, the Modula-2PC compiler does not produce run-time error-checking code unless you explicitly tell it to. Another option to the linker command instructs the linker to produce an .EXE file; without this switch, the linker would simply load the required library modules and run the resulting program.

The documentation provided with the

continued

Paul A. Sand (Computer Science Department, University of New Hampshire, Durham, NH 03820) teaches computer science and has written two books on Pascal.

compiler is relatively succinct, but adequate in most areas. Installation instructions are included for single-floppy, dual-floppy, and hard disk drive systems. A Modula-2 tutorial takes up a large portion of the manual; another sizable portion describes the provided library modules, although briefly and with few examples.

At the time this was written, PCollier Systems had announced plans to offer an integrated editor, a debugger, and 8087 support routines as extra-cost options for its compiler.

Modula-2/86 Software Development System

The Modula-2/86 Software Development System by Logitech is available in a number of configurations; Logitech provided me with four disks containing an integrated editor, two versions of the compiler, two versions of the linker, four installation batch files, three example programs, and 39 library modules. The two versions of the compiler and linker are for computers with less than 512K bytes of memory and those with 512K and over. Also provided is assembly language source code for parts of the system, with the idea that competent programmers can alter the system for hardware that's not IBM PC-compatible.

You can, if you wish, run the Modula-2/86 system from the DOS command line like the other two development systems reviewed here.

Unlike the other systems, however, Modula-2/86 also has an integrated, pop-up, menu-driven programming environment that is very convenient to use.

The base of the integrated system is the program editor, a standard full-screen multiwindow editor optimized for entering Modula-2 programs. In addition to the usual editing features (e.g., auto-indent, cut and paste, and help screens), the editor has a built-in Modula-2 syntax checker that you can invoke at any time by pressing a function key. You can also call the compiler and linker via function keys; both return you to the editor when the job is done. If the compiler discovers errors in the source file, the editor will move the cursor to each and show you the compiler's error messages in a window if you repeatedly press a two-key combination.

Another feature of the editor is syntax assistance. Pressing Alt-A through Alt-Z inserts one of 26 syntax templates at the current cursor position, allowing you to fill in the blanks to complete the language construct. For example, pressing Alt-I will insert the skeleton of an IF statement at the cursor position:

```
IF THEN
END (* if *);
```

This will then position the cursor after the word IF. You can also change these keys to generate other syntax if you desire.

The 450-page Modula-2/86 manual is, with few exceptions, clearly written and well organized. Instructions for installation and use of the system are straightforward. The descriptions of the library modules are simple listings of the heavily commented definition modules. While this isn't as useful as Modula Corporation's extensive descriptions and examples, it is adequate for most use. Some library modules are described more fully in other parts of the manual.

Logitech offers a number of additional support products for its Modula-2/86 system: a Make Utility, which automatically detects dependencies and out-of-date object files in a Modula-2 program and associated library modules and produces a batch file containing the minimum number of commands necessary to bring the program back up to date; a Utilities Package containing a postmortem debugger, a disassembler, a program cross-referencer, and a preprocessing program called Version that allows conditional compilation; the Window Package, a library of routines that allows a program to use multiple independent windows; a Run Time Debugger that permits you to set breakpoints in your program and examine and alter data while the program is running; Library Sources, which contains source code to the library modules; and a Turbo Pascal to Modula-2 Translator utility (see the text box "Translating Pascal to Modula-2" below).

Benchmarks

Using all three Modula-2 compilers, I ran the standard BYTE benchmark programs, translated from BASIC into Modula-2, along with a program to write the letter *a* to the CRT screen 10,000 times, which measures how well the software does screen output. The results are shown in table 1. I also ran programs to determine the precision of the real data type and to find the largest and smallest positive real number (table 2) and the Dhrystone benchmark (table 3). Although this synthetic program does nothing of value, it was constructed by Reinhold P. Weicker to represent as closely as possible the actual mix of statement types and data access found in real programs (except I/O statements). Weicker published an Ada version of this benchmark program in *Communications of the ACM* journal; it has since been translated into C, Pascal, and Modula-2. [Editor's note: *The benchmark tests mentioned in this article are available as the file MODULA.LST on disk, in print, and on BIX. See the insert card following page 424 for details. Listings are also available on BYTEnet. See page 4.*]

Since the Dhrystone benchmark is the only benchmark I ran that makes any claim to represent real programs, I chose to make more detailed measurements on it. I took all measurements twice: once with all the compiler's error-checking code generation switches on, and once with them off.

Note that the actual speed of the Dhrystone program produced is measured in Dhrystones per second. This is a measure of how many iterations of the benchmark the program can run in 1 second. The higher the result here, the better.

Translating Pascal to Modula-2

Logitech's Turbo Pascal to Modula-2 Translator performs much of the mechanical drudgery of translating an existing Turbo Pascal program into Logitech Modula-2. Although it won't handle all possible Turbo Pascal programs properly, it will generate reasonable code, which can then be hand-tuned. For example, the graphics demonstration file ART.PAS provided with Turbo Pascal was translated correctly except for two Pascal expressions involving character sets. One of these, the Turbo Pascal expression

```
Upcase(Ch) in ['Y', 'N', #27]
```

was translated into the Modula-2 expression

```
CAP(Ch) IN BITSET {'Y', 'N', 33C}
```

This is almost right, but BITSETs are too small to hold sets of characters in Modula-2. The solution is to replace the set expression with a straightforward compound Boolean test:

```
(CAP(Ch) = 'Y') OR (CAP(Ch) = 'N')
  OR (Ch = 33C)
```

After an analogous change to the other buggy expression, the resulting program compiled and ran perfectly.

Modula-2/86 Software Development System Release 2.00

Company
Logitech Inc.
805 Veterans Blvd.
Redwood City, CA 94063
(415) 365-9852

Documentation
450-page manual

Price
Base system: $89
System with 8087 support: $129
System with 512K compiler/linker: $189

Options
Turbo Pascal to Modula-2 Translator: $49
Run Time Debugger: $69
Utilities Package: $49
Library Sources: $99
Window Package: $49
Make Utility: $29

Native Code Modula-2 for the IBM PC

Company
Modula Corporation
950 North University Ave.
Provo, UT 84604
(801) 375-7400

Documentation
450-page manual

Price
$195

Options
Interactive Symbolic Source-Level Debugger: $29

Modula-2PC

Company
PCollier Systems Inc.
7925-A North Oracle Rd.
Suite 390
Tucson, AZ 85704
(800) 522-2060

Documentation
200-page manual

Price
$99.95

Comparisons

In terms of the speed and compactness of the code generated, the Logitech Modula-2/86 compiler was the clear winner of most of the benchmarks. The only poor showing it made was in the Calculations benchmark; this is almost certainly due to the higher accuracy to which Modula-2/86 does floating-point calculations compared to the other two systems.

The Modula-2/86 compiler produced the fastest executable programs, as evidenced by the high speed in Dhrystones per second in table 3.

Although the Modula-2/86 system took longer to compile and link programs, it was the only compiler to run the Dhrystone benchmark properly without modification; there are three reasons for this.

First, the Modula-2/86 compiler is a multipass compiler; the Modula-2PC and Native Code Modula-2 compilers are one-pass compilers. While one-pass compilers are, in general, faster than multipass compilers, one-pass compilers must see the declaration for a procedure before using that procedure. The original source code for the Dhrystone benchmark used procedures before they were declared, which gave errors under the Modula-2PC and Native Code Modula-2 compilers. The solution is to define a Pascal-like forward declaration for a procedure before it is used.

Second, neither Modula-2PC nor Native Code Modula-2 recognized the standard procedure new. I had to translate calls to new into calls to allocate.

Finally, the Modula-2PC compiler would not compile a perfectly legal relational-operator comparison between two

continued

Table 1: *The BYTE standard benchmarks applied to the three Modula-2 implementations under review. Also shown are the results of the screen output test. All times are in seconds.*

Benchmark	Native Code Modula-2 run time	Modula-2PC run time	Modula-2/86 run time
Disk Write			
to floppy	161.30	159.89	160.00
to hard disk	5.44	5.44	3.46
Disk Read			
from floppy	28.72	28.67	28.67
from hard disk	5.38	4.55	2.80
Calculations	21.97	41.36	32.68
	$\epsilon = 1.19 \times 10^{-7}$	$\epsilon = 3.82 \times 10^{-8}$	$\epsilon = 1.11 \times 10^{-16}$
Sieve	19.00	31.03	16.65
Screen output time	37.57	37.52	31.31

The results for the Disk Write and Disk Read benchmarks show how long it takes to write and then read a 64K-byte sequential text file to a blank floppy disk. The Calculations results show how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The Sieve results show how long it takes to run 10 iterations of the Sieve of Eratosthenes prime-number benchmark. The screen output time results show how long it takes to write the letter *a* to the screen 10,000 times.

Table 2: *Tests of the* real *data type.*

Measurement	Native Code Modula-2 run time	Modula-2PC run time	Modula-2/86 run time
Size of reals (bytes)	4	8	8
Largest positive real	3.4×10^{38}	1.1×10^{37}	1.7×10^{308}
Smallest positive real	1.2×10^{38}	2.9×10^{39}	2.2×10^{308}
Approximate precision (decimal digits)	7 to 8	9 to 10	15 to 16

Table 3: *Dhrystone benchmark tests results. All times are in seconds except where noted; file sizes are in bytes.*

Dhrystone Benchmark	Native Code Modula-2 run time	Modula-2PC run time	Modula-2/86 run time
Compile time			
RTC on*	26.64	46.68	65.25
RTC off**	23.84	45.52	65.91
Link time			
RTC on	—	—	25.49
RTC off	—	—	26.20
.EXE file-generation time			
RTC on	8.78	7.80	22.91
RTC off	9.67	7.63	22.19
Total Modula-2 to .EXE file time			
RTC on	35.42	54.48	113.65
RTC off	33.51	53.15	114.30
.EXE file size			
RTC on	73,728	55,296	44,160
RTC off	72,464	53,760	43,136
Run speed (Dhrystones/second)			
RTC on	98.8	55.3	232.0
RTC off	88.7	53.2	150.0

* RTC on — all run-time checks enabled
** RTC off — all run-time checks disabled

variables of type CapitalLetter, which had been previously defined as a subrange of char. This is a bug, solved by renaming the subrange type to char.

All three systems' manuals left something to be desired. Modula Corporation's documentation, while excellent in most places, nowhere explains the consequences of its one-pass Native Code Modula-2 compiler. The forward declaration is never mentioned in the manual. There are also occasional anachronistic references to previous versions of the compiler.

The PCollier manual for Modula-2PC could benefit from additional examples of actual programs in documenting its library modules. The Modula-2 tutorial material is fairly well done, but too terse to stand on its own without help from a Modula-2 text. And if you have a good Modula-2 text, why do you need a tutorial?

Logitech's manual for Modula-2/86 never lists the standard procedures it supports.

As I explored these three systems, I kept an "odd man out" list: Whenever I came across a feature that was present or absent in a single system, I wrote it down. Modula-2/86, for example, is the only system without a link-and-go version of its linker; you must save the linked load module on disk, then reload it and run it as a separate command. Modula-2/86 is also the only system with a BCD library module, which allows precise arithmetic and formatting of typically monetary numeric quantities of up to 18 digits. Modula-2/86 is also the only compiler that supports the 80286 processor; this is done through a compiler switch.

Modula-2PC is the only system without either 8087 support or a debugger (although both may be available by the time you read this). It also does not support (or at least lacks documentation for) interfacing assembly language routines to your Modula-2 programs.

The Native Code Modula-2 system is the only one with a color graphics library module containing routines to draw shapes. A color graphics library module is available in Logitech's Turbo Pascal to Modula-2 Translator option for Modula-2/86, however.

Conclusions

Modula-2/86 is the clear winner when you compare these three systems. The compiler generates the fastest and most compact code, as shown most clearly in the results from the Dhrystone benchmark. It comes closest to supporting full Modula-2 as defined by Wirth. The integrated editor is a joy to use; the other systems don't offer anything to compare with it. It has the widest variety of library modules; the only real lack is the absence of a graphics library module. In addition, Logitech supports its product with optional high-quality utilities.

One final note: If you're considering Modula-2, you should compare the results here with other languages as well. Although the Modula-2/86 compiler generates relatively fast and compact code, it doesn't do well in an absolute sense. Typical C compilers will give much more compact code; the C code will also execute noticeably faster. ■

ACKNOWLEDGMENT
William Miller kindly provided me with a version of the Dhrystone benchmark written in Modula-2.

MTBASIC

Frederick D. Davis

Although a variety of languages such as Ada, Modula-2, and some varieties of FORTH have internal tasking, MTBASIC, a $49.95 compiler from Softaid Inc., appears to be the first multitasking variant of BASIC available for popular computers.

MTBASIC is available for CP/M and MS-DOS computers. The MS-DOS version comes installed for the IBM PC and compatibles. You can, however, install the compiler on just about any terminal (I tested it on a Corona PC). It will also run under Digital Research's Concurrent PC DOS 4.1. MTBASIC requires 128K bytes of RAM in MS-DOS machines and 48K on CP/M systems. It does not use memory in excess of 128K on MS-DOS machines.

MTBASIC does not offer the true concurrent processing that is usually present in multiuser operating systems. It provides the ability only to schedule the relative frequency of starting a task—not the concurrent processing of multiple tasks. You can define up to 10 different tasks to run at the individual frequency you specify.

Although its tasking is not concurrent, MTBASIC lends itself to interesting applications such as periodic sensor sampling and games. You could, for example, easily write a program that periodically updates a counter on the display and controls a moving graphic while awaiting keyboard input (see listing 1). Unfortunately, MTBASIC does not allow any kind of accurate scheduling if other tasks are executing during a significant part of the interval.

All the programming examples in the reference manual show only short tasks that can be completed within the time span before the next task is supposed to start. The manual does not mention what might happen if the designated tasks take longer to execute than the allotted time. Based on my experiences, I found that actual allocation of time among tasks is erratic. Task switching occurs, but the time spent on a task can vary by a factor of eight.

Fast Compiler

MTBASIC is a semi-interactive compiler. You can invoke it just as though it were an interpreter. And like an interpreter, it has its own line-entry capability with a limited syntax checker, but no line editing. The only way to change a line from within MTBASIC is to replace it entirely. Fortunately, you can use almost any programming editor to create and edit MTBASIC files, and the compiler will check syntax as it loads the file for compiling.

Compilation is very fast. Softaid claims the rate is in excess of 100 lines per second. Such high-speed compilation is difficult to measure without writing very long programs, but I saw nothing to make me doubt that claim. See the benchmark results in tables 1 and 2.

If you have enough room in memory for both MTBASIC and your program, you need only type RUN, and the program compiles and then immediately runs. If a program has already been compiled in memory, the GO command will execute the program from the beginning. However, GO does not reset variables to zero or null. The variables retain their values from the last execution whether the program was aborted or ended with STOP in the code. Unlike most interpreters, MTBASIC does not allow you to examine the values of variables if the program has stopped running, and there is no way to resume execution at a particular line number.

Additionally, pressing Control-C does not always stop the program. If you hit the Escape key, or if the keyboard input buffer is full, Control-C simply will not work. To make matters worse, if you compile a program using the minimal error-checking parameter (NOERR), MTBASIC checks only occasionally for a Control-C, delaying the response.

If your program is too large to fit into memory along with MTBASIC, you can compile from a disk file and output to a new disk file. The output file has the .COM extension and you can directly execute it from DOS. Also, Softaid permits users to distribute executable files compiled by MTBASIC without paying royalties.

Listing 1: *A windowing program that executes three tasks. After establishing the windows, the main task accepts input at a specified location and prints it at another location after blanking out the previously printed message.* TASK 1 *prints a number at approximately 1-second intervals in a window at the upper left corner of the screen.* TASK 2 *prints an asterisk moving diagonally from the upper left to the lower right corner of another window. All tasks run until the counter reaches 60.*

```
990  STRING IN$(20)
1000  INTEGER A,CNT1,MAXCNT
1005   MAXCNT=13
1010  ERASE
1020  WSELECT 0
1030  WINDOW 0,0,23,79
1040  WFRAME CHR$($C4),CHR$($B3)
1050  WINDOW 1,1,22,78
1056  CURSOR 21,10
1057  PRINT "ENTER HERE"
1060  WSELECT 1
1070  WINDOW 3,3,7,10
1100  WFRAME CHR$($C4),CHR$($B3)
1200  WINDOW 4,4,6,9
1300  WSELECT 2
1400  WINDOW 3,12,18,27
1500  WFRAME CHR$($C4),CHR$($B3)
1600  WINDOW 4,13,17,26
1700  RUN 1,7
1710  RUN 2,2
1715  WSELECT 0
1720  CURSOR 21,21
1730  INPUT IN$
1733  CURSOR 12,45
1736  PRINT " "
1740  CURSOR 12,45
1750  PRINT IN$
1760  CURSOR 21,21
1770  PRINT " "
1800  GOTO 1715
1900  TASK 1
2000   A=A + 1
2100  WSELECT 1
2200  CURSOR 1,1
2300  PRINT A
2310   IF  A < 60 THEN  GOTO 2400
2320  STOP
2400  EXIT
2550  TASK 2
2600  WSELECT 2
2610  CURSOR CNT1,CNT1
2620  PRINT " "
2630   IF  CNT1 < MAXCNT THEN  GOTO 2700
2640   CNT1=0
2700   CNT1=CNT1 + 1
2900  CURSOR CNT1,CNT1
3000  PRINT "*"
3100  EXIT
END
```

Language Features

MTBASIC has a reasonably standard, though limited, syntax in areas other than file access, windows, and tasking. It has retained the file commands CVI, CVS, MKI$, and MKS$ for use with MBASIC files. However, those commands are optional; MTBASIC does not require them for its own file handling. Missing are the LSET and RSET commands, although the FIELDS command is present and is required for record lengths other than the 128-byte standard.

You must declare variables as REAL, INTEGER, or STRING before using them for the first time. All variables are strictly global, including those in user-defined functions and tasks. I deplore the lack of

continued

MTBASIC

Type
Multitasking BASIC Compiler

Company
Softaid Inc.
P.O. Box 2412
Columbia, MD 21045
(301) 964-8455

Format
MS-/PC-DOS: 5¼-inch floppy disks
CP/M: 8-inch single-sided, single-density disks

Computer
MS-DOS or PC-DOS computers with 128K or more; CP/M-80 computers with 48K or more

Documentation
104-page reference manual; READ.ME file on distribution disk

Price
Standard package: $49.95
MT8087 version: $79.95

local variables in user-defined functions because it makes the naming of variables critical if you should try to pull in previously programmed functions. Furthermore, avoiding variable-name collision in a large program is tedious.

You can use a dollar sign to distinguish strings from numeric variables; however, variable names must be unique. For example, the compiler considers A1$ and A1 to be the same variable. Variable names must begin with a letter and can be up to seven characters long.

The compiler has no DIM statement—arrays are specified in the declaration of the variable. Strings have a length of 20 characters, unless specified otherwise. The maximum length is 127 characters for either simple string variables or array elements. Arrays of real numbers and integers can have a maximum of two dimensions; string arrays, one dimension.

Real numbers are limited to single precision. You must be careful when trying to compare real numbers for equality. The compiler's real numbers are rarely equal unless they are integer values. According to Softaid, another version of the compiler, MT8087, handles real numbers with accuracy up to 18 places.

User-defined functions are apparently a recent addition to MTBASIC. Their use is not described in the manual but instead is in the READ.ME file on the distribution disk. Unfortunately, the compiler's error checking does not prohibit passing fewer parameters than the number declared in the function definition. This feature could certainly cause problems if your parameters are of different types.

MTBASIC requires line numbers, but it has no built-in renumbering capability. Unfortunately, line-number branching is limited. An IF. . .THEN statement allows either the execution of a single statement or branching to a specified line number. You cannot use an ELSE clause, and you cannot have nested IFs without very cumbersome spaghetti code using multiple line-number branchings, nested subroutine calls, or nested function calls. The only method of looping is the FOR . . . NEXT statement. There is no WHILE . . . WEND statement, which I sorely missed. Also, error checking with the FOR . . . NEXT statement is lacking. When I omitted a NEXT in a loop, the compiler generated no error message at compile time, nor at run time. When executed, the program just wouldn't work correctly.

MTBASIC allows one interesting variation from standard BASIC. It allows a limited amount of recursion in subroutines, but not in user-defined functions. The amount of recursion is limited by the variable space available. Softaid claims it has successfully written routines that call themselves as many as 50 times.

Table 1: *Single-task benchmarks. The Sieve runs much faster with integers than with real numbers. Turning error-trapping routines off before compiling the program makes an obvious difference. Real-number versions run faster when all numbers have embedded decimal points. The additional tasks are simple loops. All times shown are in seconds.*

	SIEVE				
	Integer	2-task integer	3-task integer	Implicit real	Explicit real
With error trapping	7.6			98.5	87.0
Without error trapping	3.05	6.1	9.2	93.5	82.5

Table 2: *Multitasking Disk Access, Write Only tests. The Disk Access tasks are two standard benchmarks running concurrently. In the single-file test, both tasks write to the same 40K-byte file, doubling the resulting file. In the two-file test, each task writes to a separate 40K-byte file. The total elapsed time from start is shown. As the results show, the time allocation between the two tasks is not even. By comparison, however, if you run the two-file test under Concurrent PC DOS, treating each task as separate programs, task 1 and task 2 finish virtually simultaneously. All times shown are in seconds.*

	Task 1	Task 2	Single task
One file	328	420	261
Two files	610	628	—

Windows and More

In addition to multitasking, MTBASIC supports windows and user-configured devices. You can create up to 10 windows on any kind of terminal under either CP/M or MS-DOS. You can also use graphics characters, if your computer supports them, for window borders.

Three special commands create the windows: WINDOW defines the size of a window, WFRAME draws a border on the outside edge of the window, and WSELECT selects which of the 10 possible windows is the active window. Another command, CURSOR, allows you to position the cursor within a window. All positions are in relation to the upper left corner of the window (0,0). If the position that you request is outside the window, the cursor is positioned at the window edge closest to the requested position. This protects the contents of the other windows and the screen in general. Three more commands deal with window management: WCLEAR erases only the selected window, WSAVE allows you to save the contents of a window to an integer array so that you can restore it later, and WUPDATE restores a window that you have saved. These three commands allow you to easily overprint windows and quickly restore their contents.

Another interesting feature allows you to load machine language drivers into memory for up to three user-configured devices. You can also modify the jump table with the addresses of those drivers. This means you could access additional terminals for multiplayer games that have simultaneous displays, input, and even private communications between two of the terminals. The possibilities are intriguing. Another use of this capability could be to access analog or digital interfaces or any other external device easily from within MTBASIC. The obvious catch, of course, is that you must have the necessary device driver.

An added plus is that you can address the terminal, the printer, or any user-configured device by the same line of code. This is done by assigning a channel number of 0 to the terminal, −1 to the printer, 1 through 3 to disk files, and 4 through 6 to user-configured devices. Few other BASICs provide this versatility. However, MTBASIC does not take full advantage of this feature with disk files because the syntax is different for output to a file than it is for output to the screen or printer.

Shortcomings

MTBASIC suffers from several major weaknesses that make it inappropriate for some kinds of programming. Its most crippling handicap is file handling. First, you can have only three files open at once. Second, the file reading and writing is abysmally slow (as shown in table 2). Finally, you must open a file in read-only or write-only mode. You cannot open a file, read a record, and then update the same record. You first have to open the file for reading, position for a read, read the record, close the file, open it in write mode, position for a write, and then write the record. This arrangement is very slow and cumbersome.

Another problem is the time allocation for each task. If you program two or more tasks and the tasks take longer to complete than the time allotted before the next task is supposed to start, the scheduling becomes quite erratic. If the tasks are disk-intensive, time allocation between them varies even more.

Another failing is the documentation. The MTBASIC reference manual severely lacks in-depth coverage of multitasking. Absent is any information on problem situations that commonly occur in multitasking. No mention is made of how to program two routines when both need disk access. But the most important deficiency of the manual is that it does not cover tasks that cannot be completed before the next task is to start.

The manual implies that you can schedule events based on known intervals, such as updating a second counter on the screen while other tasks run. I could not make this happen. However, since I was using a Corona PC rather than an IBM PC, it is possible that I was not intercepting the system clock ticks properly.

Summary

Certainly, MTBASIC is not for every programming need. However, although I found its tasking ability disappointing, it still offers some advantages that are not available in other BASIC compilers. If file handling in your application is limited and the frequency of tasks can be on a relative basis rather than absolute, MTBASIC should fit the bill. In addition, when you consider that you get the added benefits of windows, the ability to address up to three user-configurable devices, and fast compilation, the trade-offs in using an otherwise limited MTBASIC are worthwhile. ■

Frederick D. Davis (P.O. Box 427, Riverton, UT 84065) is an independent software consultant.

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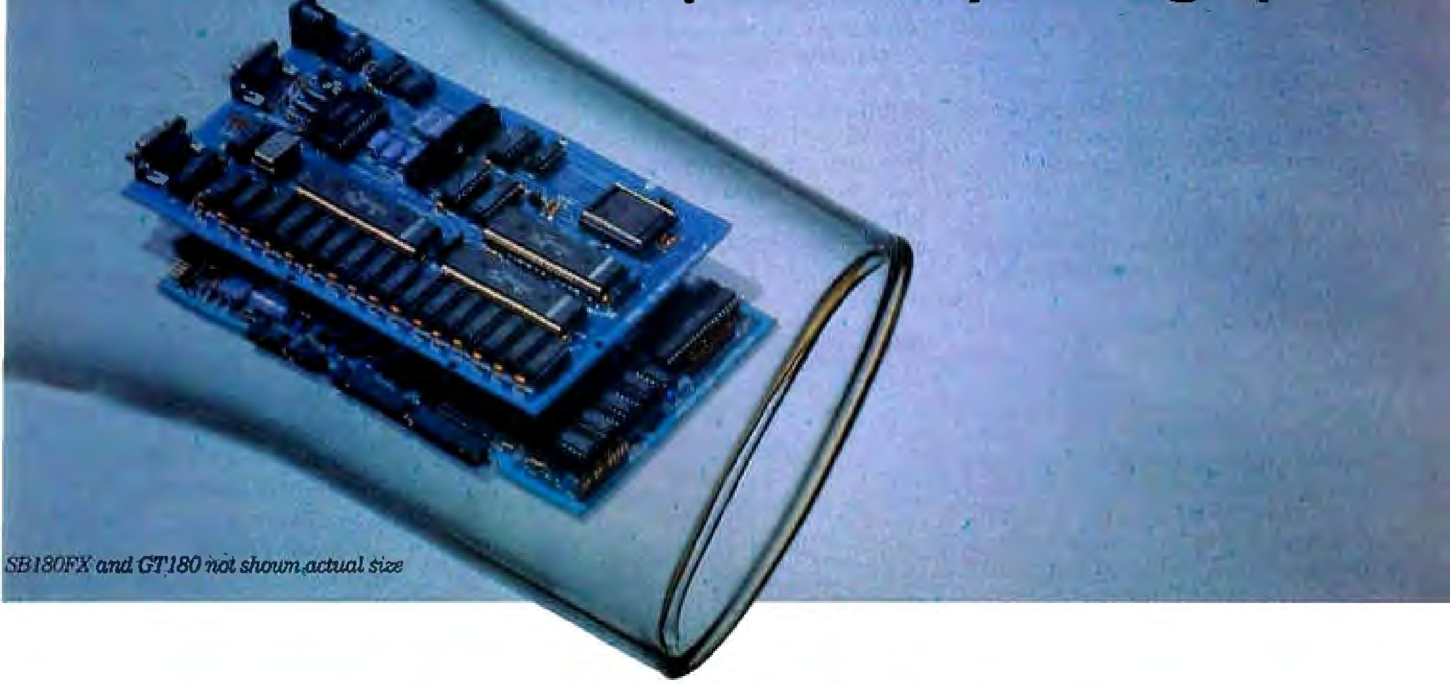

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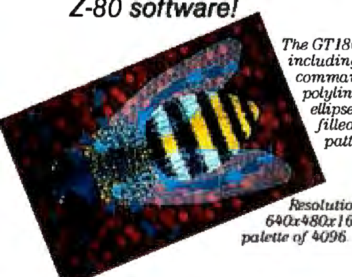

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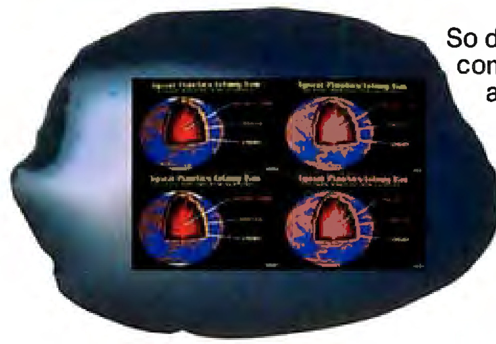

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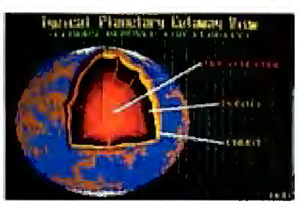

Software: Modula 2 by Borland International including SB180/GT180 Grafix Toolbox.

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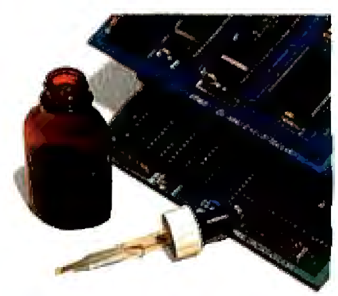

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*minimum configuration: 256K bytes of RAM and ROM monitor.

To order or for technical information call

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MICRO MINT

Micromint, Inc. 4 Park Street Vernon, Connecticut 06066 TELEX: 643331

Programming Credit: Tom Hudson

RuleMaster

Mike Van Horn

An expert-system software package for MS-DOS machines

A couple of years ago, Radian released RuleMaster, an expert-system development package for use with UNIX, VMS, and XENIX on the IBM PC XT. You can install the more recent MS-DOS version on the IBM PC XT, PC AT, or clones. It requires 512K bytes of RAM (640K is recommended) and at least 1.5 megabytes on a hard disk. Radian has cut the price of the MS-DOS version substantially from $5000 to $995.

RuleMaster is the first major package to combine these three important features: You can develop rules by induction from sets of examples or by programming them with a structured language; you can compile RuleMaster programs into C, thus making them much more transportable from one kind of system to another and much more compact and faster; and you can run RuleMaster on MS-DOS machines.

You can use RuleMaster for expert systems that diagnose a problem from its observed symptoms, predict an outcome from observed conditions, or identify something from available clues. It then advises the best action to take and offers explanations why. You can use the program with either forward- or backward-chaining search strategies or a combination.

Features

RuleMaster automatically induces decision rules from examples entered by the expert-system developer. Suppose you wanted to develop a program that predicts whether it will rain, based on observed current conditions. First you would define the outcome that is to be predicted (e.g., "rain" or "wontrain") and the key variables you can observe to reliably predict the outcome (e.g., "cloudy," "clear," "windy," "calm," "cold," "cool," or "warm"). Then you enter a number of examples from your experience that show the relation between different values of the variables and different outcomes. These examples are entered in a spreadsheet-like format:

```
Conditions                    Outcome(Goal)
cloudy  windy   ——            > rain
clear   ——      ——            > wontrain
cloudy  calm    cool          > rain
cloudy  calm    cold          > wontrain
cloudy  calm    warm          > wontrain
```

Technically, this is similar to setting up a Lotus 1-2-3 spreadsheet. Thus, RuleMaster at its simplest level is accessible to a nonprogrammer.

You then enter the text of the questions, the menu choices, and the advice that you want to appear on the screen to the user of the system:

```
Conditions
clouds     [ask "How is the sky?"
           "cloudy, clear"]
winds      [ask "How windy is it?"
           "windy, calm"]

Outcomes
rain       [advise "I think it will rain"]
wontrain   [advise "I do not think it will
           rain"]
```

After you enter the examples, RuleMaster automatically induces a decision tree of IF. . .THEN. . .ELSE rules from the logic of these examples. These rules are stated in RuleMaster's built-in Radial language, which has a structure similar to Pascal.

You can revise and expand RuleMaster programs easily by editing the example set. In addition to inducing rules from examples, you can state rules directly in Radial. Decision rules can be hierarchically nested, thus allowing backward or forward chaining through any number of levels.

Using the cgen utility, you can translate a RuleMaster program automatically into a compiled C program, which runs faster and is more compact. If you then have problems with the program, you go back to the interpreted version, make your changes using either RuleMaster induction or Radial statements, and then recompile it into C.

RuleMaster can explain its decisions by showing the chain of decision rules it has used, whenever you type in WHY. These explanation formats, or templates, are programmed in by the designer. An example might be

"Since..[condition]..and..[condition]..it follows that..[outcome]."

The explanatory statements that accompany the advice given can be as long and detailed as you want.

RuleMaster accommodates both sources of uncertainty in expert systems. One source is the uncertainty built into the knowledge rules (e.g., "If you see factors A, B, C, and D, then there is a 75 percent chance that condition M prevails."). The other source is uncertainty in the observations made by the user (e.g., "Factors A and B are definitely present, D is absent, but I'm only 65 percent certain that Factor C is present."). RuleMaster has fuzzy logic capability to evaluate such input in arriving at its recommendations.

Ease of Use

At the basic level, it is quite easy for nontechnical people to learn and use RuleMaster, much easier than preceding systems such as KEE or ART. Even so, developing an expert system is considerably tougher than building a spreadsheet or database program. The user must thoroughly understand the conceptual relationships and be able to devise a set of examples that encompasses all the important variables. The user must also reach

continued

Mike Van Horn (13 LaLoma Court, San Rafael, CA 94901) is the author of Understanding Expert Systems *(Bantam, 1986).*

RuleMaster version 3.0

Company
Radian Corp.
8501 Mo-Pac Blvd.
P.O. Box 9948
Austin, TX 78766-0948
(512) 454-4797

Format
Four 5¼-inch disks

Computer
IBM PC, AT, or XT; most UNIX systems, including the AT&T PC 6300, VAX, or MicroVAX running VMS, UNIX, or XENIX

Documentation
Reference manual; 3½-day training seminar available for additional $500

Price

MS-DOS version:	$995
Single-user workstation:	$5000
Multiuser workstation:	$17,500

accurate, unambigous conclusions that are logically structured for efficiency and ease of troubleshooting and refinement.

Knowledge engineering is crucial. In some complex systems that have been developed with RuleMaster, only about 60 percent of the rules can be induced from examples. The other 40 percent must be programmed in Radial code, especially the rules instructing RuleMaster when and how to move between different levels of rules in a hierarchical decision tree, which is often called the inference engine. Even when using RuleMaster with rule-induction capability, developing a working expert system still takes extensive savvy about constructing a compact, reliable program.

Furthermore, when RuleMaster asks a question, you must choose from one of the menu options offered. If your interpretation of the situation doesn't fit into the choices offered, the system can't do its job.

Refining the System

Once the basic decision structure is complete, you can make changes in the rule base by induction from examples. You can add and refine examples and switch entire modules in and out with great ease. Thus, a working system can be refined and upgraded by knowledge experts who are nonprogrammers.

If the system designers have done their job, RuleMaster is easy for the end users. They need little computer background—they need only the ability to turn the system on and, when questions appear on the screen, to answer by making a menu selection or entering numerical data. However, this is a very big "if."

Inadequate Explanations

As mentioned above, RuleMaster's explanations are limited to statements tied to each rule by the system designer. With backward-chaining programs using multilevel logic, RuleMaster explanations seem somewhat ambiguous. This is a crucial factor. The user—the person who did not construct the system—wants to ask "Why?" and get a cogent explanation for the specific recommendation. Otherwise, he or she has no basis for trusting the recommendation and will not use it. This problem is not unique with RuleMaster.

Training and Documentation

Radian provides 3½-day training seminars for RuleMaster for $500. After that, system developers can link their expert systems with a computer at Radian Corporation to get troubleshooting help.

The reference manual is written for the UNIX system and contains a brief section on the differences between the UNIX and MS-DOS versions. The manual has a brief tutorial but nothing on the potential applications of RuleMaster or how to get the most out of it.

UNIX and MS-DOS Versions

The differences between the UNIX and MS-DOS versions stem from the limitations of MS-DOS when compared to UNIX.

When setting up or revising example sets, you must use both the sysed and inded editors. In the UNIX version, you can switch from one to the other, but with the MS-DOS version, you must go back to the main menu each time you switch—a great annoyance.

A complex RuleMaster program can easily exceed the capacity of MS-DOS, which can address at most 640K bytes at any one time. This amount of memory won't hold a very large expert system with its knowledge base programmed in Radial. However, after you recompile a program in C, it works fine under MS-DOS limitations. One recommendation is to develop the expert system using the UNIX version of RuleMaster, then compile the completed program in C and transport it over to the MS-DOS system. Another approach is to build the program in modules so that the 640K limit is not reached.

80386 Impact

The value of RuleMaster will be enhanced when more personal computers that are based on the 80386 chip appear. This chip will greatly speed up processing power, be compatible with existing MS-DOS programs, and will support MS-DOS and UNIX simultaneously. It can address more than 4 gigabytes of main memory. Thus, the 80386 will be ideal for coping with the symbolic processing demands required by expert systems like RuleMaster.

Summary

RuleMaster combines the ease of rule induction in a package powerful enough to build full-scale expert systems previously available only on a minicomputer-based program, such as KEE or ART. ■

Scribble!

Warren Block

Scribble! is a general-purpose word-processing package for the Commodore Amiga from Micro-Systems Software. It works with the Amiga's standard Intuition user interface, so you can run other programs concurrently with it.

Menus and Windows

Scribble! lets you edit documents within a window, which can be resized and moved about on the screen. At the bottom of the window is a status line that shows the current page number, the line and column location of the cursor, and the current action mode (e.g., Edit, Copy, Cut, Paste, Style, or Spell). Also indicated is whether or not the Insert mode is on. Scroll bars located just above the status line and on the right side of the display allow you to move the cursor throughout the text. Scribble! also uses the WordStar diamond cursor-control method.

When you press the mouse's Menu button, the bar at the top of the screen shows the names of several menus that you can select. You can also access many of the menu functions through keyboard shortcuts. By selecting Open from the Project menu, you can open a new window. This is similar to running another copy of Scribble!—the new window can contain a completely different document or a copy of the document that's in the original window. Since you specify how much memory to allot for the new window, you can make efficient use of memory space. You can transfer text between windows and open up to four windows at one time.

Text Formatting

You format text using dot commands (named for the periods that always precede them), which Scribble! obeys when it prints your document. Because of this, the way the document appears on the screen is not the way it will look when printed. To help save paper and time, a preview function is provided to let you examine the document's formatted appearance on the screen.

The dot commands let you put headers and footers on a document (including different ones on odd and even pages), create hanging indents to set off areas of text, justify text, send escape codes to the printer, and more. Scribble! shows a complete list of these commands when you press the F2 key.

A useful (and somewhat unusual) feature is the program's ability to send printed output to a file or device. Using this option, you could prepare a preformatted file for sending over a modem or to another computer.

Built-in Utilities

A 40,000-word spelling checker is included with Scribble!. It allows you to check a single word, the contents of the current window, or an entire document for errors. You can add words to a temporary file or the permanent dictionary so that future spelling checks will recognize special terms you use. A mail-merge feature allows you to create customized form letters and other documents.

There is also a useful Status command that shows such things as page length, margins, character count, and word count.

Saving Files

When you save a document, Scribble! can create an accompanying .info file so that an icon represents the document on the screen. You can disable this option if you want. The program can still identify document files without icons because a .doc extension is added to their names. There is also a provision for adding a 30-character comment to a filename. This comment shows up when Scribble! presents a list of document files on a disk, and it can help in identifying the contents of files with ambiguous names.

You can change the screen colors to any combination, then save them in a file and reload them at any time. If you name this file Scribble!.fmt, it is loaded when the program is executed, setting all the startup default values to your preference.

Problems

While using Scribble! I noticed that the words *Page, Line, Column*, and *Action* would occasionally disappear from the status line. The numbers (like the 2 in "Page 2," or 31 in "Line 31") didn't disappear like the words, so it really wasn't a problem. However, it certainly didn't give me a lot of confidence in the program's reliability. When I called Micro-Systems Software's technical support number about this, I was told that the release of version 1.2 of the Kickstart and Workbench disks by Commodore would correct the disappearing status line and several other problems. As I write this, however, the version 1.2 upgrade has yet to be released.

Another problem with Scribble! is that the scroll bars that allow you to move the cursor throughout the document flicker every time the screen is scrolled. This is a very annoying distraction. Eliminating the scroll bars would cure the problem, and since it is difficult to position the cursor accurately with them anyway, most users would find it no great loss.

Yet another problem concerns Scribble!'s requesters. A requester is a small window that a program presents when it needs information of some type. Scribble! shows a requester for a filename when you save a file, but before typing in the filename, you must move the mouse pointer to the requester's text box and click its Select button. In other programs, like Commodore's Textcraft word-processing program, the requester is automatically ready for text input. Supplementary information files included on the Scribble! disk state that the version 1.2 upgrade of the operating system will correct the requesters as well.

Another problem is that Scribble!'s command verification messages are not always enough to prevent mistakes. For example, when you load a new document, it erases the one currently in memory. The program doesn't ask "Are You Sure?" or say "Current Document Will Be Erased"; it just goes ahead and erases it. This is very similar to what happens when you select Quit from the Project menu. A requester pops up that says Okay to Quit Project? and accepts a Yes or No response. This works well until you have several windows open with different documents in them. Selecting Quit from the Project menu should get rid of just the current window with its document. Scribble!, however, dumps them all.

The function keys have many uses in the program, and while it may be easier to press one function key than a two-key combination, the function keys are not labeled, and this forces you to move your hands from the normal position. The Amiga keyboard has a place for a function-key label, but none is provided with Scribble!.

Scribble! has no specific command to print a document in the printer's near-letter-quality mode, although you can accomplish this by using dot commands to send escape codes to the printer. This allows you to use a printer's special functions that are not supported by the Amiga's Preferences program, but it is beyond the capacity of many casual users.

Despite all these complaints, Scribble! is fairly easy to use, although the large number of commands that are accessed by the use of the Ctrl key, the right Amiga logo key, and the function keys tend to cause confusion. It is generally easier to use the mouse and the program's menus.

Documentation

The *Scribble! User's Manual* is no help at all with simple functions like setting margins or line spacing. The lists of dot commands, escape sequences for the

continued

Table 1: *A comparison of benchmark results for Scribble! and Commodore's Textcraft. All times are in seconds.*

Test	Scribble!	Textcraft
Load	3.0	4.6
Save	5.5	7.8
Search	2.7	4.6
Scroll	41.8	39.2

Scribble!

Company
Micro-Systems Software Inc.
4301-18 Oak Circle
Boca Raton, FL 33431
(800) 327-8724

Format
One 3½-inch disk; not copy-protected

Computer
Commodore Amiga with at least 512K bytes of RAM

Documentation
Scribble! User's Manual, 156 pages

Price
$99.95

printer, and key commands are scattered throughout the book. Nowhere is there a comprehensive command list, and many functions are never demonstrated. Examples are few and far between. The index is not comprehensive enough to be of much help, and it certainly isn't good enough to redeem the rest of the book.

Conclusions

Although Scribble! has many good features, the inconsistent user interface, the awful documentation, and the flickering display were enough to quell my enthusiasm. Novices looking for an Amiga word-processing program would be best advised to look elsewhere. Advanced users may be able to operate Scribble! productively, but the experience won't be painless. [Editor's note: *See table 1 for results of the benchmark tests.*] ■

Warren Block (645 King St., Chadron, NE 69337) currently comprises the entire computer repair department of Chadron State College.

Laser Author

Mick O'Neil

Laser Author (formerly Laser Quill) by Firebird Licenses is a word-processing program for the Macintosh and Mac Plus. It requires 512K bytes of memory.

Style Editor

Laser Author's first major departure from conventional Macintosh word processors is the inclusion of a Style Editor. This editor allows you to create a text style and assign it to a title, paragraph, phrase, or word. For example, in writing newsletters, you may want to use a variety of font sizes and styles for titles, and alternate between two different fonts for regular text. To do this with MacWrite is simple, but tedious. Using Laser Author, you can define each of these requirements as a separate style, create a pile of stationery that includes these styles in pull-down menus, and enter text in the style of your choice. You can also change text style locally by clicking anywhere in a paragraph or title and then choosing the appropriate menu option, or globally by using the Style Editor to change a previously designed style.

Laser Author 1.0

Type
Word processor

Company
Firebird Licenses Inc.
P.O. Box 49
Ramsey, NJ 07446
(201) 444-5700

Format
Two disks; copy-protected

Computer
512K Macintosh or Macintosh Plus

Documentation
User's manual with tutorial

Price
$199.95

Frames

Another important feature of Laser Author is its use of frames. Frames are rectangular areas with Move Bars and Grow Handles that can contain text, graphics, or other frames. Essentially, frames behave like minipages. You can use the left edge of a frame as a left margin and trigger word wrap at the right edge. A Continuation option creates a new frame when the present one becomes full. Thus, a touch-typist could easily prepare a multicolumn document without any of the hassle of WordStar's column-select and column-move procedures. You can insert and move frames, change text styles, and insert graphics while maintaining the overall structure of the document.

You import graphics via the clipboard from MacPaint or MacDraw and scale them to fit the frame or clip them. A scaled picture will conform to the shape of the frame and change size when the frame is resized, while a clipped picture will retain its normal size but show more if the frame is enlarged, and less if it is reduced. Because you can alter the size of a graphic while keeping its original proportions and place a text frame next to a graphics frame, Laser Author allows for much more sophisticated integration of graphics with text than MacWrite or Microsoft Word.

Page Layout

Laser Author has a comprehensive Page Setup option. You can use it to choose the

Table 1: *The results of performing various functions with Laser Author using a 4000-word text file converted to proper format. All tests were done on a Macintosh Plus with the System file loaded on a RAM disk with the program disk in the internal drive and the data disk in the external drive.* Run program *shows the time required to run the program directly from the Finder.* Load document *refers to the time required to load a document while the program was running, while* Load from Finder *results from double-clicking the document icon while in Finder mode.* Save document *refers to the first save of a formatted text file, and* Save revision *shows the time required to resave the same document after it has been revised.* Search document *indicates the time required for the program to find a unique word inserted at the end of the file, and* Scroll document *refers to a manual scroll from the beginning of the document to the end. Times are in seconds.*

	Laser Author 1.0	Microsoft Word 1.0	MacWrite 4.5	Write Now B.02
Run program	61.0	12.4	15.7	20.3
Load document	4.8	5.6	14.4	11.5
Load from Finder	52.0	15.7	26.6	17.9
Save document	16.5	23.2	12.4	10.6
Save revision	8.8	20.0	7.4	3.8
Search document	45.0	17.9	7.2	1.5
Scroll document	55.0	73.5	64.5	82.9

size of the paper and its orientation, position the top, bottom, left, and right margins, and allocate space for headers and footers. The program has a scaled-down image of a page that graphically reflects any changes made to the page setup, eliminating a lot of the guesswork. You can change the units of measurement to inches, millimeters, points, or picas.

You can insert headers and footers, which can include automatic page numbers, the date, and the time, as well as standard Laser Author text and graphics. The header or footer window is sized in accordance with the page layout instructions, and you can vary the formatting on left- and right-hand pages.

Other Features

Another useful feature of this program is its ability to create stationery pads. To do this, you open an empty document, create a set of styles to be used, insert text and graphics (such as an inside address) that are to appear in every document on the pad, and then issue a Save command. The options in the Save Dialogue box include Entire Document, Text Only, and Stationery Pad. Choosing the latter will create formatted stationery that can be opened and used over again.

Laser Author has other useful features. One is a flexible search-and-replace option with UNIX-like wild-card characters. Laser Author can also overstrike and adjust the spacing between pairs of characters, and it permits seven levels of superscripting.

An import/export utility allows Laser Author to accept formatted text from applications like MacWrite and ACTA. A document information window keeps track of the date and time, time spent on the document, total number of words, words typed this session, and words typed last session. Laser Author is compatible with the Apple Imagewriter printers and the LaserWriter, can spool printing when memory permits, and can have four documents open at once.

Laser Author has a periodic key-disk system whereby copies of the program, at times, will require you to temporarily insert the master disk so the program will work. However, you can install up to three copies of Laser Author on a hard disk and, in the event that the disk has to be reformatted, you can remove any installed copies to the original master disk.

Conclusion

Although Laser Author has many innovative features and goes more toward full exploitation of the Macintosh interface than any other word processor, some facilities are still lacking. A complete word processor should include a spelling checker, thesaurus, mail-merge facilities, and the capability of handling automatic footnotes. Firebird Licenses plans to augment Laser Author with a series of add-on modules and, hopefully, address some of these concerns. [Editor's note: *See table 1 for results of the BYTE benchmark tests.*] ■

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REVIEW FEEDBACK

Turbo Lightning

I agree with most of Ross Ramsey's comments in his review of Turbo Lightning (November 1986 BYTE). But the program has one useful feature that is obscured by his complaint that, since the highlighting disappears with the next keystroke, "you find yourself. . .requesting another screen check to find the next trouble spot." Actually, you can request a review of the checked screen, which is much faster at highlighting the remaining misspellings than a full screen check. This considerably reduces the tedium of using Turbo Lightning to check a long document; so does using a hard disk and a V30 chip (I use an AT&T PC 6300).

Turbo Lightning's most noticeable weakness, in my view, is its relative stinginess with alternative spellings that begin with different letters than the word being checked. If you mistype the word *before* with any letter other than *b* at the beginning, the spelling checker will not give you *before* as a possibility. (The same is true of WordPerfect's spelling checker.) I find it amusing, but sometimes annoying, that Turbo Lightning indulges in semisubliminal advertising for Borland. Running the *before* test, I found only seven instances in which a suggested word began with a letter other than the beginning letter of the misspelled word; in each instance, the odd-lettered word was *Reflex,* complete with the capital *R.* The spellings that produce that suggestion do not include *refore,* oddly enough. And if you check *sidelick,* the first choice that pops up is *SideKick,* ahead of the more generic *sidekick.* The dictionary also contains Philippe Kahn's first and last names. If you have to evade perfection, you may as well have fun.

Henry Taylor
Lincoln, VA

24-pin Dot-Matrix Printers

I read Robert D. Swearengin's review entitled "Three 24-pin Dot-Matrix Printers" (November 1986) with interest, not because I contemplate buying one, but to see how well I did in having already purchased a Fujitsu DL2400.

Mr. Swearengin neglected to compare the three printers' methods of paper handling. Possibly every printer available today has the same kind of tractors the Fujitsu DL2400 offers. However, I think that they are nearly the best feature of the machine. They are located below the paper roller, making it possible to tear off the letter you have just written without having to waste a sheet of blank paper. The machine has dual modes: one for cut sheets and one for tractor feed. After you press two keys on the control panel, the tractor-fed paper backs out of the way, allowing a gear shift to permit feeding separate sheets. The guide for the sheets pops easily into place with a simple one-finger action. This guide also drops down to a horizontal position to receive tractor-fed documents conveniently.

I agree with Mr. Swearengin that the Fujitsu DL2400's control sequence is difficult to learn, but he fails to mention that its set-up printout gives you a clear record of just what condition the machine is in, that it can emulate the Epson and IBM printers exactly, or that all the really remarkable font variations are software-controllable from almost any word processor's software. The range of extra fonts available are far more impressive than Mr. Swearengin indicates. The Fujitsu DL2400 is a professional machine that, in my view, has a price that scarcely hints at its power.

Edward T. Dell Jr.
Peterborough, NH

Commodore Amiga

I enjoyed Tom Thompson's review of the Commodore Amiga (October 1986). There are, however, a few mistakes. In Mr. Thompson's description of the Snapshot, he states that you must repeat the click/Snapshot operation for all icons. This is not exactly true—if you hold down the Shift key when clicking icons, you can select more than one at a time. All you do is click on all the icons that you want held in place, plus the drawer they are in, and then click on Snapshot. Although the Shift key is not intuitive, it is described in the manuals. One feature that is missing is the ability to box in a number of icons by dragging, as you can on the Macintosh. This is just one of the things we all hope to find in version 1.2 of the operating system.

One big mistake Mr. Thompson makes is in his description of the CLI. To say that CLI is hard to use because it is dissimilar to MS-DOS is unfair. CLI has many commands that do not act as their MS-DOS counterparts do, but they usually work better. For help in using them, check the excellent AmigaDOS manual or use the ? command.

Mr. Thompson says that the FORMAT command gives you argument descriptions, while most of the other commands do not. This is not true. To see the arguments that a command expects, you simply type COMMAND?. Typing COPY?, for example, returns FROM,TO/A, ALL/S, QUIET/S:. If you ever get an error you don't understand, just type WHY to get a little more help.

Finally, Mr. Thompson states that the operating system does not support virtual memory. This is true, but segmenting programs is not hard, and Aztec C supports automatic loading/unloading of program segments.

Adam Silverstein
Chicago, IL

Thanks for bringing these facts to my attention. Icons can be arranged more easily by the method you describe, but it would be better if the operating system did this automatically, as on the Macintosh. Maybe this will happen in version 1.2.

A lot of readers have pointed out the ? entry for AmigaDOS command input. However, this information is, as you said, in the AmigaDOS User's Manual, *which is not bundled with the Amiga. If every command were to output the argument list as the* FORMAT *command does, the absence of this manual wouldn't be a problem.*

You can sit in front of practically any IBM clone and use it immediately if you know MS-DOS. As I pointed out in the review, these differences between AmigaDOS and MS-DOS are frustrating and can hamper the acceptance of the Amiga. The situation is not helped by the absence of the AmigaDOS User's Manual. *I don't mind deviations from a standard if the deviation is sufficiently imaginative and useful to justify it. While the Amiga's hardware is innovative, its CLI software is not, and it should adhere to the MS-DOS standard.*

I am familiar with the concept of loading/unloading program segments, but I don't know how well this can be implemented in a multitasking environment. It's safer to allow the operating system to do this in any case: A program that manipulates memory blocks behind the operating system's back is a potential source of trouble.

—Tom Thompson ■

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Kernel

WE APOLOGIZE TO CHARLES DICKENS for the title we assigned to Jerry Pournelle's column. That aside, the two computers were IBM PC AT clones: the TeleCAT-286 from TeleVideo and the AT&T PC 6300 Plus. Unfortunately, because of trips being taken and mix-ups with the companies involved, Jerry learned little about the machines. He does suspect the PC 6300 Plus may be a good computer. Some of Jerry's travels took him to an Atari Faire in San Jose and to the PC Faire in San Francisco. While he did collect numerous items, he hasn't had much of a chance to check them out. But he is favorably impressed with Zenith's new portable computer, the Z-181, which he may adopt as his traveling companion.

Bruce Webster covers a good deal of ground in his column. He has obtained an Apple IIGS and gives his first impressions of this new addition to the II series. Bruce describes what Apple has done both right and wrong with the IIGS and gives it a qualified approval. He then goes on to review his 1986 predictions, ending up with a pretty decent batting average. Next, Bruce institutes the Fritzie awards, for products or accomplishments in different categories. And finally, brave soul that he is, Bruce makes new predictions for 1987, knowing full well that he might have egg on his face by the time this issue hits the stands.

The subject of software customization is Dick Pountain's concern this month. Though awareness of ergonomics and the need for customizing are gaining hold in the industry, primitive operating systems impose limits on what can be done. What has been needed is a program that can sit on top of an operating system and pull all the strings for us. One such program is now available. Dick looks at Automator mi from Direct Technology Ltd., which has all the features of a robot. This product impressed Dick a great deal. It provides the total control over a computer that DOS should have given in the first place. The only drawback is cost. At present, Automator mi is too expensive to be considered a personal productivity tool.

In a departure from his normal modus operandi, Ezra Shapiro investigates just one product, hence, the title. Microsoft hopes that Word 3.0 for the Macintosh will be received as the best word processor ever developed. Ezra is not yet willing to go that far, but he does believe it is an important product, one that retains powerful features from earlier versions of Word but also adds many new features. He feels that the Macintosh can now be a legitimate environment for writing and editing. Thus, Word 3.0 has cemented Ezra's decision to buy a Macintosh Plus, the highest compliment he can offer a piece of software.

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A Tale of Two Clones

Jerry Pournelle

Jerry has some problems with two new IBM PC AT-compatible systems

The trouble with "media relations specialists" is they never read the media they specialize in. They don't read much else, either. It's that or they're deliberately trying to drive me crazy.

The first case in point is TeleVideo. One of their marketing people got my home address, heaven knows how, and proposed sending their new AT, called the TeleCAT-286. This seemed reasonable. I'm quite happy with Big Kat, the Kaypro AT I've been using for more than a year now, but I ought to write about something else once in a while. I also need a test bed for a whole bunch of IBM PC AT boards. The standard TeleCAT seems to be a high-resolution monochrome system, and I doubt that the monitor is large enough for me to use the machine to write books on. Still, I haven't done anything with TeleVideo equipment for years, and I'm certainly happy with my ancient TeleVideo 950 terminal. The TeleCAT looked like a good machine to try.

I sent them my policy letter on equipment. That letter very specifically states that I am neither an employee nor an agent of BYTE or McGraw-Hill and that I don't do formal reviews. It says that while I won't deliberately damage the machine, I can't assume responsibility for it: I have far too much equipment here to be able to afford insurance on all of it. It also says that I don't accept equipment on short-term "evaluation loans."

There's a reason for that last item. Despite appearances, I am not primarily a computer writer. I'm a novelist and essayist. Certainly I enjoy writing these columns, but it isn't my primary way of making a living. I don't really have time to do tests and evaluations of equipment. I may sometimes do that, but I can't do it at anyone else's convenience.

I do *use* the machines. I might write a book, or install new accounting software, or just use the machine as a test bed for the tons of software that I receive here. The idea is to really get to know the machines. If I like it enough, it may even become my current system—which means that if I'm going to take the trouble to get used to the equipment, I'm not going to send it back just after I've done so.

My policy letter says that I don't normally accept equipment for less than six months, I prefer a year, and frankly it's to the manufacturer's advantage that I keep it as long as I like it, since I'll keep mentioning it as long as I'm actually using it. If I hate the machine, I'll send it back real fast. If I like it, I want to go on using it awhile. Of course I never own it, and if the original owner doesn't want it any longer, it goes to a school or a foundation. Nothing gets sold.

TeleCAT Arrives

We went off to Atlanta for the World Science Fiction Convention. Just as we left, the TeleCAT arrived. I left it crated up. When we got back, there were mounds of mail to deal with, as well as trips to Washington and other places, and I wanted to take a few days off to concentrate on *Storms of Victory*, Book III of the *Janissaries* series. Thus, more than two weeks went by before we unpacked it.

When we get a new machine, I generally set it up on a rolling test table. (Actually, the tables were designed for microwave ovens; I bought them at Builder's Hardware for about $25 each, and I modified them by installing a pullout keyboard drawer I bought from a mail-order house.) There's room near my desk for one of those tables, so if I like a machine it can be rolled into place and kept there.

The TeleCAT was a handsome little machine, sturdy and well made, but quite petite compared to Big Kat. The keyboard was well laid out, with a big Return key, and had a good feel. Overall I had quite a good impression.

We set up the TeleCAT-286 and turned it on. It booted off the hard disk to a menu. One option was a demonstration of graphics, so we ran that. It was pretty impressive: fast, with good resolution. Of course, you *expect* demo programs to be impressive. Time to look for software.

Before I found the software I found the paperwork.

The machine had been sent to BYTE at my home address on a 30-day evaluation loan. I'd already had it nearly 20 days. The papers also showed the full list price of the machine and said that I couldn't return it without prior authorization.

"Surely some mistake," thought I, and called the only name on the papers. This proved to be a young lady who knew absolutely nothing about it. I turned the problem over to an assistant, who spent several hours getting instructions on how to return the machine.

Thus, I regret to report that all I know about the TeleCAT-286 is that it has an impressive graphics demo.

Flash: At COMDEX I met Dr. K. Philip Hwang, chairman of TeleVideo. He has promised to speak to the media relations people; so I should have a longer report on TeleCAT Real Soon Now.

AT&T

The second case in point comes from AT&T. I first saw the AT&T PC 6300 Plus back at the 1986 COMDEX in Atlanta; I was so impressed with it that I made it one of my picks of the show. What I particularly liked was the color, which seemed crisp and bright and steady.

The 6300's product manager was at the Atlanta booth. Better still, he was a BYTE

continued

Jerry Pournelle holds a doctorate in psychology and is a science fiction writer who also earns a comfortable living writing about computers present and future.

reader and quite familiar with this column. He even knew I'm not a BYTE employee.

I had a long conversation with him about the machine. I emphasized that I was impressed with its color capability. "I haven't changed over from what I'm using largely because I've yet to find a color system I could write books on. Most are just not good enough to stare at day after day," I told him. "But this looks like it might do."

He expressed considerable interest. "We'll get one out to you right away," he said. I left Atlanta. Nothing happened.

Weeks later I tried to call him. I never did get him; eventually I was turned over to an AT&T media relations specialist. I explained what I wanted and what my policy was. "We're having a little trouble getting evaluation units," she said. "But we'll get you one."

I sent her a copy of my policy letter. Weeks went by. Then months. Finally, at the end of September, some crates arrived.

There was also paperwork. Pages and pages of it, all made out by a lawyer. The machine and all the software is here on a 90-day loan. (At least it's not 30.) One of the first items in the paperwork makes me liable for the machine in the event of fire, flood, theft, earthquake, act of God, neglect, abuse, mopery, or dopery. Meanwhile, in capital letters I'm informed that there are no warranties and AT&T assumes no liabilities whatever. There's a page of stuff about my obligations to them regarding the software they sent, too.

I wouldn't sign that agreement blind drunk.

It doesn't matter much anyway. Despite all the conversations about wanting this for the color capability, AT&T sent me a monochrome machine.

The PC 6300 Plus

I set up the 6300 Plus on the stand I'd used for the TeleCAT.

The first problem was the keyboard. About half the keys, including the space bar, had fallen off and were rattling around in the bottom of the box. It took 20 minutes to get them all back on. Once I got the 6300 Plus assembled, though, it wasn't bad. My son Alex hates it, in part because the Control key is by the space bar, but I find it has a decent feel and something approaching a Selectric layout.

The Return key is too small, and for my money a *real* keyboard has the comma and period in both lowercase and uppercase (and a separate key entirely for > and <, which are what the AT&T keyboard has for uppercase comma and period); still, I could live with this keyboard.

The green screen is crisp and clear, but the letters are too small for me. Now understand they're not smaller than those on an IBM PC monochrome screen, but then I don't like the IBM either. Like most bifocal wearers, I really hate to have to tilt my head up to peer at a computer screen. What I want is to put the screen 30 inches away and have the letters large enough that I can see them through the distance part of my glasses. When I saw the 6300 Plus color system in Atlanta I thought I'd be able to do that, and maybe I can. I sure can't with the monochrome system.

The machine had one floppy disk and one hard disk. There wasn't any indication of what kind of floppy disk: high-density or normal. Once I had the 6300 Plus set up I turned it on, figuring it would boot from the hard disk. It did, went through an enormous number of tests, and eventually invited me to log on. When I hit the Return key, it asked for a password. Then it told me my logon was incorrect and invited me to try again. After five minutes, it was clear I wasn't going to log on to that system without reading some instructions.

The AT&T PC 6300 Plus came with an enormous box of software and documents:

Inquiry 180

indeed, that box was larger than the ones the machine itself came in. When we got it open, we found it was more documents than software. Volume after volume of documents, mostly about UNIX. Formidable.

There was, however, a thin thing no more than half a dozen pages long that called itself a *Quick Reference Guide*. I thought that would surely do the trick. Alas, no. It merely tells you, "To turn your computer on, press the switch, located on the back of the computer just above the power cord, to the ON position." Nothing else. With grammar like that, why should I expect information? There was another little packet, but that consisted of pages that I could, if I really wanted to, insert in the spiral-bound *Quick Reference Guide*, after which I'd have a summary of DOS commands. Since my problem was that I couldn't get to DOS, that didn't seem a useful thing to do.

Next thing to do was fish around in the software box. Sure enough, there was a boxed book called *Getting Started With Your AT&T Personal Computer 6300 Plus*. As is customary nowadays, the pages of the loose-leaf book were shrink-packaged separately from the tab cards; it takes a good five minutes to render the thing usable. Eventually I got it together, only to discover that it wasn't much help.

There was a DOS disk in the package with the book. I put it in the floppy disk drive and reset the machine. The 6300 trundled for a while—it makes all kinds of tests for you—but eventually it came up with the A> prompt. So far so good. Now to see what's on the hard disk...

I can't find the hard disk. The system won't believe there *is* a C drive. Not only that, but it thinks B is the same floppy disk drive as A. I suppose there's a reason for that, but I guess I just don't care what it is.

Examining the *Getting Started* book reveals there's a great deal of discussion on partitioning the hard disk. I suppose that's what I'd have to do. That's a procedure guaranteed to scare the liver out of any casual business user, but I expect I could manage it—except that I'm afraid to try. After reading the legalese paper they sent with the machine, I'm afraid to do much of anything with it.

UNIX

When I saw the PC 6300 Plus in Atlanta, the product manager cautioned me: "This is a DOS machine that happens to know UNIX, but please, please, don't stress UNIX. Stress that this is an AT that runs PC and AT programs."

Still, it's obvious that the machine comes up in UNIX when you boot from the hard disk. It does all the UNIX-like tests and demands that you log on. Since I don't know how to log on, I had to wait for my son Alex who is a UNIX wizard. He managed to log on, I think as "root."

Meanwhile, I tried to follow what he was doing by reading the "Getting Started with the UNIX System" section of the *Getting Started* manual. That's a remarkable document. It shows you a picture of how to turn the machine on and how to insert a floppy disk—this in a section on getting started with UNIX. Foo. Anyone who doesn't know a lot more about computers than how to insert a floppy disk isn't going to get anywhere with UNIX. I rather soon gave up on the *Getting Started* document.

Meanwhile, Alex did get UNIX running, and he discovered that this particular AT&T 6300 Plus has about 500K bytes of unused space on its hard disk.

Somehow I don't think I much want a machine that has no more than 500K bytes for me to use. I suppose I could go downstairs and get the little 500K-byte bubble memory board out of our IBM PC (the PC thinks that's a remarkably fast fixed disk

continued

drive), but I'd probably have trouble making the AT&T talk to it.

One conclusion is obvious: if you want to run UNIX on the PC 6300 Plus, for heaven's sake get the largest hard disk you can buy. A hundred megabytes wouldn't be too small, especially if you intend to run it under DOS as well. I've got a 20-megabyte hard disk in Big Kat, and I've filled that under DOS alone. UNIX is *big*—far too big for a mere 20-megabyte disk.

At this point I'm stymied. I could, I suppose, reformat the hard disk, erasing UNIX and turning the machine into a pure DOS device—except I'm scared by the legalese paperwork. I don't suppose it's worth the effort. I'd only have the system for 90 days even if I went mad and signed that paper. I don't much want a monochrome system anyway.

Fortunately I saved all the boxes.

The sad part about all this is that I suspect the PC 6300 Plus is a good machine, and that if I had a color screen and a larger hard disk I'd like it a lot. The Los Angeles Science Fantasy Society has a PC 6300. As you'd suspect, LASFS being a science fiction club has attracted a fair number of wizards and hackers, and they're all very happy with the club's AT&T machine. Most people I've talked to about the color version of the 6300 Plus are quite favorably impressed.

On the other hand, I'm beginning to wonder whether AT&T will *ever* learn much about marketing.

Atari Faire

Atari has sponsored a series of Atari Faires. The one I went to was held in the San Jose Civic Center. I'm told about 5000 people came. Certainly the place was packed the Sunday afternoon I was there. The atmosphere reminded me of the early days of the West Coast Computer Faire. Lots of excitement.

The most interesting exhibit was Atari's, where they displayed an ST with a blitter chip installed. A blitter is a hardware graphics-manipulation device that speeds up animation something wonderful. It's supposed to be available for dealer installation—it takes soldering—about the time you read this.

Meanwhile, there was a lot of new software and the promise of even more. At the FTL booth you could fly a fighter plane. So could the chap at the machine next to you. The machines were linked through the MIDI port, so that you could see, and shoot at, the plane controlled by the other guy. The program is called RPV, which stands for remotely piloted vehicle.

Michtron had the arcade game Dragon's Lair set up. That is, the Atari ST controls

continued

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a Pioneer laser disk player. You have to get the Dragon's Lair laser disk from a different outfit. When Dragon's Lair first came out I would probably have put some quarters into the system, but fortunately for me the game was so popular I could never get close to it. Now I have a copy, complete with laser disk—and so far haven't had time to play it. Real Soon Now. But I know it works. I saw it at the Faire.

Paul Heckel was demonstrating a new version of Zoomracks; that's a program that reminds me a lot of the Execuscan Scan Card system, only this works on a computer. I've already recommended Zoomracks; now they've added a bunch of new features to make it even better.

Magic Sac

There was also MacCartridge. It's now called Magic Sac One. What this does is turn your Atari ST into a reasonable facsimile of a Macintosh; that is, a lot of Mac software, including Excel, runs fine on the ST plus Magic Sac. It even runs about 20 percent faster. They don't have MacWrite running just yet, but they're more than half way to it. (It seems the MacWrite developers didn't follow the MacRules.) Magic Sac Plus contains a real-time clock and calendar. Both Magic Sac One and Magic Sac Plus include transfer cable to get software from Mac to Atari.

A few notes of caution. First, not everything that runs on a Mac can be made to run on the Atari ST, although in general all software that follows the Mac developer guidelines will. Second, you have to get the Mac software into Atari ST (standard IBM 3½-inch) disk format. This is simple enough unless the Mac program is copy-protected. Finally, you need Macintosh ROMs, and David Small and company, mostly from fear of legal action by Apple, don't sell them.

Not that getting those ROMs is a problem. There were at least two dealers at the Atari Faire who offered Macintosh ROMs for about $30. As to software, it's not that hard to link up the ST to a Mac and port software over. There's plenty of public domain software available on bulletin boards.

There's also what can only be called pirate copies of commercial programs. These, I'm pleased to say, aren't being sold, and those who have them have been pretty careful not to pass them along to people who haven't already bought a copy of the original program. I suppose eventually that will get out of hand; the remedy is for the software publishers to make Mac software available in Atari ST format. I expect that will begin happening just about the time you read this.

Porting software to Magic Sac has shown some instructive lessons. For example: a great deal of Mac software writes to memory location 0. This is expressly forbidden for Mac software, but as it happens you can get away with it, since there is writable RAM at that location. The ST, however, has ROM at location 0, and any attempt to write there causes an instant bus error. Properly written Mac software won't do that, but some Mac software manages to pass a Nil (zero) pointer to a system call and survive. There are other such incurable glitches; but well-behaved Mac software really does run on the ST.

Whenever I write about the Magic Sac, I get mail protesting that there's something unethical about it: Apple spent all that money developing the Mac operating system, and Magic Sac turns a low-cost Atari ST into a machine that can run the Mac software, and even do it faster. Is this fair?

The interesting part is that few of those who think this way are unhappy about the flood of PClones on the market. Indeed, most of them revel in IBM's discomfort.

As for me, this always has been the User's Column. I'll always be for anything that benefits users and isn't illegal. Magic

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Sac will let you run about 500 Macintosh programs on the ST, and they're constantly expanding that base. I like it. Now if they can only get MacInTax ported over to it . . .

Atari Faire Wrap-up

I collected a good deal of software. Alas, I left from the Atari Faire to go to Washington, returned from Washington to the PC Faire, and had enough to keep me busy the week after that; consequently, I have collected a pile of Atari stuff I haven't been able to run yet.

One thing I should comment on is Antic's CAD-3D, which they were demonstrating coupled with a pair of goggles. The goggles are electronically controlled to blank out each eye in alternation. This is synchronized with what's painted on the screen. The result is startling. Things really jump out of the screen at you. It flickered too much to be comfortable for me. Gary Yost, Antic's marketing manager, told me that was due to the fluorescent ambient light in the room. Could be; I haven't had a chance to see it anywhere else. By next month I ought to have my own. (Update: I do now—and it still flickers.)

Antic also supplied me with a mess of demonstration programs of objects like pentagrams and dodecahedrons rotating in three dimensions; very impressive.

In my judgment, the ST really is the machine "for the rest of us." It's fun, it's powerful, and most of us can afford one.

PC Faire

It was quite a week: I went from the Atari Faire to Washington for a meeting of the board of the Space Academy, then back to San Francisco for the PC Faire.

That turned out to be larger than the Atari Faire, but not *that* much larger. Mostly it was dealers with blowout sales.

There were a few new items. I went around collecting stuff, but since this was after the Atari Faire I had even less chance to check things out. Real Soon Now.

One thing that impressed me is a program called Point Five. This bills itself as "The First Word Processor for Numbers," and my first cut shows nothing to contradict that. Point Five has 150 math functions, including the ability to invert matrices.

My first attempt to program a computer was writing a matrix-inversion program for the IBM 650; I was part of the grade-prediction project at the University of Washington. Matrix inversions can produce systems of multiple regression equations, which can be highly useful if you're trying to make complex statistical predictions. I haven't tried Point Five for that, but I see no reason why it wouldn't work.

Point Five resembles a poor man's spreadsheet, but not so formally structured. It mostly works off scratchpad notations. There's also a data entry editor.

I was pretty impressed with Point Five at the Faire. It's not copy-protected, and you get the 8087 version along with the regular one.

Back-It

Back-It is a program something like Fastback, but it is supposed to be a bit simpler to use and more flexible. It does what you expect a backup program to do, including automatically formatting unformatted disks to write the backup onto.

I've no strong reason to prefer this to Fastback, but then I've no strong preference for Fastback either. I do know that anyone who uses a hard disk and doesn't have a good backup program skates on thinner ice than I would.

Wine, Anyone?

Adam Osborne's Paperback Software is built around a concept of which I thoroughly approve, namely, that good software doesn't have to cost a lot.

One of Osborne's latest products is a specialized database/decision program, Wines on Disk. The name is a bit misleading: it ought to say "American Wines on Disk," or more precisely, "Many American Wines, mostly Californian, as interpreted by Anthony Dias Blue."

Some of you have probably heard Mr. Blue on CBS radio. I've always been impressed by him. Wines on Disk is structured like a short consultation with Blue—you tell the program what you're looking for, and it makes recommendations. I didn't find any recommendation I particularly disagreed with, and a couple surprised me rather favorably.

Zenith Z-181

The real hit of the PC Faire was the Zenith Z-181 portable computer. It's a full PClone with the usual Zenith additions. Just after I got home, my own arrived.

The Z-181 weighs 11.5 pounds, a bit heavy for a laptop, although it can be used as one. Mine boasts two 3½-inch disk drives that hold 730K bytes each, 655K bytes of memory that can be partitioned into main memory and RAM disk; a battery pack; and an electroluminescent backlit LCD that is as easy to read as any CRT monitor. The literature says it will run up to five hours on one full battery charge.

I haven't tested how long it runs, but it will go three hours under heavy use. Just after my Z-181 arrived, Roberta and I left for Santa Maria for the annual Tom and Terri Pinckard science fiction discussion,

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salon, and weekend party. Naturally I took the Z-181, and when I got it set up it was the hit of the party. Everyone wanted to play with it, and since I'd set it on a table a long way from an outlet there was nothing for it but to run it on batteries alone. Three hours later when I was ready to go home, the "low battery" light hadn't gone on.

The instructions emphasize that you have to be careful about the batteries. You shouldn't ever leave the machine plugged in too long, and you want to let it run down every now and then. I'd have thought it wouldn't be hard to put in some kind of protection from overcharge—after all, if you use this as your main machine, you'll want to leave it plugged in all the time and have done with it. Surely there's a way you can do that?

There's one other problem. When the Z-181 is all folded up, it's a tad awkward to carry around. The machine is quite handsome but also rather slick and heavy, and there's nothing like a carrying handle. Indeed, although the invoice said there was a carrying case, there wasn't one in the package I got. The next day, though, I got an unsolicited package from American Tourister. There wasn't any clue that it had anything to do with Zenith, but inside the box was a black nylon zipper bag that is certainly the right size to hold the Z-181, power supply, and some disks. If Zenith didn't cause it to be sent, there's something odd happening.

Except for trivia like that, I have found nothing I dislike about the Z-181. I don't have much software for it—I was only able to get Microsoft BASIC, Multiplan, and Word—but what I do have works fine. I've never used Microsoft Word, and the version I put on the Z-181 is an older one; I'm told that the latest Word lets you suppress the menus and do other interesting things. I'd prefer that, since Word menus take several lines.

On the other hand, all I had was a disk: Word came without documents. I'd never used it before, but I was able to plunge right in. I didn't find out about some of the fine points like style sheets, but I was able to record my comments about the Z-181.

We did have one glitch. As I mentioned earlier, I took the Z-181 up to our weekend party. The machine came with little plastic

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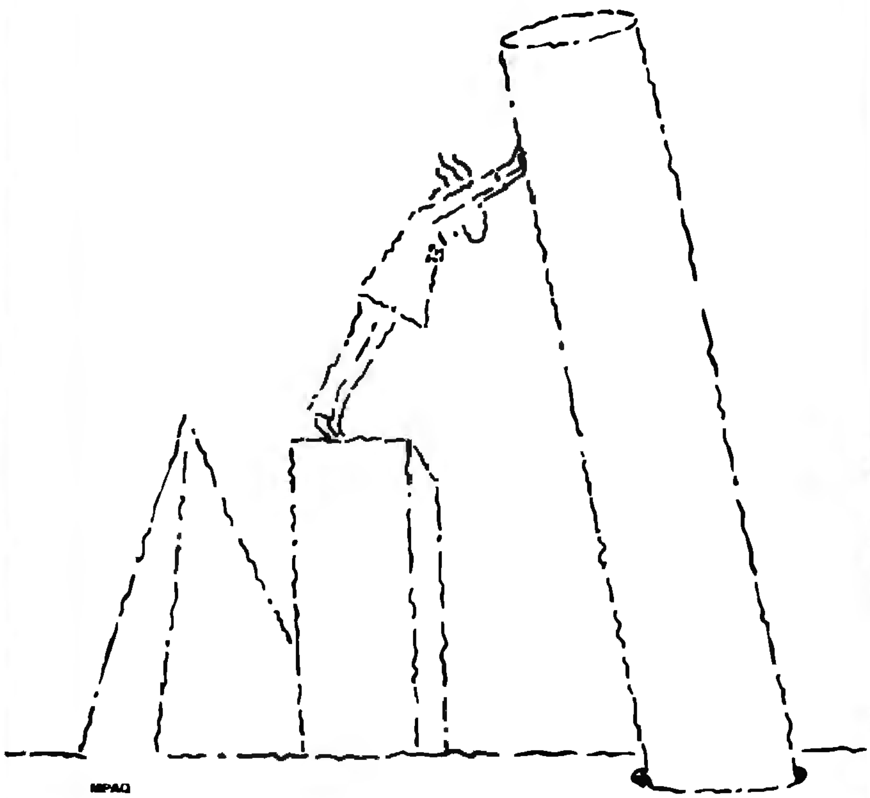

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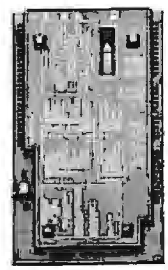

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fake disks inserted in the drives, so I put those in before packing it up in the American Tourister case and loaded it into the back seat. We certainly didn't have an unusual trip up, but when I set the machine up it wouldn't boot.

I thought at first it was the disk, but I had several boot disks, and none worked. It simply wouldn't read from the A drive.

Fortunately, this is a full Zenith PC, meaning that it has a built-in PROM monitor that you invoke by pressing Control-Alt-Function-Insert all at once. The monitor has a disk test; sure enough, it didn't want to read the A disk. However, you can, from the monitor, command the machine to boot off the B disk, which is what I did. It booted fine. I then put a disk in the A drive and asked for a directory. No trouble, so I put the boot disk in A, turned the machine off and back on—and voilà! Whatever the problem had been was cured. I suppose the A disk head got in some kind of weird position.

Anyway, my initial impression of the Z-181 is highly favorable. The screen is very easy to read. The keyboard is a Zenith. Alas, they have managed to get one too many keys between the home keys and Return, and the Backspace key is a bit harder to reach than I prefer; but Zenith has always made keyboards as good as any in the industry, and they've done it this time as well. The disk drives are as fast as any 3½-inch drives, which is to say as fast as most 5¼-inch drives but not up to the speed of 8-inch floppies. There are jacks for an external monitor.

My version of the Z-181 has a dummy module where the 300-/1200-baud modem is supposed to be installed Real Soon Now. Recall that the Z-181 has a full 25-line by 80-character screen, which means it beats heck out of the NEC PC-8201 (8 lines of 40 characters) for out-of-town communications.

When that modem is installed, I strongly think I am going to adopt the Z-181 as my traveling companion.

Winding Down

It's 4 a.m., and this is due in to BYTE by dawn. The game of the month is from Electronic Arts. Starflight is a game of exploration and combat that kept me interested long after I ought to have given up and gone back to work. Starflight is as much a career as a game: you outfit a ship, train the crew, and go off exploring. You'd better find enough minerals and stuff to pay for your fuel. I really found it fascinating.

Another nice thing about Starflight is that it isn't copy-protected. Instead, they furnish you with some hard-to-copy maps and manuals and a big circular type of slide rule: at certain critical points in the game you have to use the slide rule to generate code numbers. If you don't have the code numbers, the game goes on, then stops in a rather interesting manner.

If you like science fiction adventure games, you'll probably like Starflight.

The book of the month is by Richard Pipes, *Survival Is Not Enough* (Touchstone/Simon and Schuster, $9.95). This is simply the best analysis of the Soviet Union I've ever seen. Pipes, a Harvard professor of history, shows how Soviet foreign policy is generated and what we will have to do about it. I wish everyone would read this book.

Next month I should have WordPerfect and the latest version of Microsoft Word for the Z-181. We'll have a play-off. ■

Jerry Pournelle welcomes readers' comments and opinions. Send a self-addressed, stamped envelope to Jerry Pournelle, c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458. Please put your address on the letter as well as on the envelope. Due to the high volume of letters, Jerry cannot guarantee a personal reply.

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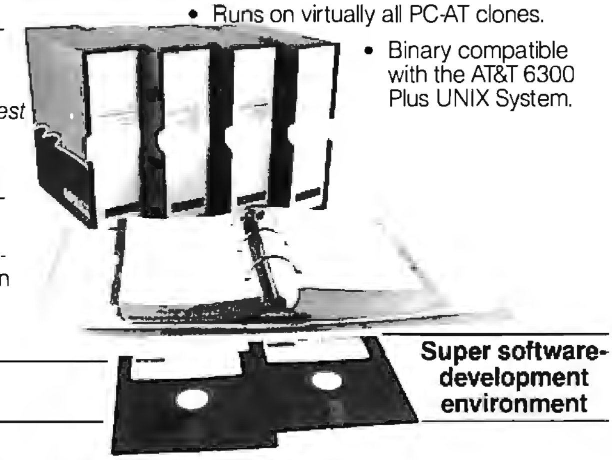

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View and Reviews

Bruce Webster

Some impressions of the new Apple IIGS, awards, and predictions

I've managed to get my hands on an Apple IIGS, and I'll give some first impressions. I've also started a new tradition in this column—the Fritzie awards for various achievements in the industry—and continued an old one, namely, predictions for the year to come. But first, the IIGS.

A First Look

An Apple IIGS sits just a foot or so to the right of me as I type this on my Compaq, wedged between that and the Atari 1040ST, preempting the space where the Epson RX-80 (in temporary exile on the floor) used to sit. It is a sleek, attractive system with three major components: a detachable keyboard, the "mainframe" (i.e., the actual system box), and a monochrome monitor sitting on top. The entire footprint is a little wider and a few inches deeper than the Macintosh, but this is an open system that can accept up to eight cards inside, so the small size is impressive.

Unfortunately, beyond looking at it and running my old Apple II software, there isn't much I can do with it. It has a monochrome display instead of the RGB monitor (I know, I know, I'm spoiled), I have almost no software for it, and I can't even find a system boot disk in the packing materials. Development software is on the way but not yet here, so my only programming tool at the moment is the miniassembler built into the ROM. However, Apple is sponsoring a IIGS developers conference in a few weeks, and I've managed to wangle an invitation to learn more about the latest product in the 10-year-old Apple II line.

The IIGS was previewed in detail in BYTE's October 1986 issue, and I suspect that a full review is due sometime soon. My comments, then, are not a review of the machine, but a collection of first impressions based on hands-on use and discussion on BIX.

What Apple Did Right

The first thing Apple did right was to bring out a new II-series machine. A few years ago, Apple seemed determined to kill off the II line, as if it were somehow embarrassed by it, even though the IIe was (at that time) Apple's major source of income. Apple II sales have been dropping for some time; that drop, combined with rising Macintosh Plus sales, has made the Macintosh Apple's new cash cow. The IIGS—when finally available in quantity—should sell well and bring lots of money to Apple's coffers.

Apple also did well to bring Steve Wozniak back and have him finish the IIx project he started a few years ago. That act won back the support of a lot of Apple owners who were not pleased with the political infighting that went on back then, especially when it resulted in Woz's departure from Apple. Apple's recognition and rectification of that mistake is shown by the "Woz signature" IIGSs that Apple is initially selling.

The IIGS itself appears to be a good compromise between IIe compatibility and new features and capabilities. The new graphics modes look clear and sharp—I was impressed with Paintworks Plus—while the ability to run old Apple programs takes advantage of a massive (if somewhat dated) software base. Of course, the super-hi-res graphics modes don't use the bizarre mapping scheme that is the legacy of the original Apple II. Instead, they have a simple but flexible method that lets you easily switch color palettes on every scan line.

Providing an upgrade path for IIes via the IIGS card was also a smart move. There are a million or two IIes out in the world, and I suspect a sizable fraction of those owners will buy IIGS cards. At $500 each—less than an Atari 520ST system—both dealers and Apple should do well. And the IIe owners won't feel left out in the cold.

The marvelous synthesizer hardware in the IIGS was a bold step. I heard some (digitized? synthesized?) music during the demonstration at the computer store running through a pair of Bose speakers, and I was extremely impressed at the quality. Likewise, some digitized voice was played back; it sounded as though it were coming off a high-quality cassette tape.

The Apple II–compatible open architecture was a wise move. The IIc has been something of a disappointment for Apple; most customers, it appears, just don't want a closed Apple II. One heard much speculation prior to the IIGS release that the slots would not be Apple II–compatible, but it appears that common sense prevailed. Of course, one now hears rumors of a 68000 card that plugs into slot 0 (the special memory-expansion slot), allowing the IIGS to run Mac software, but that might be pushing things a bit.

The IIGS Toolbox, which resides in a mixture of ROM and RAM, appears to have been a good idea. I say "appears" because I have no technical documentation nor development software, and so have no way of telling what was included and what was left out. However, the Mac Toolbox has done much to standardize the Mac interface; I suspect (from my brief experience with Paintworks Plus) that the IIGS Toolbox may do the same.

What Apple Did Wrong

The first thing Apple did wrong was not to let Woz finish the IIx project a few years ago. The IIGS is an excellent replace-

continued

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Table 1: *All prices are over-the-phone anonymous quotes from stores in Utah and represent the best prices found.*

Minimal systems:	
Atari 1040ST (1Mb, 720K drive, monochrome)	$1000
Amiga (512K, 880K drive, RGB)	$1500
Apple IIGS (256K, 800K drive, monochrome)	$1530
Mac 512K Enhanced (512K, 800K drive, monochrome)	$1700
Standard systems—1Mb, two 3½-inch disk drives, RGB monitor (except for the Macintosh):	
Atari 1040ST	$1500
Amiga (with Alegra expansion board)	$2100
Mac Plus (monochrome only)	$2250
Apple IIGS (with Apple expansion board)	$2550

ment for the Apple II line, but it's awfully late in coming. The technology is more trailing edge than leading edge in many areas. In terms of graphics performance, the IIGS is already behind the Atari ST and the Amiga, both of which are less expensive and both of which have more software taking advantage of their graphics. The IIGS doesn't leap very far ahead.

With the IIGS, Apple followed its usual high pricing policy. A minimal system—a IIGS with 256K bytes of RAM, a 3½-inch (800K-byte) disk drive, and a monochrome monitor—costs $1530. For about the same amount (a little less, actually), I can go out and buy a 1040ST with 1 megabyte of RAM, two 3½-inch drives (720K bytes each), and an RGB monitor. To buy a similarly equipped IIGS would cost me about $2550, or more than $1000 more. For the difference in price, I can buy another 1040ST, with one 3½-inch disk drive and a monochrome monitor. Table 1 shows some additional comparisons between minimal and equivalent systems. These prices are all from stores here in Utah, so I called two Apple dealers in San Diego to check on IIGS prices. I was still quoted straight list price, even on a complete system.

Of course, the high prices won't matter that much because the IIGS is going to be in limited supply for the first few months, so dealers should be able to sell all they get in. How many will they have to sell? Most estimates of shipments from now until the start of 1987 indicate an average of about 10 systems per dealer, or about one per week. The two Apple dealers in San Diego said they had received enough deposits so that I couldn't get anything until late January. The problem is, what customer having seen the IIGS is going to want to buy a IIe or (worse yet) a IIc? The IIe can at least be brought up to IIGS performance when the upgrade card comes out sometime early this year; Apple says it has no plans for a similar upgrade for the IIc (ah, the wonders of a closed architecture!). I suspect that IIc sales will be very poor at dealerships displaying the IIGS, and that even IIe sales won't be all that hot.

Some internal design decisions are also questionable. For example, it has only one super-hi-res screen display buffer, and it is in a fixed area of RAM. This is unlike the Atari ST and the Amiga, both of which give you lots of freedom as to where you place the screen display buffer, and both of which allow you to have multiple screen buffers, which you can switch between by merely changing a pointer. Even the old Apple II hi-res graphics gives you two graphics pages (at 2000 and 4000 hexadecimal), allowing you to do page flipping.

Performance is also an issue. Apple II software runs at two to three times regular speed, which is wonderful. However, Paintworks Plus—which is essentially a color version of MacPaint, complete with menus and dialog boxes—ran quite a bit slower than MacPaint on the original 128K-byte Mac. I suspect that applications using the IIGS Toolbox and the super-hi-res graphics are going to look sluggish compared to the Mac, the ST, and the Amiga.

Other minor quibbles: sound and memory. The sound is fantastic, but the audio output port on the back is monaural (as opposed to the stereo output on the back of the Amiga). You can get stereo by going directly to the sound hardware inside the IIGS, but I can't believe it would have been difficult or expensive to put the stereo output on the back. In a similar fashion, the amount of memory in a base machine—256K bytes—isn't enough for many IIGS-specific applications, so almost every IIGS owner will need the RAM expansion card. Luckily, expansion is relatively inexpensive: $130 for the card with 256K bytes, and $70 for every additional 256K bytes. But why couldn't Apple just put 512K bytes (or more) on the motherboard and go from there?

And the Verdict Is...

My overall evaluation of the IIGS is a qualified approval. It was needed to prevent the Apple II line from dying off during the next year or so. However, Apple didn't go far enough in some of the improvements that were made. Furthermore, the price/supply problems may really hurt Apple this Christmas by whetting customers' appetites for a more powerful machine, then forcing them to turn to the Amiga and the Atari ST. However, Apple is in a great financial position, with no long-term debts and half a billion dollars in the bank, so it can afford the possible drop in IIe/IIc sales while waiting for IIGS production and sales to climb.

How should Apple improve the IIGS? Well, there isn't much they can do at this point, except to possibly bring out a more powerful graphics card to replace the on-board super-hi-res graphics. Unfortunately, that would recreate the IBM confusion, where multiple incompatible graphics standards force developers to aim at the lowest common denominator. A higher clock speed on the processor would also help to improve performance. Beyond that, all I can suggest is that Apple lower the price—and they'll do that once supply starts to exceed demand, just as they've always done.

Looking Back at 1986

Some months back, I did a midyear evaluation of my predictions for 1986. My verdict: All in all, I did pretty well. The months that have passed haven't changed much, so here's my not-quite-the-end-of-the-year evaluation. My major hits: plummeting sales of the Apple IIe/IIc; Apple's efforts to change its directions; Mac penetration of the business market (though not for the reasons I had given); an MS-DOS box for the Amiga; the upsurge of 680x0-based systems; IBM's hand-sitting; introduction of an IBM laptop; and the clones taking over the MS-DOS market.

My major miss: Compaq domination of the laptop market. Predictions that haven't arrived yet: an upsurge in the home market (which may yet come, but a year later than I had predicted); introduction of an "open Mac" (which is coming, but not until next spring); and UNIX on the Mac, ST, and Amiga (also appears to be coming, but not until the end of '86/start of '87). Hard to call: Commodore and Atari both doing well. They didn't do as well as I had expected, but Commodore has sold about 100,000 Amigas in the U.S., and Atari has sold almost that many STs here and a similar number outside the U.S. Both companies are much healthier financially than they were a year ago, but they've both got a ways to go.

The year 1986 has been a good one for the industry. The competition was harsh at times, but the major players all seem to

continued

The trend in software is toward lower prices, no copy protection, and more reasonable licensing agreements.

be doing well, and the consumers are benefiting by lower prices and better products. Computer magazines are no longer failing left and right, and there is a new upswing in the computer book market. The trend in software is toward lower prices, no copy protection, and more reasonable licensing agreements. I don't think we'll ever again see the glory days of 1980–1984, but it's probably just as well. The industry is still exciting, still unpredictable (though guys like me keep trying), and still one of the best places to have a good time.

Looking back over my columns for 1986, I can see some corrections, revisions, and amendments I need to make. Step Lively Software never (to my knowledge) released its On Stage Pascal compiler for the Macintosh, and, in fact, I've never heard from them (or of them) again. The Atari 1040ST does not have RF or composite video output, contrary to Atari's press releases at the machine's announcement. Turbo Pascal for the Macintosh did not ship in the first quarter of 1986 . . . nor in the second, nor the third. Fourth-quarter shipping (mid-November 1986) looks pretty firm, though.

And speaking of Borland, letters and reports from users have tempered my initial enthusiasm for Turbo Prolog. It appears to be far less standard than my review suggested, and it lacks much of the flexibility of Prolog interpreters. This doesn't negate its positive attributes (like its excellent user interface), nor does it mean that it can't be used for serious development. What it does mean is that Turbo Prolog can't do (or do easily) many of the things that other Prolog interpreters and compilers can. Keep that in mind when deciding whether or not to purchase Turbo Prolog.

Awards for 1986: The Fritzies

As you all know, I'm in the habit of selecting a "product of the month" each column. The natural extension of that is to select a product of the year. I decline. Keeping with an old American tradition, however, I will cheerfully hand out awards for products or accomplishments in different categories. And keeping with another old American tradition, I will give these awards a cutesy name: the Fritzies, after my illustrious ancestor, Fritzworth von Webster III.

Most of the Fritzies are positive awards, recognizing achievements worthy of emulation. Some, however, point out (with perfect hindsight) efforts best unemulated. No hard feelings are intended, but if the shoe fits . . . anyway, I've also listed runners-up for most of the awards as well, anxious as I am to spread some of the recognition around. The envelopes, please.

The 1986 Fritzie for Best Publication Other than BYTE goes to *MacTutor*. I have praised *MacTutor* in the past and will continue to do so in the future. David and Laura Smith have, for nearly two years now, put out the best rag for Macintosh programmers, stuffed with enlightening diagrams, working code, explained mysteries, patched bugs, hot ads, bandied rumors, heated opinions—in short, just about everything that programmers cheerfully kill for. And there is a rough, honest edge to the magazine that the slicker publications have sanded away. A subscription to *MacTutor* (P.O. Box 400, Placentia, CA 92670, (714) 630-3730) is $30 a year. My only regret is that *MacTutor* is limited to the Mac; would that similar publications of equal quality existed for the ST and Amiga, or that *MacTutor* could somehow take the other 68000-based systems under its wings. The runners-up are *Computer+Software News*, a controlled-circulation weekly that is easily the best industry-tracking publication around, and *Computer Language* and *Dr. Dobb's Journal*, which are head-to-head competitors in the MS-DOS/C/80x86 market, with side trips to other operating systems, languages, and processors.

The 1986 Fritzie for Best Computer Language Implementation goes to LightspeedC from Think Technologies. I discussed LightspeedC in the September 1986 issue, so I won't rehash its many fine features (or its deficiencies). I will say that LightspeedC has set new standards for microcomputer development environments, much as the IBM PC version of Turbo Pascal did a few years back, and that (like Turbo Pascal) most new language implementations on the Mac will be compared to it. The runners-up are DevpacST, a 68000 assembler for the Atari ST from HiSoft, and TML Pascal, the first native code Pascal compiler for the Mac, from TML Systems.

The 1986 Fritzie for Best Utility goes to Metascope from Metadigm Inc. Metascope (reviewed in the November 1986 issue) is an interactive, multiwindow debugger for the Amiga. It's easy to use and takes advantage of the Amiga's multitasking system to let you run your program in one window while looking at memory, registers, and code in other windows. The runners-up are Acta, an outline processor disguised as a Mac desk accessory, from Symmetry Corporation and TxEd, the Amiga program editor from MicroSmiths, which—while not perfect—fills a real gap in Amiga software.

With the proviso that I don't get a chance to look at many applications, the 1986 Fritzie for Best Application goes to More, a third-generation idea-and-outline processor from Living Videotext (the makers of ThinkTank). More is the epitome of what is good about Macintosh software and the Mac user interface: easy to use, powerful, and flexible. The runner-up is Microsoft Excel, the nicest spreadsheet I've ever used.

The 1986 Fritzie for Best System goes to the Atari 1040ST. While I do have well-documented gripes about the ST, the ability to buy a 1-megabyte 68000-based system with two 720K-byte drives and an RGB monitor for $1500 covers a multitude of sins. If Atari releases a version with a blitter chip before the end of 1986, it'll just solidify my choice. The runners-up are the Commodore Amiga 1000, whose potential hasn't yet been realized, and the Mac Plus, which has finally gotten the Macintosh into the business market in respectable numbers.

The 1986 Fritzie for Best Hack goes to Dave Small and Data Pacific Inc. for Magic Sac (originally called MacCartridge), a software/hardware package that lets you run Macintosh software on your Atari ST. Against most predictions (including my own), Dave has managed to bring his product to market. He simply sells it without the Macintosh ROMs; you have to supply your own. Apparently this has not been a problem: At a recent Atari show, Dave sold out within hours, and there were lots and lots of people selling Mac ROMs to plug into it. The runner-up is the Prodigy 4 upgrade from Levco, which takes a 16.67-megahertz 68020, a 68881 math coprocessor, 4 megabytes of RAM, and a 20-megabyte hard disk, and crams it all into a regular Mac case, turning the little beige toaster into a VAX killer.

The 1986 Fritzie for Company Achievement goes to Michtron Inc., which saw an opportunity—the Atari ST—and ran with it, turning out a large number of cheap, useful, and largely unprotected programs. Michtron also gets an honorary award for Ugliest Packaging. The runner-up (for Company Achievement, not Ugliest Packaging) is Think Technologies, for releasing both LightspeedC and Lightspeed Pascal and thus setting new standards for development environments.

The 1986 Fritzie for Best Self-Inflicted Wounds (the Osborne/

continued

Jobs award) goes to Commodore Business Machines. CBM took a potentially very hot machine—the Amiga—and did just about everything wrong that they could in selling it. Examples? Pushing a not-quite-finished machine with a not-quite-finished user interface and a not-quite-finished operating system onto the market. Poorly conceived advertising—when there was advertising at all. Avoidance of just about every major trade show, even though Jerry Pournelle described the crowds around the Commodore booth at COMDEX/Atlanta—the one major show where CBM did make an appearance—as being in a "feeding frenzy." Alienation of third-party developers during several critical months. Internal confusion as to just what market the Amiga was aimed at. Despite all that, Commodore has managed to sell about 150,000 systems worldwide, about the same as Atari, and has actually outsold the ST in North America. Imagine how many Amigas CBM might have sold if they had done things right. The runners-up are IBM, for not having the foresight to see that low-powered, high-priced hardware would not thrive in the highly competitive business/MS-DOS marketplace; Apple, for bringing out the IIGS at too high a price and in too limited a quantity; and MicroPro, the makers of WordStar, who have managed to take what was a dominant position in the word-processing market and completely squander it.

The 1986 Fritzie for Best Recovery from Self-Inflicted Wounds goes to John Scully and Apple. Apple appears to be doing its best to turn things around from the misdirection of the past few years. The IIGS should have been brought out a few years ago, when Woz was originally working on it, but better late than never. And even with the problems mentioned earlier, it's still a positive step. The Mac Plus—which is what the original Mac should have been—is selling extremely well. And the much-rumored open Macs should help to entrench Apple as the main alternative to IBM cloning. The runner-up is Jack Tramiel, who took a near-moribund Atari and turned it into a profitable enterprise delivering what is probably the best price/performance system (the 1040ST) in the industry.

The 1986 Fritzie for Best Dying Industry Issue goes to copy protection, which appears to be on the way out. Lack of copy protection has become a selling advantage, with many consumers simply refusing to buy any product that is copy-protected. The continuing sophistication of "backup" programs allows those most interested in pirating to do so. And major publishers like Microsoft are announcing removal of copy protection from their products. The runners-up are Apple's legal threats against competing firms with Mac-like user interfaces and the "Real Men Don't Use Icons/Menus/Mice" retrenchment.

The 1986 Fritzie for Worst New Industry Issue goes to IBM's much-rumored proprietary operating system. For more than a year now, the ever-infamous industry analysts have been predicting that IBM would release a new line of computers using a proprietary operating system. It hasn't happened as of this writing, though it may yet (see below). My reaction: Who cares? If IBM does it, they will most likely just isolate themselves from the largest marketplace, in which they can't really compete anymore anyway. IBM isn't going to fold; neither will they magically capture the entire software industry and the *Fortune* 1000 with a proprietary operating system. The runners-up are any other IBM rumors that have surfaced recently or might surface in the coming months.

The 1986 Fritzie for Best-Kept Secret goes to the burgeoning market for synthesizers and other electronic instruments. These wonders are hot, cheap, and seductive. For the price of a home computer, you can get an electronic keyboard that plays dozens of instruments and (in most cases) can be hooked up to your computer for further tricks. Go pick up a copy of *Electronic Musician*. A subscription to *Electronic Musician* (5615 West Cer-

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mak Rd., Cicero, IL 60650, (312) 762-2193) is $22 a year. This is probably the best all-round periodical on the subject. But be warned that your pocketbook could suffer serious damage as a result. The runners-up are the "desktop video" concept: the creation of video presentations by using your computer to integrate external video, sound, and computer-generated graphics, including titles and animation; and the "home entertainment studio" concept: interconnecting computers, VCRs, optical and compact disks, stereo components, TVs and other monitors, and synthesizers into one massive complex capable of doing some pretty incredible things. Look for more coverage here of all these concepts in the coming months.

Predictions for 1987

Being insufferably (and probably unjustifiably) pleased with myself for my overall batting average on my 1986 predictions, I thought I'd come up with a new set for 1987. Technically speaking, these go from October 1986 to October 1987, since it is now early October as I write this. On the other hand, if I can stretch the calendar around to make myself look better ... anyway, here's what I think will happen in the next year or so.

The mass business market will complete its transition from an IBM standard to an Intel/MS-DOS/expansion bus standard. Though hordes of industry analysts will continue to read portents in every rumble from IBM's bowels, the market will be more concerned with price, performance, and quality, and thus won't really be affected by what IBM does or does not do. This will be the ultimate vindication of an observation by Doug Clapp in *InfoWorld* some years back: Folks aren't so much concerned about IBM compatibility as they are about Lotus 1-2-3 compatibility.

The standard for 80386-based systems will be established without any help from IBM; instead, Microsoft, the clone makers, and third-party manufacturers will create a de facto standard that will become well entrenched before IBM can get an 80386-based system out to market. This could create the amusing spectacle of watching IBM shoot itself in the foot by introducing a machine that doesn't follow that standard and that no one (except for die-hard IBM users) wants to buy, or watching IBM be forced to adopt a standard created by someone else. Think of it: IBM joins the ranks of the clones!

IBM will abandon and/or cut itself off from the mass business market. This will happen through some combination of the following events: IBM will pull its low-end PCs (anything with an 8088) off the market; IBM will introduce a system or line of systems with proprietary hardware and software, but the poor price/performance ratio and concern for software compatibility will keep it from doing well; IBM will introduce an 80386-based machine that is not compatible with the de facto standard; IBM will continue to charge too much for its systems. Whatever happens, the current trend of IBM losing market share will continue, and (as happened in 1986) the total number of units IBM sells will continue to drop.

Apple, Atari, and Commodore will all introduce computer systems with similar specs: a 68020 processor, a 68881 math coprocessor, 1 to 4 megabytes of RAM, a 20-megabyte hard disk, possibly some sort of memory management unit, a 1024 by 1024 monochrome display (or at least the capability to drive such), expansion slots, and UNIX or a UNIX-like operating system,

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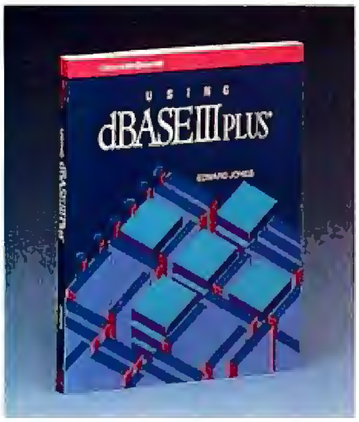

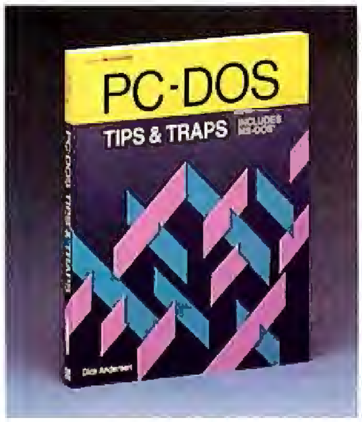

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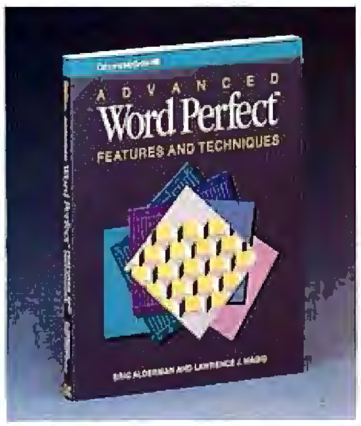

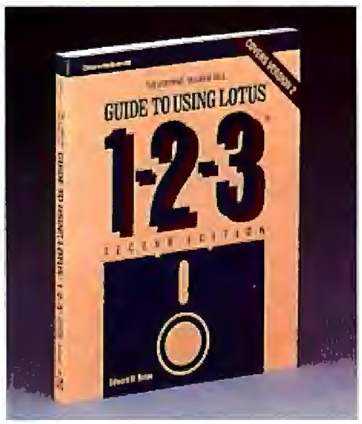

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with an optional mouse-menu-and-icon user interface. Atari's will be the cheapest, Apple's will be the most expensive, and Commodore's will have the best color graphics.

The Apple IIc will either die or be marketed at a significant discount (possibly in the mass market). The Apple IIe will be phased out as continued competition from Atari and Commodore forces Apple to drop prices on the IIGS; look for large numbers of inventoried IIes (and possibly IIcs) to flood the educational market. The IIGS will do well, due more to Apple's sharp marketing than to any real technological edge, and the IIGS upgrade for Apple IIes will also sell well, if and when it finally comes out.

Apple will introduce an open Mac, not to be confused with the UNIX box above. It will be similar to the IIGS in setup, that is, the same detachable keyboard and mouse, a "mainframe" box with a slot or slots, and a separate monitor. Only Apple's initial high price will keep this computer from selling well at first, but street prices will drop soon after introduction. An MS-DOS/8088 coprocessor system will be introduced for the open Mac. It may take the form of a separate case (two 360K-byte drives, 8088 processor, RAM, ROM, a few expansion slots) with a cable to an interface card that plugs into the open Mac.

The Mac 512K Enhanced will be phased out (another Mac bites the dust), and the Mac Plus will continue to drop in price; by mid-1987, you should be able to buy one for less than $1500. Apple might also introduce a Mac Plus Plus, that is, a Mac Plus with a single expansion slot (for memory or the MS-DOS systems mentioned above).

The Amiga 1000 will be phased out and replaced by at least two systems: the UNIX machine mentioned above and a low-end version of the 1000 with limited expandability, like one or two 100-pin (Zorro standard) slots inside and no external bus. Commodore will continue its financial recovery but—unless West Chester gets its act together—will not really impress anyone with Amiga sales.

Atari will release new versions of the 520ST and 1040ST with a blitter chip, negating much of the Amiga's current advantage, and possibly with more memory as well. The upcoming public stock offering will allow Atari to advertise heavily at Christmas (1986), and Atari may well win the Christmas battles.

The home computer market will continue to be confused, this time by the entry (in significant numbers) of cheap MS-DOS systems. More and more homes will have two computers: an MS-DOS system for the parents (word processing, financial, telecom, bringing office work home) and a graphics-based system (Apple, Atari, Amiga) for the kids. I can now go out and buy both a 520ST (512K bytes, 720K-byte drive, RGB monitor) and an MS-DOS clone (256K bytes, two 360K-byte drives, monochrome monitor) and spend less than I did two years ago for an Apple IIe with 128K bytes of RAM and an RGB monitor. Anyone want to buy a slightly used IIe, cheap?

There's more I could say, but the above should be enough with which to hang myself. It's possible that I could have egg on my face by the time this issue hits the stands, since Apple, Atari, and Commodore may all make product announcements in the next few months. But, heck, it's fun to watch a columnist totally blow it now and then, isn't it?

In the Queue

I've got a bit of traveling to do between now and the next column. In a few weeks, I hope to attend the IIGS developers conference; right after that, I'll definitely attend Hackers 2.0, the second Hackers' Conference. A week or two later, I'll be at the Amiga developers conference, and then COMDEX (though I'll probably have to get my column in before going there). Look for reports there, more coverage of the IIGS, and additional software reviews. Until then, see you on the bit stream. ■

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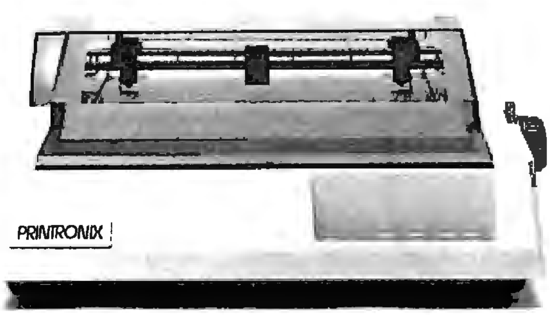

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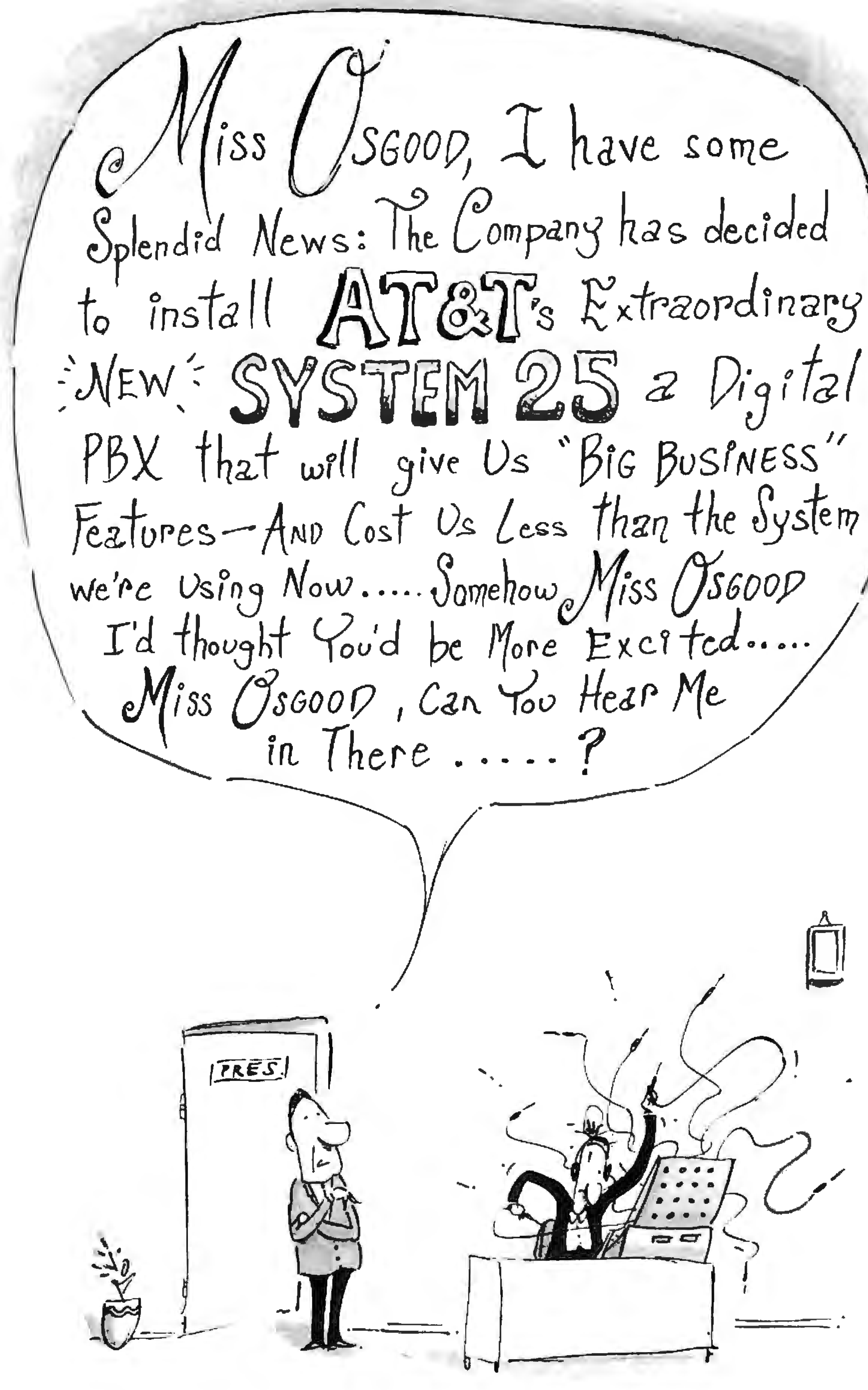
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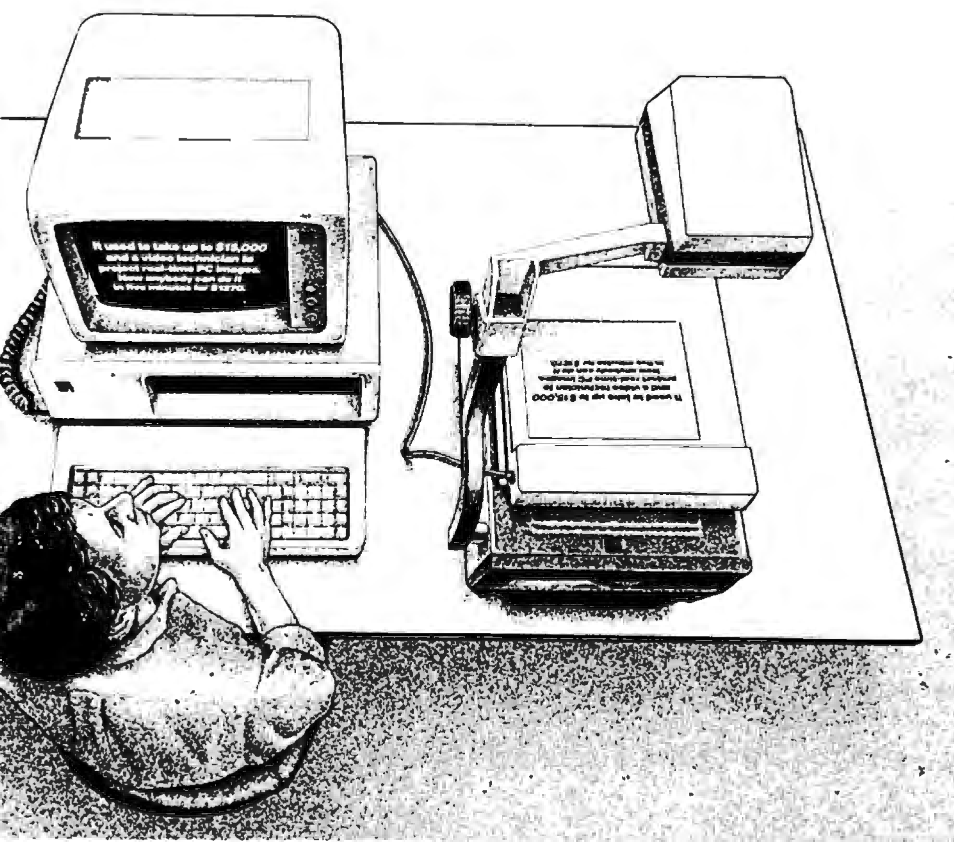

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The Software Robot

Dick Pountain

Automator mi learns and automates any task you teach it

I try not to think about all the hours I've spent customizing the software I use regularly. If this time were costed out in accountants' terms, it would add up to far more than the price of all my hardware and software put together.

It started when I began my computerized writing career using WordStar on a CP/M 2.2 machine. Various things about the way WordStar worked drove me crazy, but I assumed I had to live with them—until someone showed me a listing of the patch area, that is. I sat up for many consecutive nights making WordStar do some of the things I wanted and in the process learned 8080 assembly language. This is not meant to be a gibe at MicroPro; WordStar provided for far more customization than many programs of its day through its Winstall program. Yet it wasn't enough because the CP/M standard embraced such diverse hardware designs.

But even if all the hardware had been identical (as it almost is today in the IBM PC world), psychological factors would have intervened. Applications like WordStar are extraordinarily complex mechanisms, and different users have different mental pictures of what's going on inside the computer (known among ergonomists as the user image). And once color displays are introduced into a system, we enter the realm of personal preference with a vengeance. No software author, however smart, can hope to devise a user interface that will please everyone.

Things have improved a lot since the early WordStar days. Authors have become more aware of user interface design, and some enlightened software houses even pay heed to the research of cognitive psychologists and ergonomists. The better authors are humble enough to realize straight off that they can't please everyone and build extensive customization facilities into their programs. Most of the programs I now use (e.g., PC-Write, ProComm, SideKick) let me change screen colors and key assignments easily and, to some extent, automate frequently needed tasks. I can often work around any blind spots by using a keyboard enhancer like SmartKey, SuperKey, or Keyworks.

Though awareness of ergonomics and the need for customizing are gradually gaining hold in the industry, the primitive operating systems we have impose limits on what can be done. On the IBM PC in particular, programs that look good and work fast often use dirty tricks to get that way. When you're trying to do a job that requires two or three different programs, you may find that you can set up each individual program the way you like it, but that used together they clash. They can't export keystrokes to one another, or key assignments made inside one mess up some aspect of another. What we need is either an all-powerful operating system designed by a demigod or (more feasible) a program that can sit on top of one of our all-too-mortal operating systems and pull all the strings for us.

We now have at least one such program. Automator mi from Direct Technology Ltd. (Grove House, 551 London Rd., Isleworth, Middlesex TW7 4DS, U.K., (01)-847-1666; in the U.S.: Innovative Computer Products, 6284 Rucker Rd., Suite E, Indianapolis, IN 46220, (800) 228-5465 or Interactive Solutions Inc., 53 West Fort Lee Rd., Bogota, NJ 07603, (201) 488-3708) is advertised as the first "software robot." This claim is not just advertising hype; Automator does have all the features of a robot. You can teach the program tasks that it will faithfully reproduce, and it has "senses" with which to inspect its current environment (i.e., the state of the computer) and change its behavior accordingly.

Unlike a simple keyboard enhancer, Automator can inspect the screen and the clock as well as the keyboard. It has access to all the computer's resources at every level, down to direct memory and port accesses below the BIOS. It also includes a full-featured programming language with loops, conditionals, and interrupts. The net effect is that you can automate tasks that involve using any number of application programs, binding the different programs into an integrated system with a custom user interface.

Direct Technology developed Automator mi with a single purpose in mind: to simplify the process of linking IBM PCs to mainframes for its corporate clients (the "mi" stands for mainframe interface). But since most synchronous terminal emulators for the IBM PC are very dirty programs, Automator was forced to take control of more and more of the PC until it became a program of universal application. Automator can be used not only to simplify complex tasks but to build interactive tutorials that let the user operate with the real application rather than a dummy; to add context-sensitive help to programs; to provide automatic error recovery; to create unattended "robot" applications that operate at predetermined times; to create slide shows by capturing screens; and many more things that no one has thought of yet.

The Development System

Automator is sold as a development tool that can produce stand-alone programs that use a run-time package. Developers can purchase a license to sell such programs to third parties. The full Automator Development System comes as three main programs. LEARN.EXE is an interactive memory-resident program that you use to

continued

Dick Pountain is a technical author and software consultant living in London, England. He can be contacted c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

Pressing the designated 'hot key' after DO has been loaded will bring up a menu of compiled applications.

teach Automator tasks by doing them. As you teach it, LEARN generates a source code file in the Automator Control Language (ACL).

You can run these programs directly from LEARN while debugging and then compile them to a p-code file using the Automator compiler, AC.EXE. This doesn't produce an executable .EXE or .COM file, but rather a file that's executed by the run-time interpreter, DO.EXE. DO is also a memory-resident program. Pressing the designated "hot key" after DO has been loaded will bring up a menu of compiled applications, just like SideKick's main menu or the Macintosh's desk accessories. Alternatively, you can run compiled applications by a DOS command like DO MYPROG <parameters>, which can be put into an AUTOEXEC batch file to create a turnkey system.

The advantages of compiling to DO files are that they occupy less memory than LEARN does and that the user can't mess with them. LEARN is a large program, occupying some 81K bytes in addition to any buffers for the source code. On a computer with lots of other resident software loaded, memory can get tight. I had to reduce my SideKick notepad size to fit it into my 512K-byte IBM PC and leave room for applications, and there was not enough memory left to run my communications program from inside PC-Write. On the other hand, TDOSYS, the run-time package used by DO, occupies 40K bytes, and typical compiled programs are around 1K to 4K bytes.

Teaching Automator

The interactive resident part of Automator, LEARN, pops up a small square window that's a map of the computer's numeric keypad; you perform all LEARN operations by using the nine numeric keys. To avoid conflict with other programs, LEARN permits you to alter the hot key used to pop it up at any time. By default, it is the 5 key on the numeric keypad. You pop the window down again by hitting the space bar. The nine basic functions displayed in the window are shown in figure 1.

To start a simple Automator application, you pop up the window and probably choose Teach Keys. This offers a facility similar to that in most keyboard enhancers, or to the learn mode in Lotus's Symphony, in which the exact sequence of keys you press will be recorded and can be played back later. The keys are recorded as a series of statements in ACL. The process of learning keystrokes continues until you hit Teach Keys again to turn it off, though you can pop up the LEARN menu at any time and use the editor to see what has been learned so far.

Automator has two levels of keystroke trapping and generation called HIT and TYPE. When you switch on Teach Keys, you choose which mode you want. In

continued

7 Wait	8 Whenever	9 Teach Keys OFF
4 Capture	5 Help	6 Design Window or Menu
1 Edit	2 Files & Options	3 Run

Figure 1: *LEARN's pop-up window displays these nine basic functions.*

WAIT for ...

7 Window 1	8 Window 2	9 Window 3
4 Window 4	5 Help	6 Window 5
1 Time seconds	2 Time hrs:mins	3 Keyboard HIT

Figure 2: *The* Wait *option instructs Automator to wait for a time, a key to be hit on the keyboard, or a certain screen event.*

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TYPE mode, Automator traps and generates keystrokes as ASCII codes (i.e., key sequences that are meaningful to DOS). Thus, you can use TYPE for A or Ctrl-C but not Ctrl-Alt-Shift, because the latter does not have an ASCII code. The HIT mode works below BIOS level and traps the key scan codes before the keyboard processor has translated them into ASCII codes.

With HIT you can trap or generate any key on the keyboard that produces a code; combinations like Rshift-Ctrl-Lshift are possible since HIT can distinguish the left and right Shift keys. HIT can, for instance, invoke SideKick by generating Ctrl-Alt. Why not use HIT all the time? Because HIT sometimes picks up too much detail; it distinguishes between pressing and releasing a key, for example, which makes things more verbose than necessary. It's best to use TYPE for ordinary stuff and HIT for tricky stuff.

None of this is strictly relevant when you use Teach Keys because all you need do is press the actual keys. It matters only when you want to inspect the source code produced or to write programs directly.

After you've taught Automator a few keystrokes, you may well reach a point where you want to leave the application program for a while, say, if you're logging on to BIX. In this case, the Automator program must wait until you successfully log on. Pressing key 7 (Wait) brings up the new keypad menu shown in figure 2.

What Automator offers in this menu is the option to use one of its three "senses" to decide how long to wait. You could choose key 1 and specify an absolute wait in seconds or use key 3 to wait for a certain key to be HIT on the keyboard (you can also set this option to TYPE). The most interesting options, though, are the windows. By choosing one of these, you can say to Automator, "Wait until you see this text in this screen window."

The windows are defined in a completely interactive way. Pressing, say, 7 for Window 1 puts an empty window onto the screen. You can drag the window around the screen and alter its shape and size with the cursor keys until it covers the area where you expect a screen event to happen. The window is "transparent"; you can see the existing screen contents through it, so you can define the window on a screen that actually contains the phenomenon you're interested in, perhaps the words "BIX login (enter "bix")."

What if you can't guarantee that the target display will always be in the same place, as is often the case with scrolling teletype-like applications? No matter. Just define a window of the right width and the whole depth of the screen, and Automator can detect the target text anywhere in that window. It's also possible to use the editor to enter target text into the window, rather than using text that already exists. When you invoke the editor, the window ceases to be transparent, and you can type whatever you want to wait for into it.

This whole process is much, much easier to do than to describe. The implementation is slick, and defining a window feels rather like lassoing a picture in MacPaint.

The Whenever option of Automator's main menu works just like Wait, except that instead of waiting for a time, a key to be hit on the keyboard, or a screen event, Automator will do something every time a certain event happens—a sort of interrupt service routine. Whenever uses exactly the same method as Wait to define windows. You can use Whenever Keyboard HIT to provide an ordinary keyboard macro facility, for instance, "Whenever Alt-A is hit, type 'Automator'."

Key 4, the Capture option, again uses the windowing technique, but this time to capture the data in a defined screen window into a variable for further processing by your program. For example, when you have logged on to BIX and entered the Mail subsystem, you could capture the number from the phrase "You have 9 messages in your In-Basket" and use it to control a loop for downloading the mail.

Key 6, Design Window or Menu, lets you design a window for displaying messages from your program, and such windows can also be turned into menus. This whole process is performed interactively. You create a window, choose its border style and colors from a pop-up color palette using the cursor, and enter the names of its menu options. Then by moving a block cursor from one option to the next, you define the actions to be taken when that option is selected, using all the normal Automator facilities.

By using Design Window in conjunction with Teach Keys and Whenever, you can completely alter the user interface of any program to a custom menu-driven system of your choice. You can also provide pop-up windows of context-sensitive help or error-correction routines that take over control from a novice user at sensitive times, perform error recovery, and then return control (with a window explaining what just happened, of course).

Using ACL

The results of all your LEARN activity get written into the editor as source code in ACL. The full-screen editor uses WordStar commands; it's like the SideKick notepad, but more powerful, since it allows column moves using a selection

continued

Listing 1: *Written in the Automator Control Language, this program downloads BIX mail automatically.*

```
whenever _time = 0000                       ; EVERY MIDNIGHT
  _savattr = 0                              ; capture text only,
                                              not attributes
  logfile$ = _day$+_day+_month$+".log" ; create unique
                                              dated filename
  window 1 24 8 0 0
  window 2 0 2 3 16
  type "{Alt C}{Alt D}"                     ; dial a number
                                              from ProComm
  wait until window 2 contains "==>"
  type "1{Enter}"
  wait until window 1 contains "ADD?"       ; ProComm will
                                              handle retries
  type "A9310600157878{Enter}"
  wait until window 1 contains "BIX login"
  type "bix{Enter}"
  wait until window 1 contains "Name?"
  type "dickp{Enter}"
  wait until window 1 contains "Password:"
  type "I'm not dumb enough to publish my real
    password{Enter}"
  window 1 0 7 0 21
  wait until window 1 contains "You have"
  startlog
  window 1 0 1 9 21                         ; location of mail
                                              number on screen
  m$ = window 1                             ; get it
  messages = m$                             ; coerce it to a
                                              number
  if messages = 0
    write logfile$ "NO MAIL TODAY"
  else
    getmail
  endif
  signoff
endwhen                                     ; END MAIN PROGRAM

proc startlog                               ; begin logging
                                              data...
  type "{Alt F1}"
  window 2 0 7 33 12
  wait until window 2 contains "default:"
  type logfile$ "{Enter}"                   ; ...in logfile$
  wait 2 secs
endproc
proc getmail                                ; download mail
  type "mail{enter}"
  window 1 0 7 0 23
  wait until window 1 contains "Mail:"
  repeat
    type "{Enter}"
    whenever window 1 contains ".More.."  type "{Enter}"
    whenever window 1 contains " No" exit
    wait until window 1 contains "read/act"
    type "de{Enter}"                        ; delete after read
    messages - 1                            ; shorthand for
                                              messages=messages-1
    until messages = 0
endproc

proc signoff
  type "{Alt F1}"                           ; quit logging data
  wait 1 sec
  type "bye{enter}"                         ; log out, drop line
  window 1 24 8 0 0
  wait until window 1 contains "CLR PAD"
  type "{Alt H}"
endproc
```

ACL is well designed, with too many clever features to list here.

box. You can pop up the color palette in the editor at any time and change the colors of any quoted string without having to think about attribute values. Once you've learned ACL, which is no more difficult than BASIC, you can write programs directly without using LEARN. I found it was sometimes effective to combine both methods, capturing things with LEARN that I was not sure how to program.

ACL is a high-level, structured language that has a few unfamiliar constructs like wait and whenever, as well as conventional loops, conditionals, variables, arrays, strings, and arithmetic operators. The most important structures are wait and whenever since most programs are enclosed in a large outer whenever that defines their hot key. Listing 1 shows a typical ACL program written in the most verbose syntax (C programmers and other typographically disadvantaged persons may abbreviate heavily, for example, we for whenever and leave out contains altogether).

Timer and screen waits or whenevers are implemented by interrupt-driven multitasking time slicing on the timer interrupt, and they normally use so little microprocessor time that the main application program runs with no noticeable speed degradation. Keyboard waits and whenevers are triggered by the keyboard interrupt. However, too many simultaneous screen whenevers that examine very large windows will slow the application down. You can turn the whenevers on and off using the CANCEL command and a label.

ACL is well designed, with too many clever features to list here. For example, although it distinguishes between string and numeric variables (using the $ suffix as in BASIC), it provides automatic string-to-number conversion for numerals, which is just what you want since data captured from the screen is always of string type (see the twenty-second line of listing 1). A powerful feature is the ability to assign the contents of a screen window directly to a string variable; think about how much code that would take in BASIC or C.

I wrote two serious applications in ACL. One was the program shown in

continued

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Inquiry 69

I had no trouble using Automator with any of my resident programs, including SideKick.

listing 1 to download all my BIX mail automatically. The command language in my communications program would almost do it, but unfortunately it can't count. The other was a DOS shell, much simpler than QDOS or Xtree, that lets me move a block cursor (by arrow keys or mouse) through an ordinary DOS directory listing and select by hitting Return. What happens then depends upon the type of file selected. If it's a directory, select it and display its contents; if it's .EXE, .COM, or .BAT, execute it; if it's anything else, edit it with PC-Write. The program was trivially simple to write, with most of the work done by these lines:

```
; set capture window to next cursor
window 1 0 11 x y
file$ = window 1
```

ACL provides access to memory through PEEK and POKE, to machine ports through IN and OUT, to DOS interrupts (and hence external code) through INT, and to Turbo Pascal–style machine-level programming through a set of predefined register variables (_AX, _BX, _CX, etc.). ACL programs can be chained together using the DO command, which can pass parameters in addition to COMMON variables. It also has full DOS file I/O, even providing indexed files. It's difficult to imagine anything you can't do in it one way or another.

The Price You Pay

I had no trouble using Automator with any of my resident programs, including SideKick. It is well behaved and can usually be loaded last. If trouble does occur, after trying different loading orders, you can run the VC.EXE utility to inspect which interrupt vectors are free and set up Automator to use a different group by the SET MIVEC = xx command. Direct Technology tells me that the only programs it knows Automator will not fully work with are certain multitasking shells like DESQview.

At first, my Microsoft mouse wouldn't work inside the Automator editor. I was later told of an undocumented feature, Alt-+, that toggles between the Automator and DOS keyboard drivers, and this fixed the problem (incidentally, the manual is otherwise excellent). Automator did not like my Key Tronic KB 5151 keyboard at all when the separate cursor keypad was switched on; the program behaved perfectly well with the keypad off, though. Automator will work with applications running on extended memory cards, though it cannot be loaded into extended memory.

I must admit that I was thrilled by Automator mi. It provides the sort of total control over a computer that DOS should have given us in the first place. At present, though, it's too expensive to be considered a personal productivity tool like SideKick. Direct Technology designed the product mainly for large corporations, and it's priced accordingly. The Development System costs £1195 ($1995), and a single run-time license is £120 ($200), with site licensing available for corporations.

Automator mi is a development tool in just the same way as a professional C compiler, program editor, and debugger. You could probably make a good living with it by automating applications for other people, and this too is reflected in the pricing policy. I can't help wondering, though, how many copies the company would sell if it were priced at $99. ■

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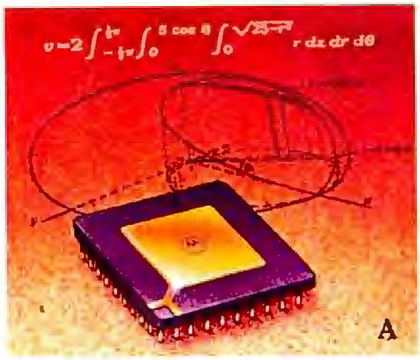
Motorola M68000



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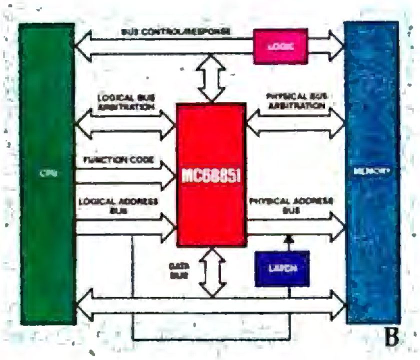

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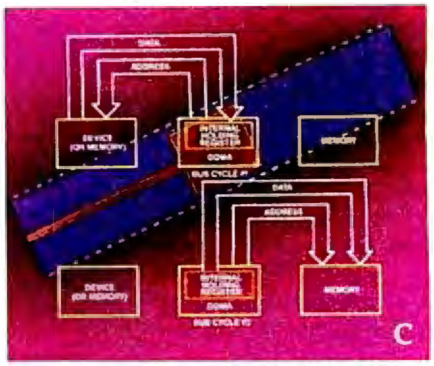

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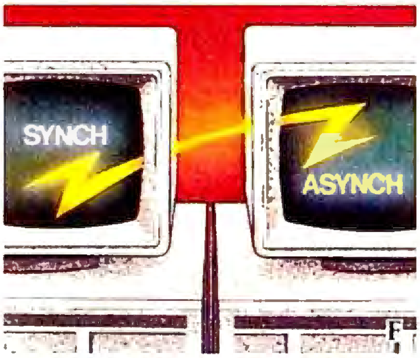

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Something Special

Ezra Shapiro

An early look at Microsoft's handsome Word 3.0 for the Macintosh

Microsoft is hoping that **Word 3.0** for the Macintosh ($395) will be received as the very best word processor ever developed—for any microcomputer. Having had only a few days to experiment with a beta release of the software, I hesitate to go quite that far. It's still too early to tell if Word will have the same impact on word processing that Microsoft's Excel has had on spreadsheets, but it is certainly an important product.

So important, in fact, that I'm devoting an entire column to it—something I've never done before. Even with that much space, I feel hard-pressed to just catalog all the product's features, let alone react to them. Word 3.0 is something pretty special.

The program cemented my decision to purchase a Macintosh Plus. I've been working with loaner machines from Apple ever since the original Lisa, but the almost total lack of quality text-handling software left me reluctant to commit my own money. Even if Word does not turn out to be the final word (and what program has *ever* turned out to be the ultimate in its category?), it does signal that the Macintosh can now be a legitimate environment for writing and editing. The new Mac—miserable thunky, echoing keyboard and all—is sitting on my kitchen table (with a sticker of Sylvester the cat pasted over the Apple logo), waiting for the official release of Word. Getting me to buy new hardware is not easy; it is probably the highest compliment I can offer to a piece of software.

The basic engine for this new version of Word is the familiar Macintosh text interface: pull-down menus, flexible font styling, and on-screen "what you see is what you get" formatting. Unlike Apple's MacWrite and the previous incarnations of Word, which were designed to operate in the limited memory of the 128K-byte Mac, Word 3.0 will run only on machines with at least 512K bytes of RAM. A few of the most obvious enhancements are directly related to this change; for example, Word 3.0 allows 16 windows to be open at one time and includes built-in spelling checking with an 80,000-word dictionary. What will be most surprising to Macintosh purists, however, is that this new version of Word owes a lot to interface techniques developed for MS-DOS programs.

Before I get into the new stuff, though, don't forget that Word retains some powerful features from earlier editions. You've got a solid mail merge with conditional branching; custom glossaries for storing boilerplate chunks and recalling them with abbreviations; and diverse formatting controls for characters, paragraphs, and sectional divisions.

For Starters

When you first load Word, the screen that greets you looks much like MacWrite. Don't be fooled: You're looking at Word's short menu mode, designed for first-time users. Complex commands and sophisticated formatting options are not visible on the primary menus, though you can still get to many of them through secondary menus or keyboard shortcuts. As soon as you're comfortable with this subset, you can move to full menus with one mouse click (thus setting a configuration toggle that won't have to be changed at the start of every session). I don't know why this strategy hasn't been used more frequently by software firms; it's a direct training path that neither cheats novices out of power nor forces them to switch software as they learn.

Once you're using Word's full menus, you'll discover another nice touch. You can add items to, or delete items from, the Font and Format menus. Let's say you rarely use Helvetica, or you frequently adjust your paragraph style; just change the menus. Another example: Word provides a number of new text attributes: word underline, double underscore, dotted underscore, strikeout, all caps, caps with small caps, and hidden (for nonprinting comments or inserting PostScript commands for a laser printer). For me, all these attributes are far more useful than the hollow outline and drop-shadow options on the standard menu. I can get rid of the old stuff and plug in the new.

You can also set up a new primary menu, called Work, where you can install documents, style sheets, and glossaries. If you know you're going to need to look at (or modify) a "things to do" list, regularly use a specialized format, or if you've created a customized glossary, the Work menu will prove to be a handy way to personalize Word. It will hold as many as 18 entries.

Different Views

Outlining is an impressive addition to Word 3.0. Functionally, it's simply a view of a document; one command toggles between your outline and full text. In outline view, paragraphs beneath headings are "body text"—you see only the first line and a continuation symbol.

When you switch into the outline mode, a bar of small icons appears below the main menu bar (and a ruler line if you're displaying one). Clicking little left or right arrows promotes or demotes items in the hierarchy; up and down arrows move items without changing their rank. On the Macintosh Plus, you can use the cursor keys for these operations; cursor movement is controlled by the numeric keypad or the mouse. Other icons are used for expanding or collapsing sections, converting headlines to body text, and assigning

continued

Ezra Shapiro is a consulting editor for BYTE. Contact him at P.O. Box 170040, San Francisco, CA 94117-0040.

levels to selected items. Each of these functions has a keyboard equivalent.

If you'd like to see your outline and full text on screen at the same time, you have two choices. You can open a second window into your document (in whichever view you want), or you can split a single window into two parts. If you use a split-window arrangement showing the outline in one half and the expanded text in the other, the views are linked and scrolling is synchronized between the two.

I won't go into the ramifications of outlining as a tool for viewing and reorganizing long documents; it has been dealt with extensively elsewhere. However, outlines in Word 3.0 take on added significance because you can assign styles to each level. Microsoft gives you predefined formats for nine levels' worth of outline. You can change them to suit your preferences or leave them as is. By installing an outline (even one that's essentially empty) as one of the entries in the Work menu, you can cut and paste styles from the outline into other documents with a few quick commands.

Fancy Formatting and Graphics

Layout possibilities are almost on par with many of the page-makeup programs on the market. Text can be printed in as many as six columns per page. MacPaint graphics can be inserted into documents, and they will be displayed as they are, not as the gray blocks used by earlier programs. Paragraph-formatting options include borders and boxes. PostScript commands can be entered as text, and PostScript code will be sent to the laser printer. For those people without laser printers (or without any desire to learn the PostScript language), Word 3.0 has a small macro language (much like traditional escape codes) that allows for the creation of rudimentary graphics and mathematical symbols, which can be displayed on-screen, unlike the PostScript stuff (see the screen shot in figure 1).

My favorite design tool is the new Page Preview feature (see figure 2). The original Macintosh "show page" command, used by many programs, merely presented a static view of what a printed page would look like. Word's Page Preview displays two pages side by side (so you can see a title page with an interior page, for example), and you can actually *do things*. Dotted lines indicate margins around the text. You can use the mouse to drag the margins on one of the pages, and the entire document will be reformatted to match the new settings. If you don't like a page break, Page Preview will let you modify a single page. You can reposition headers, footers, and page

continued

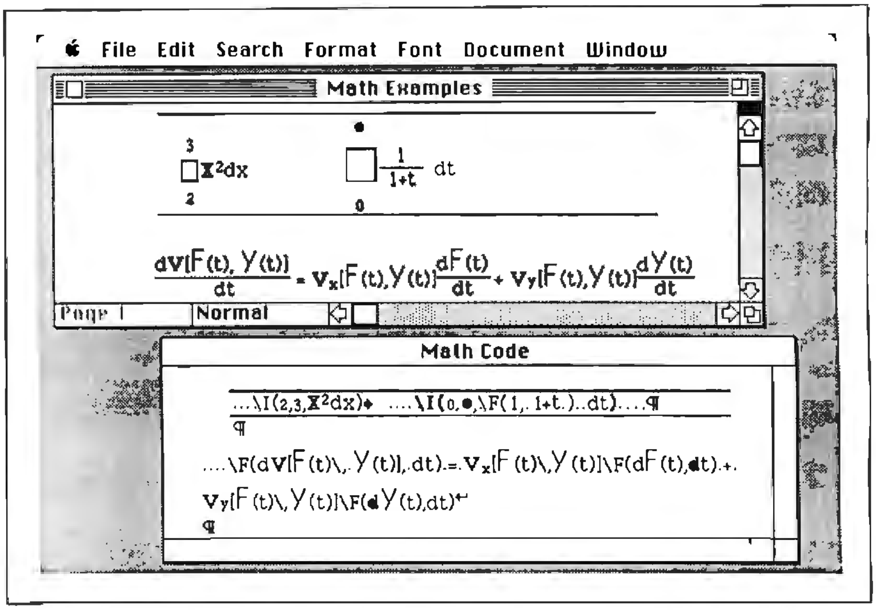

Figure 1: *Word 3.0 uses embedded formatting commands to let you enter complex formulas. The sequence in the code window produces the sequence in the top window. Because Word does not allow both versions to be shown simultaneously, the code window was created by capturing it as a MacPaint document (using a desk accessory) and pasting it into the window as a graphic.*

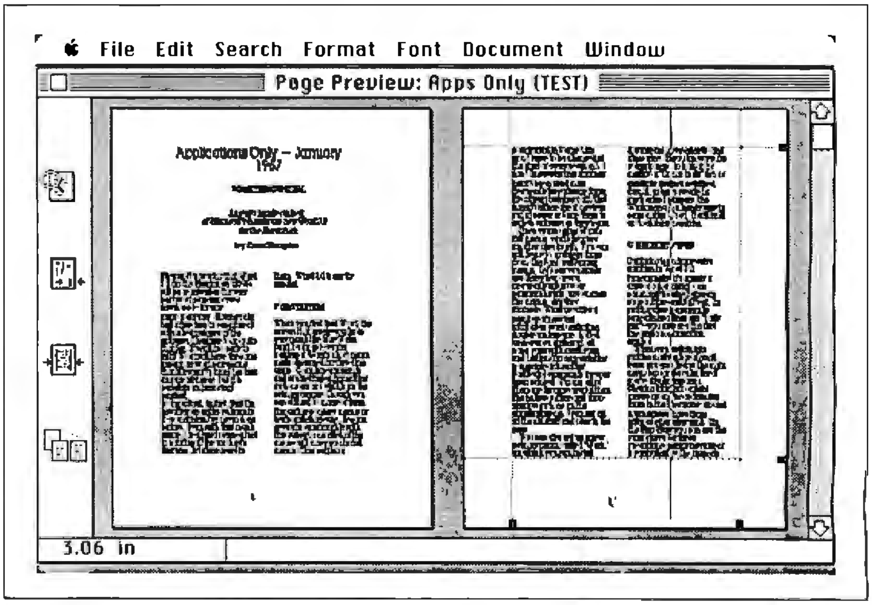

Figure 2: *Word 3.0's Page Preview feature displays two pages side by side. Dotted lines indicate margin settings; the solid line, a new right margin. Word will reformat the entire document.*

numbers. An icon of a magnifying glass lets you display any area on the page as it will be printed. For accurate control of these reduced images, a status line displays cursor coordinates in your choice of measurements.

And Furthermore

Word 1.05 took some steps toward getting away from absolute dependence on the Macintosh mouse. Keyboard shortcuts (characters prefaced with the Mac's Option and Command keys) allowed direct access to most commands for formatting, cutting and pasting, and getting to secondary menus, but the mouse was required for text manipulations and responding to dialog boxes.

All that has changed; you can now

continued

the computer chronicles

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On the Mac Plus, with its additional keys, the numeric keypad behaves much like the one on the IBM PC.

neglect the mouse entirely. The old shortcuts still work, and Microsoft has implemented a new series of combinations for cursor movement, scrolling, selecting text, window control, and moving around in menus. You can even use the keyboard to pull menus down from the menu bar; and by so doing, you'll no longer have to hold down the mouse button to keep a menu on the screen—it stays there until you make your selection. On standard and enhanced Macs, the keystroke sequences get rather obscure, but on the Mac Plus, with its additional keys, the numeric keypad is configured to behave much like the one on the IBM PC.

Have I mentioned automatic line numbering in the margins at your choice of intervals, so you can write either a BASIC program or a legal contract with every fifth line numbered? Or Quick Switch, an option that lets you zip out to another program (MacPaint, MacDraw, Excel, maybe others), modify the data, and return to Word and see the changes in place? Or math calculations on groups of numbers? Or tables with horizontal and vertical rules? Or footnotes, end notes, indexes, and tables of contents? Or exporting files to the MS-DOS version of Word? Or ... You get the idea.

Wish List

One of the amusements of trying out a prerelease version of a program is making suggestions. I had several for Word 3.0: a "resume environment" command that would let you save a complex arrangement of windows from one session to the next; a "learn" mode that would record keystrokes (both text characters and commands); simple drawing (like that in Microsoft's Works) for creating lines, boxes, circles, and ellipses; and a "count" command that would give both word and character counts for a selected area of text (the word count is important for writers, the character count for anyone exporting to a page-makeup or telecommunications program).

I have no idea if any of these will show up in the final release. If they do, give me and the other beta testers some credit. If they don't, well, I guess I'd have to say

continued

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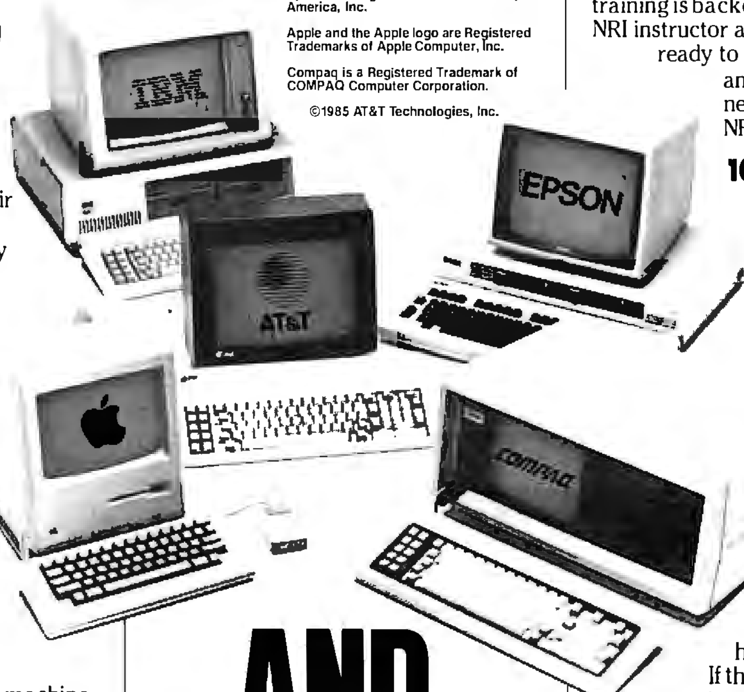

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A number of Word's features were definitely flashy, such as the neat Page Preview and the new text attributes.

at that point that Word 3.0 lacks a couple of useful features, but they're conveniences, not essentials.

Personal Reactions

The copy I played with was definitely beta software, complete with debugging tools and cryptic resource files that will be long gone by the time the product hits the market. Word 3.0 had not yet been "optimized for speed" in Microsoft's words, and many operations were slow or choppy, though the bulk of the program was functional and, in many cases, as quick as some finished products I've seen. Sections of the documentation were crossed out, pending changes in the software. So I recommend that you get a full demonstration of the product and read some formal reviews of it before you rush out to plunk down your cash.

However, what I saw was enough to leave me with my mouth hanging open. A number of Word's features were definitely flashy, such as the neat Page Preview, the new text attributes, and the outlining capability. If those sorts of things grab your eye, so be it. Sexy features are nice, but I myself am more concerned with the serious business of cranking out prose.

I was much more impressed with how easy Word makes it to get on with work. The new command strategies (which seem to take the best parts of WordStar and Framework, my two favorite text tools in the MS-DOS world) let me do what I have to do without feeling trapped by the Macintosh religion. Lots of choices, and no straitjacket—I can use the mouse, or keyboard shortcuts, or the Plus keypad as the situation dictates. High-power commands are there when I need them, so there's a feeling of safety and flexibility, but I don't feel pressed to customize the program in order to make it functional. I'm sure that as I work with it I'll institute my own menus and formats, but for now I'm quite comfortable.

If the final release lives up to the promise of the beta, Word 3.0 will be a big winner. And yes, the best word processor to date. ■

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Conducted by Jerry Pournelle

Visionary Device

Dear Jerry,

You have mentioned, in at least three columns during the eight years I have been reading them, that you have a vision problem. So do I. I want to tell you about a device that you and many readers, even those with near-normal vision, may come to find indispensable; for many it will be a godsend.

The device is a miniature variable-focus telescope mounted in ordinary eyeglasses manufactured by Walters, a Japanese company. The telescope provides a surprisingly wide and bright visual field. It is less than 1½ inches long and ¾ of an inch in diameter. It is lightweight, focuses quickly, and mine cost $107 for frame, telescope, and professional fitting.

This gizmo lets me lean back in a high-back chair, keyboard in lap, with legs, arms, and neck comfortably extended while I use my computers for 6 to 12 or more hours at a time. I can snoop about in the bowels of my computers, easily read the writing on the motherboard, DIP switches, etc., and easily insert boards, attach cables, change DIP switch settings, etc. I can also read small print laying beside a computer and work the computer at the same time; and lay a book in my lap and read it, avoiding the muscular cramps resulting from having to hold it in the air two feet away from my face. The scope also lets me work with one computer while monitoring the progress of things going on in another computer across the room.

The address and telephone number of Walters's domestic subsidiary are

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Another brief matter. Our experience is probably typical of many software companies. My company experienced a 15 percent underlying return on a mailing to all known purchasers of our Statistician's MACE program which we have been selling for only three years. What attrition! *Aftermarket* business is very important to a small company such as ours. The aftermarket encourages us to update our program, and it allows our users, whom we do indeed value, to upgrade at a very low price (typically $15). Please encourage your readers to notify companies whose software they have purchased when there is a change of address.

Carl F. Voelz
President, MACE Inc.
Madison, WI

Gosh, my eyes aren't quite that *bad. However, I know people who ought to learn about this gadget; it sounds great.*

And indeed, everyone ought to notify publishers of changes of address, but I doubt they'll remember to do it.—Jerry

MCI Mail

Dear Jerry,

You shouldn't be struggling with MCI Mail menus (July 1986, page 338). If you call MCI and sign up for advanced service (very reasonable price) you work with simple commands. These commands, like CREATE, PRINT, SCAN INBOX, SCAN OUTBOX, etc., can be shortened to the two-letter abbreviations CR, PR, SC IN, SC OU, etc. The MCI Mail promos are a bit annoying but at 1200 bits per second they go by pretty quickly. Your MCI Mail benefactor should kick you up to advanced service.

MCI Mail has dramatically improved my productivity through improved communications with my clients. I handle a lot of work in the U.K. through MCI Mail.

I. Switzer
No address given

I resent MCI's asking me to guarantee them a minimum monthly fee in order to have decent software. I feel as if I am be-

continued

ing blackmailed, and I don't much like it.—Jerry

Mouse Space

Dear Jerry,

I noticed both you and Ezra Shapiro complaining about lack of desk space to fit in a mouse for your Macintosh. Speaking as the holder of the world record for cluttered offices, and a Mac user whose three IBM PC clones seem to be getting little use these days, I feel I am in a unique position to advise you both. All you have to do to generate mouse space is to remove the material occupying an 8-inch by 8-inch space next to your keyboard and put it *on top of something else.* It really doesn't matter what else. If that's where you kept your most important things, this is a positive advantage, because you can put them on top of six other piles, thereby getting them nearer to the top of a pile than most of them were already.

I am currently exploring the use of an infrared mouse suspended around my neck and rolling on my shirt front. Less original talents often find that after 40 hours with the best of the trackballs they prefer it to any alternative.

Michael Scriven
Nedlands, Western Australia

Well, that's one solution.

I think there ought to be a standard error message: INSUFFICIENT MOUSE SPACE.

Thanks.—Jerry

Learning Dvorak

Dear Jerry

I am an Apple II+ user, soon to upgrade to an Apple IIe, and I have already bought a Video Technology Laser 128. I find the 128 to be a very good computer, easily on a par with the IIc, not to mention its price. One of the attractive features is the option to choose between the standard QWERTY keyboard layout or the Dvorak layout. I learned to type years ago on the QWERTY keyboard, yet even when I was experimenting with the Dvorak layout, my hands felt less fatigued. From what I've read in recent articles, this is precisely the advantage of the Dvorak layout: less fatigue and therefore longer periods of typing with fewer errors.

Not only would I like to learn the Dvorak layout, I would like my teenage children to learn to type (on whatever keyboard). Alas, I don't have the time to teach myself nor do they have the motivation, so I've been looking for a typing tutor program that teaches both keyboard layouts. All the programs I've seen use methods that depend upon the physical arrangement of the keys; they all assume the QWERTY layout. Can you suggest any source that might provide a program that would allow the Dvorak keyboard?

Robert A. Goff
Gansevoort, NY

Many years ago I worked for Professor August Dvorak, the inventor of the Dvorak keyboard. He was quite proud of it and had extensive test results showing its superiority. It never caught on, though, largely because, while learning the keyboard isn't so hard, if you then have to use a QWERTY some of the time, you'll go nuts.

Alas, I don't do much with the Apple II, although Mrs. Pournelle has two of them. In looking about Chaos Manor, I see no Apple II Dvorak programs; perhaps a reader can help.—Jerry

Expansion Chassis Worries

Dear Jerry,

I am writing to you for advice before I jump in and buy my first home computer. What I have in mind is an IBM PC, Orchid Technology's PCturbo 286e or PCturbo 186 board, and a PC expansion chassis from Fortron Corporation. My apprehension is mainly about the expansion chassis. I don't know anybody who has gone this route so I am worried about construction quality and compatibility problems that the interface card may present. If you, your staff, or any of your contacts knows anything about these expansion chassis, I would very much like to hear from them.

John F. Weller
Milford, OH

Well, I can recommend Orchid boards. I have never had an expansion chassis; every time I think of getting one I am dismayed by the price. I can get a new motherboard and new case for less! —Jerry

Advice for a Writer

Dear Jerry,

I write. I plan to do more. Forgetting all the marvelous things a computer can accomplish, what's the best basic machine for a writer? I promise that I won't try to balance my bank account, keep my calendar, try to produce graphics, or work on spreadsheets.

Simply, I want a machine that will allow me to type in sentences, edit them, store them, and print them out when I need them. I should be able to store a good-size book (say, 150,000 words) or two.

Aside from those basic functions, I might appreciate a good on-line dictionary, thesaurus, and spelling checker. However, they are not vital.

Bob Feeney
Littleton, CO

Best basic machine for a writer. Good question. My wife is very happy with her Ampro Littleboard Z80 machine with Ampex terminal; she got it from Disks Plus in Chicago. It does all the things you say you want and does them fast, proving that CP/M is not dead. It didn't cost much, either.

On the other hand, there's getting to be a lot of nifty software for writers that runs on IBM PCompatibles. Indexing programs, file comparison programs, programs that check to see if you doubled words, and others to see if you use some words too often.

I'm still writing on an ancient Z80 CP/M machine with memory-mapped video, but I have other machines to do the rest of the work.

The main thing is to get a machine with a keyboard and screen you're comfortable with. That's more important than what kind of computer. Incidentally, I went through all this in my Adventures in Microland *(Baen Books, 1985).*—Jerry

Matrix Benchmark

Dear Jerry,

You published the Matrix20 benchmark in the October 1982 issue of BYTE. I ran the test 14 times, with different computers, operating systems, and languages, and got one anomaly—the result. What is the correct result, 342,540 or 465,880, and why the same two results from different languages? Maybe you could publish the answer in the form of a military cryptogram in the upcoming volume of *Janissaries*, which I assume will be out Real Soon Now.

Tom Cage
Titusville, FL

Gee—that was a LONG time ago. My "benchmark of sorts" was intended to test something other than loops and suchlike; it seemed to me that doing matrix operations was a lot closer than sieves to what computers really do. I was also going to devise an I/O benchmark, but I never did.

I'd guess the different answers come

continued

from rounding errors; although all the numbers in my benchmark are eventually converted to integers, they live as floating-point numbers for a while. The real answer is 465,880.

Janissaries III—Storms of Victory *is in first draft and ought to be turned in to the publisher soon.*—Jerry

Nasty Chip

Dear Jerry,

I think that you will find my experience with a form of copy protection most interesting. I recently purchased a speed-up BIOS chip for PC compatibles made by Softpatch Inc. I discovered that this chip has a worm in it that engages if any change is made to the manufacturer's *logo.* This worm does not immediately take effect but is included in the BIOS's clock-tick interrupt routine, along with a time delay of several hours. When the time delay runs out, a message appears on the screen: PLEASE POWER OFF OR YOUR DISK WILL BE TRASHED! If any key is pressed, or was previously pressed, your hard disk is totally wiped out.

The distributor, Microware Exceltek, did not include any documentation warning that this chip contained such a destructive protection scheme!

The worm activated on my chip because I wanted to use it on a TeleVideo 1603 computer that I had converted to a PC compatible by the addition of a "clone" motherboard. In order to use the excellent 14-inch monochrome monitor that was on the 1603, I needed to change two bytes in the video parameters and one other byte to make the BIOS checksum come out to zero. I innocently decided that the best byte to change would be in the manufacturer's logo, since it would probably not be used by any part of the BIOS program as a constant. The person who wrote this BIOS program told me that this was an "unfortunate" choice, as this activated the worm. Fortunately, I was testing the new BIOS by copying data between two RAM disks overnight and had all my hard disks powered off. The creator of the BIOS even told me that he had wiped out his own hard disk twice while testing it. Serves him right!

There has to be a better way of copy protection than to trash a person's hard disk without warning, especially someone who is just trying to improve the performance of his converted machine. I was not amused. What would happen to a program developer who always runs the risk of his program testing branching to the location of a hidden worm, even if he hadn't pirated the chip?

Robert G. Curry
Tucson, AZ

continued

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I see from your enclosures that Softpatch's program will indeed destroy your fixed disk if the worm is activated. If that happened to me I'd hire the best lawyers in town and do my best to destroy that company. I will certainly never put any Softpatch product in any computer under my control, and I advise my readers to deal with this outfit in an appropriate way.

Ye gods.

Thanks for the warning.—Jerry

Bit or Baud?

Dear Jerry,

I was struck by your statement about the distinction (or lack thereof) between kilobaud and kilobits per second (June 1986, page 298). A baud is a unit of signaling speed and refers to the number of times the state or condition of a line changes per second. It is the reciprocal of the length (in seconds) of the shortest element in the signaling code. Historically, it is a contraction of the surname of the Frenchman J. M. E. Baudot, whose five-bit code was adopted by the French telegraph system in 1877. By contrast, a bit is the smallest unit of information in the binary system. The baud rate is therefore equal to the bit rate only if each signal element represents one bit of information.

Where amplitude is used as a coding method, let us take the example that has four line conditions, one for each of four combinations of two bits. Each line-change signal element is therefore represented by two bits and if we can have one line change in one millisecond, the baud rate is 1000, whereas the bit rate is actually 2000 bits per second. Similarly, if the signals are coded into eight possible states, one line condition could represent three bits, and one baud would then equal three bits per second, and so on.

Unfortunately, in much of today's literature the terms baud and bits per second are used synonymously and this is what I object to in your article. This would be true in the case where pure two-state signaling is used but in general this is incorrect. This is why the term baud is being replaced by bits per second, since the latter is independent of the coding method and truly represents the information rate.

As a service to readers, you really should publish a clarification in your next column.

Dennis L. Venerus
Scarborough, Ontario, Canada

Well, if I'd known anyone felt that *strongly about it...*

I still think, though, that we need a decent term, and "baud" is a good one; why not redefine it? It won't likely be needed in the old sense.—Jerry ■

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The Best of BIX is a brief look at a few of the messages posted each month on the BYTE Information Exchange. This month, messages are presented from the Amiga, Atari ST, IBM PC, Macintosh, Apple, and FORTH conferences. The format of the messages changes slightly, with the addition of the date on which the message was originally posted. In a field that sees change as often as small computer systems, the date should help in understanding the context of the speaker. For information on joining BIX, please see the advertisement on page 409.

AMIGA

The Amiga section focuses on hardware problems this month. In the first thread, questions of hard-disk access times and the effects of partitioning are answered. The section closes with a discussion on the particulars of controlling the Amiga's serial port.

DISK ACCESS TIMES

[Message #393 continues a thread that was discussing the time required to load a picture file, MANDRIL, from various makes of hard disks.]

---

amiga/hardware #393, from althoff (Thomas Althoff), Wed Sep 10 09:56:33 1986. A comment to message 392.

I don't have a copy of MANDRIL. I used DOZER.HI, which is a 128K file. Time from the prompt "Showing IFF file click at top left", etc., on the MicroForge 20 Mb was 10.5 seconds. On the MAS20 it was 11.0 seconds. These are very rough times. How did you do the write to disk? Did you copy the picture to the RAM disk and then copy back? If so, I'll check that out also.

---

amiga/hardware #394, from lmarco (Lou Marco), Wed Sep 10 11:55:19 1986. A comment to message 393.

Gee, I thought everyone would have the Workbench demos with MANDRIL in the picture drawer. Still one of my favorites. I suspect that your times could be faster with effective use of the disk. The easiest way to do the test is to open up a RAM disk window and a hard disk window in Workbench, then move the icon back and forth.

This has a little overhead compared with the CLI copy command. For quickest speeds without formatting disk or other drastic measures, 1) copy COPY to RAM 2) copy DOZER to RAM 3) cd RAM 4) copy DOZER to hard disk. This will reduce the DOS overhead. For a read, follow the same pattern with copy command in current directory on the hard disk. This may all seem like cheating, but I am looking at max speed with as few variables as possible.

Tell me a little more about your setup and I may be able to make suggestions about getting better results. 1) What version of DOS, 1.1 or 1.2? 2) What software is supplied with the drive? Does it come formatted? What utilities are available with the drives or through other sources? 3) Is the disk partitioned? How much information is floating around about the mountlist and partitioning? By the way, I am a hardware type but I find partitioning to be extremely easy. Since I have been living in a vacuum lately, I have lost touch with what's known and not known. So, if there are questions on using hard disks or anything about expansions, memory, etc., let me know. I have some free time now.

---

amiga/hardware #395, from althoff, Wed Sep 10 12:11:47 1986. A comment to message 394.

My system here is running 1.2 beta 4. MicroForge supplied hard disk driver driving an expansion bus interface. MAS20 used custom parallel port driver. I think our time for disk to RAM and back to disk was about 30 secs. Divided by two gives guesstimate of 15 seconds. Redmond can correct me on those figures. Redmond, how do I interpret the values passed in the dhmount command? Can the MAS20 be partitioned? I don't think there is any way to do it with the MicroForge. I have not had the time to get much done here. Visitors from Virginia are here for the week. I'll try some timings this weekend.

---

amiga/hardware #396, from jdow (Joanne Dow), Wed Sep 10 12:38:36 1986. A comment to message 394.

Um, I'd play on my four-drive system, but the speeds are standard floppy speeds, which are well-known. And I cannot load MANDRIL with all four drives and interlaced mode. (In fact, I'm not sure I can load it in lo-res mode, either. Those furshlugginer buffers take a lot of memory. Wish we had a "dismount" command to accompany the "mount" command.) <^_^>

---

amiga/hardware #397, from lmarco, Wed Sep 10 13:00:20 1986. A comment to message 395.

It sounds to me like the MAS20 can be partitioned. Tonight when I have more time I will post something on how it might be done. I use one partition just to back up things that are important. Since each partition can be formatted independently, if you guru on a partition and get a read/write error, you can reformat that partition and replace stuff from the backup partition.

---

amiga/hardware #399, from jdow, Wed Sep 10 13:30:43 1986. A comment to message 397.

Hm, I gotta look at that mount command - is that what is used to make the partitions? <^_^>

---

amiga/hardware #400, from lmarco, Wed Sep 10 14:08:22 1986. A comment to message 399.

No. Mount command utilizes the mountlist, but editing the mountlist is easy when you know how. Some things are mounted automatically, like "ser: dh0: par:". Devices that aren't automatically mounted must appear in the devs directory file mountlist. This would include additional serial devices as well as hard drives and other peripherals. After booting, type "binddrivers" to get DOS to recognize any new drivers like the one supplied by the hard drive company. Then type "mount (device name)" and if things are set up your partition will be available. But before this can happen, the hard drive must be formatted one partition at a time. If you have a disk full of stuff now, you will have to back it up to reformat your drive for your partitions. Actually, it's not as bad as it sounds; some partitions can be changed without starting from scratch. But if you don't have any partitions, you need to format all of the disk. I will try to put something together off-line that is more coherent on how to actually do all the steps. Look for it tonight.

---

amiga/hardware #403, from jdow, Wed Sep 10 15:46:51 1986. A comment to message 400.

I know about the mountlist. It sounds like a clever way to reduce storage area yet give a bit more speed from the DF2: and DF3: I have. If I turn them off I have it set up (not properly, I know) so that there is no bus load. Hence ADOS doesn't find them. If I then issue a special mountlist command, I was suspicioning I might be able to do it with some partitions. What names do your HD partitions have in the "info" list? Are they a bunch of DHn:'s or something else? <^_^>

---

amiga/hardware #406, from rsimonsen (Redmond Simonsen), Wed Sep 10 20:29:10 1986. A comment to message 400.

It should be pointed out that partitioning is NOT a function of a particular maker's hard drive; it is a function of AmigaDOS commands. To suggest that a hard drive might *not* be partitionable under 1.2 is, of course, misleading and confusing.
--Redmond

continued

amiga/hardware #408, from lmarco, Thu Sep 11 01:40:43 1986. A comment to message 403.

The assign command will show the name given in the mountlist for each device. This will appear after binddrivers and by using the mount command. That is, mount DH3: T. If DH3: has been formatted, it is available (access DH3: once or do a cd DH3: to have icon visible on Workbench). The names in the mountlist can be anything, but I have never tried more than 3 symbols because the names would overlap in assign display (I would also avoid DH0: because the new kickstart does that automatically).

DRIVING THE SERIAL PORT

amiga/softw.devlpmt #2649, from skbower (Steven Bower), Fri Sep 12 20:48:20 1986.

Hello everybody! I have a rather specific question about manipulating the serial port. We have just installed a new voice/data network on campus and in order to start communicating with it, one must toggle the DTR signal on the RS-232C. StarTerm 3.0 doesn't do that, so I figured I'd write a little program to flick the DTR whenever you select some gadget. Problem: I can't find a way to do this! No info about it in the RKM, although DTR is mentioned once. Anybody have any ideas? It's getting awfully tiresome unplugging my serial cable and plugging it back in every time I need to do some communicating (which is a LOT!).
Thanks, Steve Bower, Lehigh University.

amiga/softw.devlpmt #2652, from jdow, Sat Sep 13 02:17:47 1986. A comment to message 2649.

I don't think you're gonna like this news one bit. StarTerm 3.0 works the DTR line correctly. I just checked with my other modem. You may have an Amiga with a weak RS-232C line driver chip. It may be weak as delivered from the factory or it may have been mangled in cabling. The other possibility is that the Amiga drives the + side of RS-232C at the ragged edge of the drive voltage spec. It is well above what the receiver is spec'ed to recognize; but, it is a couple hundred millivolts below the proper drive level. A way to help this requires an external +12 source, a diode, and a pullup resistor. This is a kludge, but it'll probably work for you. The other alternative is a small amplifier on the DTR line. <^_^>

amiga/softw.devlpmt #2653, from jimomura (Jim Omura), Sat Sep 13 10:38:59 1986. A comment to message 2649.

What do you mean by 'flick' it? Turn it 'on' or 'off'?

amiga/softw.devlpmt #2654, from skbower, Sat Sep 13 15:10:43 1986. A comment to message 2653.

I mean turn it off and then on again. At will, that is, not just when your input buffer fills up. Our network is awakened when your DTR signal goes from 0 to 1; if it's already at 1, you, of course, must make it go to 0 before you can make it go to 1 again. I think the levels of the signal itself are within the range allowed by the network interface; when I start up StarTerm, it raises the DTR so if I set my baud rate to 9600 really fast I can catch it before the network times out. All I really want to do is tell the serial device (or whatever) to: a) drop the DTR, b) wait a second or so, and c) raise the DTR again. I'm just afraid I'm gonna bend a pin or something from pulling my connector out and plugging it back in so much!

amiga/softw.devlpmt #2655, from jdow, Sat Sep 13 19:05:53 1986. A comment to message 2654.

What puts your network to sleep? DTR is always true when the serial port is open. Therefore, there is no real safe way to build a serial port flicker such as you want. You'd have to try direct hardware control and that is not at all easy if you want other things to keep running properly.

Could you describe how your network works just a little better? Perhaps a hardware device could make the flicker you want or perhaps better use of the serial port might do it. Anyway, once the port is open DTR is always asserted. It is the CTS line that indicates buffer full if you open the port in the 7-wire handshake mode. <^_^>

amiga/softw.devlpmt #2658, from skbower, Sat Sep 13 22:08:19 1986. A comment to message 2655.

The network goes to sleep when I drop the DTR; basically the DTR determines whether or not you can communicate with it. Raising the DTR causes the MKO (Machine Keyboard Originator, I think) to give you its prompt, and if you don't respond within a certain amount of time (5 seconds, +/-), you get a time-out message and you must play with the DTR to reawaken the sleeping beast. Now, if StarTerm were to drop the DTR when you exit it, that might make things easier, though having to unload and then load it in for consecutive/ different logins would be excessive. Although I don't think that's StarTerm's fault: does the system software drop the DTR when the serial device is closed (hint)? It seems like such a simple thing to do, too. I know that the Computing Center here is using a modified Kermit on the IBM that uses the hangup command to do just what I'm trying to do. Speaking of which, if I used this IBM Kermit on the SideCar, would it be able to toggle the DTR? Something interesting to look into, anyway; if the SideCar, routed through AmigaDOS (I think?), can do it, I should be able to, too, no?
Still open to any ideas! -Steve.

amiga/softw.devlpmt #2662, from jdow, Mon Sep 15 00:42:34 1986. A comment to message 2658.

Gee, doncha just LOVE systems that misuse RS-232C lines? DTR on any terminal I am familiar with simply means the terminal is on-line, turned on, and ready to be active. A network that drops you in spite of DTR active after any length of time is built wrong. This doesn't help you one bit. What you'll need to do is get one of the PD sources, probably that VT100am.1 and .2, and alter it to include a close/open on a menu selection. The only way to drop DTR is by closing the port. There is no way you can build a separate serial port fiddler program to multitask and do this. All open invocations of the serial port must be closed before DTR drops. If StarTerm doesn't drop DTR when you exit, there is something strange. Perhaps your preference is set to have a serial printer? I thought version 1.1 handled at least this much correctly. Lemme think back a bit.... Memory tells me that both Online! and MaxiComm made DTR drop correctly. In fact, we had quite a discussion some months ago wherein we discovered that the serial port driver chips can get blown. I seem to remember the failure mode left DTR off rather than on.

Another thing that comes to mind that you could patch into a program that you recompile is a little timer on the main program loop that sends a null character or something equally nondestructive if there's been no serial activity after some 4 seconds or so. Would that serve to keep things alive for you? (This sounds like a Big Blue Frame monster you're talking to. If so, see if there is a plug the fellows can pull to allow you indefinite inactivity.) <^_^>

amiga/softw.devlpmt #2665, from langeveld (Willem Langeveld), Mon Sep 15 03:50:49 1986. A comment to message 2662.

Actually, VT100 (from VT100am.1 and VT100am.2) also doesn't drop DTR on exit. I have been trying for days now to change that program to 7-E-1 without success. I have read the pertinent pages in the RKM several times. What am I doing wrong? As I understand it, all I need to do is OR the SerFlags with SERF_PARTY_ON and AND it with <not> SERF_PARTY_ODD, and set the ReadLength and WriteLength to 7. Then do DOIO with io_Command set SDCMD_SETPARAMS. Right? This is version 1.1.

Willy.

amiga/softw.devlpmt #2667, from jdow, Mon Sep 15 15:22:44 1986. A comment to message 2665.

That's right. Very easy to do. You only have to close the serial device and reopen it when you need to change from standord to 7-wire control. Not dropping DTR is odd. That is the same program as Aterm at its core. Some of the code can be vastly improved; but it does close things on the way out as I remember, so DTR should drop. (It opens the serial in shared mode twice, once for read and once for write. Best be sure it closes both.) I have massaged the serial device handler greatly here and am 90% finished gaining GREAT control over the serial port for Aterm-derivative programs. I don't know whether I'll patch it into VT100am or make the rest of the beast my own development. Maybe some of both. VT100am seems a bit, er, organic for easy modification. Aterm was even worse... <^_^>

amiga/softw.devlpmt #2668, from afinkel (Andy Finkel, Commodore/Amiga), Mon Sep 15 17:41:16 1986. A comment to message 2665.

DTR should be dropped when the serial device is closed. There were parity problems in v1.1. Those have been fixed for v1.2. (For those who noticed, and calculate parity in your own terminal programs, please make sure you turn off parity when doing your own. Because funky things will happen when we both do parity at the same time, right?)

amiga/softw.devlpmt #2688, from skbower, Thu Sep 18 22:11:25

Well, guys, thanks for all the info and speculation about my DTR problem! I just went down and got myself a funny little connector with a switch on it that connects/disconnects the DTR line; works fine. Somehow, though, it just doesn't feel very satisfying to have this thing. Something about making an elegant solution that you can call your own (i.e., through software). Ah, well, I guess I'll learn to live with it!

ATARI ST

The Atari conference excerpts cover a wide range of applications. The first question concerns reading the arrow keys from C. Next, there is a description of the file format used to store pictures created by DEGAS. Finally, there is a discussion of the problems and benefits of using an Atari ST as an instrument control computer for the laboratory.

READING THE ARROW KEYS

atari.st/questions #515, from jim_kent (Jim Kent), Fri Sep 12 05:28:42 1986.

Anyone know of a good way to read the arrow keys? I've tried Ccrawin, but it just ignores them.

atari.st/questions #516, from sprung (Ron Sprunger), Fri Sep 12 09:25:00 1986. A comment to message 515.

Jim, I was going to ask *YOU* how to read the arrow keys.

atari.st/questions #521, from jim_kent, Fri Sep 12 14:27:59 1986. A comment to message 516.

Ahh, I figured it out. Cconin/Crawin return a long. The low word contains the ASCII value, if any. The high word is 0 for most keys. However, for the arrows the low word is 0 and the high word is things like 0x4c, 0x4d.

continued

```
atari.st/questions #522, from mpack (Don Milne), Fri
Sep 12 14:57:46 1986. A comment to message 515.

Do you get nothing with Ccrawin, or do you get NUL?
You may have to use assembly, 'cause what you need is
in high word of the BIOS return longword (you want the
scan code).

 Suggest you do it this way:

/*.......................................*/

char rawread(scancode)
int *scancode;
{
    char c;

    asm{
         move.w  #7,-(sp)
         trap    #1
         addq.l  #2,sp
         move.b  d0,c
         swap    d0
         move.w  d0,(scancode)
       }
     return(c);
}

/*.......................................*/

So you get the char back as the function result. Then,
if it's NUL, you should check the scan code. The scan
codes returned for the arrow keys are 48H=up, 50H=down,
4BH=left, and 4DH=right.

Does that help? (Now back to M2 mode....)
```

```
atari.st/questions #524, from jim_kent, Fri Sep 12
16:03:03 1986. A comment to message 522.

Exactly. Only it's even simpler than thot since Cconin
already returns the long (at least from the Megamox C
binding).
```

DEGAS PICTURE FILE FORMAT

```
atari.st/questions #577, from dmick (Dan Mick), Sat Sep
20 13:57:04 1986.

If this has been discussed, point away, but here goes:

 What's the format of a DEGAS picture file (or, as I
understand there are different types, in particular the
320x200 4-color version)? If you could explain in
terms of colors and pixels without using ST lingo, I'd
appreciate it, having never seen an ST.  I'm gonna try
to make an IBM version of a DEGAS reader. It's not IFF
format, right?
```

```
atari.st/questions #578, from jruley (John Ruley), Sat
Sep 20 14:44:46 1986. A comment to message 577.

No, it's not IFF format.  The format is 2 bytes
resolution + 32 bytes color map + 32,000 bytes direct
screen dump.  It's really an extremely simple format to
implement - on an ST.  For another computer you'll have
to decode the screen dump data.        --- John ---
```

```
atari.st/questions #579, from dmick, Sat Sep 20
15:20:37 1986. A comment to message 578.

Is the extension somehow significant, or is that just
for user convenience?
```

```
atari.st/questions #580, from jruley, Sat Sep 20
18:26:02 1986. A comment to message 579.

Most programs use the extension as an identifier - if
you are in high res, for instance, only the files with
a ".PI3" extension will show up in the file selector.
In effect, this makes the resolution data in the first
data word redundant.        --- John ---
```

continued

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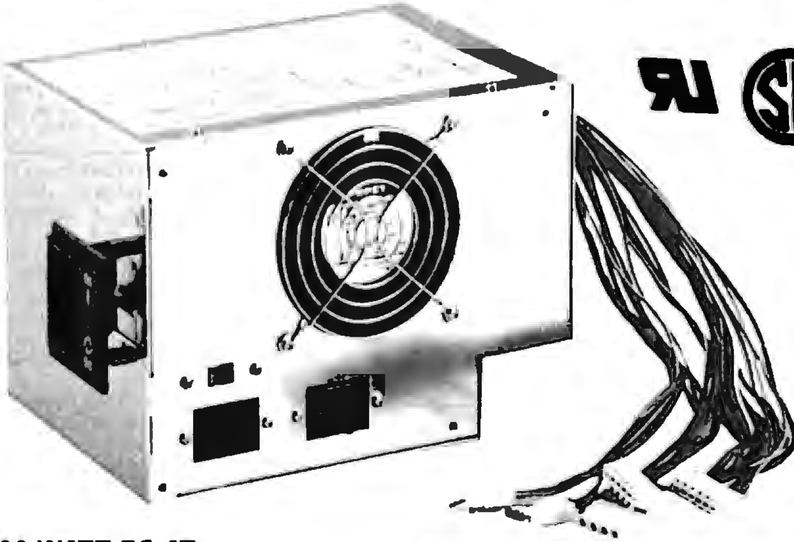

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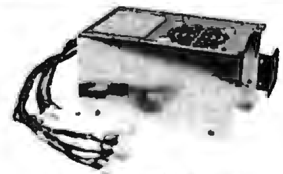

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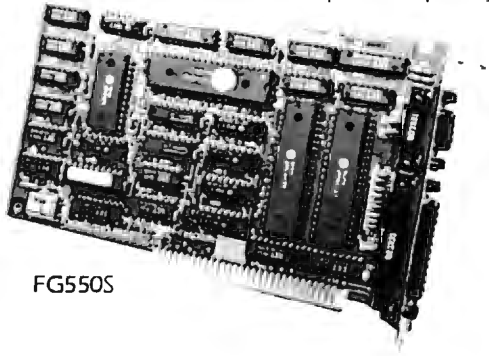

FG550S

Inquiry 141 for End-Users. Inquiry 142 for DEALERS ONLY.

atari.st/questions #582, from jim_kent, Sat Sep 20 22:54:58 1986. A comment to message 580.

Anyway, you've got an EGA, right? The format for a .PI2 file is so:

byte 0 - 0 byte 1 - 2

Bytes 2 through 33 have the colormap. This is grouped by words in Motorola format (high-order byte first). In the .PI2 file, only the first four of these 16 words are significant. They hold the RGB values of the four colors in the format so that: white = $777(hexadecimal), black = $000, red = $700, green = $070, yellow = $770, etc., with, say, a dark blue being $007, $557 being a pastel blue.

Then we get to the fun part: the pixel data. These are represented as two word-interleaved bitplanes. The words are again Motorola words (you might have to swap bytes, or even make bit 0 bit 15, bit 1 bit 14, i.e., mirror the bits). Don't know the EGA format.

The two words contain the pixel data for the first sixteen pixels, starting from the upper left and going right. The pixels are ordered right to left, top to bottom. The high-order bit (bit 16) of the first word together with the high-order bit of the second word make a 2-digit binary number that indexes into the color map.

---

atari.st/questions #584, from dmick, Sun Sep 21 23:38:52 1986. A comment to message 582.

Two clarifications: Do you really mean right to left, or do you always reverse that, like me? Most graphic screens go l-r, which doesn't mean anything, but I's just checkin'. Second: Do you mean the screendump data is two words of 16 bits, one word for each color bit? That is, not only the hi bit, but all bits, form the color of that pixel, regardless of color code in the first word? I assumed that, but you only said the hi bit. (Nitpicker, I know, but I hate redoing good code trying to fix an error with the description, and I'm just not quite sure. Surely, all 16 bits don't have to be the same color, though.)

---

atari.st/questions #585, from jim_kent, Mon Sep 22 00:31:04 1986. A comment to message 584.

It goes left to right.

I'm no good at making generalized descriptions when there's no basic vocabulary to start with. Let me give you an example.

If the first two words are %0011000000000000, %0110000000000000 (where % means binary), then the first four pixels are color 0, 1, 3, 2. The next twelve are zero. Frankly I'm a little dyslexic. The first four may be 0, 2, 3, 1, too. If someone knows for sure, say so. I have to experiment both ways every time I do it.

---

atari.st/questions #586, from dmick, Mon Sep 22 02:00:55 1986. A comment to message 585.

Thanks. That'll be enough to experiment. (Fascinating to find someone else who says r-l when 'e means l-r! Can be a real problem, can't it?) Since Omura's picture of Bob Brown isn't up yet, I'm gonna play with the PICTURE.00x files. They don't have .PI2 extension or 0002 as the first word, but they are just big enough. I suspect it's a different number of colors, as the color map has more entries, but I'll forge ahead just interpreting any color as on, and 00 as off, unless someone knows what format *they're* in. (hint!)

---

atari.st/questions #587, from al (Alastair Mayer), Mon Sep 22 11:33:31 1986. A comment to message 586.

If they're in lo-res mode (16 colors), then you take the 1st bit of each of the first *four* words as the color of the first pixel, the 2nd bit of each of the first four words as the color of the 2nd pixel, and so on. (Who dreams these mapping schemes up, anyway? I've yet to see a personal computer on which they made sense from a software standpoint (no doubt they make sense to the hardware). Give me a word-per-pixel machine!)

---

atari.st/questions #588, from dmick, Mon Sep 22 18:02:10 1986. A comment to message 587.

Well, if you load the bitplanes (or dump them) one at a time, makes perfect sense, no? Problem is I can't access bitplanes like that on the IBM. I betcha can on the ST or the Amigoid, though. Thanks for the info. Is lo res defined as a "0000" in the first word, then a longer colormap? I doubt these PICTURE.000-.016 files are DEGAS format, actually, but they're bitmap of some kind. Tony tells me BBrown's picture is up, so I'll let you know how well your advice (well, Jim Kent's advice) did. Thanks, all, again.

---

atari.st/questions #589, from batteriesinc (Mark Skapinker, Batteries Included), Tue Sep 23 16:27:26 1986. A comment to message 577.

If you look in the back of the manual, we have a full description of the format. DEGAS Elite - our new version, supports IFF for partial screens/blocks. It is described in the back of the new manual - IFF to DEGAS is possible as well within the program. If I may ask, why are you making an IBM version of a DEGAS reader?

---

atari.st/questions #590, from al, Tue Sep 23 16:29:22 1986. A comment to message 589.

I believe he wants to be able to look at pictures that are uploaded in DEGAS format.

---

atari.st/questions #591, from dmick, Wed Sep 24 01:07:51 1986. A comment to message 589.

Sure you may ask. I'm trying to display DEGAS-created pictures on an IBM, and I don't own DEGAS, an Atari, or Amiga, or Deluxe Paint, or... (see, now aren't you sorry you asked?)

---

atari.st/questions #592, from dmick, Wed Sep 24 01:37:52 1986. A comment to message 587.

Is that 0001 resolution ID, and then what pixel dimensions? I think the .PI2 file is not a .PI2 file, Jim Omura. It has a 0001 in the first word. Um... Would someone please do a little summary of bits/pixel vs. ID words for the different .PIx files? (I'd appreciate it if someone would.) Thenkew.

---

atari.st/questions #593, from jimomura (Jim Omura), Wed Sep 24 09:37:17 1986. A comment to message 592.

No, it was definitely .PI2. Batteries Included has allowed me to quote from their manual, so:

Screen resolution indicator:

"This is a WORD value which indicates the resolution of the picture to be dumped. A zero in this indicator means that the picture is a 320x200, 16-color picture. The number 1 in this indicator means that the picture is a 640x200, 4-color picture. The number 2 means that the picture is a 640x400, monochrome picture."

---

tari.st/questions #594, from batteriesinc, Wed Sep 24 13:17:16 1986. A comment to message 591.

Are you doing this under GEM? (No real reason I asked, just interested.)

---

atari.st/questions #596, from dmick, Thu Sep 25 11:16:45 1986. A comment to message 593.

640x200! I had thought you said 320x200. Okay. Thanks.

atari.st/questions #597, from dmick, Thu Sep 25 11:17:19 1986. A comment to message 594.

Nope. DOS. Turbo, for ease of access.

AN ATARI FOR INSTRUMENT CONTROL

atari.st/tech #942, from sgrant (Steven Grant), Sat Sep 6 21:37:09 1986.

I am considering using an Atari ST or an Amiga in my laboratory for data acquisition and instrument control. I have used an Apple IIe for several years for these tasks, but I would like a faster system and a larger memory space. However, to make the port worth my time, the major system improvement I require is that interrupts are not disabled during a disk operation as in the Apple IIe and the IBM PC. I would like to be able to double-buffer my data, and thereby write to disk without missing any of the incoming data. Is this possible on the ST or Amiga? Second, does anyone know of a digital-to-analog converter board for these machines? Finally, my instrument control needs are rather simple; each bit on a parallel port either turns a device on or is a signal from that device that it is on. Do either the Atari ST or Amiga have the requisite hardware or expansion capabilities for this type of I/O? Thanks...Steve

atari.st/tech #943, from al, Sat Sep 6 21:56:15 1986. A comment to message 942.

Just off the top of my head, I imagine the Atari can handle it, perhaps with some kluging. After all, it handles the mouse input (i.e., position sensing) during disk I/O. You could use that port for input with a bit of programming, or the parallel (printer) port.

Don't know about boards. I'd be interested in that info myself.

atari.st/tech #971, from jtittsler (Jim Tittsler, Atari Corp.), Thu Sep 11 02:06:03 1986. A comment to message 942.

One company whose product I have seen demonstrated is G/P-Elektronik. They take an ST out of its case and mount it and a floppy or two (their brochure also indicates the availability of hard disk versions) inside a metal case especially for control applications. They saw off the front of the ST to create a detachable keyboard. The result is a pretty rugged looking 68000-based controller. They have a chassis that allows the installation of modules that contain digital I/O ports, 8 channels, 12-bit analog inputs, and 2 analog outputs. If you would like more information, I suggest you contact them directly: Ingenieur-Buro F. Godler, G/P-Elektronik, Schoenleinstrasse 12, D-1000 Berlin 61, West Germany, Tel.: (030)691 25 09 or 694 34 67

atari.st/tech #972, from jtittsler, Thu Sep 11 02:14:50 1986. A comment to message 942.

If your application is straightforward, and only needs a limited amount of parallel I/O, you might try using the printer port. On the ST computers, it is bidirectional (although at any given time all of the bits must be going in the same direction). You can also use the printer STROBE for output control and the printer STATUS line for on input. The STATUS bit is very easy to read/count. Slow speed sampling could be done using the Joystick Fire Button Monitoring mode which will give you about a 6-kHz sampling of a single input bit (at the expense of other keyboard functions). For high-speed applications, the AHDI/DMA port is probably the best way to go.

atari.st/tech #946, from hisoft (Andy Pennell, Hisoft), Mon Sep 8 13:28:20 1986. A comment to message 943.

There is an ST D/A converter available for 80 pounds (UK) or so, which plugs into the cartridge slot. Don't

continued

know anything else, except that the company (2-Bit Systems) is a DevpacST customer, so they've got to be good. I'll try to get more info.

---

atari.st/tech #948, from sgrant, Mon Sep 8 17:18:50 1986. A comment to message 946.

Thanks for the info. Also, can the cartridge slot be used as a poor man's bus? .....Steve

---

atari.st/tech #950, from jrahn (John Rahn), Mon Sep 8 23:53:12 1986. A comment to message 946.

Am very interested in that D/A converter -- any more information will be appreciated.

---

atari.st/tech #952, from chriskuku (Christoph Kukulies), Tue Sep 9 02:59:35 1986. A comment to message 946.

Do you mean D/A or A/D? D/A shouldn't be a problem. I guess you meant fast (12-16 bit) A/D.

---

atari.st/tech #949, from jsan (Jez San), Mon Sep 8 18:21:53 1986. A comment to message 948.

Steve - The cart port CAN be used as a poor man's bus. Except... a) It has no read/write line! b) It is limited to only 128K addressing. c) Even if it HAD a read/write line, Atari engineers have ensured that all writes to this area of memory are blocked by the Custom Memory Controller chip! (To ensure pirates can't use RAM as ROM, I assume!) -- Jez.

---

atari.st/tech #951, from sgrant, Tue Sep 9 01:26:11 1986. A comment to message 949.

Well, if you can't write to the cartridge slot, then it's a neat trick to initialize a hardware device such as an A/D converter. I wonder how they do it? Again, where might I at least find an ad for this company? ....Steve

---

atari.st/tech #954, from jsan, Tue Sep 9 06:42:45 1986. A comment to message 951.

Sgrant -

Using sneak hardware addressing, you can use the chip select' lines to talk to your devices... e.g., whenever address 'X' is on the address bus, AND 'chip-select' is asserted, then you can enable your device! That is, only a 'READ' is necessary to activate! -- Jez.

---

atari.st/tech #955, from al, Tue Sep 9 20:06:22 1986. A comment to message 951.

There are ways to do it if you don't need the whole address space of the cartridge port. Just treat some of the address lines as write lines. That is, you initialize something by 'reading' from a nonexistent address, which gets decoded by whatever's in the cartridge slot. The 'soft switches' in the Apple II work something like this.

---

atari.st/tech #957, from sgrant, Tue Sep 9 22:58:35 1986. A comment to message 952.

Yes, sorry; I meant A/D, not all that fast. Less than 250-1kHz sampling would be fine, and multiple channels would be best.

IBM PC and Compatibles

The IBM PC section features two discussions concerning IBM PC clones. In the first, there is a question of power supply and slot-sensitive boards. In the second, hardware interrupts are a problem on a Compaq. The final excerpt discusses a method of scrolling text in specific regions of the screen.

POWER SUPPLY PROBLEMS

ibm.pc/clones #274, from j.mott (Jim Mott), Fri Sep 12 22:55:09 1986.

I recently purchased a locally manufactured XT compatible (BEST Mk II) and immediately experienced a problem with the RT clock. The date and time would be maintained throughout a hardware reset (reset button) and a Ctl-Alt-Del, but not a powering down and up. After much fiddling around, the salesman told me that the multi-function card would have to be located in either the first or last slot. Because of the way the power supply is "split," a powering down will interfere with the clock when it is located in a middle slot. This solved the problem.

Has anyone heard of this before? Can anyone offer me a lucid explanation of the problem? I am really wondering whether I should be concerned. Can the performance of any other add-on boards be affected detrimentally?

Another disturbing characteristic of this power supply is the short, harsh buzz that it occasionally makes when powering up.

---

ibm.pc/clones #275, from barryn (Barry Nance), Fri Sep 12 23:05:44 1986. A comment to message 274.

That *is* odd. On IBM motherboards, and on most clones I've seen, the P8 and P9 power connectors lead from the power supply to the board right next to slot #8. That power (+12V, +5V, -5V, -12V) is fed across the board and should be available equally to all the slots. There's nothing special about the 8 slots, except that (on IBM XTs) slot 8 has a few timing differences that make it special. The technical specs for the other 7 slots say that their electrical characteristics are identical.

---

ibm.pc/clones #278, from cdanderson (C. David Anderson), Sat Sep 13 14:57:07 1986. A comment to message 275.

But doesn't the order in which the cards are placed in the (identical) slots sometimes make a difference?

---

ibm.pc/clones #279, from barryn, Sat Sep 13 15:13:05 1986. A comment to message 278.

The slots in an IBM PC are electronically identical (except for slot 8 in an XT, as I mentioned). How could an add-in board possibly *know* which slot it was in? I can imagine that some clones might be different. However, having different specs for the different slots would make it less compatible (and less of a clone). On an IBM machine, or a true clone, an add-in board will function the same no matter what slot it is installed in.

---

ibm.pc/clones #280, from cdanderson, Sat Sep 13 15:18:41 1986. A comment to message 279.

I seem to recall that a Qubie hard disk controller didn't work until I put it next to the floppy controller and "before" the AST SixPak - but maybe I'm remembering Apple days, where order could definitely be a problem.

---

ibm.pc/clones #339, from hans (Henry Bottjer), Fri Oct 3 18:29:48 1986. A comment to message 279.

How about an AT? I was told to put my IBM EGA in slot 1 and only slot 1. Why do you suppose...?

---

ibm.pc/clones #281, from barryn, Sat Sep 13 15:22:44 1986. A comment to message 280.

Maybe the cables to the disk weren't long enough to put it in a different slot?

---

ibm.pc/clones #282, from dondumitru (Donald Dumitru), Sat Sep 13 15:36:38 1986. A comment to message 281.

And maybe some of the components were touching each other? It should make no difference what order the boards are in there. And if you happen to have two boards that conflict (like two memory boards, or two serial ports), it is most likely that *neither* will work.
Donald

---

ibm.pc/clones #283, from cdanderson, Sat Sep 13 16:45:31 1986. A comment to message 281.

Cable length wasn't the problem. Also, maybe it was the 2-meg expanded memory card I am thinking of. Plus, I recall that the Microsoft Mouse bus card wouldn't work in the short slot and I think it didn't work in anything except that last long slot (all this on a Campaq Deskpro). Sorry to be so nonspecific--in general, my point was that maybe a "preceding" card would cause conflicts, even if the slots themselves are electrically identical.

---

ibm.pc/clones #284, from cdanderson, Sat Sep 13 16:46:53 1986. A comment to message 282.

No touching problem; of that, at least, I am sure, since I got burned by this problem in the bad old Apple days and now watch closely for it. It is amazing (to me) how much boards can warp.

---

ibm.pc/clones #285, from barryn, Sat Sep 13 17:00:04 1986. A comment to message 283.

Well, it does occur to me that if there's any ROM code on a card, it gets executed during the POST so that it can initialize itself if need be (the BIOS looks for certain "footprints" in certain locations and, finding one, does a Far Call into the ROM code). I suppose that the ROM code *could* somehow discover what slot it's in if it worked very hard at it. According to the IBM guidelines, such board-based program code is not supposed to do this, however.

---

ibm.pc/clones #292, from rschnapp (Russell L. Schnapp), Mon Sep 15 11:19:27 1986. A comment to message 283.

The MS Mouse card doesn't work in the shortest slot of an IBM PC or XT because of that slot's timing and signal differences from the rest. The only other possible difference between the remaining slots is signal run length. Otherwise, they are all identical. Boards cannot "tell" which slot they are in, and the CPU cannot distinguish them either. The Apple II series distinguishes cards by giving them distinct address decoding for memory-mapped I/O and driver code.
...Russ

---

ibm.pc/clones #305, from josephs (Joseph S. Hupert), Wed Sep 17 01:59:49 1986. A comment to message 283.

When we got a Tall Tree JRAM card for our Z-150, Tall Tree pointed out that placement of the card as far as possible from the HD controller was desirable to minimize possible electromagnetic interaction between the two. So the nature of the components and their relationship may in fact have an effect; however, this is entirely spatial.

---

ibm.pc/clones #286, from dondumltru, Sat Sep 13 17:31:36 1986. A comment to message 285.

But *how* would it find out which slot it's in? The data lines are hooked to the connectors in bus-fashion, right? How would a board know that it is connected after two empty slots - or even two full slots? I don't think it could be done.
Donald

---

ibm.pc/clones #287, from skluger (Sigi Kluger, Definicon Systems, Inc.), Sat Sep 13 18:51:50 1986. A comment to message 285.

Short of measuring propagation delay, there is no way for a board to find out which slot it is in. This, of

continued

course, excludes AT-style boards which CAN sense whether they're plugged into a 16-bit slot...

---

ibm.pc/clones #290, from dmick (Dan Mick), Sun Sep 14 01:22:00 1986. A comment to message 285.

Couldn't unless there was some difference in the bus connector for the cards; there's not supposed to be, according to the hardware refs, (excepting 8), but I'll swear we've had async cards that didn't work in one slot and worked in another. Probably connection problems on one socket pin or some such, but surely annoying.

---

ibm.pc/clones #288, from geary (Michael Geary), Sat Sep 13 20:03:28 1986. A comment to message 287.

Right. Also, all the slots on an AT are electrically identical whether they have the second connector installed or not. I've had a few people ask me whether they could plug an 8-bit card into a 16-bit AT slot. The answer is yes, as long at it physically fits into the socket. The second connector was left off a couple of the AT slots just to allow for 8-bit cards that have some overhang and physically won't fit into a 16-bit slot. If you look at the motherboard you'll see that there are pads where the second socket could be soldered into those 8-bit slots.

---

ibm.pc/clones #289, from barryn, Sat Sep 13 21:15:45 1986. A comment to message 287.

You're right. I stand corrected.

---

ibm.pc/clones #293, from cdanderson, Mon Sep 15 12:10:56 1986. A comment to message 292.

Conceding that the board can't tell what slot it is in, might it still be possible (as a matter of abstract logic) that conflicts between two boards might be resolved differently, depending on which gets the signal (a tiny bit) sooner?

---

ibm.pc/clones #294, from dmick, Tue Sep 16 00:08:31 1986. A comment to message 293.

It's much more likely that the gates (TTL for address decode, data latches, etc.) would be different from the extra 2 inches of solder the bus travels. Gates are guaranteed faster than x, but how much faster is pretty much anyone's guess, at least in the units of "(speed of light)/2," they are.

HARDWARE INTERRUPTS FOR DATA ACQUISITION

ibm.pc/hardware #1292, from buzz (Steven Rotyliano), Wed Oct 1 12:47:09 1986.

I need help in using hardware interrupts on my Compaq Plus. I'm setting up a data acquisition system with the Campaq and a Lab Master ADC board. I'd like to use a 200-Hz timer to generate an IRQ request to start the aquis routine, but so far haven't had any luck using IRQ2. Is this a reserved interrupt? If not, what are the necessary steps in the interrupt handler? So far, I've created a main routine in Lattice-C that calls an assembler routine to initialize the interrupt vector to another 8088 routine, which calls a C routine to do the actual aquis. I've verified the initialization by calling a software interrupt (INT 0Ah) and everything appears OK, but when the timer generates the interrupt, the system crashes in a big way. The last step in the interrupt handler does a nonspecific EOI to the 8259. I'm lost at this point. Any advice sure would be helpful.

Thanks, Buzz

---

ibm.pc/hardware #1293, from skluger, Wed Oct 1 13:58:12 1986. A comment to message 1292.

I use IRQ2 all the time with no problems. Assuming that IRQ2 is not used already by anything in your system, the only possibility is that your software is corrupting things. First off, if your IRQ handler does anything at all, it should set up its own stack and save ALL registers that could possibly be used (be sure to also save register BP!). Next, if the interrupt handler does any sort of file access, things will get very confusing very fast. I haven't actually dug that far into things to be of help in that case. If you need to do any DOS functions it may be best to use the IRQ handler for very rudimentary things and set a flag that can be interrogated by a running user program and let the program handle all the complicated stuff.

---

ibm.pc/hardware #1294, from drifkind (David H. Rifkind), Wed Oct 1 15:34:21 1986. A comment to message 1292.

1. Make sure that you are saving and restoring ALL registers that might be changed.

2. Remember, you CANNOT count on the contents of the DS, ES, or SS registers in your interrupt handler. When you generate the software interrupt from within a C program, they will be set correctly, but with the hardware timer, the interrupt might occur while DOS or BIOS code is executing.

3. If you reenable interrupts while your handler is executing (which you probably should), disable them BEFORE generating the EOI.

---

ibm.pc/hardware #1295, from sparks (Dave Sparks), Thu Oct 2 00:55:06 1986. A comment to message 1292.

I've done several interrupt drivers for the PC. As previously mentioned, there are lotsa gotcha's.

1) The most critical is saving all the regs. If you don't do that, it will blow up every time.

2) If the interrupts are occurring only while your program is running (i.e., not a part of a TSR), you probably don't have to fool around with another stack, since you can just make sure that there's always enough stack to go around. If you're writing a TSR background task, you'd better use your own stack.

3) DOS calls are verboten from the interrupt. If you must do DOS calls, see the earlier discussion in ibm.pc/software (I think it starts at message #999).

4) You must restore the segment registers (other than CS) that are used in the interrupt service routine. The easiest way to do this is to copy the values into variables located in the code segment:

```
_prog   segment para public 'CODE'

dataseg dw  (?)
            ;data segment address
            ;initialization code start
   proc far
        ...
        mov ax,ds              ;get the data segment
        mov cs:[dataseg],ax    ;save for later
        ...
 start  endp

;interrupt service routine isr
    proc far
        push ds                ;save regs
        push ax
        ...
        mov ax,cs:[dataseg]    ;get data segment address
        mov ds,ax              ;into DS reg
        ...                    ;now DS references are OK
        pop ax                 ;restore regs
        pop ds
        iret isr
    endp
 _prog  ends
```

Hope this helps.

SCROLLING IN REGIONS

ibm.pc/programming #532, from skluger, Sat Oct 4 12:06:49 1986.

I'm too lazy to go to the office to pick up my copy of Norton's or the BIOS listing... Can anyone please tell me how to freeze a line (the top or bottom line) on a PC so that when the whole screen scrolls, that one line stays put? I know this is possible by telling the BIOS - or at least I think I know. So let's say I want to freeze the top line in place until my program terminates. How?

ibm.pc/programming #533, from dondumitru, Sat Oct 4 15:15:11 1986. A comment to message 532.

This is not built into the BIOS - you would need to write your own ISR to handle the TTY-Write function of the BIOS video interrupt. I would say that it is not too hard to do such a thing - *IF* you are familiar with writing interrupt service routines.
Donald

ibm.pc/programming #534, from skluger, Sat Oct 4 15:29:41 1986. A comment to message 533.

I don't believe that. I could have sworn that one time when I had nothing better to do I read Norton's book and played with a debugger scrolling partial screens up and down, using just BIOS calls!

ibm.pc/programming #535, from dondumitru, Sat Oct 4 15:36:11 1986. A comment to message 534.

OK - here's the deal. The BIOS has "scroll" functions that scroll windows. That is, you can scroll the region from (x1,y1) to (x2,y2) either up or down (or clear it altogether). (But the BIOS doesn't have left/right scroll routines.) You can use these routines to scroll whatever region you want. But from your message I got the impression that you wanted to have, say in DOS or some other already-existent application, the top two lines stay put. This can't be done, because most "serial" screen writes go through the TTY-Write function, which scrolls the entire screen. So - what exactly do you want to do? Write your own application that has a custom scrolling region, or get some other application to do it? The first is no big deal. The second requires you to take over the BIOS TTY-Write function.

ibm.pc/programming #536, from skluger, Sat Oct 4 15:41:03 1986. A comment to message 535.

Yes, I remember now. You have to tell the BIOS to scroll. That, in my application (a primitive terminal program) would simply mean ignoring incoming LFs and calling the scroll routine instead. All I want is a status line that stays put when the screen scrolls. I'm doing a few funny things on the screen and my backscroll function doesn't work right with a scrolling top line/status display (I can backscroll up to 300 lines worth of status lines, heh heh heh!).

ibm.pc/programming #537, from dondumitru, Sat Oct 4 15:44:03 1986. A comment to message 535.

Here's the info on the BIOS scroll routines. They are accessed through INT 10h. AH=06h - Scroll region up, AH=07h - Scroll region down. BH=attribute - to be used on new lines, AL=number of lines - to scroll (0 means to clear the region), ch=y1, cl=x1, dh=y2, dl=x2. Neither function changes the cursor position.
Donald

ibm.pc/programming #538, from dondumitru, Sat Oct 4 15:45:21 1986. A comment to message 536.

I forgot to mention in my previous message on the scroll routines - the home position is (0,0).

continued

MACINTOSH

In the first thread of the section, the importance of a program's name is discovered. In the second, there is a discussion dealing with hard disk problems. Then, a question on how to uninstall a program leads to a discussion on the state of public domain software. Next, there is a thread dealing with problems encountered when programming in Pascal. Finally, there is a question on how MacPaint files may be displayed using an assembler program.

MEGAROIDS BY ANY OTHER NAME...

macintosh/news #555, from kschmucker (Kurt Schmucker), Wed Sep 3 07:32:07 1986

Megaroids+ does NOT work on a Mac Plus. I downloaded it (with no transmission error except the customary timeout before BIX begins the XMODEM transmission), put it on a disk with System 3.2 and Finder 5.3, booted my Mac Plus, double-clicked on the Megaroids+, and promptly got the bomb (ID = 26). Repeated the same sequence on the same machine and on another Mac Plus.

---

macintosh/news #556, from tom_thompson (Tom Thompson, Technical Editor, BYTE), Wed Sep 3 09:28:03 1986. A comment to message 555.

Maybe a bad upload. I ran it under System 3.2/Finder 5.3, shot a few rocks and a saucer, said: "Yep, it works all right," and uploaded it using XC and Red Ryder 9.2. It also works on a friend's Mac Plus. Hmmm... let me check it out again. Let's see, it's on a floppy here somewhere...copy it to the HD20 and fire that puppy up... *** BONG *** ID = 26...Uh oh...

Well, it WAS working before I uploaded it. I don't upload stuff without checking it out. Something has happened, but yeah, you're right... ---tom_thompson

---

macintosh/news #557, from tom_thompson, Wed Sep 3 10:18:05 1986. A comment to message 556.

Megaroids DOES work. When I first obtained Megaroids, it was named exactly that: Megaroids. And it ran! To prevent confusion with an earlier copy of Megaroids, I named it "Megaroids+" and uploaded it. I got to thinking about that (Do you think the programmer would *really* be paranoid about somebody changing the name of his game? Now...). Nevertheless, I stuck that disk with Megaroids+ on it into the disk drive and renamed it "Megaroids." Then I copied it to the HD20. And doubled-clicked on the icon, while tensing for a System Bomb Visitation. And it RAN!!! So, quick now: change the name of your file to Megaroids and let me know what happens. I've already deleted the file from BIX and will upload it with the proper name. My apologies! ---tom_thompson

---

macintosh/news #562, from rschnapp (Russell L. Schnapp), Thu Sep 4 11:45:26 1986. A comment to message 557.

I bet I know what's up! It's not programmer paranoia. It's screen flipping. To get access to the alternate screen buffer, you've got to relaunch a program with a special request. The straightforward way to do this is to simply hard-code the name of the program to launch into the program. Thus, Megaroids+ is trying to relaunch "Megaroids", which you may just have on your disk, and which is not Plus-compatible. By the way, I understand there is a better way to obtain the name of your program (someone told me about it when I distributed the demo for my book, "Macintosh Graphics in Modula-2," which has a screen-flipping demo). I don't remember how it works, though. I'm sure I could dig it up. ...Russ

---

macintosh/news #563, from dbetz (David Betz, Senior Editor, BIX), Thu Sep 4 11:56:51 1986. A comment to message 562.

Isn't the application name stored as one of the application parameters? I used to open the data fork of an application to find bytecodes so that I could build double-clickable applications for interpreted code and I used one of the application parameters to determine the name of the application file. David Betz

---

macintosh/news #567, from frankb (Frank Boosman), Fri Sep 5 11:05:01 1986. A comment to message 563.

Yes, CurApName, at $910, is a global variable containing the name of the current application.

---

macintosh/news #568, from tom_thompson, Fri Sep 5 13:14:20 1986. A comment to message 567.

I dunno. All of the above may be true, but I've poked around in Megaroids with Fedit, and it has a sizable data fork. I'm guessing he stores his startup screen and images in here and hardwired the filename in somehow. At least he's learned his lesson on hardwiring the screen buffer addresses: I've got a Mac Plus with the extra meg of memory and Megaroids works on it just fine. ---tom_thompson

NOISY HARD DISK PROBLEM

macintosh/prod.discussn #550, from dbetz, Sat Oct 11 10:59:20 1986.

My Dataframe 20 disk has started making a chirping sound. The dealer tells me that some of the drives have a problem with an antistatic brush and the fix is simple. Has anyone else had any experience with this sort of problem? Should I allow the dealer to "fix" it or would I be safer trying to get him to replace the entire unit?

This is the second problem I have had with this drive. The first was that it seems to have a bad power supply. The line voltage in my house is higher than normal (about 127 volts) and most of the time the drive refuses to come on. If I wait long enough, it eventually does power up, but it almost never does immediately. The Dataframe people said that they got some power supplies that were slightly out of spec and that a few people had reported this same kind of problem. They promised to replace the power supply, but that was well over a month ago and my dealer still hasn't received the replacement supply. I know other people have had good things to say about the Dataframe 20. I really like mine, but I wish I would stop having these minor, but annoying, problems. David Betz

---

macintosh/prod.discussn #551, from rschnapp, Sat Oct 11 17:40:27 1986. A comment to message 550.

Get the dealer to replace the drive, if you can. The chirp generally turns into an intermittent squeal that resonates at headache-frequency. There was some discussion of this in, I think, ibm.pc/drives. There are fixes for the chirp/squeal, but they are only temporary. They generally involve application of lubricant to the antistatic bushing. This requires disassembly and reapplication every couple of months. I sure wish we could get rid of these darned moving parts and precise machinery, and get back to solid-state electronics again! Whatever happened to bubble-memory technology? Did it hit its price/performance limits? ...Russ

---

macintosh/prod.discussn #552, from dbetz, Sat Oct 11 17:43:29 1986. A comment to message 551.

Thanks for the advice. I'll try getting my dealer to replace the drive. David Betz

THE GREAT PUBLIC DOMAIN DEBATE

macintosh/prod.discussn #554, from ccrawfor (Chris Crawford), Mon Oct 13 00:44:22 1986.

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JANUARY

I wonder if anyone can help me clean up a problem. I received a disk full of PD and shareware stuff and went through it looking for interesting programs I might want to keep. One program was called JClock but had no further information, so I double-clicked it to see what would happen. (The source of the stuff was pretty reliable, so I felt that there was no danger.) Well, it seems that this little monster installs a digital clock on your menubar. Fine, but how does one uninstall it? No provision seems to have been made for such an option.

The person who wrote this example of poor programming is one James T. Sulzen of Lexington, MA, but no further information on how to reach this fellow for information is provided. If anybody out there knows who this guy is, or how I can clean out his damnable program (it apparently installs itself in your system file, as I can find no special files for it), I would greatly appreciate the help. I may have to disassemble the program to figure it out. What a pain!

---

macintosh/prod.discussn #556, from modal (Marcia Odal), Mon Oct 13 07:07:16 1986. A comment to message 554.

As far as I know, you can't uninstall it.

---

macintosh/prod.discussn #557, from lloeb (Larry Loeb), Mon Oct 13 08:28:52 1986. A comment to message 554.

Does it show up in the system file with ResEd? If so, that may be one way to pull it. --Larry

---

macintosh/prod.discussn #558, from obrz (OBRZ is a group account used by the members of the Oerlikon-Buehrle Rechenzentrum AG company in Zurich, Switzerland), Mon Oct 13 08:44:31 1986. A comment to message 554.

I don't have the original JClock, but I have the version which is on the "JClock31.p2t" file in listings/macintosh. That one contains an "INIT 31" resource. You may want to look (with ResEdit) at your copy of JClock, see what INIT resources it contains, find the corresponding resources in the System file and remove them.

P.S. The BIX-listings version of JClock is easy to install AND uninstall.

P.P.S. Not having the original version of JClock, I can't know if this information is of any help to you.

---

macintosh/prod.discussn #559, from lloeb, Mon Oct 13 08:52:09 1986. A comment to message 558.

Remembering that there may be INIT 31s in there that you want... --Larry

---

macintosh/prod.discussn #560, from dbetz, Mon Oct 13 09:59:40 1986. A comment to message 554.

I know Jim Sulzen. He is the director of the Boston Computer Society Macintosh Technical Group. I don't know his phone number, but you should be able to get in touch with him through the BCS main office in Boston. David Betz

---

macintosh/prod.discussn #561, from rschnapp, Mon Oct 13 10:56:08 1986. A comment to message 554.

Chris, you can perform a JClock-ectomy via ResEdit. Using ResEdit, open your System file and inspect the INIT resources. Then select the one named JClock and cut it. Close the System file and OK the change. I'm not sure, but I think that you cannot edit the active System file this way, so boot off (or transfer to) a different disk, first. ...Russ

---

macintosh/prod.discussn #562, from frankb, Mon Oct 13 11:24:11 1986. A comment to message 554.

1. The version of JClock you have was written at a time when there was no other way to cause an INIT resource to be run at boot time then to install it in the System file. If you're going to criticize Sulzen for doing so, I'm going to patiently wait for you to criticize Andy Hertzfeld for doing the same thing with HFSFix.

The newest version of JClock, 3.1, fixes this problem using Apple's new method of placing INIT files in the System Folder--a much different proposition.

2. The documentation that comes with JClock 3.1--which is available from the listings section here on BIX--tells exactly how to remove the old version from your System files. I also understand that there was a program floating around to do the same thing, but I don't know anything else about it.

3. And why go off the deep end on the author of this piece of PD software? It's not like it's a Trojan horse or somesuch... My feeling is, Confucius say, he who

continued

run unknown software soon find out what it does hard way. Next time, ask around on BIX before you run a program you know nothing about.

---

macintosh/prod.discussn #564, from ccrawfor, Mon Oct 13 23:12:12 1986.

Wow! I really stirred the pot with that comment on JClock. Some generalized responses:

Severol people suggested I use ResEdit to banish it from the System file. I made a not-too-thorough effort in thot direction and failed. It should have worked, but I couldn't find anything that was obviously, indisputably JClock; in the absence of certainty I didn't want to make matters worse.

I ended up rebuilding a new System file. I started with a standard that I keep on backup and loaded it up with my fonts and DAs. Took all of five minutes. Brute force, yes. Clumsy, yes. But it worked and took little time.

Several people pointed out that "idiot" is a strong term to use in this case, especially seeing as how Mr. Sulzen was generous to make it PD. Well, yes, "idiot" is a strong term. Perhaps I should have used a milder epithet. But there can be absolutely no defense of a program that irreversibly alters a system file, especially one that does so in the manner that JClock does. PD Software is *intended* to be spread around, and always leaves its documentation behind. What Sulzen should have done is: 1) post a longer message on the title page (he had plenty of room) explaining what the program does; 2) provided an "Abort" option along with a "Proceed" option; and 3) provided some explanation of how to remove JClock, or even better, provide a "Delete existing JClock" option.

The argument that JClock *must* be installed in the System file because that is the only way that was technically feasible back then is irrelevant. I do not question the author's decision to use the System file, only his failure to provide a means to remove it should the user decide so.

Finally, there is the question of trusting PD software. One respondent suggests in so many words thot anybody stupid enough to run unvouched-for PD software deserves everything he gets. In my case, the stuff came through a source that I had placed (obviously undeserved) trust in. But there is a broader question here for all of us: What do we *expect* of PD software? Let us put aside the matter of Trojan horse software or other deliberate forms of mischief. What about serious PD software? When a man like Mr. Sulzen lets a program of his take wing and fly out into the community, does he accept *any* responsibility (ethical, not legal) for this act?

Imagine the spectrum of misbehavior from PD programs. At one extreme is the program that accidentally wipes out files on a hard disk. This is very bad indeed; were someone to release such a program, he would quickly earn the universol condemnation of the community. At the other extreme is the program that creates some minor inconvenience for owners of abnormal systems.

Where do we draw the line? How bad does a PD program have to be before we all start screaming that the author is an idiot or a scoundrel?

---

macintosh/prod.discussn #565, from dbetz, Tue Oct 14 08:12:12 1986. A comment to message 564.

One problem with the concept of PD software is that the authors of such software are often "convinced" by their friends and associates to make a program that wos only intended for their own personal use available to others through the PD. They are told that "we can live with the limitations." Well, maybe the original users can live with the limitotions, but they poss the program on to others and the others expect more. This results in the author getting a bad reputation for releasing a program that he/she never intended for public consumption in the first place.

This has happened to me with early versions of XLISP. People would get copies and be outraged that I was not willing to defend every little design decision and limitation.

What does this all mean? Should software authors refuse to distribute anything that isn't up to commercial standards or should they continue to provide software on an "as is" basis to users who know how to overcome whatever limitations might be present? I often appreciote being able to use software thot is in a "not ready for prime time" state because it is often available in source form and can be fixed by a knowledgeable user or it is available at a price that is much lower than similar commercial products.

I don't want to start expecting PD software authors to live up to the standards of commercial software vendors because it is likely to reduce substantially the number of PD programs that are released to the public. David Betz

---

macintosh/prod.discussn #567, from nz_mhamel (Michael Hamel), Wed Oct 15 00:52:46 1986. A comment to message 565.

> I don't want to start expecting PD software authors
>to live up to the standards of commercial software
>vendors because it is likely to reduce substantially
>the number of PD programs that are released to the
>public.

I'm afraid my reaction to this is that that is precisely what ought to happen. I would argue that a PD author is under exactly the same ethical obligations as any programmer anywhere to do a good job. Why should the fact that you're not asking money for a program alter the nature of a programmer's job? It doesn't. Instead, what happens? Software overload from PD programs cast onto the high seas by people who are learning to program the Mac. I'm sure you all have those terrible disks full of PD software that really are 98% junk, but you can't throw them away because you might just need something in there sometime.

If a PD author doesn't think his program adds to the sum of Mac software or doesn't work properly, he is under an obligation to users *not* to release it. I'm doing this right now with my profiler DA. Sure it works, looks good and all that. But now and again it goes blooey in a most spectacular manner and I'm not letting it go PD until I find out why. Michael

---

macintosh/prod.discussn #568, from dpallen (David P. Allen), Wed Oct 15 00:53:26 1986. A comment to message 564.

Observation:

1. Why would anyone trust the untested admixture of unknown software with anything of importance that wasn't a copy of the valued program?

2. I think it took more time for you to write your grumble than it did to foreclose on the cause of your discontent.

Tweedle-dum and tweedle-dee, Chris.

Uncle David

---

macintosh/prod.discussn #569, from ccrawfor, Wed Oct 15 02:09:46 1986. A comment to message 565.

Yours is, I think, an odd case. Seldom do we see entire languages released as PD. For the most part, PD software consists of trinkets: odds-and-ends programs that perform minor functions. In this sense, JClock is very much a "mainstream" PD program. I think that it is fair, reasonable, and proper for the community to expect such trinkets to be nondestructive and perform pretty much as advertised. When we start talking about big PD programs such as languages or an adventure construction set, then it is quite unfair to expect that such ambitious programs be up to the standards of commercial software. There is a need for PD software; the commercial houses will never bother to create little trinkets like JClock because they are too small, too minor to merit the advertising and packaging expenses. Moreover, PD work is an excellent vehicle for an aspiring young programmer to make his mark, or an established author to release some minor item that he whipped together one day (I've done quite a few that way myself). So I will not argue against the existence of PD software, just the Wild West atmosphere in which much of it is spread around.

---

macintosh/prod.discussn #570, from dbetz, Wed Oct 15 09:09:17 1986. A comment to message 567.

I certainly wouldn't suggest releasing known bad software into the PD. I was just saying that sometimes an author doesn't have the time or resources to support a commercial product. There are often people who want to use the program anyway in spite of its lack of commercial support.

Originally, most PD software came with source code. I think that this should continue to be true. That way, any user can uncover and fix problems him/herself. I am always anxious to find the source code for an interesting program, but I don't expect that something that I get from the PD will replace a commercial product. If I want the (supposedly) high reliability of a commercial product, I am willing to pay real money. I am in favor of all PD software coming complete with source code so that users can support it themselves. If you aren't a programmer, you might need to stay away from some PD programs because you don't understand the source code well enough to fix any problems that come up. (I'm not talking here about *you* in particular, merely stating that some PD software is intended to serve as example code and isn't really for general consumption.)

Let's stop thinking of PD software as an alternative to commercial software. It is instead a source of a wide variety of varying-quality programs that should be used with caution by anyone who doesn't have the technical ability to evaluate the quality of the program or the appropriateness to their intended purpose.

In conjunction with this, I really don't think that it is very useful to distribute unsupported PD software that doesn't include source code. Here the user really is left without any support. I must admit that I use such software occasionally, but I would really like to see PD authors start including source will *all* PD programs.

One of the greatest advantages of PD software is that the source code can serve as an example of how to approach a particular type of problem. Spreading this kind of knowledge can only improve the quality of both PD and commerciol software.

Please don't start expecting unreasonable things of people who are merely trying to share the results of their own efforts with colleagues. David Betz

---

macintosh/prod.discussn #571, from dbetz, Wed Oct 15 09:17:32 1986. A comment to message 569.

I think one real problem with PD software is the uncontrolled way in which it gets distributed. I have often given a copy of a program that I have written to a friend for his own use and then found that program distributed through a user group library. The friend understood that I was providing the program *as is* and didn't expect it to live up to commercial standards. The other users in the group (and other groups as well) expected the program to be bug-free and documented and supported like a commercial product. I have no idea how these people think such support is paid for with free software, but they seem to expect it nonetheless.

Another problem with PD software distribution is the way user groups repackage software. XLISP comes on a disk with the executable code, the documentation, sample programs and full source code for the interpreter. I often get calls from people who got one part or the other, but not the complete package. It seems that one person will get my distribution disk and upload only the executable to a BBS. Then users of the BBS will download the executable and complain that it doesn't have needed documentation.

I know it is possible to require that all of the pieces be distributed as a unit, but how often is that requirement actually followed? I don't have the legal resources to prosecute everyone who violates such a requirement, but I don't want to deprive users of my program from continuing updates either. David Betz

---

macintosh/prod.discussn #573, from nz_mhamel, Thu Oct 16 04:46:58 1986. A comment to message 571.

Um, yes. It would be nice if PD software were always distributed *only* as source code. That would mean

continued

"this is for programmers - if you can compile it you take responsibility for it." But the real world doesn't work that way, especially the Mac world.

Software spreads in strange ways. There are a lot of users out there to whom the Mac is a tool, not a computer, and they haven't the least idea of the sort of grubby things that go on in its interior. These people have no notion of how difficult programming is, and their exposure to computers is limited to the Finder, MacWrite, and MacPaint. They are complete innocents who expect everything to behave nicely. They don't know how to use something with caution because they literally don't realize what can go wrong. When they run into some useful-looking piece of PD software that turns out to crash about their ears every second day, it somewhat destroys their faith in the machine and they get very nervous about any sort of change to software at all.

I work for a university and I do see this happening - I meet people who are still using Finder 1.1 and never back anything up. The Mac lets such people exist and get along fine. Less than adequate software is a threat to them. Michael

---

macintosh/prod.discussn #574, from dbetz, Thu Oct 16 08:10:34 1986. A comment to message 573.

Maybe we should invent yet another category of PD software. This would be "sourceware" that is available in source form and is intended for people who know what they're doing. I don't know what category XLISP would fit into then. I do provide source, but I think it is stable enough to be used by someone who doesn't know C or have access to a C compiler. I just don't want to stop seeing good (but maybe not excellent) example code being distributed by people who have done interesting things for their own amusement and are willing to share the results with others on an "as is" basis. I myself can't afford to support XLISP as a commercial product, but I know that there are *lots* of people (and companies and educational institutions) making good use of it who would be unhappy to see its distribution cease. David Betz

PASCAL BUG

macintosh/softw.devlpmt #622, from nz_mhamel, Mon Oct 27 01:50:04 1986.

I have just started using TML Pascal version 2.0, and what do you know, I immediately find zee bug. If you try to pass a character from a packed string as a character parameter, the compiler does a word access into the string and either gets a second character in the high byte or an address error. Thus,

```
function Uppercase(ch:char):char; .... var s:Str255;
.... TheChar := Uppercase(s[i])
```

dies horribly, where "s" is a Str255. Someone might need to know this. I don't suppose Tom Leonard is on BIX, is he? If someone in the US can reach him you might mention this to him. Otherwise, it really is a great improvement on version 1, so much faster. Has anyone tried out MacApp on it yet? Michael

---

macintosh/softw.devlpmt #623, from kschmucker, Tue Oct 28 07:11:46 1986. A comment to message 622.

Even though TML v2.0 supports the Object Pascal extension, you can NOT use it to write MacApp programs. This is because the MacApp class library uses many other features of MPW Pascal (like conditional compilation and compiler variables) that TML doesn't yet have. I spoke with Tom about this in August and he is well aware of the problem. Kurt

---

macintosh/softw.devlpmt #624, from paul.hoffman (Paul Hoffman), Tue Oct 28 23:17:33 1986. A comment to message 622.

How did you get version 2? I ordered mine months ago, but it never arrived....

---

macintosh/softw.devlpmt #626, from nz_mhamel, Thu Oct 30 21:11:51 1986. A comment to message 624.

I take it all back: We just got version 2.01 and Tom Leonard's fixed it, along with that bug that was on USENET a while ago. I have found one he hasn't fixed though:

```
  const huge = 65536; var i : integer;      j : longint;

i := HiWord(huge + j); i := LoWord(huge + j);
```

generates the same thing for both HiWord and LoWord; the HiWord code is wrong. I think it only does it for expressions.

I heard Larry Rosenstein saying they were working with TML on MacApp back in August; I thought something might have happened by now. But from this it looks as though Tom's still stamping on bugs...
Michael

(Paul: We just ordered it. Perhaps New Zealand gets its mail before you do?)

DISPLAYING MACPAINT FILES FROM ASSEMBLER

macintosh/softw.devlpmt #628, from jargabright (James Argabright), Sat Nov 1 23:33:34 1986.

I have spent the last month trying to display a MacPaint file from an assembley program and, quite frankly, I haven't been very successful. As a novice assembly programmer, I would appreciate any help or information on how to accomplish this. I seem to be able to open and read the file, but I can't get the file to display inside a window.

---

macintosh/softw.devlpmt #629, from ccrawfor, Sun Nov 2 23:58:40 1986. A comment to message 628.

The trick to making use of MacPaint files is a Toolbox routine called UnPackBits. It takes as its inputs: 1) a pointer to the MacPaint file; 2) a pointer to the bitmap image that you wish to construct from the MacPaint file (one of the items from the BitMap record); and 3) the number of bytes (?) that you want it to translate per horizontal line of image.

Basically, you read in the file, skip the first 512 bytes (it's header information), then start UnPackBits'ing it into your bitmap file. It's a simple operation if you're willing to use big buffers. If you want to save RAM, it gets trickier taking it a chunk at a time. Scott Knaster published a very clear code fragment that shows the process. It should be somewhere in the Tech Notes or the Software Supplement. If you need it, I can try to look it up.

---

macintosh/softw.devlpmt #630, from jargabright, Mon Nov 3 22:35:06 1986. A comment to message 629.

Thank you for your reply. If I could get an example that shows how to open and display MacPaint files it would really help. I don't have the Tech Notes or the Software Supplement, but I could order them from Apple. Are they worth the expense? Jim Argabright

---

macintosh/softw.devlpmt #631, from ccrawfor, Mon Nov 3 23:16:36 1986. A comment to message 630.

There's a source listing in your mail.

---

macintosh/softw.devlpmt #632, from frankb, Tue Nov 4 00:19:16 1986. A comment to message 631.

Execute the following sequence of commands:

j listings a mac.supplmnt r tn86.wrt xc b

... and set your computer to receive MacBinary XMODEM, and you'll get Macintosh Technical Note #86, which describes in very complete detail the fine points of working with MacPaint documents. Highly recommended.

---

macintosh/softw.devlpmt #634, from jargabright, Wed Nov 5 10:21:40 1986. A comment to message 632.

I got the source listing in my mail and I downloaded the Technical Note. This is great. I thank you both.
Jim Argabright

---

macintosh/softw.devlpmt #635, from jargabright, Tue Nov 11 22:54:31 1986.

I'm still having problems displaying a MacPaint file from an assembly program. I'm not sure how to move my bit image into the window I've created. I've been using the _SetPBits (SetPortBits) routine to transfer my bit image to the window, but it's not working. Descriptions in Inside Macintosh seem vogue. Macintosh Technical Note #86 uses a Pascal program as an example, but it uses a rather simplistic approach to display the image on the screen. I would rather transfer the image to an existing window, since that would seem like a more orthodox approach. Jim Argabright

---

macintosh/softw.devlpmt #636, from frankb, Wed Nov 12 10:58:36 1986. A comment to message 635.

I don't think SetPortBits is at all what you want. Try using CopyBits instead.

APPLE II

The Apple II section begins with a discussion of disk compatibility issues and the IIGS. This discussion evolves into a look at how to use various slots within the GS, and at some of the considerations of the design team. The section ends with a review of the specifications in the area of battery-backed RAM in the IIGS.

IIGS DISK DRIVE COMPATIBILITY

apple/gs.compat #100, from waltwiz (Walter Sikonowiz), Sun Oct 19 21:18:16 1986.

Could someone please make a summary of the drive compatibility problem with the GS? Please, only include all Apple drives and interfaces.

One question. All drives with their interfaces (Apple ones only) in a IIe will work with no modification in an internal slot in the GS? Am I right? Now, the problem is the built-in port for drives in the GS. Could someone please explain which ones could be attached to it, and which ones can be daisy-chained, and the modifications necessary (the resistor). For example, in a school environment this would be really helpful if they have a wide variety of both old and new types of interfaces and drives. Could be a decisive factor to see how much of which equipment has to be bought, etc. Any help would be greatly appreciated.

---

apple/gs.compat #101, from waltwiz, Sun Oct 19 21:20:24 1986.

Also on monitors, including only Apple products, both old and new ones, that can be used with the IIGS? Should be a simple question...Thanks in advance.

---

apple/gs.compat #103, from gs.softteam (Apple Computer Inc.), Mon Oct 20 01:24:07 1986. A comment to message 100.

o Yes, all drives, when used with their current interface cards, will work when installed in an internal slot on the IIGS.

o 5 1/4-inch disk drives that are compatible with the IIGS DiskPort are: UniDisk 5.25

continued

DiskIIC
DuoDisk (with dealer-installed modification).

Of course any II owner who already has a drive and upgrades to a IIGS could use their current drive and interface card installed in a slot. When this is done, slots 4, 5, 6, or 7 should be used. The IIGS hardware detects when a drive in these slots is being accessed, and will slow down to 1MHz during disk access, regardless what the system speed is (thus maintaining compatibility with the software timing loops used to read 5.25 inch media).
Ray Montagne (IIGS Software Team)

---

apple/gs.compat #104, from waltwiz, Mon Oct 20 01:54:29 1986. A comment to message 103.

Thanks, Ray...and the UniDisk 5.25 can be daisy-chained from another drive? What about the old and new 3.5-inch drives? Which ones can be combined in daisy-chained method and which can't? Can the Apple 3.5-inch drive be daisy-chained from an Apple UniDisk 3.5 connected to the IIGS DiskPort? What about all odd combinations, such as daisy-chaining the 5.25-inch ones from the 3.5-inch ones or vice versa? And the DuoDisk (modified) can be daisy-chained off from another drive connected to the IIGS drive port?

---

apple/gs.compat #105, from gs.softteam, Mon Oct 20 16:03:47 1986. A comment to message 104.

The Apple 3.5-inch drives must be connected first (physically) on the DiskPort. Up to two AppleDisk 3.5-inch drives may be connected to the DiskPort. The UniDisk 3.5 can be daisy-chained off the AppleDisk 3.5-inch drive. The SmartPort firmware will support up to 127 devices total. For reasons due to power supply limitations, Apple suggests that a maximum of four devices be connected on the DiskPort on the IIGS. Take note that the RAM disk and ROM disk (if installed) are logically inserted into the SmartPort device chain. The 5.25-inch drives are not SmartPort devices although they share the DiskPort hardware. 5.25-inch drives must be connected last (physically) on the disk port device chain. 5.25-inch drives are interfaced through the disk II firmware, resident in internal slot 6. The disk port will support up to two 5.25-inch disk drives at the end of the DiskPort device chain. The DuoDisk would count as two 5.25-inch disk drives.
Ray Montagne (IIGS Software Team)

---

apple/gs.compat #106, from delton (Don Elton), Mon Oct 20 16:08:49 1986. A comment to message 105.

Is there any way (and I do mean *any* way) to access devices in a slot at the same time as built-in ports that are generally mapped to slots in IIGS native mode?

---

apple/gs.compat #107, from robmoore (Rob Moore, Apple Computer Inc.), Mon Oct 20 22:38:35 1986. A comment to message 101.

I believe that with the exception of the RGB color monitor 100, all of our monitors can be used fine with the GS. --Rob

---

apple/gs.compat #108, from robmoore, Mon Oct 20 22:44:23 1986. A comment to message 106.

You could do it by saving the appropriate screen hole data and changing the right enable bits in the Slot ROM register, but our software guys would hit you with a big stick. ProDOS initializes its device tables on boot-up and changing the slot meanings on the fly would really mess it up badly.

Oh, heck! They read the message and they're coming into my office. No guys! Please! Not that! You wouldn't! ....aieeeeeeeeeeeeeee..........

Rob shouldn't have told you that. His statements are inoperative. . .now.

GS.SoftMafia

---

apple/gs.compat #109, from gs.softteam, Tue Oct 21 02:05:14 1986. A comment to message 108.

You're right Rob, here comes the big stick. The system firmware configures the Slot ROM register based on control panel settings. When the operating system boots up, it builds a device list based on the current system configuration (which block devices are found in which slots). Changing the Slot ROM register behind the operating system's back invalidates the device list with potentially hazardous results. No application should ever change this register and expect to maintain compatibility with the operating system. In fact, we take a hard stand that no application should ever modify this register period. The Slot ROM register will always be set up by the system firmware based on the slot configuration set in the control panel!!!
*** TRUST US ***
Ray Montagne (IIGS Software Team)

---

apple/gs.compat #111, from robmoore, Thu Oct 23 12:43:09 1986. A comment to message 109.

Like I said - you can do it but you will probably foul things up royally. However, the info is still valid for foreign OSs. And who knows, maybe some enterprising outside programmer may figure out how to do something really useful with the Slot ROM register. ProDOS isn't the only OS that will be on the GS, I'm sure. In any case, you WILL mess up ProDOS if you change the slot switches.

---

apple/gs.compat #112, from delton, Thu Oct 23 14:02:17 1986. A comment to message 111.

I was really wondering if perhaps a new slot protocol could be devised where a card in a physical slot mapped itself away from the memory used by the port mapped to the logical slot. Not that much unlike slot 3 cards in a IIe, for example. It seems empty or unusable slots or ports are about as much use as runway behind you, so to speak.

---

apple/gs.compat #113, from gs.softteam, Thu Oct 23 19:55:04 1986. A comment to message 112.

It may seem a waste but don't forget the evolution of the Apple II. We were not just designing a new machine, but also maintaining compatibility with what already existed. The built-in peripherals had to operate the same as the existing Apple II peripherals and the existing operating systems (such as DOS 3.2, DOS 3.3, Pascal and ProDOS). If we abandoned the past, yes, we could have made it possible to access both internal and external slots, but the machine would not have operated correctly with existing operating systems and possibly existing third-party peripheral cards. If we had abandoned the past, with all the available software and hardware for the Apple II product line, this machine would not be an Apple II. Sorry guys, but those are the breaks, we made an Apple II.
Ray Montagne (IIGS Software Team)

---

apple/gs.compat #114, from delton, Thu Oct 23 23:21:21 1986. A comment to message 113.

No argument with maintaining compatibility. I guess that's why the original slot 3 was included in the IIe with warnings not to be able to use it with auxiliary slot cards active, but later revisions made it possible to use that slot after all. Just hoping that someone comes up with a similar arrangement in the future to expand the slotability of the IIGS probably via a new card design as well as software maneuvers, thus maintaining the downward compatibility of the hardware.

---

apple/gs.compat #115, from waltwiz, Thu Oct 23 23:51:18 1986. A comment to message 114.

Well, does that mean we can use slot 3 as a normal slot? Plug in other cards, perhaps?

---

apple/gs.compat #116, from delton, Fri Oct 24 00:14:09 1986. A comment to message 115.

It's not a totally normal slot, but card makers that follow a few rules can create cards that will work in slot 3. The most common example are accelerator cards such as the Accelerator IIe and Transwarp cards.

---

apple/gs.compat #117, from mdavis (Morgan Davis), Fri Oct 24 18:48:15 1986. A comment to message 113.

Ah, heck: DEATH TO DOS 3.3 once and for all! :-)

---

apple/gs.compat #118, from gs.softteam, Sat Oct 25 02:56:06 1986. A comment to message 117.

A major portion of existing software is DOS 3.3-based. Especially software used in the education marketplace. The Apple II is still the leading computer in this market. We wouldn't think of abandoning this market, its users, or its software base.
Ray Montagne (IIGS Software Team)

---

apple/gs.compat #119, from gs.softteam, Sat Oct 25 02:57:28 1986. A comment to message 115.

Sure you can, but don't expect to be able to run 80-column software based on internal slot 3 support at the same time.
Ray Montagne (IIGS Software Team)

BATTERY-BACKED RAM

apple/gs.other #209, from mdavis, Tue Sep 30 20:00:37 1986.

Could we get a technical description of the battery-backed RAM area of the machine (the stuff where your control panel configurations are stored)? How does one access it? What, if any, are the global offsets into this area? Is there any room for extra storage (i.e., not used by the control panel)?

---

apple/gs.other #210, from robmoore, Tue Sep 30 22:08:27 1986. A comment to message 209.

The battery RAM is contained in the clock chip and is 256 bytes long. Much of the area is reserved for system use. There are tools in the misc tool set that allow you to access it. Note: It is not addressed in normal fashion because it is read and written serially from the clock chip. Perhaps Ray Montagne could better describe the tools and access rules for it.

---

apple/gs.other #211, from mafischer (Michael Fischer, Apple Computer Inc.), Wed Oct 1 01:43:30 1986.

The details for the battery RAM are fairly long and a bunch of it (over half) is reserved for various system uses. The miscellaneous tool set contains one function that will read the entire 256 bytes into a buffer, one function that will write a 256-byte buffer to the battery RAM, one function that will read a particular parameter, and one function that will write a particular parameter. Writing the entire buffer is asking for trouble if you have not first read in the RAM and made appropriate modifications to it (including modifications to the checksums). The IIGS checks the checksum for the battery RAM on boot when it reads it into bank $E0, and resets the battery RAM to the default settings if the checksum test indicates a corrupted battery RAM. I will upload the application modifiable battery RAM locations later tonight. Note - a small mistake. The battery RAM is read into bank $E1 (02C0-03BF), not bank $E0.

continued

apple/gs.other #213, from gs.softteam, Wed Oct 1 23:03:11 1986. A comment to message 211.

Not all of the 256 bytes of battery RAM are available for use. The last few bytes are used for checksumming. For this reason, it is best to access only a particular parameter rather than the whole 256 bytes.

Ray Montagne (Apple IIGS Software Team)

apple/gs.other #214, from gs.softteam, Thu Oct 2 00:24:45 1986. A comment to message 210.

To read a battery RAM parameter, space for the parameter is pushed onto the stack along with a word that specifies which battery RAM parameter is to be read. Then a call to the tool locator to dispatch to the miscellaneous tool set to read the battery RAM parameter is executed. On return, the parameter is left on the stack for the application to pull off.

In a similar manner, to write a battery RAM parameter, the data to write is pushed on the stack along with a word that specifies the battery RAM parameter to be written. Then a call to the tool locator to dispatch to the miscellaneous tool set to write the battery RAM parameter is executed. On return the stack is clean and the battery RAM has been written. The miscellaneous tool set also provides the ability to read or write the full 256-byte battery RAM area by passing a pointer to the miscellaneous tool set that points to a buffer where the battery RAM data is to be written from or read into. This second method is less practical since probably no application would ever use all the parameters in the battery RAM. Some of the battery RAM is reserved for the control panel, while other areas are reserved for ProDOS16, and yet other areas are reserved for AppleTalk. Ray Montagne (Apple IIGS Software Team)

FORTH

The FORTH conference exists as one of the many language-specific conferences on BIX. In the following excerpts, memory-mapped I/O, file-to-screen conversions, and optimizing code through declarations are discussed.

PLACING MEMORY-MAPPED I/O

forth/lab #47, from dmiller (Don Miller), Wed Sep 10 23:49:13 1986.

I want to reserve a small block of RAM above the FORTH kernel PROM for memory-mapped I/O. How in FORTH do I reserve a 1K block of memory at a specific location? Should I reserve the first 1K of dictionary space and hope the kernel never changes, or is the kernel updated, changing the dictionary address?
<<dan>>

forth/lab #48, from dnye (David Nye), Fri Sep 12 19:26:14 1986. A comment to message 47.

The only way I know of to reserve a block of memory without monkeying with the systems innards is to ALLOT it, so the second option seems like your best bet. You could have the word that allocates the buffer check HERE to make sure you are where you want to be in case the kernel changes, or perhaps you could set up the block as an array using VARIABLE and ALLOT and index into it, making it position-independent.

forth/lab #49, from mkelly (Mahlon Kelly), Sat Sep 13 01:05:37 1986. A comment to message 47.

What machine are you using? If you want to do it in the dictionary space, then CREATE MYPLACE 100 ALLOT will do it. Entering MYPLACE will return the address of your protected place. If you want to do it, say, with a segment in MS-DOS, then it depends on the machine.

forth/lab #50, from dmiller, Sat Sep 13 18:35:47 1986. A comment to message 49.

I'm playing with the software composer NC-4000 board and was thinking about setting aside 1K of memory for memory-mapped I/O. 4K of memory stays resident and the upper 56K is paged. I'd like to set aside addresses 2000 to 3000 (decimal). This is position-dependent as the hardware address decoders on the I/O board I want to add have to be hardwired. Maybe I could load a relative address into a latch, say, by writing to a latch located in the fixed PROM space, and use the latched value to feed octal comparators for the I/O address decodes. But that seems complicated.

FILE-TO-SCREEN CONVERSION

forth/lab #51, from dmiller, Sun Sep 14 15:26:45 1986.

In letters to the editor in the last issue of "FORTH Dimentions," someone bemoaned the lack of good editors for FORTH. If the fellow had a PC, then HSFORTH permits editing regular DOS files with your favorite editor. I use PC-Write. (I think LMI also has this capability.) The fellow also wanted to be able to convert ASCII files to FORTH screens. I suspect you could do this in HSFORTH by loading the ASCII file to memory and then loading screen support and saving the memory region to a FORTH screen file. But this is above my level of sophistication. Maybe Mahlon Kelly could help. Does anyone have any hints on conversion of ASCII files to FORTH screen files, specifically F83? Can someone comment on what the F83 file structure is? Is a specific characters used to separate 1024 blocks or is screen separation left to multiples of the file read pointer? Does anyone have any utilities for this already written? <<don>>

forth/lab #52, from juan (Juan Orlandini), Sun Sep 14 15:46:51 1986. A comment to message 51.

For CP/M there are utilities that will convert "standard" FORTH files into ASCII files and vice-versa. (By standard I mean that every screen is a 1024-byte chunk in a large file. My impression is that this is a very common practice. I have seen a few FORTHs that take the entire disk and make it just their own, taking up the system tracks and all. These are the ones that are hard to convert. If this is what you call standard, you have a problem.)
|1|

forth/lab #53, from w.volkaegis (William Volk, Aegis Development, Inc.), Sun Sep 14 21:12:51 1986.

It's easy to move from block to files and vise versa. First off, F83 blocks are defined as 1024-byte blocks, no separators. I'd assume 16 lines of 64 characters per block. Read in 64 characters, remove trailing spaces, add the CR (or CR/LF or LF . . . love those standards) and write this out to a text file. For text-to-block conversion, you read a line of text in; if it's less than 65 characters after stripping end-of-line off it, just pad it with spaces and write out the 64 characters to the block file. Otherwise just break the line at the last space before the 64th character (if you can).

forth/lab #54, from rduncan (Ray Duncan), Mon Sep 15 02:31:14 1986. A comment to message 51.

LMI supplies screen file-to-text file-and-bock utilities in source code on the PC/FORTH distribution disk. These are easy to write. As you said, in LMI FORTHs you can compile either from screen files or from ordinary text files, and this is also true of HSFORTH, I believe. As for the structure of screen files, in our systems (and in every other one I have seen) a screen file is just a series of 1024-byte records which are the FORTH blocks. The file contains no control characters or inter-record separators. In other words, to read block 2 (for example) you just position the file pointer to offset 2048 and then read 1024 bytes into a buffer. I'd post the screen file/text file conversion code here but it is quite dependent on our

DOS interface words and I don't think it would do anyone much good unless they had an LMI FORTH system (in which case they already have the code anyway).

forth/lab #55, from dmiller, Mon Sep 15 20:25:08 1986. A comment to message 52.

No, I meant screens mapped into 1024-byte chunks of a large file, like you suggest. My FORTH runs under MS-DOS. The algorithm for converting ASCII DOS files to FORTH screens mapped into a file would be interesting. Do you have it? If each line is under 64 characters in the ASCII file, could you parse for CR/LF, strip out the CR/LF and pad with 0s to 64?

forth/lab #58, from juan, Tue Sep 16 16:16:08 1986. A comment to message 55.

I didn't quite get your meaning, but the resulting file is a CR/LF-delimited file (redundant, I know), with each line <=64 characters long. The backward process assumes this is true and hence all it does is pad the lines with 32s to 64 if needed and deletes CR/LFs.
|1|

forth/lab #59, from mkelly, Thu Sep 18 02:53:33 1986. A comment to message 51.

HSFORTH provides quite simple conversion of screens to files, but it's not so simple in the reverse (where does a definition stop?). But it seems unclear whether the files referred to are files of continuous source code or files of FORTH blocks. If the latter, then most decent FORTHs for the PC will allow their direct reading, or at least conversion. Which are we talking about?

forth/lab #60, from mkelly, Thu Sep 18 02:55:43 1986. A comment to message 52.

Blocks (screens) to ASCII file, yes. The reverse no. Most ASCII files terminate a line with a CR/LF pair, and block lines are not so terminated. Also, it is impossible to tell where a definition ends, so the blocks will be garbled. It certainly is possible to convert every 2 sectors to a screen, but those screens will not load.

forth/lab #61, from w.volkaegis, Thu Sep 18 15:15:37 1986. A comment to message 60.

Simply not breaking up a word on a line (i.e., break lines at spaces only) works just fine for file-to-screen conversion.

USING CONSTANTS TO OPTIMIZE CODE

forth/lab #76, from dmiller, Thu Oct 16 12:50:0 1986.

Simple question, but I would appreciate help: I have an I/O routine I am trying to optimize.

```
: word  constant word word ;
```

The constant is bit 13 high, all other bits = 0. Which is faster, to use the FORTH word constant, to put 2 base ! 1000000000, or 8192 word word? Which uses the least cycles?

forth/lab #77, from pwasson (Philip Wasson), Thu Oct 16 17:35:15 1986. A comment to message 76.

I think the question is: Which is faster, a constant or literal? If I recall correctly, a constant is faster.
Phil

forth/lab #79, from dmiller, Mon Oct 20 22:25:16 1986. A comment to message 77.

Thank you for restating my question so that even I could understand it. While checking out constant assignments I ran into a stack error message

```
: test [ 2 4 * dup . ] dup . constant check ;
```

What am I doing wrong? In his book, Kelly mentions something about a construct with [ ] producing an error message, but I didn't understand. Maybe he could comment it in the section on constants and doing as much work as possible during compilation to make execution faster. <<dan>>

forth/lab #80, from pwasson, Mon Oct 20 23:22:40 1986. A comment to message 79.

>What am I doing wrong?

My question is: what are you trying to do?
Phil

forth/lab #81, from mkelly, Tue Oct 21 02:19:43 1986. A comment to message 79.

The error is because you are changing the depth of the stack during compilation. [2 4 * dup .] leaves an 8 on the stack during compilation, and most FORTHs check to be sure the stack didn't change during compilation. I'm not entirely clear what you are trying to do, but if you follow the] with LITERAL, the 8 will be part of the definition, and dup . will display it. LITERAL will compile the 8 before you leave the definition. Does that help?

forth/lab #82, from dmiller, Tue Oct 21 13:40:34 1986. A comment to message 81.

I was trying to say REGISTER_STORE [H FF] CONSTANT PORTA ; The word in the previous test was just a dummy to see what part of the construct failed. Failure was inside the brackets.

: test [8] ; fails also. The problem was as you suggested, mkelly. Thank you both for your help. Could you comment perhaps on why the FORTHs don't want the stack played with during compilation in this manner? <<dan>>

forth/lab #83, from drifkind (David H. Rifkind), Tue Oct 21 16:07:27 1986. A comment to message 82.

You can't change the contents of the stack during compilation because the stack is being used to hold compiler information. For example, whenever a control-flow word (such as IF, BEGIN, WHILE) is executed, it leaves info on the stack to allow the corresponding ELSE, THEN, or AGAIN to find it. The semicolon word checks the stack to make sure it is the same as when the colon was executed, because the most likely reason for the stack to have changed is that you forgot to finish off one of those control structures.

forth/lab #84, from mkelly, Wed Oct 22 01:17:35 1986. A comment to message 82.

FORTHs don't normally want the stack played with between : and ; for several reasons; one is that IF..., BEGIN..., DO..., and their companions use the stack; another is that they can use this to be sure that there was no error that accidentally left something on the stack. And what good would it do? Surely one wouldn't want to leave a number on the stack when the definition is finished. It is very important to keep clear in one's mind the difference between compile-time and execute-time actions, which I think caused your problem.

By the way, it is often possible and desirable to use [ ] to compile literals. For example, suppose different numbers are needed when different compilations of a program are done... If 5 CONSTANT PROGCON is defined, and if a colon word contains [PROGCON] LITERAL, the 5 will be displayed. If PROGCON is set differently at the start of a program, then something different will be compiled in the : definition.
Michael ■

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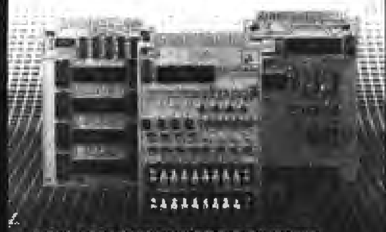

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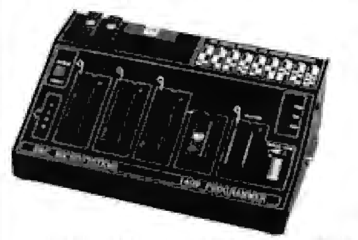

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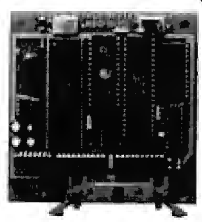

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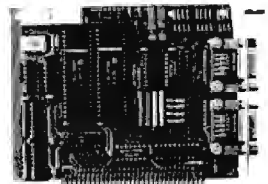

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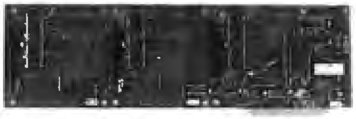

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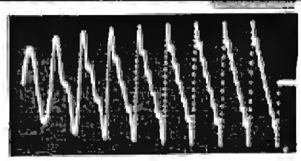

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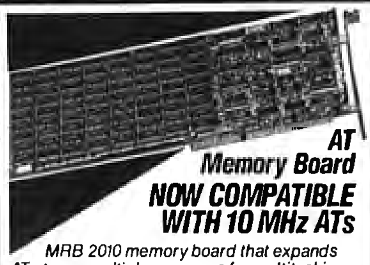

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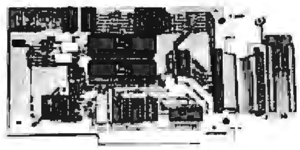

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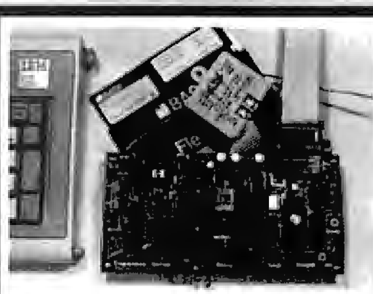

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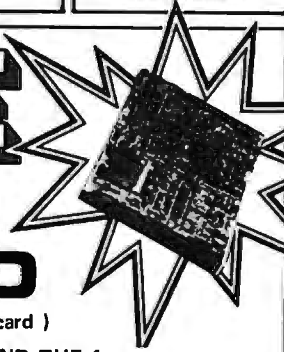

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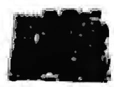

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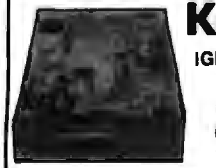

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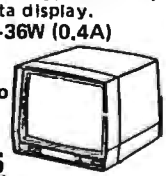

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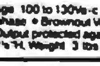

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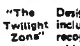

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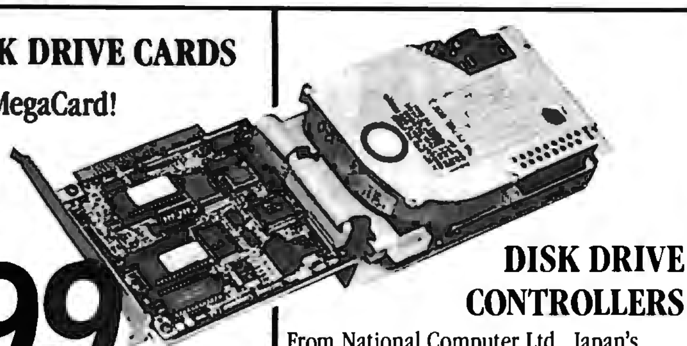

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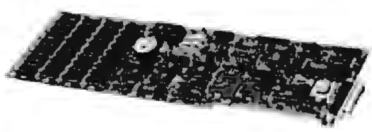

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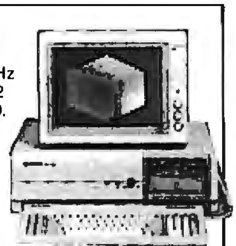

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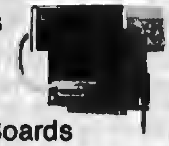

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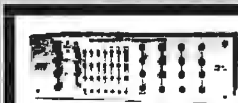

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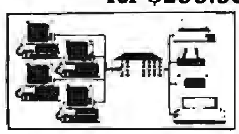

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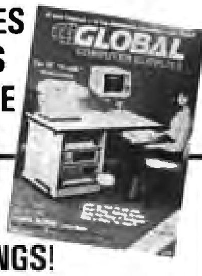

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2 Meg EMS Memory Card (Full EMS Std. w/1 Meg RAM)	$200 87
20 Meg Hard Disk Drive (Half High, w/Ctrl)	$318 61
AT Portable Case Baby 286 (AT Key, 180 Watts, Amber TTL)	$497 22

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MS DOS 3.1	
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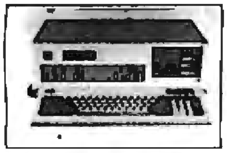
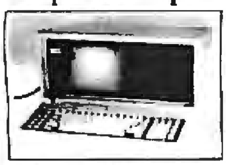
Serviced by TRW Nationwide	
Multitech softwhite + Cord	219
Multitech color + Cord	359
Multitech EGA + Cord	659
Multitech 3 MB RAM Exp OK	219
PCA 8 MHz 640K 20 MB – 1 floppy, parallel, serial, clock & game	995
PCA 8 MHz 640K 1 floppy	495
PCA 8 MHz 640K – 2 floppies, monitor, card, par., ser., clock & game	775

Desktop Computer



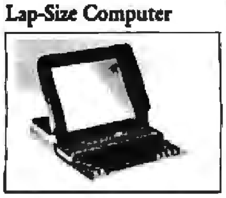
IBM PC AT 512K	2675
Compaq Deskpro 386 512K	4900
IBM PC XT 640K	1745
IBM PC 256K	995

Transportable Computer



Compaq Portable 286	3100
Compaq Portable Computer	1595
Compaq Port. II Model 4	3895
Compaq Portable Plus	1695

Lap-Size Computer

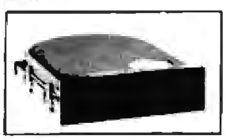


Toshiba T1100+	1575
Toshiba T3100	3595

Floppy Disk Drive

Teac 558V, 360K	99
Teac FG, 1.2MB	149
Toshiba ND 040, 360K	99
Toshiba ND 08DEG, 1.2MB	149
Fujitsu 360K	85

Hard Disk Drive



Seagate ST225, 20MB Kit	379
Seagate ST238, 30MB Kit	479
Seagate ST4026, 20MB	529
Seagate ST4038, 30MB	629
Rodime 203E, 30 MB	498
Seagate ST4051, 40 MB	729
CDC 9415-86, 80MB	1295
Western Digital 1002	125
Western Digital WA2	239
Western Digital WAH	189
Disk Manager Software	99

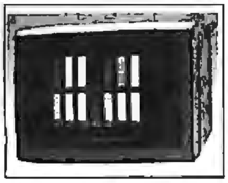
Alternative Mass Storage

Bernoulli Box 20+20+80	3895
Everex Stream 60 ext	895
Everex 60 internal	819
Alloy 60MB external	749
Irwin 10MB internal	389

Diskettes and Tapes

3M DC-600A cartridge	26
3M DC-1000 cartridge	19
Bernoulli 20MB cartridge	72
Maxell MD2-DM 10 disks	19
Maxell MD2-HD 10 disks	35

Color Monitor



Princeton HX-12	442
Princeton SR-14 770 × 400	495
Thompson color RGB	269
Taxan 630	450
Taxan 640	515

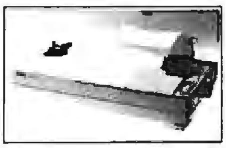
EGA Color Monitor

NEC Multisync	569
Princeton HX-12 E	539
Multitech EGA	419
Samsung EGA	399

Monochrome Monitor

Samsung amber/green/TTL	85
Amdex 310A TTL amber	159
Princeton MAX 12 amber	155
Multitech soft white TTL	119

Printer–Dot Matrix Near Letter Quality



Epson LQ-1000	830
Epson FX-286	569
Epson FX-85	434
IBM Proprinter	415
IBM Proprinter XL	629
Citizen 120D 120 CPS	190
Citizen MSP 10 160 CPS	307
Citizen MSP 15 160 CPS	414
Okidata 182 120 CPS	228
Okidata 292+ 216 CPS	399
Okidata 193+ 216 CPS	595
Panasonic KXP 1091 120	270
Panasonic KXP 1092 180	348
NEC P5 290 CPS	1053
NEC P5 XL 290 CPS	1192
NEC P6 216 CPS	475
NEC P7 216 CPS	665
Nissho 24 wire 540 CPS	1990
Toshiba P-321 216 CPS	442
Toshiba P-341 216 CPS	699
Toshiba P-351 288 CPS	949
Toshiba P-351 288 CPS	1135
Brother 1509 180 CPS	399

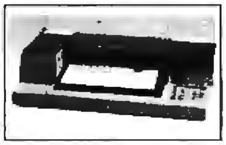
Printer–Letter Quality

Citizen Premier 35 CPS	517
Brother HR-15XL 17 CPS	369
Brother HR-35 35 CPS	895
NEC Spinwriter 3550	799
IBM Quietwriter	1215

Printer–Laser

H P Laserjet 500	3850
H P Laserjet Prof	2350
H P Laserjet Plus	3000
Cannon LBP-8A-1P	2150
Cannon LSP-8A-2P	3000

Plotter

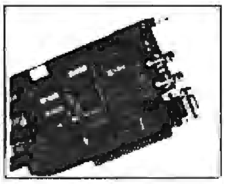


HP 7475 A Plotter	1744
Houston Ins. DPM 56	5169
Roland 880 8 pen	966

Input Device

Microsoft Mouse	119
Mouse System Mouse	139
Logic Mouse	95

Graphics Board, Monochrome



Hercules Graphics Card *(New!)*	194
Everex Edge Mono/RGB/132col.	239
ATI.. Mono/color/high/res	239
Clone monochrome graphic	95
Persyst Bob/MG mono/RGB	171

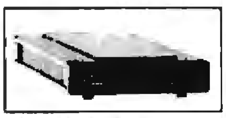
Graphics Board Color

Paradise Mod. Graphics	249
Hercules Color Graphics *(New!)*	149
Clone Color Graphics	85

Graphics Board EGA

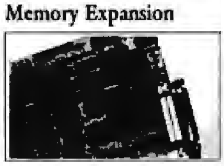
Paradise EGA/Auto Switch	359
Video 7 Deluxe/Auto	399
Multitech EGA	239

Modem



US Robotics Direct 1200	149
US Robotics 1200 PC INT	139
US Robotics 2400 PC INT	189
Everex Evercom 1200	129

Memory Expansion



AST Premium 256K 2 MB SixPakPlus	234
Clone SixPack	89
AST Rampage PC	234
AST Rampage AT	445
Toll Tree J-Rom 3	184

I/O Board

2 Floppies P/S/C/G/	89
AT I/O P/S	89

Chips

256K 150 Nano	27
256K 120 Nano	29
64K 150 Nano	8
8087	119
8087-2	158
80287-3	189
80287-8	299

SOFTWARE

Accounting

Doc-Easy Accounting	45
Accounting Software, BPI	299
Open System, Account Soft	399
PCAmerican Accounting	1695
Time Line ' Breakthrough	262

Applications Integrator

Microsoft Windows, Microsoft	65
Desqview, Quarterdeck	65

Communications

Crosstalk XVI, Microstuf	119
Smartcom II, Hayes	89

Data Management

dBASE III Plus, Ashton T	399
R Base 5000, Microrim	308
Reflex, Borland	86
Paradox Ansa Software	442
Clipper	349
Ext Report Writer	85
Clout 2	139
DGraph III	149
Quickcode III	145
Quick Report	139

Desktop Management

Sidekick, Borland	29
The Desk Organizer, Wom	65

Education

Study Program for SAT	47
Math Blaster	25
Early Learning Series	33
Newsroom, Springboard	30

File Management

PFS: File, Software Pub	76
PC-File III, Buttonware	69

Financial Modeling

1-2-3, Lotus	305
Javelin, Javelin Software	549

Games

Scenery Disks Western US	72
Flight Simulator, Microsoft	32
Jet, SubLogic Communication	33
Sargon III, Hayden Software	29
Zork I, II, and III, Inf	29
F-15 Strike Eagle MicroPro	29
Winter Games Epyx	29
Temple Of Apshai Trilogy	29
Movie Monster – The Game	29
World's Greatest Baseball	25
Comp. Novel Construction Set	29
Black Cauldron, Sierra	29
Silent Service, Microprose	25

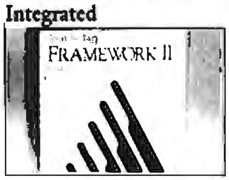
Graphics–Business

Charter-Master, Decision Re	220
Microsoft Chart, Microsoft	175
1-2-3, Lotus	305
Freelance Lotus	224
Harvard Presentation Graphics	299

Graphics–CAD

AutoCAD, Autodesk Inc.	2700
ProDesign II, American	173
In-a-Vision, Microsoft	237
Generic CAD, Generic	98
ProDesign II AmericanSBC	179

Integrated



Framework II	399
Symphony, Lotus	425
1-2-3, Lotus	305
Enable, The SoftwareGroup	333

Investment

Andrew Tobias's MECA	115
Dow Jones Market Manager	147
Dollars and Sense	107
Market Analyzer, Dow Jones	219
Market Manager Plus, Dow Jones	158
Spread Sheet Link, Dow Jones	156

Micro-to-Mainframe

IRMA, Digital Communications	1499
Crosstalk XVI, Microsoft	119

Outline Processing

ThinkTank, Living Video	99
Ready, Living Video	52

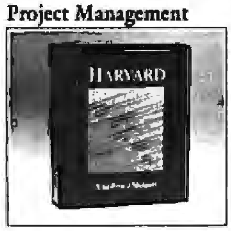
Personal Management

Andrew Tobias' MECA	115
Dollars and Sense, Mono	99

Programming Language

Turbo Pascal, Borland	41
C Compiler, Microsoft	287
Basic Compiler Microsoft	227
Turbo Prolog, Borland	58
Microsoft Quick Basic	72
R:base System V	369
Think Tank	109

Project Management



Harvard, Software Pub	299
Microsoft Project	238
Time Line, Breakthrough	235

Spreadsheet

1-2-3, Lotus	305
SuperCalc 3, Computer As	277
Multiplan, Microsoft	111
Lotus Report Writer	119

Tax Planning or Preparation

Tax Preparer, HowardSoft	299
PC/TaxCut, Best Program	85

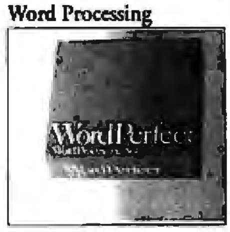
Training

Professor Dos, Individual	35
Teach Yourself dBASE III	69
PFS: First Choice SP	85
Webster's New World Writer	82
Certificate Maker, Springb	28
Print Shop, Boderbund	52
Typing Tutor III, Simon & Simon	42

Utilities

Norton Utilities, Norton	61
SuperKey, Borland	40
SideKick, Borland	28
Traveling SideKick	41
Carbon Copy, Meridian	130
PC Tool, Central Pnt	38
Copy II PC, Central Pnt	38
1 DIR+, Bourbaki	53
V Feature, Golden Bow	59
SQZ! Turner Hall	59
Fast Back, Fifth Generation	84
XTree, Executive Systems	29

Word Processing



WordPerfect, Wordperfect	210
Microsoft Word, Microsoft	265
Wordstar 2000, MicroPro	277
Easy, MicroPro	75
Multimate Advantage AshtonT	317

Most Promising Software

Turbo Lighting, Borland	58
Javelin, Javelin	549
Microsoft Windows, Microsoft	65
Q & A, Symantec Corp.	298
Generic CAD, Generic	98

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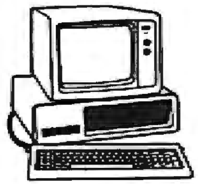

- 640K of RAM
- 7 MHz turbo mode
- 360K disk drive
- 5151-style keyboard
- 8 expansion slots

$588

- 640K of RAM
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- 1.2 MB disk drive
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OPTION #1
Two disk drives
Mono graphics card
Parallel printer port
Amdek 310A monitor

TURBO	286
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OPTION #2
20 MB hard disk
Mono graphics card
Parallel printer port
PGS MAX-12E monitor

TURBO	286
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20 MB hard disk
Color graphics card
Parallel printer port
Hitachi hi-res color monitor

TURBO	286
$1388	$1998

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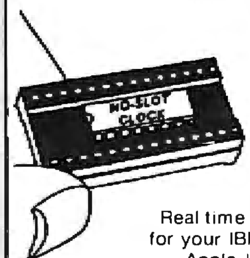
For Your Apple, PC-XT or Clone



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Real time clock/calendar for your IBM PC-XT, Clone Apple II+, IIe or IIc (Please Specify)

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- Lowpower, 11 Watts
- Head Park Zone
- Plated Media
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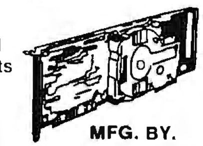
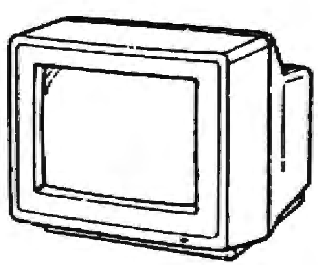


MFG. BY. Tandon

HIGH RESOLUTION COLOR MONITOR

$269

List Price $699



- High resolution 640 x 240
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- 16 true colors, 2000 characters
- Accepts standard RGB input signals
- Non-glare picture tube
- Free PC RGB cable included
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HITACHI

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$669

List Price $998

EGA Monitor Plus EGA Video Card

- Dual Mode Monitor
- Non Glare, .31 Dot Pitch
- 640 x 350, 640 x 200
- EGA, CGA, MDA &HGA
- 100% IBM Compatible
- 256K of Video RAM

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HARD DISK, CONTROLLER AND CABLES

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720K Disk Drive for Mass Storage or for Down Loading to your Lap-Top Computer

Requires DOS 3.20

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7 MHz TURBO CARD FOR YOUR PC

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- Top rated
- Uses no slots
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- Reset switch

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LIMITED QUANTITY

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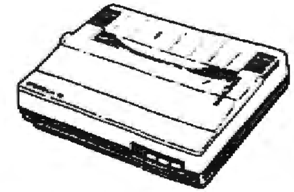
DX-35 TRACTOR ____ $99
DX-35 CABLE ____ $19



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Supports 3½" Drive

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Thompson Ultra Scan 800 x 560	$579
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PGS HX-12 640 x 240	$439
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PC Mouse w/Dr. Halo II	$119
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JADE EGA+ Above Plus HGA	$289

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8087-3 5 MHz	$119
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80287-3 5 MHz	$179
80287-8 8 MHz	$269
NEC V-20 5 MHz	$11
NEC V-20 8 MHz	$14
NEC V-30 8 MHz	$16

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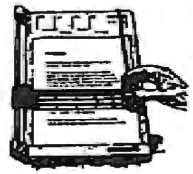
Jade green Hi-res TTL	$99
Jade amber Hi-res TTL	$99
Amdek 310A amber	$149
Magnavox green Hi-res TTL	$119
Magnavox amber Hi-res TTL	$119
PGS MAX 12E amber	$159

OMNI-READER TEXT SCANNER



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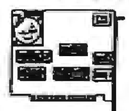
Reads and inputs type written text into your computer.

Uses a standard RS-232 serial port. Software & cable kit for IBM or Macintosh $29

Modems

1200 BAUD MODEM

$129



Internal 1200 baud card with software	$129
External 1200 baud	$139
Internal 2400 baud card with software	$299
Hayes 1200B internal card w/o software	$329
Hayes 1200B internal card w/Smartcom II	$359
Hayes Smartmodem 1200	$389
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Hayes Smartmodem 2400	$589

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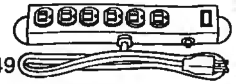
6 socket, UL listed, U.S. made Power/surge strip

$14.95



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6 button, under-monitor, swivel Power/surge control center

$59.95

List Price $129

Iso-Bar

These industrial quality ISO-BAR's contain surge suppression circuitry & built-in noise filters plus a 15 amp circuit breaker.

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1000W standby power supply	$899

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Roland DXY-800 8 pen	$399
HP 7470 2 pen	$899
HP 7475 6 pen	$1699
HP 7550A 8 pen	$3399
HP Color Pro 8 pen	$1699
Houston Inst. PC 695	$599
Houston Inst. DMP 40P	$849
Houston Inst. DMP 29	$1699
Houston Inst. DMP 41/42	$2495
Houston Inst. DMP 51/52	$3795
Houston Inst. DMP 56	$4495

PC Multifunction Cards

384K Jade Seven Pak w/0K, p, s, c, c, g, software	$89
384K Jade Seven Pak with 384K installed	$139
AST Six Pak Plus 64K	$159
AST Six Pak Plus 384K	$229
AST Six Pak Premium 512K	$389

64K BUFFER FOR YOUR EPSON

Serial or parallel input. Fits MX, RX, FX printers

Limited Quantity

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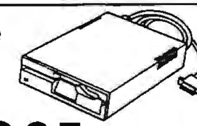
Disk Drive For Your Apple IIc



$119.95

IIc ½ high disk drive	$119
IIe ½ high disk drive	$99
IIe, II+ disk drive	$129
IIe 64K, 80 column card	$49
II+ 80 column card	$119
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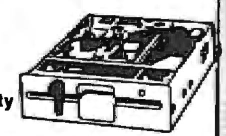
II+, IIe printer card & cable	$49
II+, IIe cooling fan	$59

DISK DRIVE

$79

- Double Sided
- Double Density
- 360K for PC



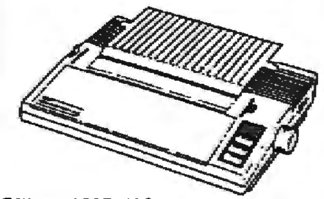
Epson Printers In Stock

EPSON HW-10

100 CPS

Including Free Interface and Cable

$189



Citizen 120D 120 cps	$198
Okidata 192 160 cps	$339
Epson LX-86 120 cps	IN STOCK
Epson FX-85 160 cps	IN STOCK
Epson FX-286 200 cps	IN STOCK
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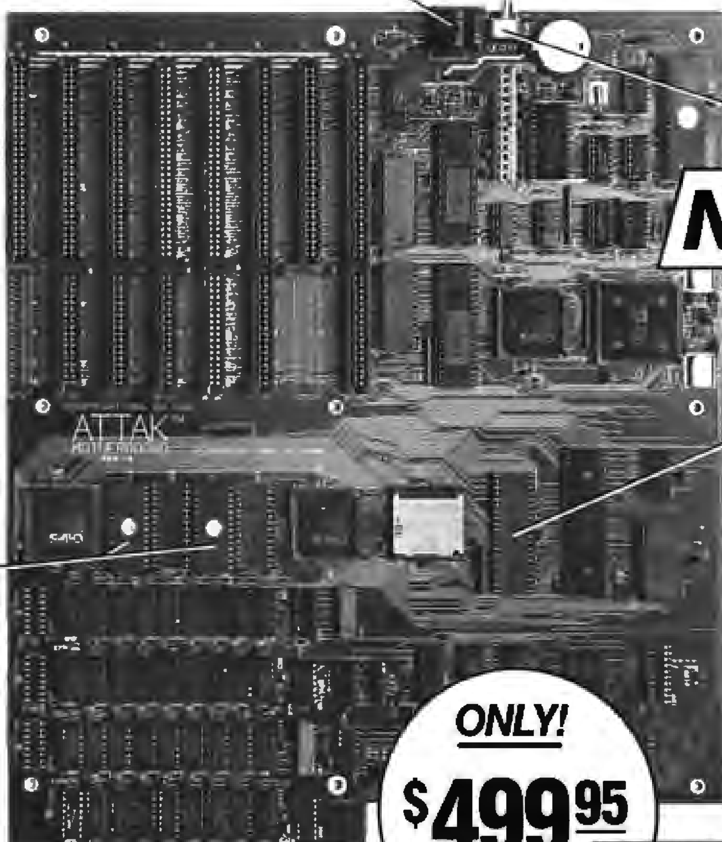

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The Desk Director is a management tool engineered to increase the efficiency of any one who spends any time behind a desk. The unit incorporates: a speaker telephone with autodial, clock calendar, calculator and more all into a handsome leather desk pad. You have seen the same product selling at Sharper Image for $995. While supplies last the Desk Director is a able from California Digital for only $479. Please specify mah any brown or black leather. Will consider volume trade.

FOUR PEN COLOR PLOTTER $159

The manufacturer has asked us not to publish their name. But this four color plotter was produced by one of the Worlds largest makers of personal computers.

The 410 color plotter will connect to the serial port of virtually any micro-computer. Simple ASCII commands direct one of the four color pens to draw circles, arcs or ellipses on paper or transparency material up to 11 by 17 inches. The plotter is capable of producing the full upper and lower case alphabet along with seven international character sets. Text can be printed horizotal, vertical or diagonal in sizes from 1/16 to 6 inches, slanted forward or backward to 85 degrees.

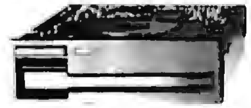
Enlargements or reductions are achieved through elaborate firmware. Pen travel is four inches per second with .004" pen resolution. Standard pens are available in an assortment of 32 different colors and widths.

The ideal plotter for architecture, CAD engineering or graphic design. At $595 it was a great buy, at $159 its a steal. Support packages or specific computers available. Manual only $15 refundable upon purchase or plotter.

SONY 53W Floppy Disk Drive

3 1/2" New IBM portable compatible

$139



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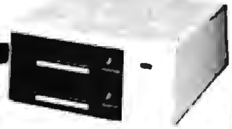
TEAC FD55FV 96 TPI, half ht.	119	109	105
TEAC FD55GF for IBM AT	169	159	155
PANASONIC 455 Half Height	109	99	89
PANASONIC 465 ½ Ht. 96TPI	139	129	125
TANDON 100-2 full height	129	125	119
MITSUBISHI new 501 half ht.	129	119	109
MITSUBISHI 504A AT comp.	169	159	155
QUME 142 half height	99	89	89
Switching power supply			49
Installation Kit with manual			10
Dual enclosure for 5¼" drives			59
34 pin edge connectors			5
Scotch head cleaning kit			19
Flip & File Storage tubs			15

Bernoulli Box

was $3540 now only

$1595



The Bernoulli Box by Iomega, features 10 and 20 megabyte removable cartridges, and delivers reliability, expandability, transportability, security and speed in one versatile subsystem. It lets you transfer megabytes of information safely and swiftly for primary or backup storage. Or combine several software programs onto a single cartridge for easy switching from one to another.

Reliable... the Box has incredible resistance to shock and vibration completely eliminating the possility of head crash.

Expandable..., grow at your own pace by adding inexpensive cartridges. When security is essential, don't lock up your system... just lock up the cartridges.

The Bernoulli Box delivers preformance that often exceeds the best of hard disk speed and the convenience of floppy disks. At these prices don't be caught wishing you had one after a loss of irreplacable data.

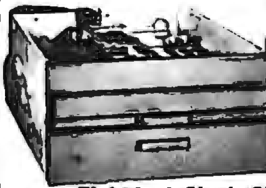
		List	Our Price
10+10 Meg.	A2210H	$3450	1595
20+20 Meg.	A2220H	4540	2095
Bootable Controller		255	159
10 Meg. Cartridge		79	49
20 Meg. Cartridge		99	65

PLOTTERS

Four pen colorplotter, 11 by 17 IBM/PC compatible	APL-410	$159
Sweet "P" 100 (Comrex) 8½ by 120"	COM-C1	$159
Houston Instruments DMP29, 11 by 17	HOU-29	1779
Houston Instruments DMP40, 11 by 17, B size	HOU-40	959
Houston Instruments DMP41/42 C/D 24 by36	HOU-41	3779
Houston Inst. DMP51/52MP C/D, 14 pen plotting	HOU-51MP	4859
Houston Instruments DMP56, E size 34 by 44	HOU-56	4795
Houston Instruments PC695, 11 by 17 multi-pen	HOU-695	579
Roland DYX-101 flat bed 11 by 17	ROL-101	419
Roland DYX-800 11 by 17 multi-pen 8 color	ROL-800	899
CalComp 1043GT plotter	CCP-1043	7899
DIGITIZERS ● MOUSE		
Hitachi Tiger Tablet 11 by 11"	HIT-TT2	615
Summagraghics Summasketch 12" four button	SUM-SK12	399
Summagraphics SummaMouse 100 line resolution	SUM-MS	99
MicroSoft serial mouse with paint brush	MST-MS232	139
MicroSoft bus mouse card w/paint brush	MST-MSB	129

QUME

$119



Eight Inch Single Sided Drives

QUME 841 single side	129	119	call
SHUGART 801R	359	359	354
SIEMENS FDD 100-8	119	115	109
Eight Inch Double Sided Drives			
QUME 842 "QUME TRACK 8"	189	179	call
SHUGART SA851R	495	485	475
OLIVETTI double sided	189	179	159
REMEX RFD-4000	179	169	159
MITSUBISHI M2896-63 ½ Ht.	459	449	409
Dual 8" enclosure with power and fan			259
Switching power supply			89
Installation kit with manual			10

PRINTERS

MATRIX PRINTERS

NEC/P7 132 col., par'l interface.	NEC-760	659.00
Star Gemini NL-15, 300cps., 136 col. 24 wire head	STR-NB15	
Star Gemini NX-10, 120 cps/30 cps NLO, tractor	STR-NX10	
Citizen MSP/10FT 160char/sec	CIT-MSP10	259.00
Panasonic KX1091 120cps. draft, 29 NLO tract & fric	PAN-KX1091	259.00
Toshiba 351P/S, 240 char/sec, 24 wire head	TOS-351PS	1099.00
Toshiba 341PS/E parl. 180 cps. 24 wire head	TOS-341PSE	759.00
Okidata 182P/IBM parallel 9½" paper	OKI-182P	239.00
Okidata 192A parallel interface, 160 char/sec	OKI-192A	379.00
Okidata 84P parallel 15" paper	OKI-84P	695.00
EpsonLX-80 10" 120Char/sec.	EPS-LX80	259.00
Epson LQ800 near letter quality	EPS-LQ800	629.00
Epson FX85 160 cps. draft 32 cps. NLQ, 240 dot/inch.	EPS-FX85	399.00
Epson FX286 132 col., 200 cps, 29 cps NLQ. graphics.	EPS-FX286	599.00
Dataproducts B-600-3, band printer 600 LPM.	DPS-B600	6985.00
Printronix P300 high speed printer 300 lines per minute.	PTX-P300	3995.00
Printronix P600 ultra high speed 600 lines per minute.	PTX-P600	5795.00

WORD PROCESSING PRINTERS

Starwriter F10 (6400) parallel. 40 char/sec	PRO-F10P	429.00
Same as above but 55 char/sec., 50 pin Diablo interlace	PRO-F55P	559.00
NEC8810 55 char/second, serial interface	NEC-8810	1179.00
NEC8830 55char/sec, par'l interface	NEC-8830	1179.00
NEC3550 popular printer designed for the IBM/PC	NEC-3550	819.00
Silver Reed EXP600, 25 cps. 10/12/15 pitch, serial/par'l	SRD-EXP600	319.00
Silver Reed EXP800 same as 600 but 40 char/sec.	SRD-EXP800	729.00
Diablo 620, proportional spacing, horz & vert tab 20 cps.	DBL-620	[illegible]
Juki 6100 18 char./sec	JUK-6100	
Juki 6300 40 char./sec	JUK-6300	[illegible]

XEROX Sunrise Computer $299

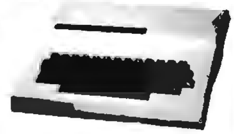
The Xerox Sunrise 1810 is by far the st value we have ever s n in a microcomputer. This is a self contained battery and AC portable. The Sunrise was originally prices at $2995. Xerox has since elected to drop the computer from their product list. California Digital has purchased all the remaining inventory and is making the unit available at a fraction of its original cost.

This portable features a built in 80 column liquid crystal display, 64K of memory along with both RF monitor and television outputs. The internal 300/1200 baud modem includes an auto dial telephone assembly. The units has both centronics parallel and a serial port programmable to 19,200 baud. The self contained micro cassette is capable of capturing data from the keyboard as well as doubling as an recorder for dictating messages.

An optional dual floppy disk drive module, pictured above, is available for only $219. Also available, for $59 is an 80 column printer that mounts in the drive module. The Sunrise features a CP/M operating system which allows the operator to use any CP/M program in Xerox 5¼" disk format and over 5000 CP/M programs available in public domain

Dragon Compu

$89



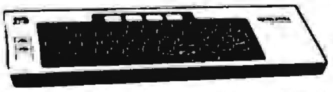
Compatible with most Radio Shack Color C
er is now available in the United States. I
ritish Broadcasting Company.
he Dragon comes complete with 64KByte
sor and comes standard with Microsoft Color
processing package. The computer outputs
allows the unit to be used in conjunction with any color television.
This is the ideal low cost computer to be used with
Source. EasyLink or any other time share service

Adeus Daisy Wheel $159

The Adeus CP/2000, is a 22 character per second daisy wheel printer which accepts 96 character Diablo wheels and ribbons. This printer was manufactured by the Olympus Typewriter Company for Cosmo World USA.

This unit will print 10, 12 and 15 characters per inch proportionally spaced with increments of 1/120". Bi-directional printing. 2 K/Byte buffer (expandable to 6K) and both serial and Centronics parallel interfacing make the Adeus CP/2000 an exceptional buy at only $159. Original price $595

Quick-Link 300

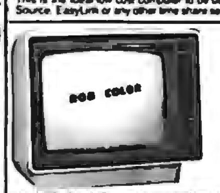


$59

The Quick-Link 300 gives you an instant link to any dial up data base. Such as Dow Jones, Western Union or the Source. The Quick-Link has four user programmable log-on keys, allowing the operator, with only one key stroke, to dial the data base, log-in and give the password. All this information is permanently stored in non-volatile RAM.

Features include video output to television or monitor, auto dial, auto-log, full sized keyboard, 300 baud modem and 1200 baud auxillary printer port. All this is available for only $59

RGB Color



The NEC JC-1401D is a 13" medium/high resolution RGB monitor suitable for use with the Sanyo MBC-550/555 or the IBM/PC. The monitor features a resolution of 400 dots by 240 lines. Colors available are Red, Green, Blue, Yellow, Cyan, Magenta, Black and White.

The NEC monitor carries the Litton-Monroe label and was originally scheduled for use in their "Office of the Future" equipment. A change in Monroe's marketing strategy has made these units excess inventory which were sold to California Digital. We are offering these "new" RGB monitors at a fraction of their original cost. IBM/P/C Computer compatible NEC-1401/PC

Also available 12" Amdek Color 1 composite $159

VISA

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7400

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7402	.29	.19	7486	.45	.35
7404	.35	.25	7489	2.05	1.95
7405	.39	.29	7490	.49	.39
7406	.39	.29	7493	.45	.35
7407	.39	.29	74121	.45	.35
7408	.35	.25	74123	.59	.49
7410	.35	.25	74125	.55	.45
7414	.49	.39	74126	.75	.65
7416	.45	.35	74143	4.05	3.95
7417	.45	.35	74150	1.35	1.25
7420	.35	.25	74154	1.35	1.25
7430	.35	.25	74158	1.59	1.49
7432	.39	.29	74173	.85	.75
7438	.39	.29	74174	.65	.55
7442	.55	.45	74175	.65	.55
7445	.79	.69	74176	.99	.89
7446	.89	.79	74181	1.95	1.85
7447	.89	.79	74189	2.05	1.95
7448	2.05	1.95	74193	.79	.69
7472	.75	.65	74198	1.85	1.75
7473	.45	.35	74221	.99	.89
7474	.45	.35	74273	2.05	1.95
7475	.49	.39	74365	.69	.59
7476	.45	.35	74367	.69	.59

74LS

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74LS02	.29	.19	74LS166	.99	.89
74LS04	.35	.25	74LS173	.59	.49
74LS05	.35	.25	74LS174	.49	.39
74LS06	1.09	.99	74LS175	.49	.39
74LS07	1.09	.99	74LS189	4.59	4.49
74LS08	.29	.19	74LS191	.59	.49
74LS10	.29	.19	74LS193	.79	.69
74LS14	.49	.39	74LS221	.69	.59
74LS27	.35	.25	74LS240	.79	.69
74LS30	.29	.19	74LS243	.79	.69
74LS32	.35	.25	74LS244	.79	.69
74LS42	.49	.39	74LS245	.89	.79
74LS47	.99	.89	74LS259	.99	.89
74LS73	.39	.29	74LS273	.89	.79
74LS74	.35	.25	74LS279	.49	.39
74LS75	.39	.29	74LS322	4.05	3.95
74LS76	.55	.45	74LS365	.49	.39
74LS85	.59	.49	74LS366	.49	.39
74LS86	.35	.25	74LS367	.49	.39
74LS90	.49	.39	74LS368	.49	.39
74LS93	.49	.39	74LS373	.79	.69
74LS123	.59	.49	74LS374	.79	.69
74LS125	.49	.39	74LS393	.89	.79
74LS138	.49	.39	74LS590	6.05	5.95
74LS139	.49	.39	74LS624	2.05	1.95
74LS154	1.09	.99	74LS629	2.29	2.19
74LS157	.45	.35	74LS640	1.09	.99
74LS158	.45	.35	74LS645	1.09	.99
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74LS164	.59	.49	74LS688	2.05	1.95

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74S04	.35	74S189	1.69
74S08	.35	74S196	2.49
74S10	.29	74S240	1.49
74S32	.35	74S244	1.49
74S74	.45	74S253	.79
74S85	1.79	74S287*	1.49
74S86	.35	74S288*	1.49
74S124	2.95	74S373	1.49
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74ALS

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74ALS02	.35	74ALS174	.89
74ALS04	.39	74ALS175	.89
74ALS08	.39	74ALS240	1.49
74ALS10	.39	74ALS244	1.49
74ALS27	.39	74ALS245	1.49
74ALS30	.39	74ALS373	1.69
74ALS32	.39	74ALS374	1.69
74ALS74	.49	74ALS573	1.69

74F

74F00	.39	74F139	.89
74F04	.39	74F157	.95
74F08	.39	74F193	3.95
74F10	.39	74F240	1.39
74F32	.39	74F244	1.39
74F74	.49	74F253	.99
74F86	.59	74F373	1.39
74F138	.89	74F374	1.39

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CD4013	.29	CD4093	.35
CD4016	.29	CD4094	.89
CD4017	.55	CD40103	2.49
CD4018	.59	CD40107	.69
CD4020	.59	CD4503	.35
CD4024	.49	CD4510	.69
CD4027	.35	CD4511	.69
CD4030	.29	CD4520	.75
CD4040	.65	CD4522	.79
CD4049	.29	CD4538	.79
CD4050	.29	CD4541	.69
CD4051	.59	CD4543	.79
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COMMODORE CHIPS

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6510 CPU	9.95	6572 VIC PAL-N	14.95	*82S100PLA (906114-01)**	13.95
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6526 CIA	14.95	8502 MPU	7.95	*901229-05 Upgrd. ROM	15.95
6529 SPI	4.95	8563 CRT Contr.	15.95	*No spec. available	
6532 128x8 RAM, I/O, Tim Arr	6.49	8564 VIC	15.95	**NOTE: 82S100PLA = U17 (C-64	

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Replace the 8086 or 8088 in Your IBM-PC and Increase Its Speed by up to 40%!

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MICROPROCESSOR COMPONENTS

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8155-2	2.49
8156	2.49
8202	9.95
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4164-200	65,536 x 1	(200ns)	.95
TMS4416-12	16,384 x 4	(120ns)	4.25
8118	16,384 x 1	(120ns)	.69
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50464-15	65,536 x 4	(150ns) (4464) (41464)	4.95

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2114N-L	1024 x 4	(450ns) Low Power	1.09
2114N-2	1024 x 4	(200ns)	1.05
2114N-2L	1024 x 4	(200ns) Low Power	1.49
21C14	1024 x 4	(200ns) (CMOS)	.49
2149	1024 x 4	(45ns)	4.95
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6264LP-12	8192 x 8	(120ns) Low Power CMOS	4.25
6264P-15	8192 x 8	(150ns) CMOS	3.59
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TMS2564	8192 x 8	(450ns) 25V	8.95
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TMS2716	2048 x 8	(450ns) 3 voltage	9.95
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27C16	2048 x 8	(450ns) 25V (CMOS)	6.49
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2732A-20	4096 x 8	(200ns) 21V	4.25
2732A-25	4096 x 8	(250ns) 21V	3.95
2732A-45	4096 x 8	(450ns) 21V	3.75
27C32	4096 x 8	(450ns) 25V (CMOS)	6.49
2764-20	8192 x 8	(200ns) 21V	4.25
2764-25	8192 x 8	(250ns) 21V	3.75
2764A-25	8192 x 8	(250ns) 12.5V	4.25
2764-45	8192 x 8	(450ns) 21V	3.49
27C64	8192 x 8	(450ns) 21V (CMOS)	5.49
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27128A-25	16,384 x 8	(250ns) 12.5V	4.95
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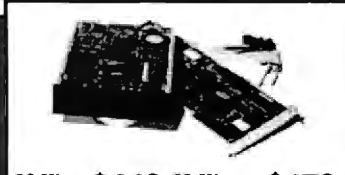

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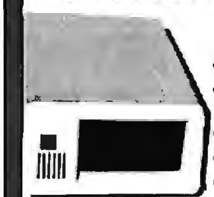

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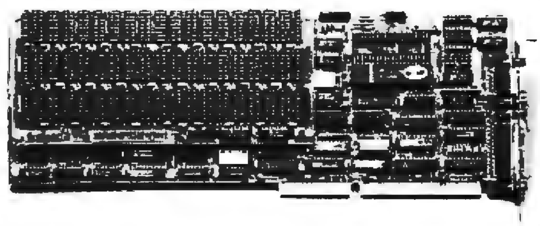

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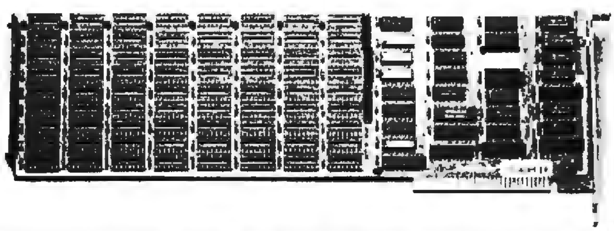

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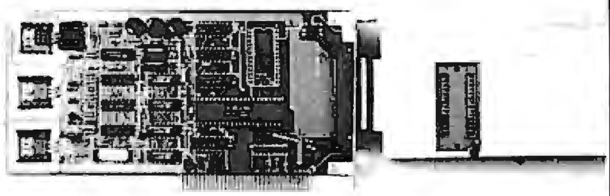

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2112	256x4	(450ns)	2.99
2114	1024x4	(450ns)	.99
2114L-4	1024x4	(450ns)(LP)	1.09
2114L-2	1024x4	(200ns)(LP)	1.49
2114L-15	1024x4	(150ns)(LP)	1.95
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TMM2016-100	2048x8	(100ns)	1.95
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HM6116-3	2048x8	(150ns)(CMOS)	1.95
HM6116LP-4	2048x8	(200ns)(CMOS)(LP)	1.95
HM6116LP-3	2048x8	(150ns)(CMOS)(LP)	2.05
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HM6264LP-15	8192x8	(150ns)(CMOS)(LP)	3.95
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LP=Low power

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4116-120	16384x1	(120ns)	1.49
MK4332	32768x1	(200ns)	6.95
4164-200	65536x1	(200ns)(5v)	1.19
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4164-120	65536x1	(120ns)(5v)	1.95
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TMS4164	65536x1	(150ns)(5v)	1.95
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41128-150	131072x1	(150ns)(5v)	5.95
TMS4464-15	65536x4	(150ns)(5v)	6.95
41256-200	262144x1	(200ns)(5v)	2.95
41256-150	262144x1	(150ns)(5v)	2.95

5v=Single 5 Volt Supply REFRESH=Pin 1 Refresh

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2716	2048x8	(450ns)(5V)	3.49
2716-1	2048x8	(350ns)(5V)	3.95
TMS2532	4096x8	(450ns)(5V)	5.95
2732	4096x8	(450ns)(5V)	3.95
2732A	4096x8	(250ns)(5V)(21V PGM)	3.95
2732A-2	4096x8	(200ns)(5V)(21V PGM)	4.25
27C64	8192x8	(250ns)(5V)(CMOS)	5.95
2764	8192x8	(450ns)(5V)	3.49
2764-250	8192x8	(250ns)(5V)	3.95
2764-200	8192x8	(200ns)(5V)	4.25
MCM68766	8192x8	(350ns)(5V)(24 PIN)	17.95
27128	16384x8	(250ns)(5V)	4.25
27C256	32768x8	(250ns)(5V)(CMOS)	10.95
27256	32768x8	(250ns)(5V)	7.49

5V=Single 5 Volt Supply 21V PGM=Program at 21 Volts

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Model	Timer	Capacity Chip	Intensity (uW/Cm²)	Unit Price
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PE-14T	YES	9	8,000	$119.00
PE-24T	YES	12	9,600	$175.00

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8035	1.49
8039	1.95
8080	2.95
8085	2.49
8087-2	169.95
8087	129.00
8088	6.95
8088-2	9.95
8155	2.49
8155-2	3.95
8748	7.95
8755	14.95
80286	129.95
80287	199.95

8200

8203	24.95
8205	3.29
8212	1.49
8216	1.49
8224	2.25
8237	4.95
8237-5	5.49
8250	6.95
8251	1.69
8251A	1.89
8253	1.89
8253-5	1.95
8255	1.69
8255-5	1.89
8259	1.95
8259-5	2.29
8272	4.95
8279	2.49
8279-5	2.95
8282	3.95
8284	2.95
8286	3.95
8288	4.95

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Z80-CPU 2.5 MHz	1.69
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Z80A-CPU	1.79
Z80A-CTC	1.89
Z80A-DART	5.95
Z80A-DMA	5.95
Z80A-PIO	1.89
Z80A-SIO/0	5.95
Z80A-SIO/1	5.95
Z80A-SIO/2	5.95
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Z80B-CPU	3.75
Z80B-CTC	4.25
Z80B-PIO	4.25
Z80B-DART	14.95
Z80B-SIO/0	12.95
Z80B-SIO/2	12.95
Z8671 ZILOG	19.95

6500

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6502	2.69
65C02 (CMOS)	12.95
6507	9.95
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6526	26.95
6532	6.95
6545	6.95
6551	5.95
6561	19.95
6581	34.95
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6502A	2.95
6520A	2.95
6522A	5.95
6532A	11.95
6545A	7.95
6551A	6.95
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6502B	6.95

6800

1.0 MHz	
6800	1.95
6802	4.95
6803	9.95
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6809E	5.95
6810	1.95
6820	2.95
6821	1.95
6840	6.95
6843	19.95
6844	12.95
6845	4.95
6847	11.95
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68B00	4.95
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68B09	6.95
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2793	19.95
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1.8432	2.95
2.0	1.95
2.097152	1.95
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4.032	1.95
5.0	1.95
5.0688	1.95
6.0	1.95
6.144	1.95
6.5536	1.95
8.0	1.95
10.0	1.95
10.738635	1.95
12.0	1.95
14.31818	1.95
15.0	1.95
16.0	1.95
17.430	1.95
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24.0	1.95
32.0	1.95

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2.4576	5.95
2.5	4.95
4.0	4.95
5.0688	4.95
6.0	4.95
6.144	4.95
8.0	4.95
10.0	4.95
12.0	4.95
12.480	4.95
15.0	4.95
16.0	4.95
18.432	4.95
20.0	4.95
24.0	4.95

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74LS02	.17	74LS169	.95
74LS03	.18	74LS173	.49
74LS04	.16	74LS174	.39
74LS05	.18	74LS175	.39
74LS08	.18	74LS191	.49
74LS09	.18	74LS192	.69
74LS10	.16	74LS193	.69
74LS11	.22	74LS194	.69
74LS12	.22	74LS195	.69
74LS13	.26	74LS196	.59
74LS14	.39	74LS197	.59
74LS15	.26	74LS221	.59
74LS20	.17	74LS240	.69
74LS21	.22	74LS241	.69
74LS22	.22	74LS242	.69
74LS27	.23	74LS243	.69
74LS28	.26	74LS244	.69
74LS30	.17	74LS245	.79
74LS32	.18	74LS251	.49
74LS33	.28	74LS253	.49
74LS37	.26	74LS256	1.79
74LS38	.26	74LS257	.39
74LS42	.39	74LS258	.49
74LS47	.75	74LS259	1.29
74LS48	.85	74LS260	.49
74LS51	.17	74LS266	.39
74LS73	.29	74LS273	.79
74LS74	.24	74LS279	.39
74LS75	.29	74LS280	1.98
74LS76	.29	74LS283	.59
74LS83	.49	74LS290	.89
74LS85	.49	74LS293	.89
74LS86	.22	74LS299	1.49
74LS90	.39	74LS322	3.95
74LS92	.49	74LS323	2.49
74LS93	.39	74LS364	1.95
74LS95	.49	74LS365	.39
74LS107	.34	74LS367	.39
74LS109	.36	74LS368	.39
74LS112	.29	74LS373	.79
74LS122	.45	74LS374	.79
74LS123	.49	74LS375	.95
74LS124	2.75	74LS377	.79
74LS125	.39	74LS378	1.18
74LS126	.39	74LS390	1.19
74LS132	.39	74LS393	.79
74LS133	.49	74LS541	1.49
74LS136	.39	74LS624	1.95
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74LS145	.99	74LS669	1.29
74LS147	.99	74LS670	.89
74LS148	.99	74LS682	3.20
74LS151	.39	74LS683	3.20
74LS153	.39	74LS684	3.20
74LS154	1.49	74LS688	2.40
74LS155	.59	74LS783	22.95
74LS156	.49	81LS95	1.49
74LS157	.35	81LS96	1.49
74LS158	.29	81LS97	1.49
74LS160	.29	81LS98	1.49
74LS161	.39	25LS2521	2.80
74LS162	.49	25LS2569	2.80
74LS163	.39	26LS31	1.95
74LS164	.49	26LS32	1.95

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74HC02	.59	74HC151	.89
74HC04	.59	74HC154	2.49
74HC08	.59	74HC157	.89
74HC10	.59	74HC158	.95
74HC14	.79	74HC163	1.15
74HC20	.59	74HC175	.99
74HC27	.59	74HC240	1.89
74HC30	.59	74HC244	1.89
74HC32	.69	74HC245	1.89
74HC51	.59	74HC257	.85
74HC74	.75	74HC259	1.39
74HC85	1.35	74HC273	1.89
74HC86	.69	74HC299	4.99
74HC93	1.19	74HC368	.99
74HC107	.79	74HC373	2.29
74HC109	.79	74HC374	2.29
74HC112	.79	74HC390	1.39
74HC125	1.19	74HC393	1.39
74HC132	1.19	74HC4017	1.99
74HC133	.69	74HC4020	1.39
74HC138	.99	74HC4049	.89
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74HCT08	.69	74HCT194	1.19
74HCT10	.69	74HCT240	2.19
74HCT11	.69	74HCT241	2.19
74HCT27	.69	74HCT244	2.19
74HCT30	.69	74HCT245	2.19
74HCT32	.79	74HCT257	.99
74HCT74	.85	74HCT259	1.59
74HCT75	.95	74HCT273	2.09
74HCT138	1.15	74HCT367	1.09
74HCT139	1.15	74HCT373	2.49
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74HCT157	.99	74HCT393	1.59
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74F00

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74F02	.69	74F86	.99	74F253	1.69
74F04	.79	74F138	1.69	74F257	1.69
74F08	.69	74F139	1.69	74F280	1.79
74F10	.69	74F157	1.69	74F283	3.95
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74F64	.89	74F244	3.29	74F374	4.29

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4013	.35	4511	.69
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4016	.29	4518	.85
4017	.49	4522	.79
4018	.69	4526	.79
4020	.59	4527	1.95
4021	.69	4528	.79
4024	.49	4529	2.95
4025	.25	4532	1.95
4027	.39	4538	.95
4028	.65	4541	1.29
4035	.69	4553	5.79
4040	.69	4585	.75
4041	.75	4702	12.95
4042	.59	74C00	.29
4043	.85	74C14	.59
4044	.69	74C74	.59
4045	1.98	74C83	1.95
4046	.69	74C85	1.49
4047	.69	74C95	.99
4049	.29	74C150	5.75
4050	.29	74C151	2.25
4051	.69	74C161	.99
4052	.69	74C163	.99
4053	.69	74C164	1.39
4056	2.19	74C192	1.49
4060	.69	74C193	1.49
4066	.29	74C221	2.49
4069	.19	74C240	1.89
4076	.59	74C244	1.89
4077	.29	74C374	1.99
4081	.22	74C905	10.95
4085	.79	74C911	8.95
4086	.89	74C917	12.95
4093	.49	74C922	4.49
4094	2.49	74C923	4.95
14411	9.95	74C926	7.95
14412	6.95	80C97	.95

7400/9000

7400	.19	74147	2.49
7402	.19	74148	1.20
7404	.19	74150	1.35
7406	.29	74151	.55
7407	.29	74153	.55
7408	.24	74154	1.49
7410	.19	74155	.75
7411	.25	74157	.55
7414	.49	74159	1.65
7416	.25	74161	.69
7417	.25	74163	.69
7420	.19	74164	.85
7423	.29	74165	.85
7430	.19	74166	1.00
7432	.29	74175	.89
7438	.29	74177	.75
7442	.49	74178	1.15
7445	.69	74181	2.25
7447	.89	74182	.75
7470	.35	74184	2.00
7473	.34	74191	1.15
7474	.33	74192	.79
7475	.45	74194	.85
7476	.35	74196	.79
7483	.50	74197	.75
7485	.59	74199	1.35
7486	.35	74221	1.35
7489	2.15	74246	1.35
7490	.39	74247	1.25
7492	.50	74248	1.85
7493	.35	74249	1.95
7495	.55	74251	.75
7497	2.75	74265	1.35
74100	2.29	74273	1.95
74121	.29	74278	3.11
74123	.49	74367	.65
74125	.45	74368	.65
74141	.65	9368	3.95
74143	5.95	9602	1.50
74144	2.95	9637	2.95
74145	.60	96S02	1.95

74S00

74S00	.29	74S163	1.29
74S02	.29	74S168	3.95
74S03	.29	74S174	.79
74S04	.29	74S175	.79
74S05	.29	74S188	1.95
74S08	.35	74S189	1.95
74S10	.29	74S195	1.49
74S15	.49	74S196	2.49
74S30	.29	74S197	2.95
74S32	.35	74S226	3.99
74S37	.69	74S240	1.49
74S38	.69	74S241	1.49
74S74	.49	74S244	1.49
74S85	.95	74S257	.79
74S86	.35	74S253	.79
74S112	.50	74S258	.95
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74S138	.79	74S287	1.69
74S140	.55	74S288	1.69
74S151	.79	74S299	2.95
74S153	.79	74S373	1.69
74S157	.79	74S374	1.69
74S158	.95	74S471	4.95
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7805T	.49	7905T	.59
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7815T	.49	7915T	.59

TO-3 CASE

7805K	1.59	7905K	1.69
7812K	1.39	7912K	1.49

TO-93 CASE

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16 PIN ST	.12	.10
18 PIN ST	.15	.13
20 PIN ST	.18	.15
22 PIN ST	.15	.12
24 PIN ST	.20	.15
28 PIN ST	.22	.16
40 PIN ST	.30	.22
64 PIN ST	1.95	1.49
ST=SOLDERTAIL		
8 PIN WW	.59	.69
14 PIN WW	.69	.52
16 PIN WW	.69	.58
18 PIN WW	.99	.90
20 PIN WW	1.09	.98
22 PIN WW	1.39	1.28
24 PIN WW	1.49	1.35
28 PIN WW	1.69	1.49
40 PIN WW	1.99	1.80
WW=WIREWRAP		
16 PIN ZIF	4.95	CALL
24 PIN ZIF	5.95	CALL
28 PIN ZIF	6.95	CALL
40 PIN ZIF	9.95	CALL

ZIF=TEXTOOL (ZERO INSERTION FORCE)

LINEAR

TL066	.99	LM733	.98
TL071	.69	LM741	.29
TL072	1.09	LM747	.69
TL074	1.95	LM748	.59
TL081	.59	MC1330	1.69
TL082	.99	MC1350	1.19
TL084	1.49	MC1372	6.95
LM301	.34	LM1414	1.59
LM309K	1.25	LM1458	.49
LM311	.59	LM1488	.49
LM311H	.89	LM1489	.49
LM317K	3.49	LM1496	.85
LM317T	.95	LM1812	8.25
LM318	1.49	LM1889	1.95
LM319	1.25	ULN2003	.79
LM320	see 7900	XR2206	3.95
LM322	1.95	XR2211	2.95
LM323K	4.79	XR2240	1.95
LM324	.49	MPQ2907	1.95
LM331	3.95	LM2917	1.95
LM334	1.19	CA3046	.89
LM335	1.79	CA3081	.99
LM336	1.75	CA3082	.99
LM337K	3.95	CA3086	.80
LM338K	6.95	CA3089	1.95
LM339	.59	CA3130E	.99
LM340	see 7800	CA3146	1.29
LM350T	4.60	CA3160	1.19
LF353	.59	MC3470	1.95
LF356	.99	MC3480	8.95
LF357	.99	MC3487	2.95
LM358	.59	LM3900	.49
LM380	.89	LM3909	.98
LM383	1.95	LM3911	2.25
LM386	.89	LM3914	2.39
LM393	.45	MC4024	3.49
LM394H	5.95	MC4044	3.99
TL494	4.20	RC4136	1.25
TL497	3.25	RC4558	.69
NE555	.29	LM13600	1.49
NE556	.49	75107	1.49
NE558	1.29	75110	1.95
NE564	1.95	75150	1.95
LM565	.95	75154	1.95
LM566	1.49	75188	1.25
LM567	.79	75189	1.25
NE570	2.95	75451	.39
NE590	2.50	75452	.39
NE592	.98	75453	.39
LM710	.75	75477	1.29
LM723	.49	75492	.79

H=TO-5 CAN, K=TO-3, T=TO-220

DATA ACQ / INTERFACE

ADC0800	15.55	8T26	1.29
ADC0804	3.49	8T28	1.29
ADC0809	4.49	8T95	.89
ADC0816	14.95	8T96	.89
ADC0817	9.95	8T97	.59
ADC0831	8.95	8T98	.89
DAC0800	4.49	DM8131	2.95
DAC0806	1.95	DP8304	2.29
DAC0808	2.95	DS8833	2.25
DAC1020	8.25	DS8835	1.99
DAC1022	5.95	DS8836	.99
MC1408L8	2.95	DS8837	1.65

EDGECARD CONNECTORS

100 PIN ST	S-100	.125	3.95
100 PIN WW	S-100	.125	4.95
62 PIN ST	IBM PC	.100	1.95
50 PIN ST	APPLE	.100	2.95
44 PIN ST	STD	.156	1.95
44 PIN WW	STD	.156	4.95

36 PIN CENTRONICS

MALE

IDCEN36	RIBBON CABLE	6.95
CEN36	SOLDER CUP	4.95

FEMALE

IDCEN36/F	RIBBON CABLE	7.95
CEN36PC	RT ANGLE PC MOUNT	4.95

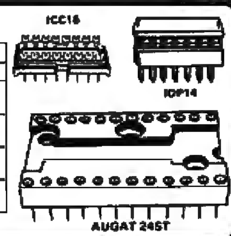
INTERSIL

ICL7106	9.95
ICL7107	12.95
ICL7660	2.95
ICL8038	4.95
ICM7207A	5.95
ICM7208	15.95

DIP CONNECTORS

DESCRIPTION	ORDER BY	CONTACTS 8	14	16	18	20	22	24	28	40
HIGH RELIABILITY TOOLED ST IC SOCKETS	AUGATxxST	.62	.79	.89	1.09	1.29	1.39	1.49	1.69	2.49
HIGH RELIABILITY TOOLED WW IC SOCKETS	AUGATxxWW	1.30	1.80	2.10	2.40	2.50	2.90	3.15	3.70	5.40
COMPONENT CARRIES (DIP HEADERS)	ICCxx	.49	.59	.69	.99	.99	.99	.99	1.09	1.49
RIBBON CABLE DIP PLUGS (IDC)	IDPxx	---	.95	.95	---	---	---	1.75	---	2.95

FOR ORDERING INSTRUCTIONS SEE D-SUBMINIATURE BELOW



DIODES/OPTO/TRANSISTORS

1N751	.25	4N26	.69
1N759	.25	4N27	.69
1N4148	25/1.00	4N28	.69
1N4004	10/1.00	4N33	.89
1N5402	.25	4N37	1.19
KBP02	.55	MCT-2	.59
KBU8A	.95	MCT-6	1.29
MDA990-2	.35	TIL-111	.99
N2222	.25	2N3906	.10
PN2222	.10	2N4401	.25
2N2905	.50	2N4402	.25
2N2907	.25	2N4403	.25
2N3055	.79	2N6045	1.75
2N3904	.10	TIP31	.49

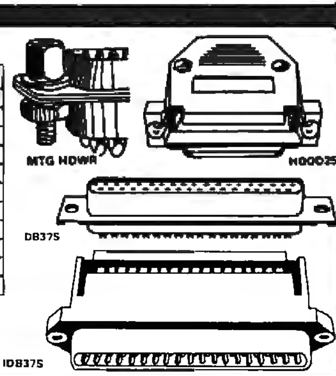
D-SUBMINIATURE

DESCRIPTION		ORDER BY	CONTACTS 9	15	19	25	37	50
SOLDER CUP	MALE	DBxxP	.82	.90	1.25	1.25	1.80	3.48
	FEMALE	DBxxS	.95	1.15	1.50	1.50	2.35	4.32
RIGHT ANGLE PC SOLDER	MALE	DBxxPR	1.20	1.49	—	1.95	2.65	—
	FEMALE	DBxxSR	1.25	1.55	—	2.00	2.79	—
WIRE WRAP	MALE	DBxxPWW	1.69	2.56	—	3.89	5.60	—
	FEMALE	DBxxSWW	2.76	4.27	—	6.84	9.95	—
IDC RIBBON CABLE	MALE	IDBxxP	2.70	2.95	—	3.98	5.70	—
	FEMALE	IDBxxS	2.92	3.20	—	4.33	6.76	—
HOODS	METAL	MHOODxx	1.25	1.25	1.30	1.30	—	—
	GREY	HOODxx	.65	.65	—	.65	.75	.95

ORDERING INSTRUCTIONS: INSERT THE NUMBER OF CONTACTS IN THE POSITION MARKED "xx" OF THE "ORDER BY" PART NUMBER LISTED

EXAMPLE: A 15 PIN RIGHT ANGLE MALE PC SOLDER WOULD BE DB15PR.

MOUNTING HARDWARE $1.00



LED DISPLAYS

FND-357(359)	COM CATHODE	.362"	1.25
FND-500(503)	COM CATHODE	.5"	1.49
FND-507(510)	COM ANODE	.5"	1.49
MAN-72	COM ANODE	.3"	.99
MAN-74	COM CATHODE	.3"	.99
MAN-8940	COM CATHODE	.8"	1.99
TIL-313	COM CATHODE	.3"	.45
TIL-311	4x7 HEX W/LOGIC	.270"	9.95
HP5082-7340	4x7 HEX W/LOGIC	.290"	7.95

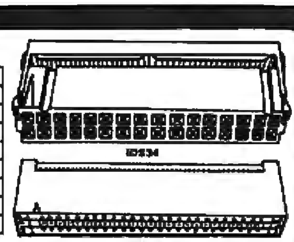
DIFFUSED LEDS

		1-99	100-UP
JUMBO RED	T1¾	.10	.09
JUMBO GREEN	T1¾	.14	.12
JUMBO YELLOW	T1¾	.14	.12
MOUNTING HDW	T1¾	.10	.09
MINI RED	T1	.10	.09

IDC CONNECTORS

DESCRIPTION	ORDER BY	CONTACTS 10	20	26	34	40	50
SOLDER HEADER	IDHxxS	.82	1.29	1.68	2.20	2.58	3.24
RIGHT ANGLE SOLDER HEADER	IDHxxSR	.85	1.35	1.76	2.31	2.72	3.39
WW HEADER	IDHxxW	1.86	2.98	3.84	4.50	5.28	6.63
RIGHT ANGLE WW HEADER	IDHxxWR	2.05	3.28	4.22	4.45	4.80	7.30
RIBBON HEADER SOCKET	IDSxx	.79	.99	1.39	1.59	1.99	2.25
RIBBON HEADER	IDMxx	—	5.50	6.25	7.00	7.50	8.50
RIBBON EDGE CARD	IDExx	1.75	2.25	2.65	2.75	3.80	3.95

FOR ORDERING INSTRUCTIONS SEE D-SUBMINIATURE ABOVE



SWITCHES

SPDT	MINI-TOGGLE ON-ON	1.25
DPDT	MINI-TOGGLE ON-ON	1.50
DPDT	MINI-TOGGLE ON-OFF-ON	1.75
SPST	MINI-PUSHBUTTON N.O.	.39
SPST	MINI-PUSHBUTTON N.C.	.39
SPST	TOGGLE ON-OFF	.49
BCD OUTPUT 10 POSITION 6 PIN DIP		1.95

DIP SWITCHES

4 POSITION	.85	7 POSITION	.95
5 POSITION	.90	8 POSITION	.95
6 POSITION	.90	10 POSITION	1.29

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Scott Feickert

RIBBON CABLE

CONTACTS	SINGLE COLOR 1'	SINGLE COLOR 10'	COLOR CODED 1'	COLOR CODED 10'
10	.18	1.60	.30	2.75
16	.28	2.50	.48	4.40
20	.36	3.20	.60	5.50
25	.45	4.00	.75	6.85
26	.46	4.10	.78	7.16
34	.61	5.40	1.07	9.35
40	.72	6.40	1.20	11.00
50	.89	7.50	1.50	13.25

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Inquiry 193

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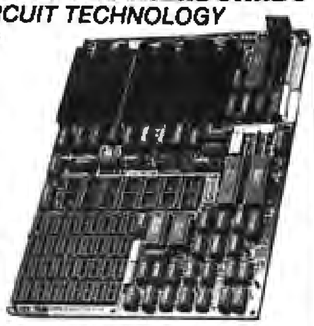

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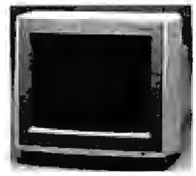

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- .38mm DOT PITCH
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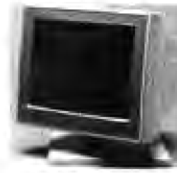

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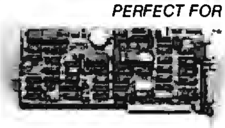

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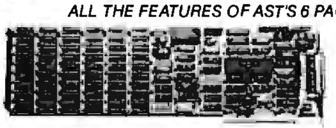

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- PARALLEL PORT
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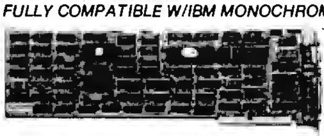

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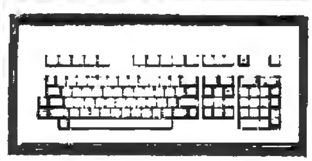

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BOMB RESULTS

Practical Interests

Winner of $100 for October's issue is Rubin Rabinovitz for his review of three programs, "The Norton Utilities, PC Tools, and Super Utility." Second place and $50 goes to Anthony Zackin, author of "Enhanced Console Driver." "PD PROLOG" by Robert Morein came in third. An additional award of $50 for quality goes to Rubin Rabinovitz for his triple review.

Inside the IBM PCs

The winning article from the IBM special issue is "Intel's 80386 Architecture," whose author Paul Wells wins $100. Winner of $50 for placing second is Stephen S. Fried for "IBM PC Accelerators." In third is Jon Shiell's "Virtual Memory, Virtual Machines." Paul Wells also wins the $50 prize for quality. Congratulations to all winning authors.

COMING UP IN BYTE

Theme:

Everybody talks about the place of computers in education, but nothing fundamental ever really changes, true or false? Next month we'll give you a look at just what's going on in computer pedagogy—and why.

Features:

A special feature for February will be a staff-written look at several high-performance workstations—some of which are still under final development. An advance, up-to-the-minute report of what you can design into a microcomputer when imagination and money are liberally applied. Other upcoming features include a C++ programming language article, one on an adventure authoring system, and a piece on the Turing machine.

Reviews:

One review concentrates on new 80386 machines; another deals with new laptops. An individual system review looks at the Atari 1040ST. Peripherals reviewed include the Cauzin Softstrip and four ink-jet printers. QuickBASIC and the Operating System Toolbox will be featured in the technical software section, and application reviews include a look at public domain programs for the Commodore Amiga.

Circuit Cellar:

Steve Ciarcia will present an infrared remote controller.

Special MC68000 Series:

Do-it-yourself Commodore Amiga expansion.

Programming Articles:

"IFP Tutorial," programming project; "Nyquist Compression," "Teaching Screens New Tricks," and "Calculating the Areas of Polygons," programming insights.

Plus Chaos Manor, According to Webster, BYTE U.K., Applications Only, Mathematical Recreations, Best of BIX, Book Reviews, What's New, Microbytes, and more.

COMPANY INDEX

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** Correspond directly with company.*

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SUBSCRIBERS ONLY!*

Use BYTE's Telephone Inquiry Processing System

Using TIPS can bring product information as much as 10 days earlier.

SEND FOR YOUR SUBSCRIBER I.D. CARD

1) If you are a new subscriber or have lost your I.D. card, circle #1 on the Reader Service Card; **attach mailer label**. We will immediately send your personal TIPS subscriber card.

GET PREPARED

2) Write your Subscriber Number, as printed on your Subscriber I.D. Card, in boxes in Step 5 below. (Do not add 0's to fill in blank boxes)

3) Write numbers for information desired in boxes in Step 7b below. (Do not add 0's to fill in blank boxes.)

CALL TIPS

4) Now, on a Touch-Tone telephone dial: (413) 442-2668 and wait for voice commands.

ENTER YOUR SUBSCRIBER AND ISSUE NUMBERS

5) When TIPS says: "Enter Subscriber Number"
(Enter by pushing the numbers and symbols [# or * enclosed in the boxes] on telephone pad ignoring blank boxes)
Enter ☐☐☐☐☐☐☐☐☐☐ [#] [#]

6) When TIPS says "Enter magazine code & issue code"
Enter [1] [#] [1] [7] [#] [#]

ENTER YOUR INQUIRIES

7a) When TIPS says "Enter (next) Inquiry Number"
Enter one inquiry selection from below (ignore blank boxes)

b) Repeat 7a as needed (maximum 17 inquiry numbers)

1. ☐☐☐☐ [#] [#] 6. ☐☐☐☐ [#] [#] 10. ☐☐☐☐ [#] [#] 14. ☐☐☐☐ [#] [#]
2. ☐☐☐☐ [#] [#] 7. ☐☐☐☐ [#] [#] 11. ☐☐☐☐ [#] [#] 15. ☐☐☐☐ [#] [#]
3. ☐☐☐☐ [#] [#] 8. ☐☐☐☐ [#] [#] 12. ☐☐☐☐ [#] [#] 16. ☐☐☐☐ [#] [#]
4. ☐☐☐☐ [#] [#] 9. ☐☐☐☐ [#] [#] 13. ☐☐☐☐ [#] [#] 17. ☐☐☐☐ [#] [#]
5. ☐☐☐☐ [#] [#]

END SESSION

8) End session by entering [*] [*] [9] [1] [#] [#]

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Name ____________________

(Title) ____________________

(Company) ____________________

Address ____________________

Telephone ____________________

City ____________________

State __________ Zip __________

A. What is your principal occupation? (Please check one only.)

1. ☐ Business Owner
2. ☐ Manager/Administrator
3. ☐ Professional (law, medicine, architecture, etc.)
4. ☐ Computer Programmer
5. ☐ Computer Analyst
6. ☐ DP/MIS
7. ☐ Engineer, Computer/Electronics
8. ☐ Engineer, Other
9. ☐ Scientist, Computer/Electronics
10. ☐ Scientist, Other

(continued)

11. ☐ Marketing/Sales
12. ☐ Finance/Accounting
13. ☐ Educator
14. ☐ Student
15. ☐ Other (please specify) ____________________

B. How many people does your company employ?

1. ☐ 1–49
2. ☐ 50–999
3. ☐ 1,000 or more

C. Information requested for:

1. ☐ Business use
2. ☐ Personal use
3. ☐ Both

D. Do you plan to purchase items inquired about within:

1. ☐ Next 3 months?
2. ☐ Next 6 months?
3. ☐ Next 12 months?

E. Will you save this information for future reference?

1. ☐ Yes 2. ☐ No

(continued)

F. For how many different computer brands do you buy products? (Consider both company and personal units.)

1. ☐ 1
2. ☐ 2–4
3. ☐ 5–9
4. ☐ 10 or more

G. Please check the statement that best describes your involvement in your company's purchasing decisions. (Check all that apply.)

1. ☐ I determine the need
2. ☐ I select the vendor
3. ☐ I approve/authorize the purchase
4. ☐ I influence the purchase
5. ☐ I evaluate products/systems

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2	24	46	68	90	112	134	156	178	200	222	244	266	288	310	332	354	376	398	420	442	464	486	508	530	552	574	596	618	640	662	684	706	728	750	772	794
3	25	47	69	91	113	135	157	179	201	223	245	267	289	311	333	355	377	399	421	443	465	487	509	531	553	575	597	619	641	663	685	707	729	751	773	795
4	26	48	70	92	114	136	158	180	202	224	246	268	290	312	334	356	378	400	422	444	466	488	510	532	554	576	598	620	642	664	686	708	730	752	774	796
5	27	49	71	93	115	137	159	181	203	225	247	269	291	313	335	357	379	401	423	445	467	489	511	533	555	577	599	621	643	665	687	709	731	753	775	797
6	28	50	72	94	116	138	160	182	204	226	248	270	292	314	336	358	380	402	424	446	468	490	512	534	556	578	600	622	644	666	688	710	732	754	776	798
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9	31	53	75	97	119	141	163	185	207	229	251	273	295	317	339	361	383	405	427	449	471	493	515	537	559	581	603	625	647	669	691	713	735	757	779	801
10	32	54	76	98	120	142	164	186	208	230	252	274	296	318	340	362	384	406	428	450	472	494	516	538	560	582	604	626	648	670	692	714	736	758	780	802
11	33	55	77	99	121	143	165	187	209	231	253	275	297	319	341	363	385	407	429	451	473	495	517	539	561	583	605	627	649	671	693	715	737	759	781	803
12	34	56	78	100	122	144	166	188	210	232	254	276	298	330	342	364	386	408	430	452	474	496	518	540	562	584	606	628	650	672	694	716	738	760	782	804
13	35	57	79	101	123	145	167	189	211	233	255	277	299	321	343	365	387	409	431	453	475	497	519	541	563	585	607	629	651	673	695	717	739	761	783	805
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16	38	60	82	104	126	148	170	192	214	236	258	280	302	324	346	368	390	412	434	456	478	500	522	544	566	588	610	632	654	676	698	720	742	764	786	808
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18	40	62	84	106	128	150	172	194	216	238	260	282	304	326	348	370	392	414	436	458	480	502	524	546	568	590	612	634	656	678	700	722	744	766	788	810
19	41	63	85	107	129	151	173	195	217	239	261	283	305	327	349	371	393	415	437	459	481	503	525	547	569	591	613	635	657	679	701	723	745	767	789	811
20	42	64	86	108	130	152	174	196	218	240	262	284	306	328	350	372	394	416	438	460	482	504	526	548	570	592	614	636	658	680	702	724	746	768	790	812
21	43	65	87	109	131	153	175	197	219	241	263	285	307	329	351	373	395	417	439	461	483	505	527	549	571	593	615	637	659	681	703	725	747	769	791	813
22	44	66	88	110	132	154	176	198	220	242	264	286	308	330	352	374	396	418	440	462	484	506	528	550	572	594	616	638	660	682	704	726	748	770	792	814

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Article No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Excellent	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93	97
Good	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94	98
Fair	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71	75	79	83	87	91	95	99
Poor	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100

Article No.	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Excellent	101	105	109	113	117	121	125	129	133	137	141	145	149	153	157	161	165	169	173	177	181	185	189	193	197
Good	102	106	110	114	118	122	126	130	134	138	142	146	150	154	158	162	166	170	174	178	182	186	190	194	198
Fair	103	107	111	115	119	123	127	131	135	139	143	147	151	155	159	163	167	171	175	179	183	187	191	195	199
Poor	104	108	112	116	120	124	128	132	136	140	144	148	152	156	160	164	168	172	176	180	184	188	192	196	200

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(Title) ____________________

(Company) ____________________

Address ____________________

Telephone ____________________

City ____________________

State ____________ Zip ____________

A. What is your principal occupation? (Please check one only.)

1. ☐ Business Owner
2. ☐ Manager/Administrator
3. ☐ Professional (law, medicine, architecture, etc.)
4. ☐ Computer Programmer
5. ☐ Computer Analyst
6. ☐ DP/MIS
7. ☐ Engineer, Computer/Electronics
8. ☐ Engineer, Other
9. ☐ Scientist, Computer/Electronics
10. ☐ Scientist, Other

(continued)

11. ☐ Marketing/Sales
12. ☐ Finance/Accounting
13. ☐ Educator
14. ☐ Student
15. ☐ Other (please specify) ____________________

B. How many people does your company employ?

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3. ☐ 1,000 or more

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1. ☐ Next 3 months?
2. ☐ Next 6 months?
3. ☐ Next 12 months?

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1. ☐ Yes 2. ☐ No

(continued)

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	28	50	72	94	116	138	160	182	204	226	248	270	292	314	556	578	600	622	644	666	688	710	732	754	776	798
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Article No.	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
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Good	102	106	110	114	118	122	126	130	134	138	142	146	150	154	158	162	166	170	174	178	182	186	190	194	198
Fair	103	107	111	115	119	123	127	131	135	139	143	147	151	155	159	163	167	171	175	179	183	187	191	195	199
Poor	104	108	112	116	120	124	128	132	136	140	144	148	152	156	160	164	168	172	176	180	184	188	192	196	200

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